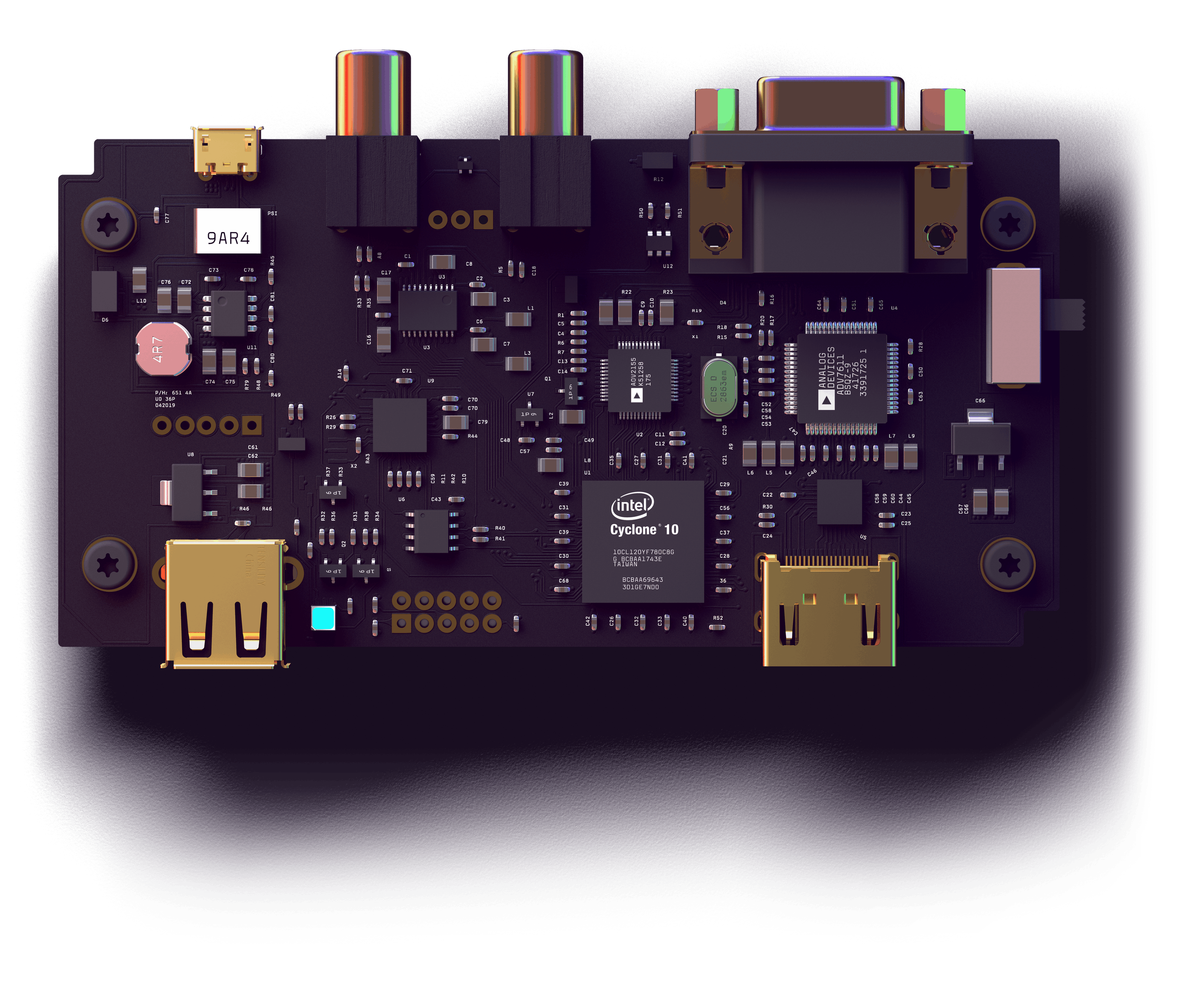
**EC201**

**Analog Electronics Lab**

**Lab – 1**



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**Experiment 1: Logic Gates using Diodes**

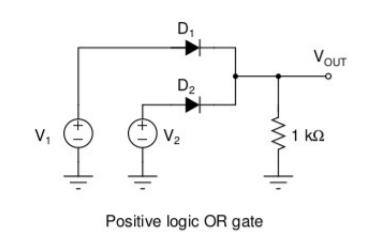
**Aim: To design OR and AND gates using diodes and resistors for:**

**A) Positive logic**

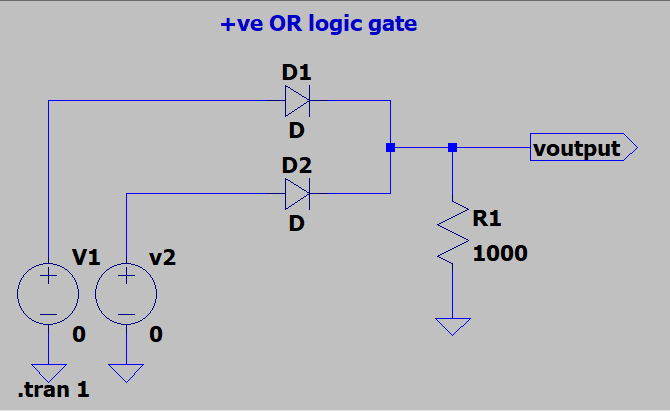
**B) Negative logic**

**1.a]** **Positive Logic OR Gate**

**Output is high whenever any one of the inputs, or both the inputs are high. Circuit diagram:**

****

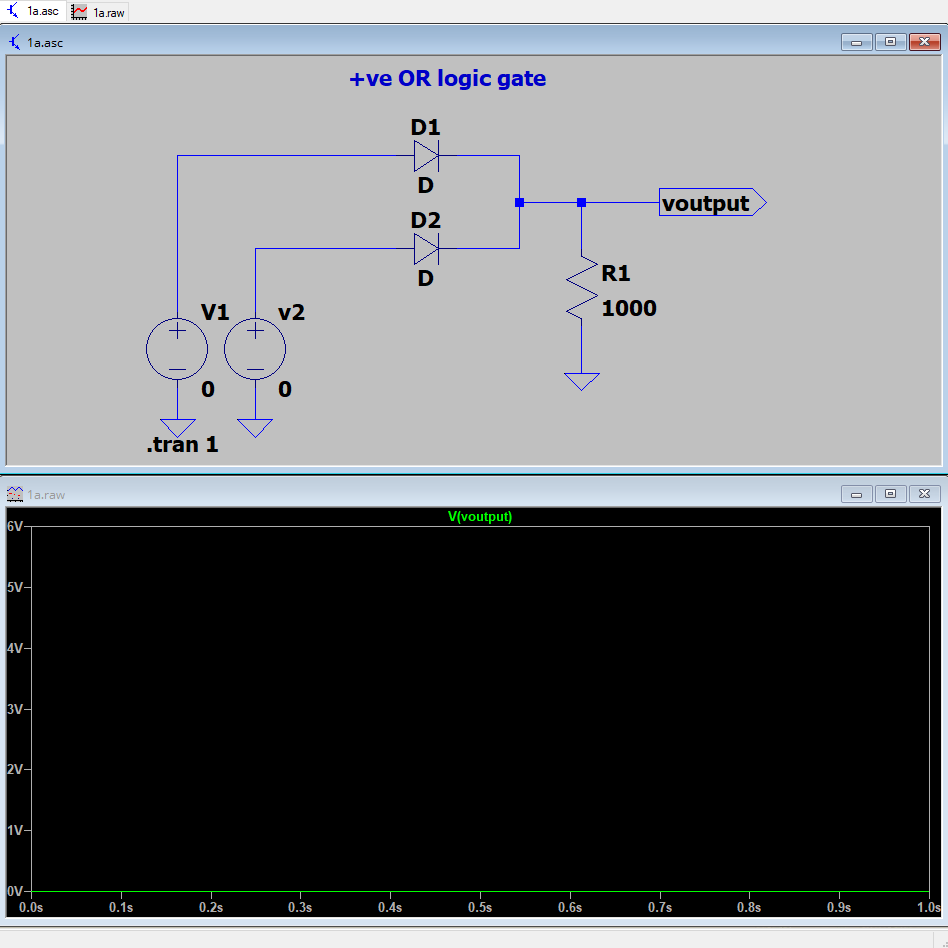
**Circuit in LTspice:**

****

**Case 1: V1=0V, V2=0V**

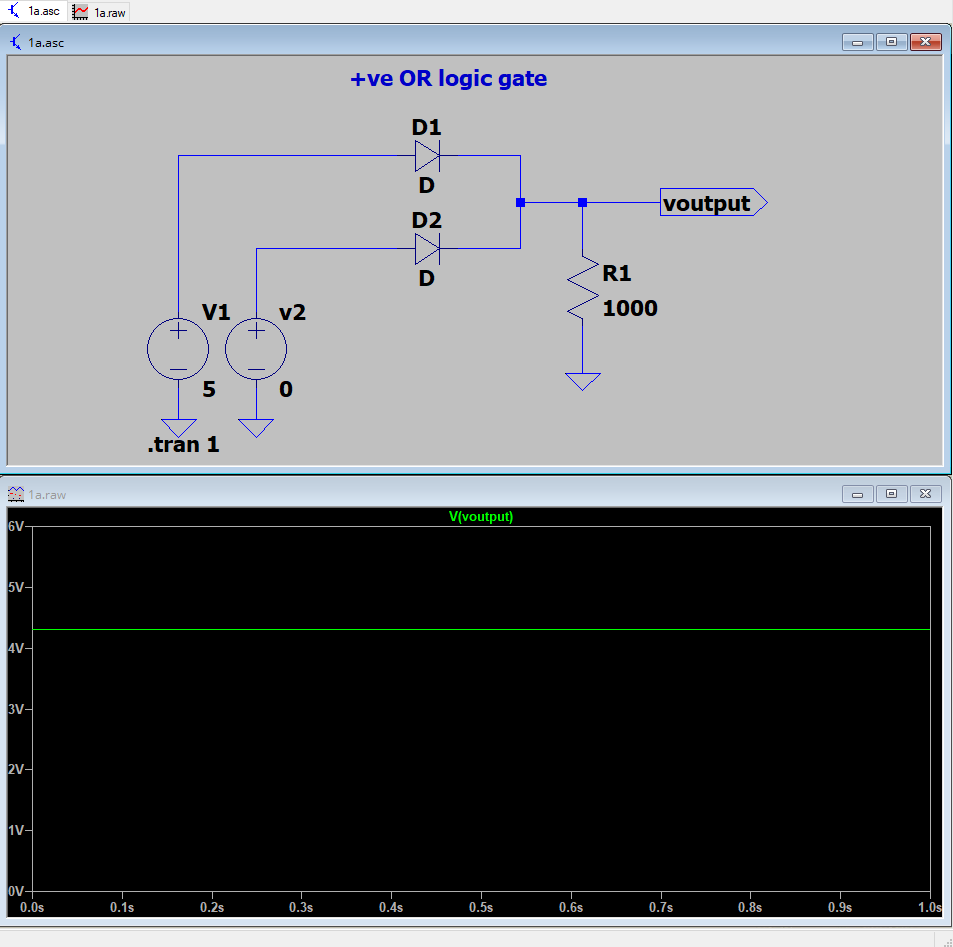
**Both the inputs are low So the expected output is also low.**

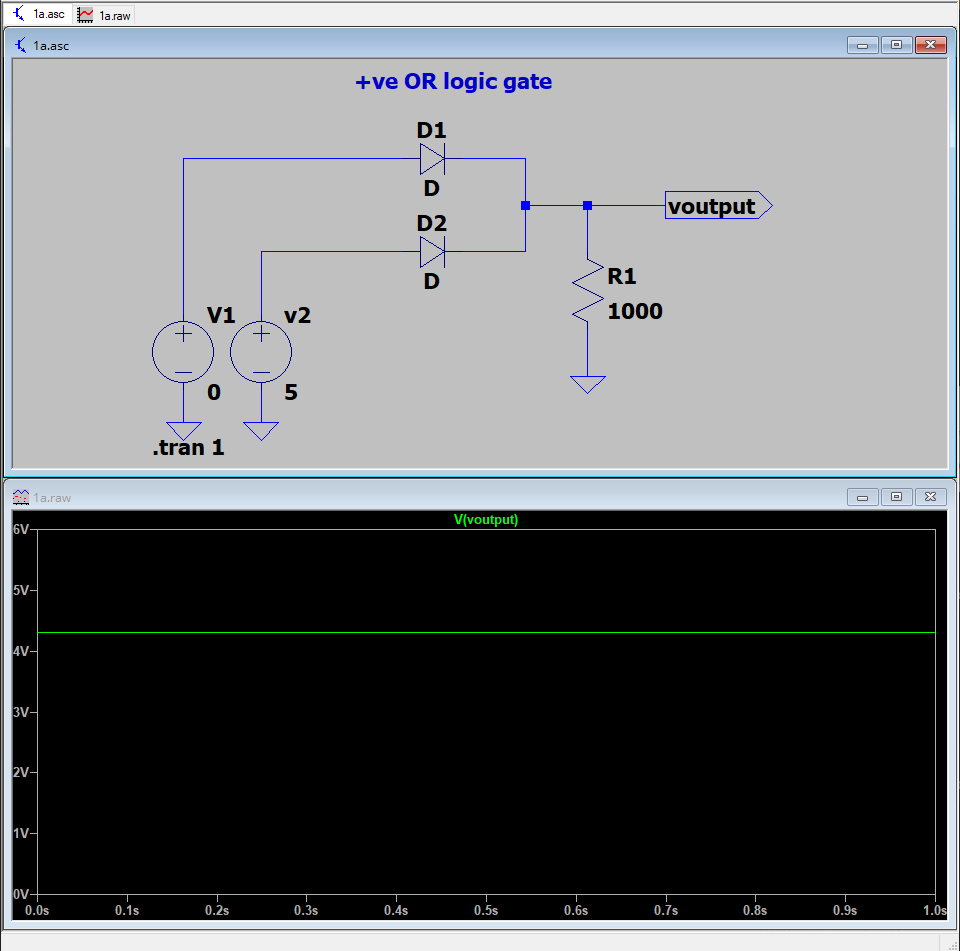
**now Simulation in LTspice:**

****

**As we can see, the output voltage Vout is 0V, which is low and is the expected output.**

**Case 2: V1=0V, V2=5V or V1=0V, V2=5V**

**One of the inputs is high, hence the expected output is also high. Simulation in LTspice: **

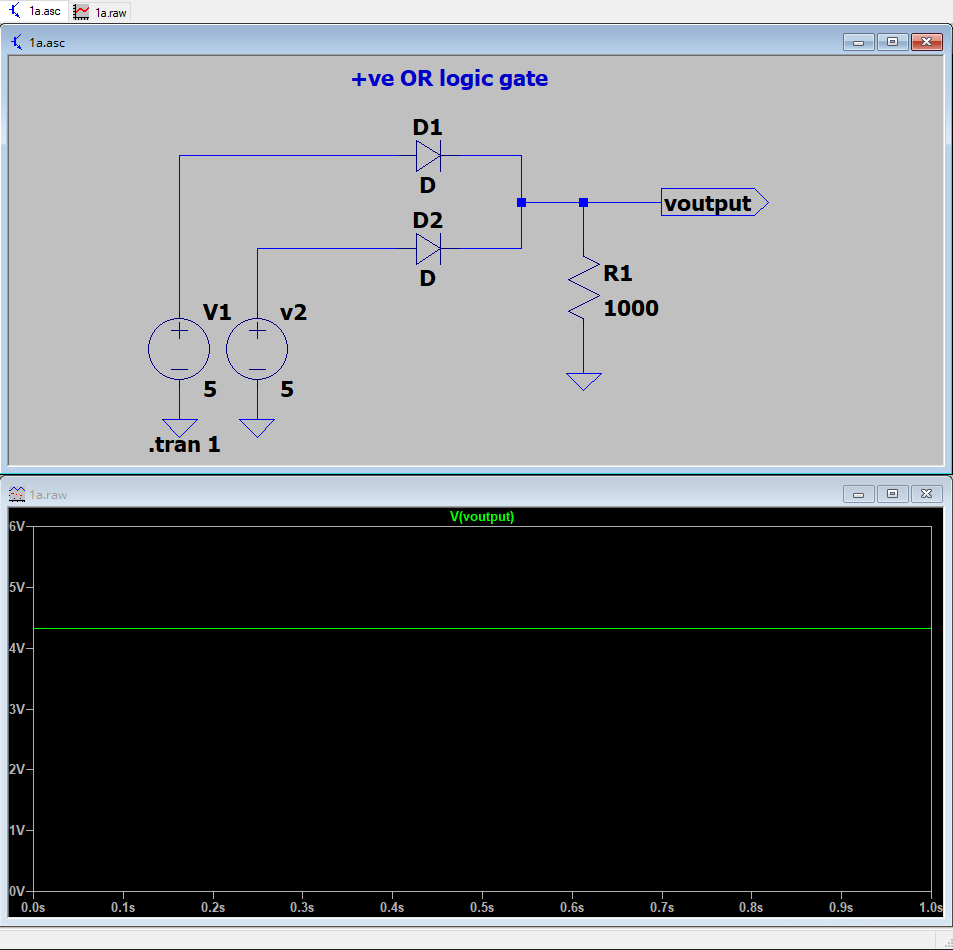
****

**As we can see, the output is 4.3V, which is expected because the Diode has a potential of its own, and we can conclude that our Vout is also high.**

**Case 3: V1=5V, V2=5V**

**Since both inputs are high, The expected output is high.**

**Simulation in LTspice:**

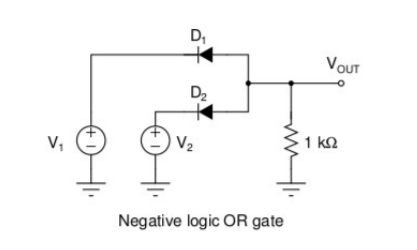
****

**Results:**

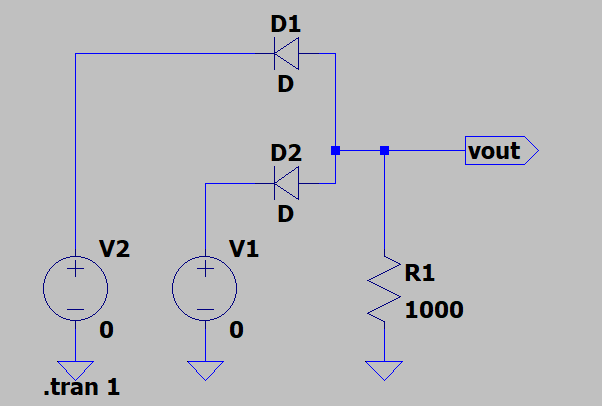
|  |  |  |  |
| --- | --- | --- | --- |
| V1 | V2 | Vout | Y |
| 0 | **0** | **0** | **0** |
| 0 | **5** | **4.3** | **1** |
| 5 | **0** | **4.3** | **1** |
| 5 | **5** | **4.3** | **1** |

**b]** **Negative Logic OR Gate**

**Output is high whenever any one of the inputs, or both the inputs are high. Circuit diagram:**

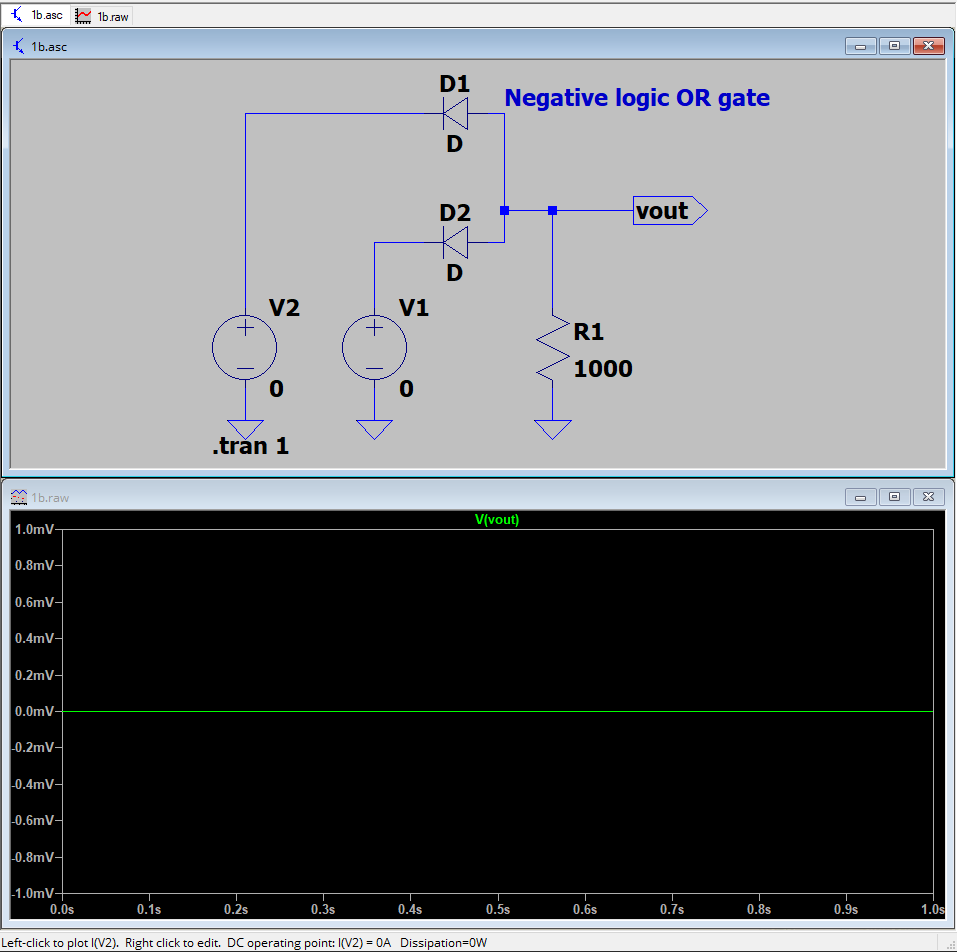
****

**Circuit in LTspice:**

****

**Case 1: V1=0V, V2=0V**

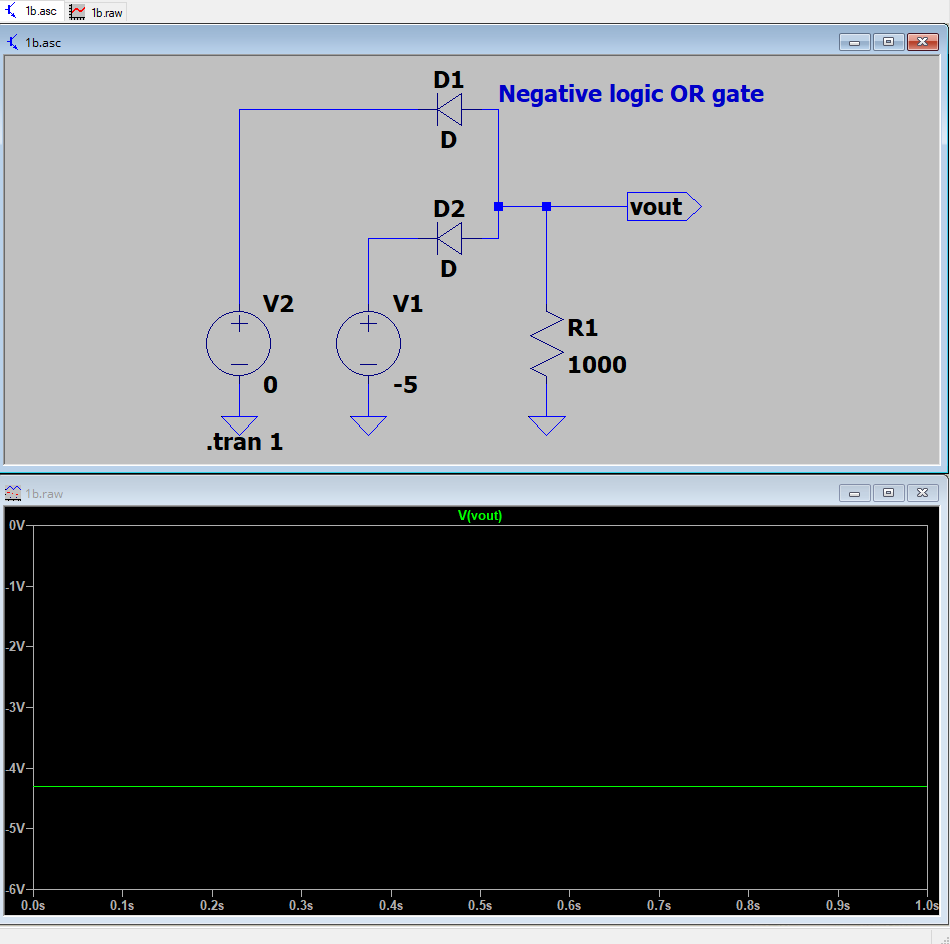
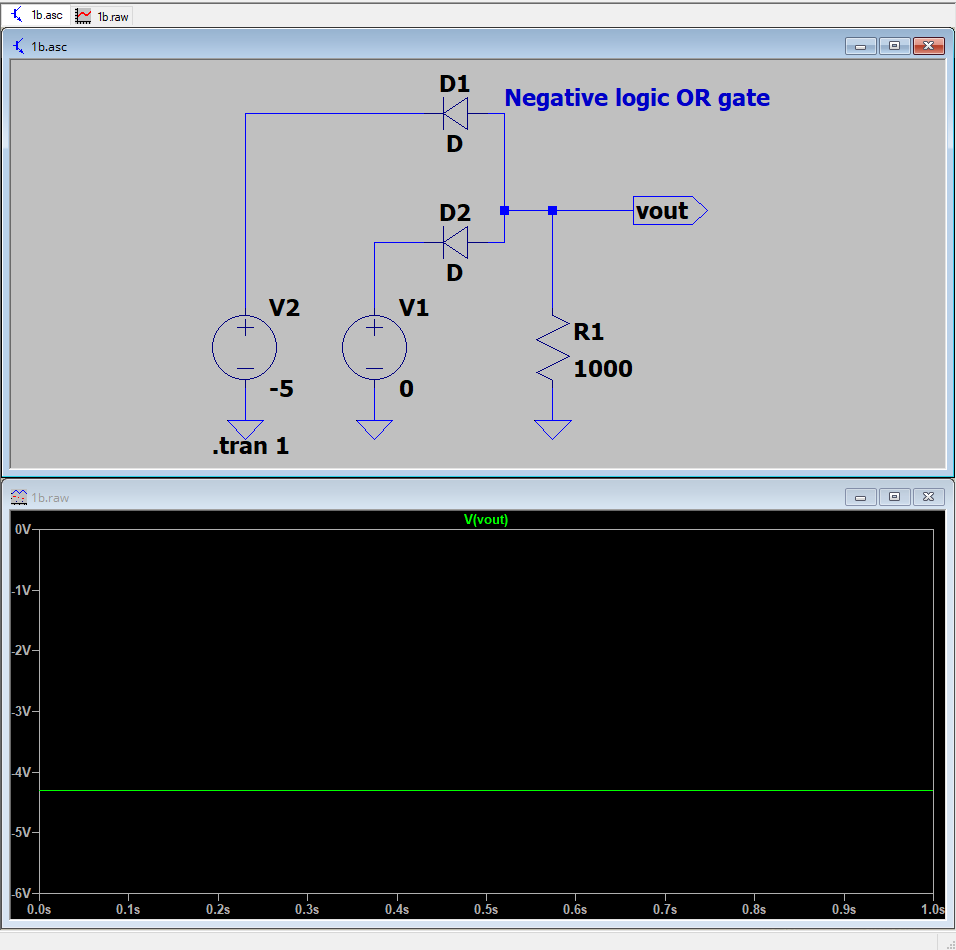
**Both the inputs are low So the expected output is also now Simulation in LTspice:**

****

**As we can see, the output voltage Vout is 0V, which is low and is the expected output.**

**Case 2: V1=0V, V2=-5V or V1=-5V, V2=0V**

**One of the inputs is high, hence the expected output is also high. Simulation in LTspice:**

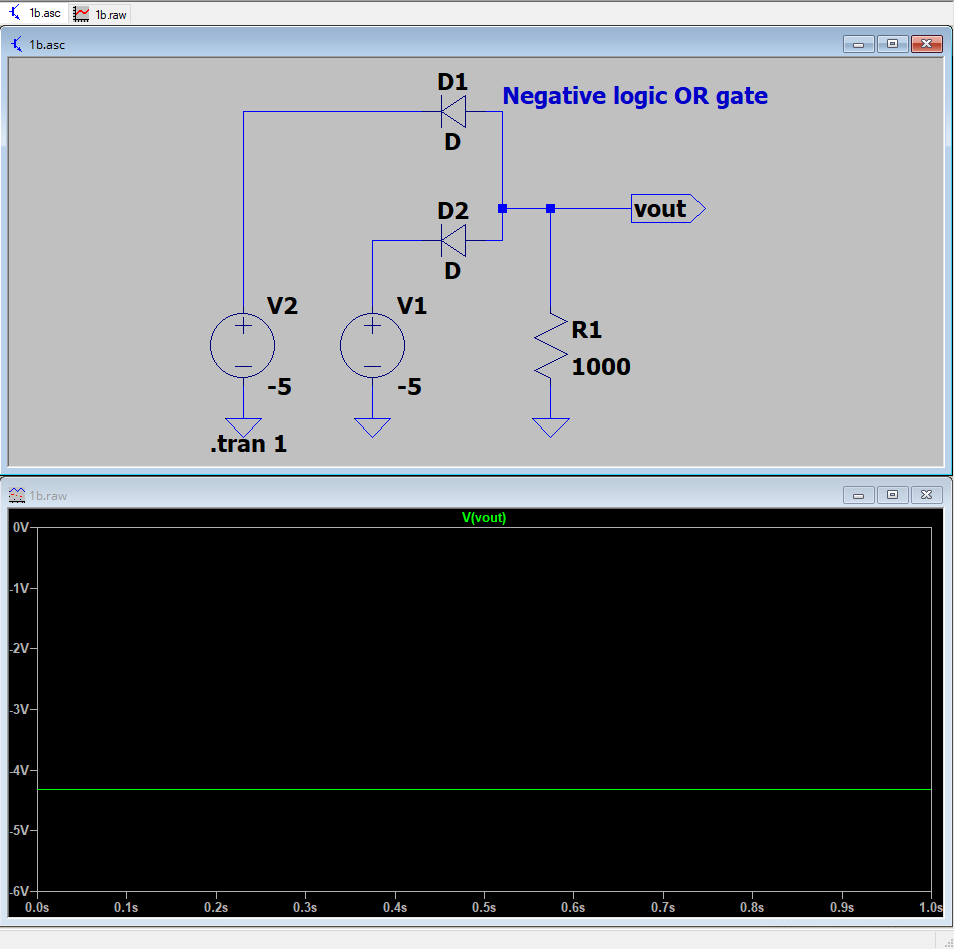
****

**As we can see, the output is -4.3V, which is expected because the Diode has a potential of its own, and we can conclude that our Vout is also high.**

**Case 3: V1=-5V, V2=-5V**

**Since both inputs are high, The expected output is high.**

**Simulation in LTspice:**

****

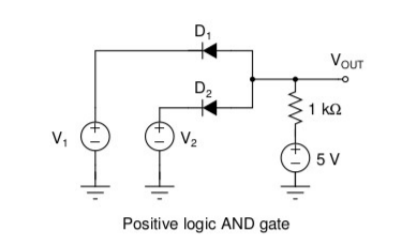
**Results:**

|  |  |  |  |
| --- | --- | --- | --- |
| V1 | V2 | Vout | Y |
| 0 | **0** | **0** | **0** |
| 0 | **-5** | **-4.3** | **1** |
| -5 | **0** | **-4.3** | **1** |
| -5 | **-5** | **-4.3** | **1** |

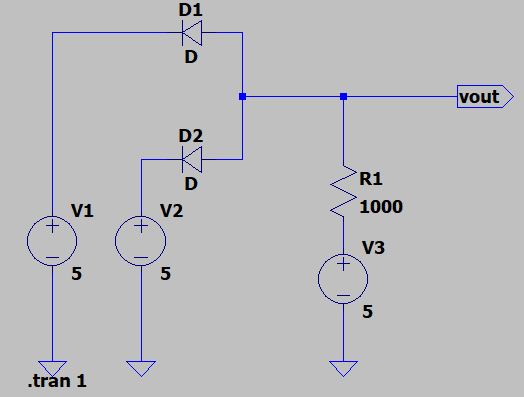
**c]** **Positive Logic AND Gate**

**Output is high whenever both of the inputs are high.**

**Circuit diagram:**

****

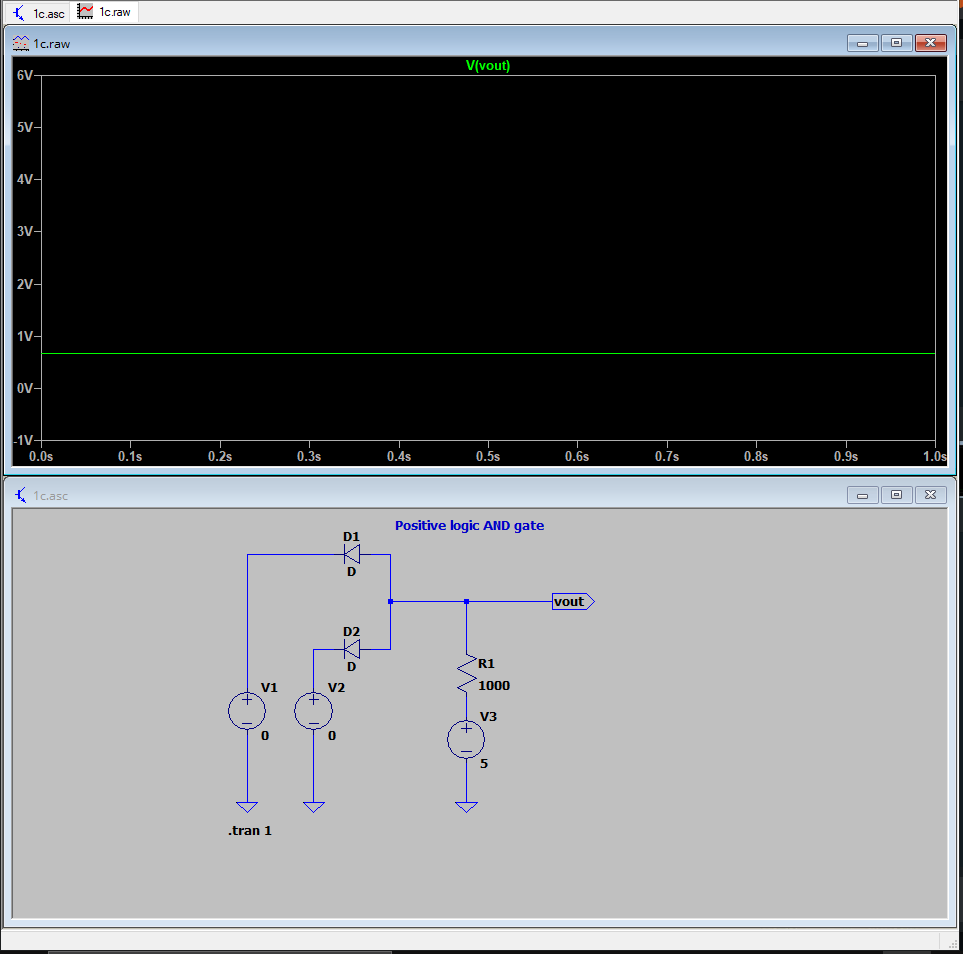
**Circuit in LTspice:**

****

**Case 1: V1=0V, V2=0V**

**Both the inputs are low So the expected output is also low.**

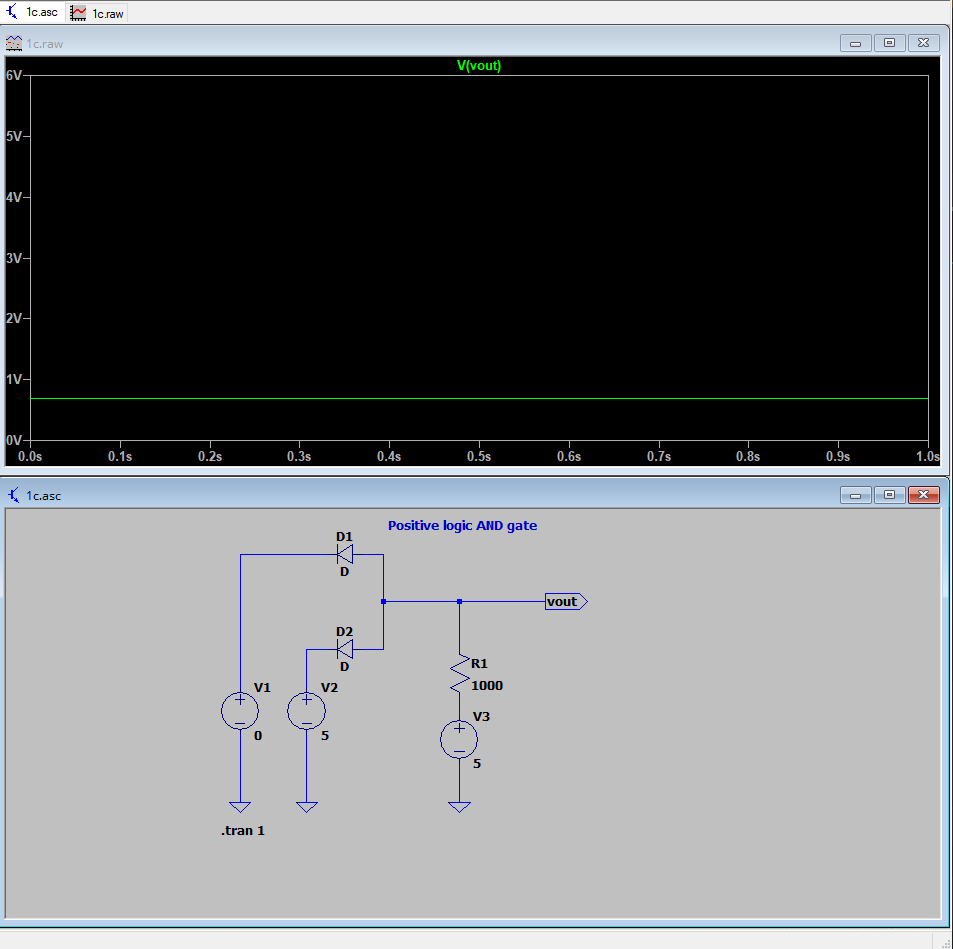
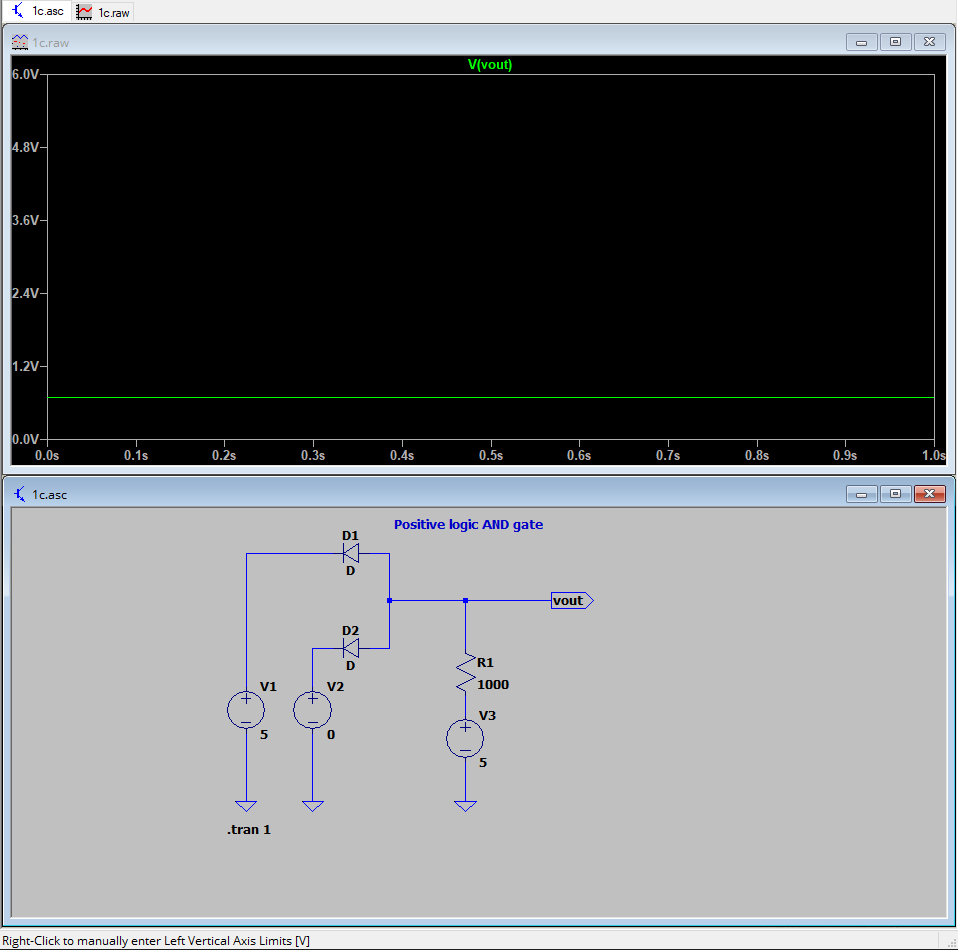
**now Simulation in LTspice:**

****

**As we can see, the output voltage Vout is 0V, which is low and is the expected output.**

**Case 2: V1=0V, V2=5V or V1=5V, V2=0V**

**Only one of the inputs is high, hence the expected output is low. Simulation in LTspice:**

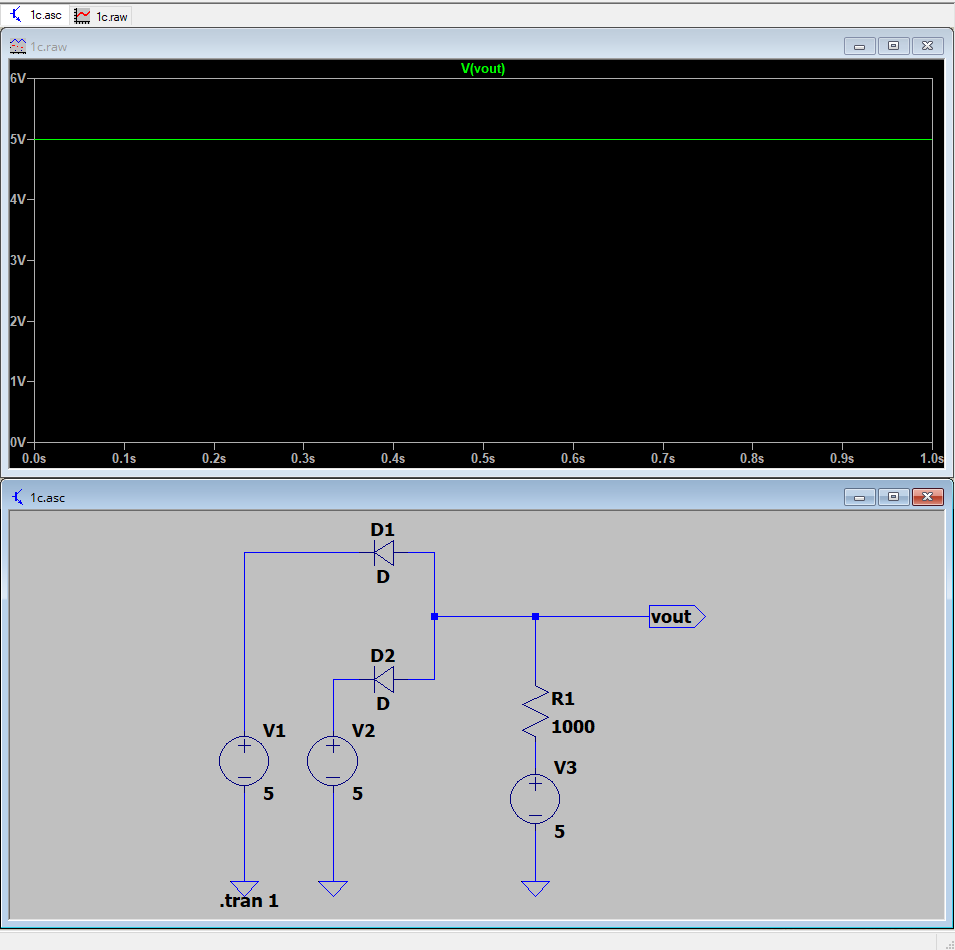
****

**As we can see, the output voltage Vout is 0V, which is low and is the expected output**

**Case 3: V1=5V, V2=5V**

**Since both inputs are high, the expected output is high.**

**Simulation in LTspice:**

****

**As we can see, the output voltage Vout is high and is the expected output.**

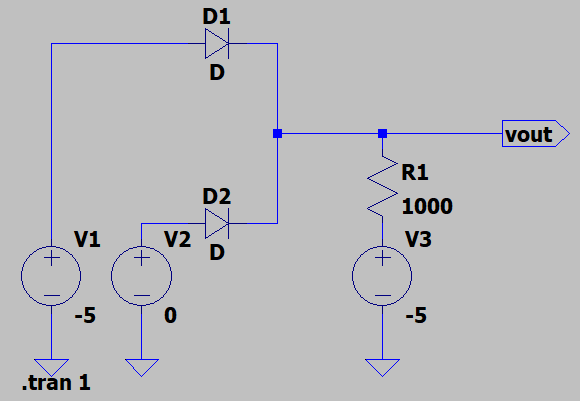
**Results:**

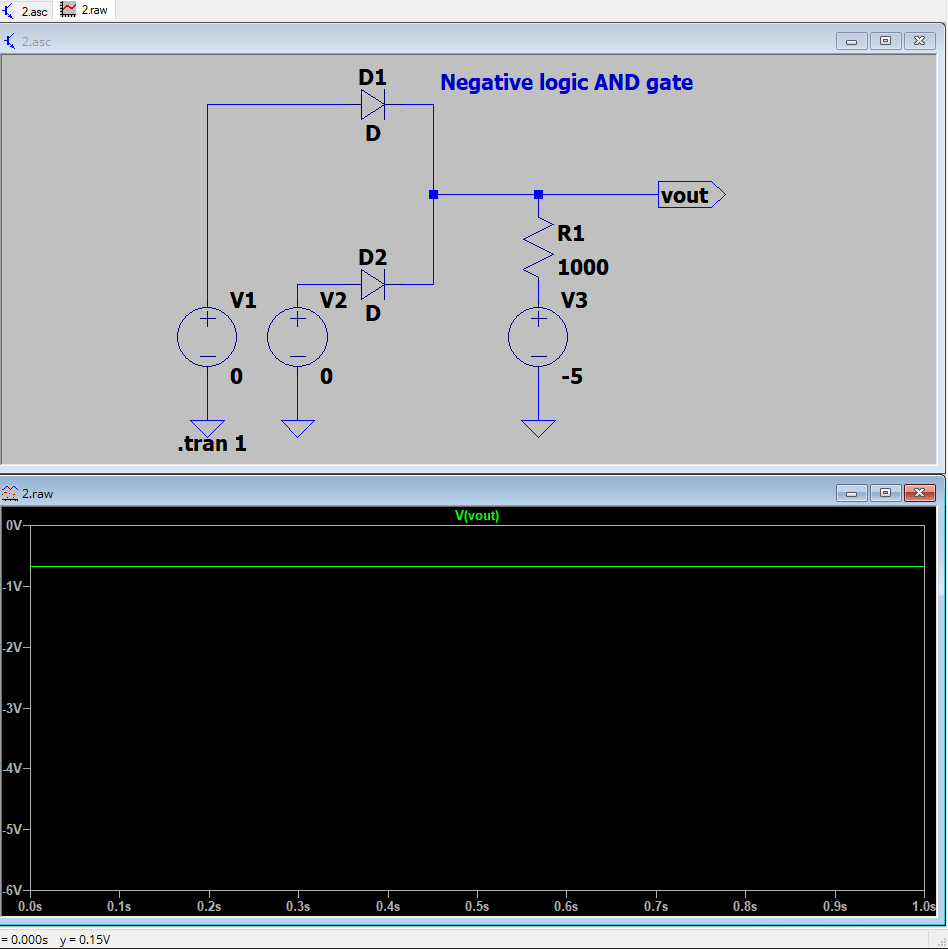
|  |  |  |  |
| --- | --- | --- | --- |
| V1 | V2 | Vout | Y |
| 0 | **0** | **0** | **0** |
| 0 | **5** | **0** | **0** |
| 5 | **0** | **0** | **0** |
| 5 | **5** | **4.3** | **1** |

**2]** **Positive Logic AND Gate**

**Output is high whenever both of the inputs are high.**

**Circuit diagram in LTspice:**

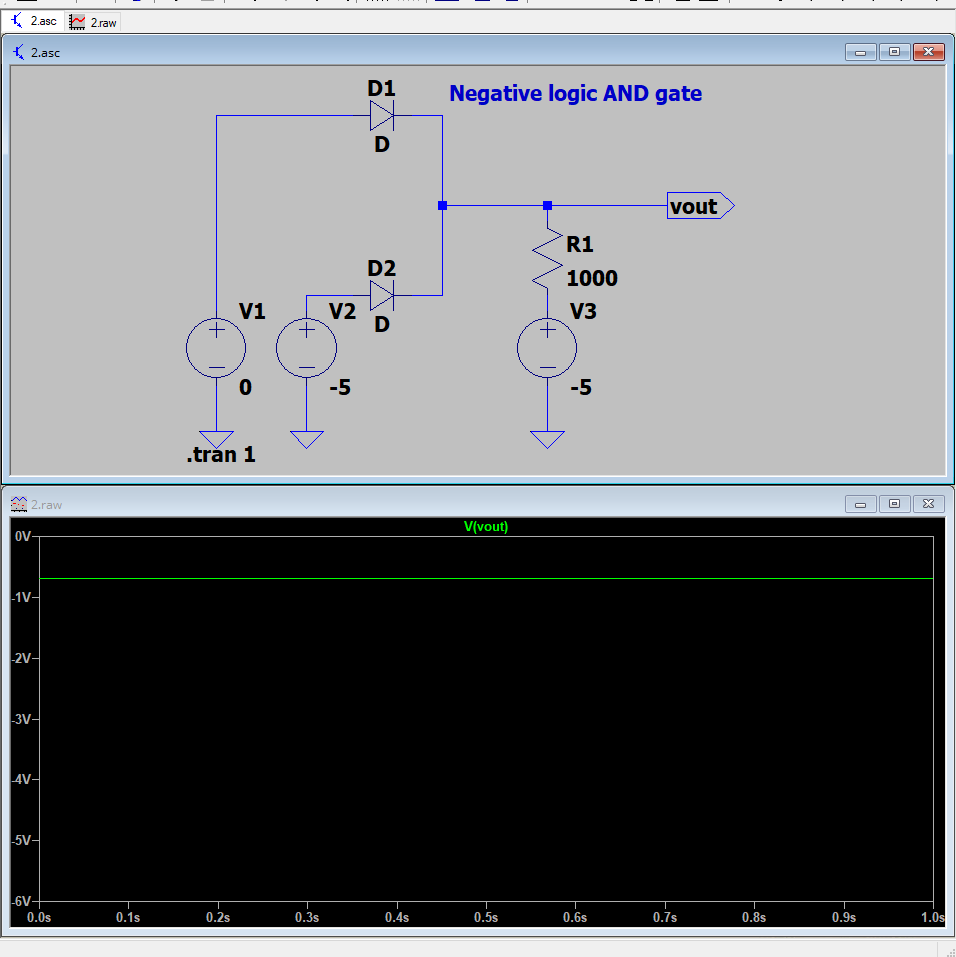
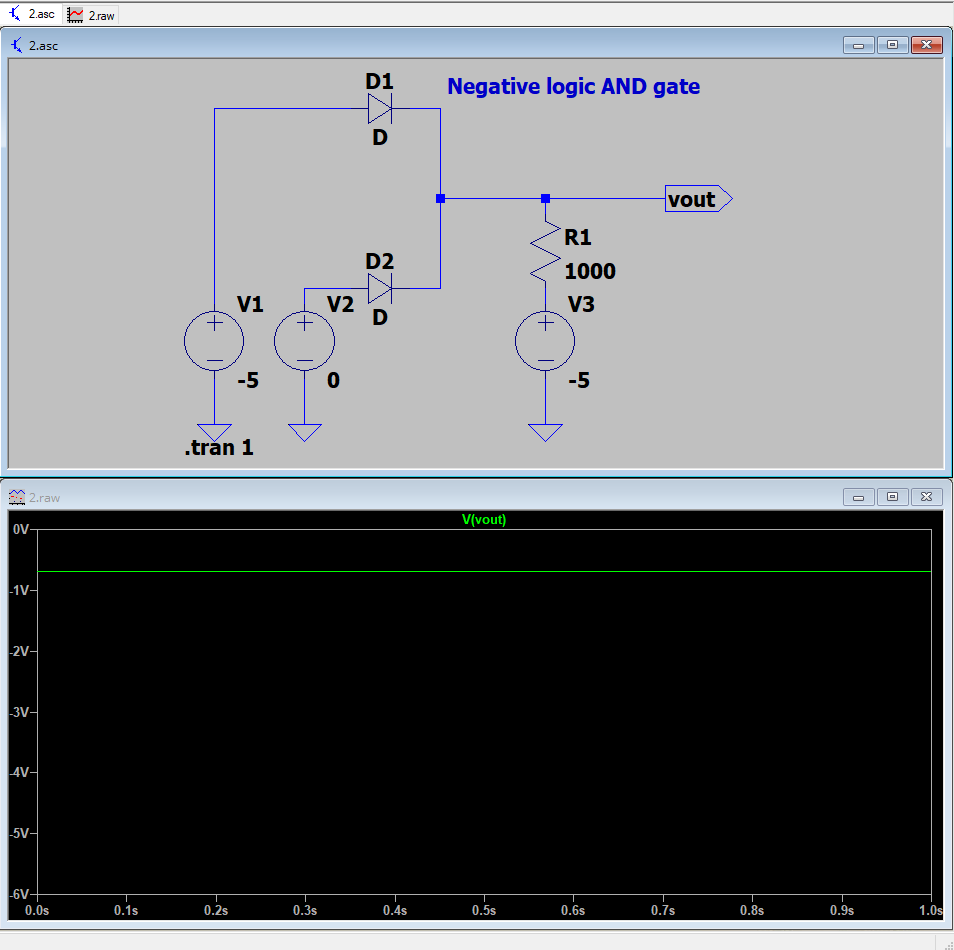
****

****

**As we can see, the output voltage Vout is 0V, which is low and is the expected output.**

**Case 2: V1=0V, V2=-5V or V1=-5V, V2=0V**

**Only one of the inputs is high, hence the expected output is low. Simulation in LTspice:**

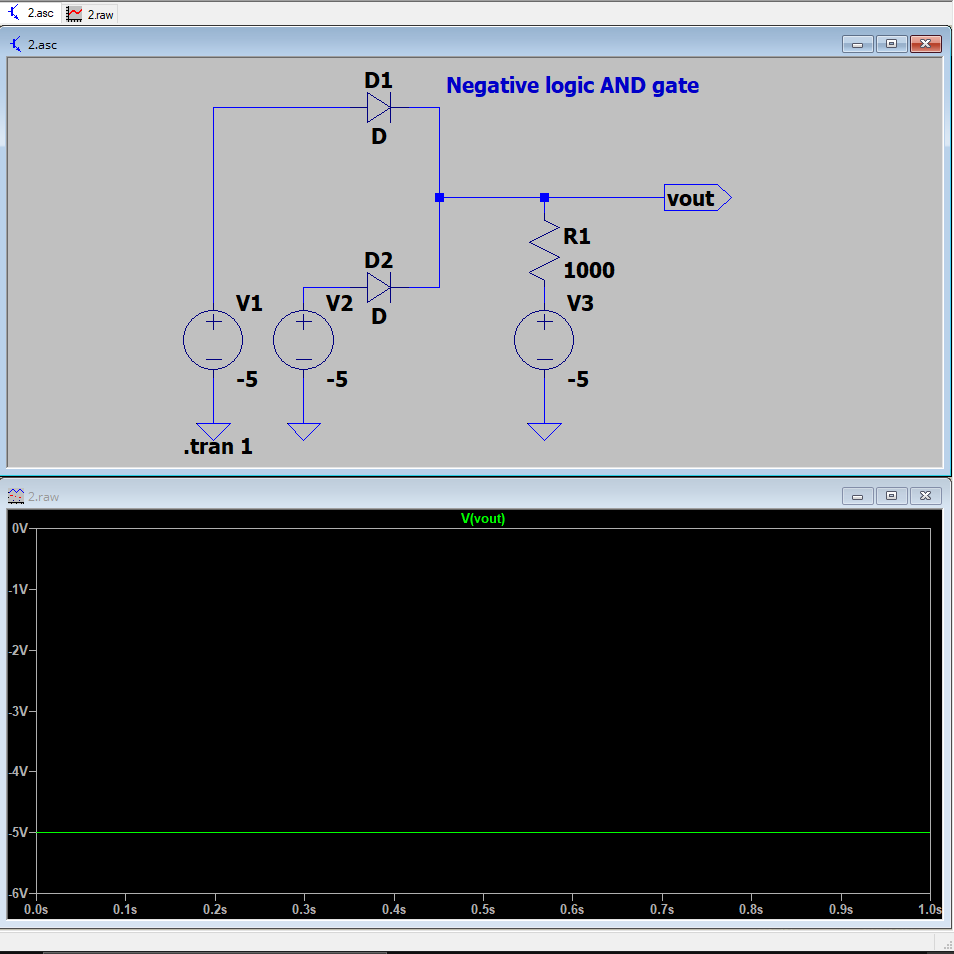
****

**As we can see, the output voltage Vout is 0V, which is low and is the expected output**

**Case 3: V1=5V, V2=5V**

**Since both inputs are high, the expected output is high.**

**Simulation in LTspice:**

****

**As we can see, the output voltage Vout is high and is the expected output.**

**Results:**

|  |  |  |  |
| --- | --- | --- | --- |
| V1 | V2 | Vout | Y |
| 0 | **0** | **0** | **0** |
| 0 | **-5** | **0** | **0** |
| -5 | **0** | **0** | **0** |
| -5 | **-5** | **-4.3** | **1** |

**2:** **List/Explain the following**

**1] Typical voltage drop across the diode (Silicon, Germanium and Gallium Arsenide) for 10mA of forward current.**

|  |  |
| --- | --- |
| **Diode** | **Voltage Drop** |
| **Silicon (Si)** | **0.7V** |
| **Germanium (Ge)** | **0.3V** |
| **Gallium Arsenide (GaAs)** | **1.2V** |

**Since the voltage drop in case of forward bias depends upon the material of the diode, it is independent of the forward current.**

**2]** **typical reverse saturation current in 1N4001 diode**

|  |  |  |
| --- | --- | --- |
| **TA** | **Reverse Saturation Current** | **Units** |
| **25 °C** | **5** | **µA** |
| **125 °C** | **50** | **µA** |

**We can see that the reverse saturation current increases with increase in temperature because it leads to more electron-hole pairs which increase the conductivity.**