

COURSE INFORMATION

1									
1.	Name of Course				Archite	cture			
2 .	Course Code		DCS						
3 .	Type of Course		Core/	Majo	r				
4 .	(e.g. : Core, major, elective etc.) Synopsis		Stude repres	ents w sentat	ill learr tion, in	n how structi	central processing on set design. The	g unit processes in e importance of me	structions, data emory systems, bus
5 .	Version (State the date of theSenate's approval - previous and the current approval of	late)						The importance of memory systems, bus pipelining techniques will be covered too. 18 , Mohd Azizi bin Sanwani, Muhammad Kamis, Nun Shwu Huey, Ruzanna binti and functions of a computer system, he importance of bus architecture, input and by introducing the historical development of The importance of this subject could be traced instructions. Independent Learning Total SLT	
6 .	Name(s) of Academic Staff		Loqm	an bir	n Sam	at, No	or Hisham bin Kar		
7.	Semester and Year Offered		+						
8.	Credit Value		4						
	Pre-Requisite		None						
	Objective of the course in the programme: To introduce the architectural and organisational design of a typic instructions processing by a processor, machine instruction design output interfaces in computer architecture.								
	Justification for including the course in the programme: To enable students to understand computer architecture as it ack computers, instruction set design, addressing modes, instruction from the basic functions of computer to the real understanding of	cycle and pi	pelinin	g as v	vell as	syste	m bus design. The	e importance of this	
14 .	Transferable Skills: Problem solving								
	Problem solving						enate Jan 2018 7 ar, Lim Liyen, Mohd Azizi bin Sanwani, Muhammad r Hisham bin Kamis, Nun Shwu Huey, Ruzanna bintin components and functions of a computer system, o discusses the importance of bus architecture, inputer organisation by introducing the historical development bus design. The importance of this subject could be and executes instructions.		
15 .	Distribution of Student Learning Time (SLT)				the of computer organisation by introducing the historical divided well as system bus design. The importance of this subject unit operates and executes instructions. State				
	Course Content Outline **CLO			rning ided (F2	Activi Learni 2F)*	ities ing	Learning	Learning	Total SLT
	<u> </u>		*L	*T	*P	*0			
	Topic 1: Introduction This chapter presents the introduction of computer architecture as well as classifications of architectures. This chapter also includes history of computers and designing for performance. Also, this chapter includes the explanation of computer components and computer functions.	CLO1, CLO2	4	2				4	10
	Topic 2: Data representations This chapter introduces the Arithmetic and Logic Unit (ALU), integer representation and integer arithmetic. This chapter also presents various number bases inclusive of binary number system and hexadecimal number system. This chapter also introduces floating-point representation.	CLO1, CLO2	6	2				6	14
	Topic 3: Instruction-Set Architecture This chapter describes machine instruction characteristics and instruction cycle. Besides, this chapter also discusses types of operands and type of operations. Also, this chapter covers data types, elements of machine instructions and instruction representations. Addressing modes is also included.	CLO1, CLO3	6	4				6	16
	Topic 4: Memory-System Architecture This chapter describes characteristics of memory and memory hierarchy. Semiconductor main memory subsystems, cache memory, cache organisation and external memory will be discussed. This chapter includes the discussion of design issues of memory system.	CLO2	6	4			2	6	18

5	Topic 5: Buses This chapter begins by differentiating internal and external bus. Bus interconnection, bus hierarchy, characteristics of bus, various bus standards such as PCI and PCI Express are also covered in this chapter.	CLO1	4	2			1	4	11	
6	Topic 6: Input Output Interfaces This chapter reviews external devices, I/O modules structure and function, I/O techniques which inclusive of programmed I/O, interrupt-driven I/O, and direct memory access (DMA). The external interfaces is also covered in this chapter.	CLO1	4	2			2	6	14	
7	Topic 7: Pipelining and RISCs This chapter introduces instruction pipelining and discusses the performance of pipelining. This chapter also describes characteristics of RISC and distinguishes between RISCs and CISCs.	CLO1	6	2			2	6	16	
8	Lab 1: Introduction to 8085 Simulator The brief introduction on 8085 simulators which inclusive of the basic operation of the simulator will be covered. Basic 8085 instructions will be introduced.	CLO4			2			2	4	
9	Lab 2: Assembly Language Program This topic will cover the assembly language program for arithmetic operations such as addition, subtraction, multiplication and division.	CLO4			4			4	8	
				ı	ı			Total SLT	111	
<u> </u>	SUMMATIVE ASSESSMENT Continuous Assessment Percentage % Total SLT									
Test	Continuous Assessment				Perc	entag 20%		Total SLT 5		
Quizz	700	10%						4		
	kulzzes ab/Tutorial Submissions ssignment		10% 10%						12 6	
			Total	SLT	or Co	ntinu	ous Assessment		27	
-			ı					7	otal SI T	
2. Fir	nal Assessment				Perc	enta	ge %	F2F	otal SLT	
	nal Assessment Exam				Perc	enta			ILT 20	
		Total	SLT fo	or Fina		50%		F2F	ILT	
Final	Exam	Total	SLT fo	or Fina	al Ass	50% essm	ent (F2F + NF2F)	F2F	ILT 20	
Final Gran **Indi					al Ass	50% essm	ent (F2F + NF2F)	F2F	ILT 20 22	
Gran **Indi *L= L	Exam Id Total licate the CLO based on the CLO's numbering in Item 12. Lecture, *T= Tutorial, *P= Practical, *O= Others, F2F*= Factify Special Requirement to Deliver the Course (e.g., software)	ce to Face,	NF2F	*= No	al Ass	50% essm 100% e to Fa	ent (F2F + NF2F)	F2F	ILT 20 22	
Final Gran **Indi *L= L Ident 8085	Exam Id Total Icate the CLO based on the CLO's numbering in Item 12. Lecture, *T= Tutorial, *P= Practical, *O= Others, F2F*= Factify Special Requirement to Deliver the Course (e.g., software simulator (j8085 simulator), Computer Lab References:	ce to Face, are, nursery	NF2F	*= No	al Ass	50% essm 100% e to Fa	ent (F2F + NF2F)	F2F	ILT 20 22	
Final Gran **Indi *L= L Ident 8085 Main Stallir	Exam Id Total Icate the CLO based on the CLO's numbering in Item 12. Lecture, *T= Tutorial, *P= Practical, *O= Others, F2F*= Factify Special Requirement to Deliver the Course (e.g., softwater instruments). Computer Lab	ce to Face, are, nursery	NF2F	*= No	al Ass	50% essm 100% e to Fa	ent (F2F + NF2F)	F2F	20 22	