

ACAD/FORM/01  
Ver. 2  
01.08.2017

8	<b>Counters</b> Asynchronous and synchronous counter. Counter timing diagram. Counter circuits. Modulus of a counter. 4-bit binary counter and a decade counter. Up/down counter. IC counter. Cascaded counter.	CLO3	4	4				8	16
9	<b>Shift Registers</b> Operation of serial in/serial out, serial in/parallel out, parallel in/serial out, and parallel in/parallel out shift register. Johnson counter. Ring counter.	CLO3	3	3				6	12
<b>Total SLT</b>								<b>112</b>	
<b>SUMMATIVE ASSESSMENT</b>									
<b>1. Continuous Assessment</b>			<b>Percentage %</b>				<b>Total SLT</b>		
Quizzes			10%				3		
Test			20%				5		
Assignments			20%				18		
Project									
<b>Total SLT for Continuous Assessment</b>							<b>26</b>		
<b>2. Final Assessment</b>			<b>Percentage %</b>				<b>Total SLT</b>		
Final Exam			50%				F2F	ILT	
							2	20	
<b>Total SLT for Final Assessment (F2F + NF2F)</b>							<b>22</b>		
<b>Grand Total</b>			<b>100%</b>				<b>160</b>		
<b>**Indicate the CLO based on the CLO's numbering in Item 12.</b>									
<b>*L= Lecture, *T= Tutorial, *P= Practical, *O= Others, F2F*= Face to Face, NF2F*= Non Face to Face</b>									
16	Identify Special Requirement to Deliver the Course (e.g., software, nursery, computer lab, simulation room):								
17	<b>Main References:</b> Floyd, T. (2015) Digital Fundamentals (11th Edition), Pearson Education International.								
18	<b>Additional References:</b> Tocci, R. J., Widmer N. S., Moss G. L. (2011). Digital System, Principles and Applications (11th Edition). Prentice Hall.								

**Note:**

Cells shaded light grey contain formulas / fixed values. Edit these formulas only if needed.