

traffic_light_controller - [C:/Users/utkar/traffic_light_controller/traffic_light_controller.xpr] - Vivado 2024.1

File Edit Flow Tools Reports Window Layout View Help Quick Access

write_bitstream Complete ✓

Default Layout

Flow Navigator

PROJECT MANAGER - traffic_light_controller

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Run Linter
- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

Sources

Source File Properties

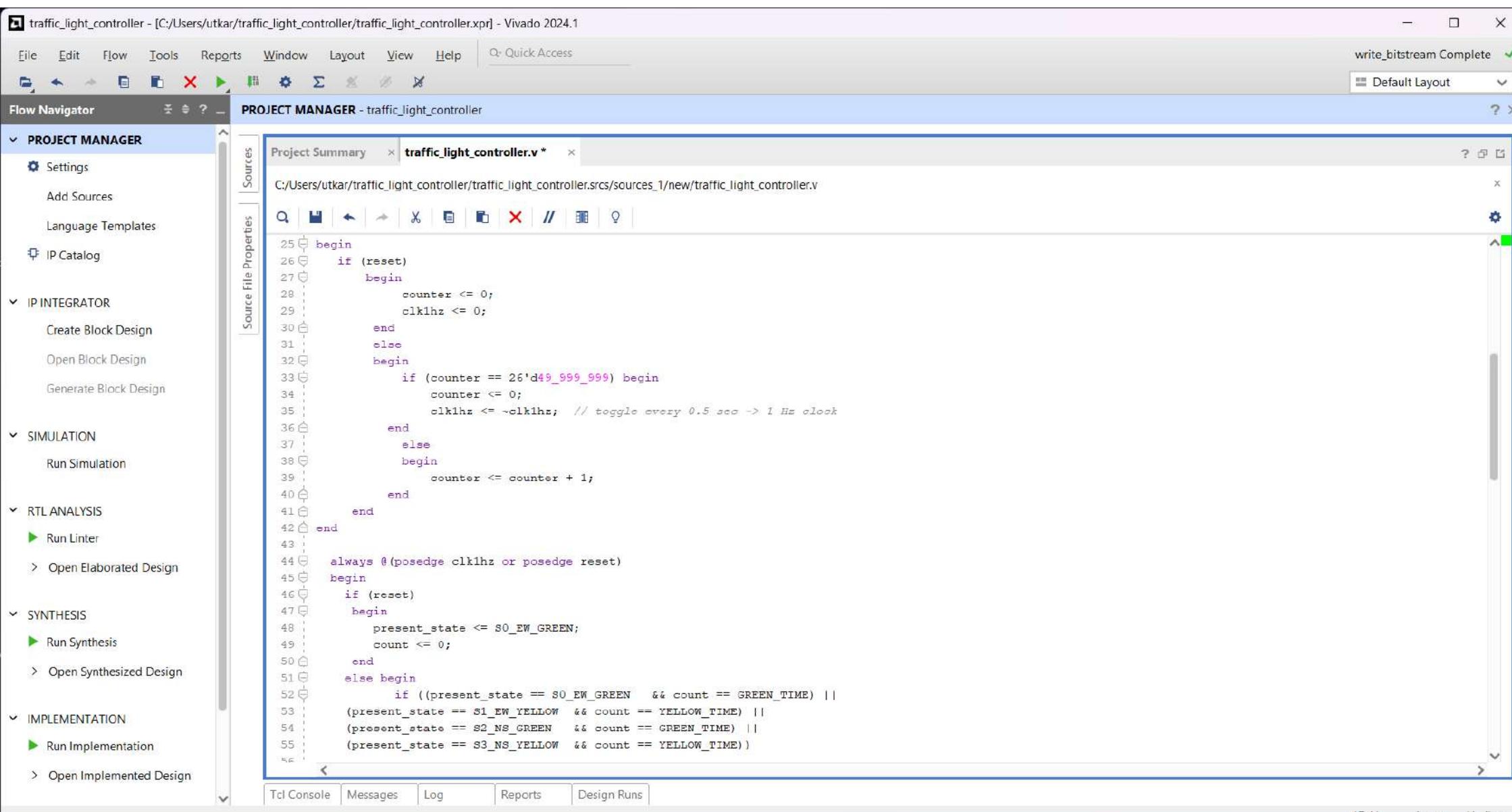
Project Summary × traffic_light_controller.v *

C:/Users/utkar/traffic_light_controller/traffic_light_controller.srcts/sources_1/new/traffic_light_controller.v

```
1 `timescale 1ns / 1ps
2 module traffic_light_controller(
3     input clk, reset,
4     output reg east_red, east_green, east_yellow, //Controls the East direction traffic lights
5     output reg west_red, west_green, west_yellow,
6     output reg north_red, north_green, north_yellow,
7     output reg south_red, south_green, south_yellow
8 );
9
10 parameter S0_EW_GREEN = 2'b00, //East-West green, North-South red
11     S1_EW_YELLOW = 2'b01,
12     S2_NS_GREEN = 2'b10,
13     S3_NS_YELLOW = 2'b11;
14
15 reg [1:0] present_state, next_state;
16 reg [3:0] count; // counts clock cycles for state duration
17 parameter GREEN_TIME = 4'd9, // 10 sec
18     YELLOW_TIME = 4'd2; // 3 sec
19
20 reg [25:0] counter;
21 reg clk1hz;
22
23
24 always @(posedge clk or posedge reset)
25 begin
26     if (reset)
27         begin
28             counter <= 0;
29             clk1hz <= 0;
30         end
31     else
32         begin
```

Tcl Console Messages Log Reports Design Runs

69:1 Insert Verilog



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PROJECT MANAGER - traffic_light_controller

Project Summary × traffic_light_controller.v *

C:/Users/utkar/traffic_light_controller/traffic_light_controller.srcts/sources_1/new/traffic_light_controller.v

Source File Properties Sources

```
56 begin
57     count <= 0;
58     present_state <= next_state;
59 end
60 else
61 begin
62     count <= count + 1;
63 end
64 end
65 end
66 end;
67
68 always @(*)
69 begin
70     case(present_state)
71         S0_EW_GREEN:   next_state = S1_EW_YELLOW;
72         S1_EW_YELLOW:  next_state = S2_NS_GREEN;
73         S2_NS_GREEN:   next_state = S3_NS_YELLOW;
74         S3_NS_YELLOW:  next_state = S0_EW_GREEN;
75         default:       next_state = S0_EW_GREEN;
76     endcase
77 end
78
79 always @(*)
80 begin
81     east_red = 0; east_yellow = 0; east_green = 0;
82     west_red = 0; west_yellow = 0; west_green = 0;
83     north_red = 0; north_yellow = 0; north_green = 0;
84     south_red = 0; south_yellow = 0; south_green = 0;
85
86     case(present_state)
87         S0_EW_GREEN:
```

Tcl Console Messages Log Reports Design Runs

17:41 Insert Verilog

The screenshot shows the Vivado 2024.1 interface with the 'traffic_light_controller' project open. The 'PROJECT MANAGER' is visible on the left, and the 'Sources' tab is selected in the center. A code editor window displays the Verilog source file 'traffic_light_controller.v'. The code implements a state machine with four states: S0_EW_GREEN, S1_EW_YELLOW, S2_NS_GREEN, and S3_NS_YELLOW. It also handles traffic light signals for East, West, North, and South directions. The code uses a counter to manage transitions between states and assign colors to each signal. The Vivado interface includes various toolbars and status indicators at the top and bottom.

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PROJECT MANAGER - traffic_light_controller

Project Summary traffic_light_controller.v *

C:/Users/utkar/traffic_light_controller/traffic_light_controller.srcts/sources_1/new/traffic_light_controller.v

```
85 case(present_state)
86     S0_EW_GREEN:
87         begin
88             east_green = 1;
89             west_green = 1;
90             north_red = 1;
91             south_red = 1;
92         end
93     S1_EW_YELLOW:
94         begin
95             east_yellow = 1;
96             west_yellow = 1;
97             north_red = 1;
98             south_red = 1;
99         end
100    S2_NS_GREEN:
101        begin
102            north_green = 1;
103            south_green = 1;
104            east_red = 1;
105            west_red = 1;
106        end
107    S3_NS_YELLOW:
108        begin
109            north_yellow = 1;
110            south_yellow = 1;
111            east_red = 1;
112            west_red = 1;
113        end
114    endcase
115 end endmodule
```

Tcl Console Messages Log Reports Design Runs

115:6 Insert Verilog