

traffic_light_controller - [C:/Users/utkar/traffic_light_controller/traffic_light_controller.xpr] - Vivado 2024.1

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PROJECT MANAGER - traffic_light_controller

Project Summary x traffic_light_controller.v * x

C:/Users/utkar/traffic_light_controller/traffic_light_controller.srcs/sources_1/new/traffic_light_controller.v

timescale 1ns / 1ps
module traffic_light_controller(
input clk, reset,
output reg east_red, east_green, east_yellow, //Controls the East direction traffic lights
output reg west_red, west_green, west_yellow,
output reg north_red, north_green, north_yellow,
output reg south_red, south_green, south_yellow
);

parameter S0_EW_GREEN = 2'b00, //East-West green, North-South red
S1_EW_YELLOW = 2'b01,
S2_NS_GREEN = 2'b10,
S3_NS_YELLOW = 2'b11 ;

reg [1:0] present_state, next_state;
reg [3:0] count; // counts clock cycles for state duration
parameter GREEN_TIME = 4'd9, // 10 sec
YELLOW_TIME = 4'd2; // 3 sec

reg [25:0] counter;
reg clk1hz;

always @(posedge clk or posedge reset)
begin
if (reset)
begin
counter <= 0;
clk1hz <= 0;
end
else
begin

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69:1InsertVerilog

traffic_light_controller - [C:/Users/utkar/traffic_light_controller/traffic_light_controller.xpr] - Vivado 2024.1

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Project Summary x traffic_light_controller.v * x

C:/Users/utkar/traffic_light_controller/traffic_light_controller.srscs/sources_1/new/traffic_light_controller.v

```
25 begin
26   if (reset)
27     begin
28       counter <= 0;
29       clk1hz <= 0;
30     end
31   else
32     begin
33       if (counter == 25'd49_999_999) begin
34         counter <= 0;
35         clk1hz <= ~clk1hz; // toggle every 0.5 sec -> 1 Hz clock
36       end
37     else
38       begin
39         counter <= counter + 1;
40       end
41     end
42   end
43
44   always @(posedge clk1hz or posedge reset)
45   begin
46     if (reset)
47       begin
48         present_state <= S0_EW_GREEN;
49         count <= 0;
50       end
51     else begin
52       if ((present_state == S0_EW_GREEN && count == GREEN_TIME) ||
53         (present_state == S1_EW_YELLOW && count == YELLOW_TIME) ||
54         (present_state == S2_NS_GREEN && count == GREEN_TIME) ||
55         (present_state == S3_NS_YELLOW && count == YELLOW_TIME))
```

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17:41 Insert Verilog

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Project Summary x traffic_light_controller.v x

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```
56
57     begin
58         count <= 0;
59         present_state <= next_state;
60     end
61     else
62     begin
63         count <= count + 1;
64     end
65 end
66 end
67
68 always @(*)
69 begin
70     case(present_state)
71         S0_EW_GREEN: next_state = S1_EW_YELLOW;
72         S1_EW_YELLOW: next_state = S2_NS_GREEN;
73         S2_NS_GREEN: next_state = S3_NS_YELLOW;
74         S3_NS_YELLOW: next_state = S0_EW_GREEN;
75         default: next_state = S0_EW_GREEN;
76     endcase
77 end
78
79 always @(*)
80 begin
81     east_red = 0; east_yellow = 0; east_green = 0;
82     west_red = 0; west_yellow = 0; west_green = 0;
83     north_red = 0; north_yellow = 0; north_green = 0;
84     south_red = 0; south_yellow = 0; south_green = 0;
85
86     case(present_state)
87         S0_EW_GREEN:
```

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```
85 case(present_state)
86   S0_EW_GREEN:
87     begin
88       east_green = 1;
89       west_green = 1;
90       north_red = 1;
91       south_red = 1;
92     end
93   S1_EW_YELLOW:
94     begin
95       east_yellow = 1;
96       west_yellow = 1;
97       north_red = 1;
98       south_red = 1;
99     end
100  S2_NS_GREEN:
101    begin
102      north_green = 1;
103      south_green = 1;
104      east_red = 1;
105      west_red = 1;
106    end
107  S3_NS_YELLOW:
108    begin
109      north_yellow = 1;
110      south_yellow = 1;
111      east_red = 1;
112      west_red = 1;
113    end
114  endcase
115 end endmodule
```

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115.6 Insert Verilog