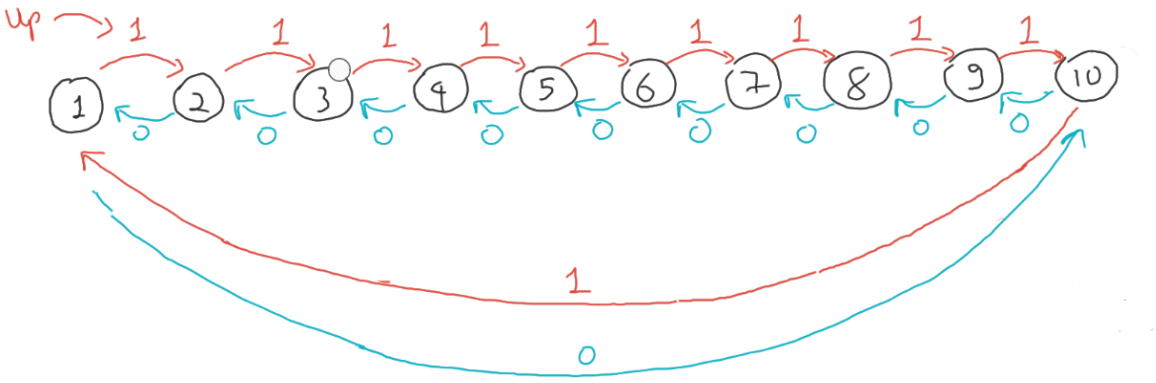
Assignment-5 (CS 232) by Utkarsh Ranjan

mod-10 up-down counter

Idea

- The simple state machine had just two states 0 and 1.
- This state was being changed in every rising edge of the clock if x was '1' else it was kept same
- Here, we implemented a mod-10 up-down counter using the same idea but with 10 states 0-9, each state is a 4-bit std_logic_vector(3 downto 0) which is increased/decreased based on the input up being '1'/'0' respectively at every rising edge of the clock.

Following diagram would explain the design :-



State	1	2	3	4	5	6	7	8	9	10
Encoding	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001