Assignment 7

Description of design:

There is a traffic junction with five lanes L0, L1, L2, L3 & L4. Among these, L1 & L4 are small side lanes with light traffic, and the rest are highways with heavy traffic. To control the traffic, placed at the centre of the junction is a single traffic signal lights pole which has 15 lights - 3 for each lane - red, green and yellow. You need to design a digital circuit called a traffic lights controller to control these 15 lights. The controller has 15 output wires connected to each of the lights. The controller turns on a particular light by sending a logic '1' on the corresponding wire and turns off the same by sending a logic '0'.

At a time only one lane should be given a green signal, and during that time, the rest of the lanes should be given a red. After a green on a particular lane, yellow should be given on the same lane for a short while, after which it turns red, and simultaneously the next lane will be made green. The green signal duration for the smaller lanes (L1 & L4) is 30 seconds. For the rest of the lanes, which are highways, it is 60 seconds. Also on the smaller lanes, some sensors are placed which will try to detect the traffic. If there is no one waiting on the smaller lanes then they will not be given green and skipped to the next lane. If there is at least one person on the lighter lane, only then it will be given a green for 30 seconds. The yellow signal duration is 5 seconds for all the lanes. As soon as the traffic lights controller is powered on (which is the same as making the reset input of the circuit high for one clock cycle), L2 should be given a green followed by L3, L4, L0 and L1. After L1, the pattern repeats again from L2, and it keeps going on infinitely. The entity statement is given below, and the purpose of the outputs is intuitive. 'tr1' and 'tr4' inputs are coming from the sensors placed on the smaller lanes. If 'tr1' is logic '1', then it means there is some traffic on lane L1. If it is '0' then it means there is no one on lane L1 and it is completely free. Similarly 'tr4' is for lane L4. **The clock frequency should be fixed, and it should not vary during the operation of the circuit.**

```
entity TrafficLightsController is
        port ( clk, rst, tr1, tr4  : in std_logic;
        r, g, y: out std_logic_vector (4 downto 0) );
end entity;
```

Things required in Submission:

1. All VHDL files of top-level and sub-components and also the **testbench** (.vhd or .vhdl files).
2. Screenshot of Waveforms (Few input patterns are sufficient).
3. A report explaining how you designed (pdf format).

Submission rules:

1. **Deadline:** Sunday (20h Mar 2022), 23:59 pm.
2. Create a folder named **lab7** (all small letters and no spaces).
3. Inside the folder, put all the .vhd or .vhdl files of both top-level entity and sub-components. Also, in the same folder, put the related waveform screenshots and the pdf report.
4. Finally, before you submit the lab7 folder on moodle, you will be zipping it. The zip file should have your id number as the name. For eg: if your id is 184070026 then your zip file will be 184070026.zip.