Design and analysis of second order sigma delta modulator*

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***Abstract*—Converters are generally the bottleneck of a mixed technology system. Process control measurement requires modulator with resolution of 16 bits and operating input frequency from 1 to 100 Hz. The designed system will reduce the dependency process control operation on high precision analog circuits. They are best for applications that manage to provide very high resolution at comparatively lower frequencies. Nyquist rate converters cannot provide good accuracy with high-speed conversion. In contrast, Delta Sigma Modulators are able to provide a better resolution at a reasonable conversion speed. The objective of this paper is to simulate and analyze a stable, second-order Delta Sigma Modulator of CIFB topology in three different levels, Hardware-level (ADS1115 and ESP8266), Circuit level (LTSpice) and Software level (MATLAB) and analyze the findings in the time domain and frequency domain. For a given oversampling ratio of 512, the aim is to achieve an optimal SQNR of 125 dB which leads to better performance overall with the use of the same lower resolution ADC. The ideal converter is simulated and designed in MATLAB and the practical behaviour of the system is simulated in LTSpice.**

Keywords: ADC, CIFB topology, Delta-Sigma Modulation, Frequency Domain Analysis, Oversampling Ratio, Signal to Noise Ratio, Switched Capacitor Cirucits

I. Introduction

The evolution of CMOS technology over the last few decades has allowed the accomplishment of major reduction in size and increase in speed of digital devices. The latest INTEL® CORE™ SKL Core i9-7000X has 7 billion transistors on board. The power consumption of these devices has reduced dramatically, enabling a huge increase in efficiency. The design of Delta Sigma Modulators reaches these application requirements featuring low power consumption and standard CMOS fabrication [4].

Convertors are generally the bottleneck of a mixed technology system. The resolution, dynamic range and speed requirements have increased with the advancement of technology that uses it. The analog part of ADCs are generally implemented in digital CMOS processes and hence are not fully optimized. Among the existing topologies, the Delta Sigma Modulator is most suitable for SOC implementation as it is able to achieve high accuracy at a reasonable speed. This leverages the digital CMOS processes and is relatively insensitive to variations during fabrication. Electrical energy measurement applications require a bandwidth that ranges from 40Hz to 2kHz and high accuracy which can easily be achieved by Sigma-delta Modulators.

The need for Sigma Delta modulators can be understood by looking at the 4 pillars of a delta sigma modulators namely, Oversampling, Noise shaping, Digital filtering and Decimation as shown in figure 1. It can be observed how they provide cost effective, higher resolution conversion from the analog domain to the digital domain [7]. The SDM is an Analog to Digital convertor that has an oversampling architecture. This oversampling enables us to achieve a higher resolution with the use of the same lower-resolution ADC. When performing the FFT analysis on the digital output, there exists a single tone and lots of random noise, known as quantization noise. In essence, this noise is shaped away from our interest region by sampling the signal at a frequency that is much higher than the Nyquist rate [4]. The number of states of the digital output is determined by the convertor's resolution and the magnitude of the error arising due to conversion from analog to digital can vary from +LSB to -LSB. One main Figure of Merit that quantifies the performance of the ADC is Signal to Quantization Noise Ratio (SQNR). For 1-bit Quantizer of second order with Oversampling ratio of 512, the expected SQNR is 126dB, as shown in figure 2. SQNR of 1-bit Quantizer can be calculated with the help of equation 1.

$$SQNR = 6.02 * (N) + 1.76\ dB + 10 * log_{10}\ \frac{f_s}{2 * BW} \quad (1)$$

Hence, to increase the resolution, the number of bits needs to be increased or the order of the modulator must be increased [9]. However, as the number of integrators increase, there is a possibility of instability due to accumulation of large signals at the integrator. Hence, an architecture of several first order integrators cascaded together is suggested. In addition to this, the use of an over-sampled input signal, reduces the noise floor

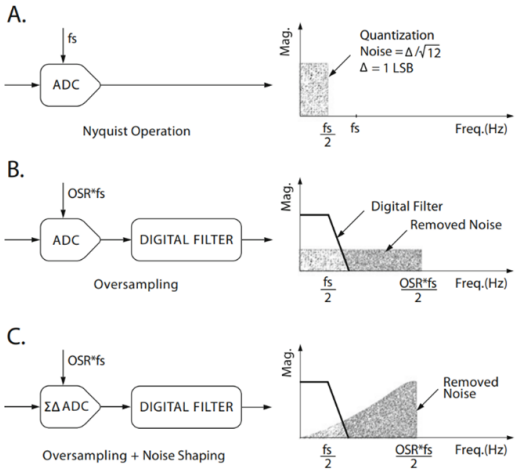


Fig. 1. Pillars of sigma-delta modulator

with the SNR remaining constant. Thus, providing a wider dynamic range from a low-resolution ADC. A problem that arises now is Hardware limitations in the real world. These often hinder technical realization of theoretical concepts. For a 1-bit ADC to achieve the 16-bit resolution, the signal must be over sampled by the factor of 4^{15} [7].This is not realizable. However, this barrier is overcome with the help of noise shaping.

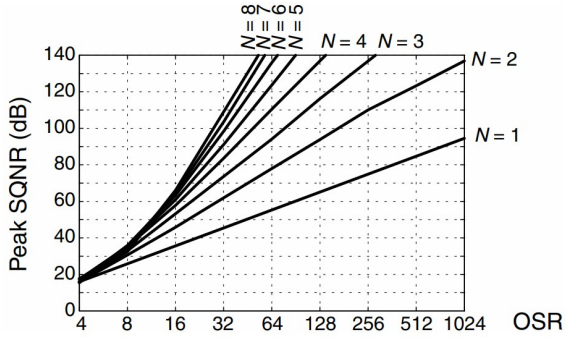


Fig. 2. SQNR limit for 1-bit Quantizer, N^{th} order

Looking at the structure of a second order DSM, the purpose of the feedback DAC is to maintain the average output of the integrator near the comparator's reference level. The integrator, which gets the difference of the input signal and the feedback signal, acts as a low pass filter to the input signal and thereby limits the quantization noise. This keeps the desired signal in the low frequency range and pushes the unwanted noise to the higher frequencies, acting like a low pass filter. Thereby enabling the removal of more noise than simple oversampling. A second order DSM results in an increase of 2.5 bits of additional resolution, and a 15 dB improvement in SNR for every doubling of sampling rate [7].

The output of the DSM is a data stream whose sampling rate can be in the order of MHz. Digital filtering and decimation enable reduction of this data rate. The digital filter, in the case of a DSM is a SINC filter whose order must be one greater than the order of the modulator used. In this case, it is a SINC filter of order 3. This performs down sampling in 3 steps in order to make sure stability is not lost. A droop correction filter is then employed in order to correct for the damping produced by the SINC filters. This droop correction filter compensates the magnitude loss caused by the SINC filter. The corrected signal is then sent into a Decimation filter which comprises of 2 half band filters. This preserves only certain input samples and discards the rest [3].

II. MATLAB & SIMULINK

A. Design specifications

The given specifications for the design of 2nd order Delta Sigma MOdulator in MATLAB can be found in TABLE 1. For the specified Signal Bandwidth (BW) of 215 Hz and Oversampling ratio (OSR) of 512, the nyquist frequency will be twice that of signal bandwidth.

TABLE I
DESIGN SPECIFICATION PARAMETER VALUE

Parameter	value
Order of Modulator	2
Number of bits	16
Oversampling ratio	512
Number of bits	16
Bandwidth	215 Hz
Nyquist frequency	430 Hz
Sampling frequency	220 KHz

$$f_n = Nyquist\ frequency = 430\ Hz \tag{2}$$

Sampling frequency can be calculated with the help of over-sampling ratio. It is calculated as 220 KHz.

$$Over\ sampling\ Ratio = OSR = \frac{f_s}{f_n} \tag{3}$$

$$f_s = OSR * f_n = 220\ KHz \tag{4}$$

B. Noise transfer function synthesis

The design of second order DSM consists of two integrators cascaded together, the NTF can be generalized into a second order transfer function for Simulink. For MATLAB, a NTF is generated using the already existing Delts Sigma Toolbox by R. Schrier. This NTF depends on the order of the modulator and the oversampling ratio being used. The NTF generated is shown in equation 5.

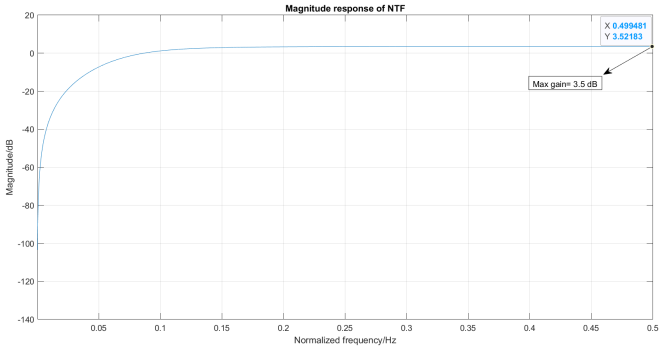
$$NTF = \frac{(z-1)^2}{z^2 - 1.225z + 0.4415} \tag{5}$$

This generated NTF along with the form- "Cascaded Integrator Feedback" can be used to realize the gains being used for the circuit. The calculated coefficients after accounting for scaling are shown in table II.

These constants were used as gains in the Simulink circuit to model the second order Delta Sigma Modulator.Another

TABLE II
GAIN COEFFICIENTS REALIZED VALUES FROM NTF

Coefficients	value
a_1	0.1131
a_2	0.1829
b_1	0.1131
b_2	0
c_1	0.4517
c_2	4.2369



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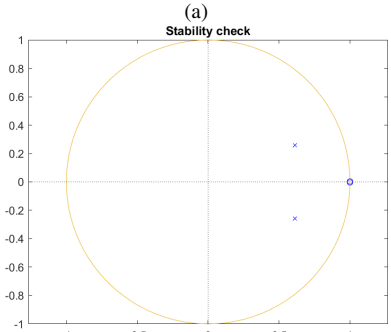


(b)

Fig. 3. Magnitude and stability analysis of NTF.

important focus was to make sure that the designed modulator is stable. This was ensured by plotting the pole zero map and checking if the zeroes were inside the unit circle as shown in figure 3.

C. Simulink design

The Simulink design follows the Cascaded Integrator Feedback form. It consists of 2 Integrators and the calculated [a b c] gains inherited/ supplied directly from the MATLAB workspace. The integrator leads onto a comparator which converts the analog signal into the digital domain and supplies it as the output of the system.

D. Decimation filter

The signal at the output of the Delta Sigma Modulator is still in the oversampled range. This needs to be decimated with the use of digital filters to reduce the output data rate. This is done with the help of SINC filters and Half band filters. The order of the SINC filter must be one greater the order of the modulator. Since a 2nd order modulator is taken into the consideration, the order of the SINC filter must be 3. The SINC/ Moving average

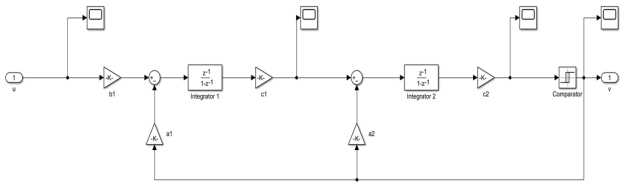


Fig. 4. Simulink model for second order cascaded Integrator Feedback form for sigma-delta modulator.

filter down samples the incoming signal. However, to ensure stability, this is done in steps. In this case, down sampling is done in 3 steps. The output of this is then sent to a droop correction filter to compensate for the damping produced by the previous stage of digital filtering. This output is then passed onto two Half band filters to bring the output to Nyquist rate. These filters are implemented directly in MATLAB. The output of one filter is passed onto the other by the means of convolution. After ensuring a stable modulator, the data obtained is analysed in the time and frequency domain.

E. Result and Discussion

The stability of the Delta Sigma modulator can be confirmed by the fact that the zeroes of the Noise Transfer Function lie within the unit circle. A stable second order DSM has been designed. Now, observing the time domain and frequency domain analysis.

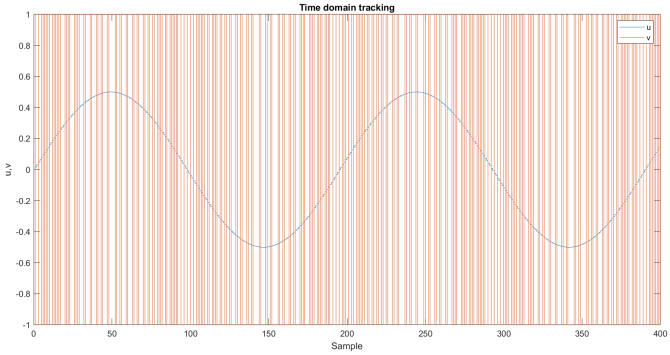


Fig. 5. Time domain tracking of second order sigma-delta modulator

From figure 5, it can be observed that when the sinusoidal input to the Delta Sigma Modulator is nearby plus full-scale value, the output is positive during most of the clock cycles. Similarly, when the input is close to negative full scale, the output is negative during most clock cycles and when the input is near zero, the output of the modulator continuously oscillates between the positive and negative boundary of output. In both cases of positive and negative full scale the output of the modulator tracks the input signal. This proves that the modulator is working.

Upon frequency domain analysis of the input signal and modulator output, it can be observed in figure 6 that the output tracks the input. The pink line would the expected output, whereas the blue line represents the simulated Delta Sigma

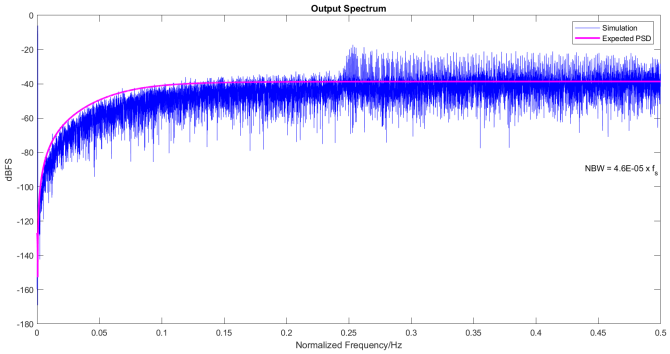


Fig. 6. Frequency domain tracking of second order sigma-delta modulator

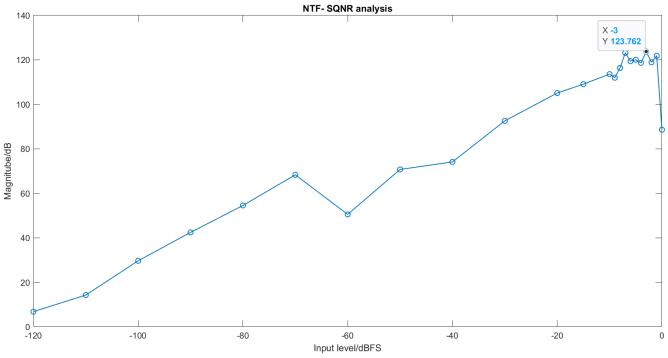
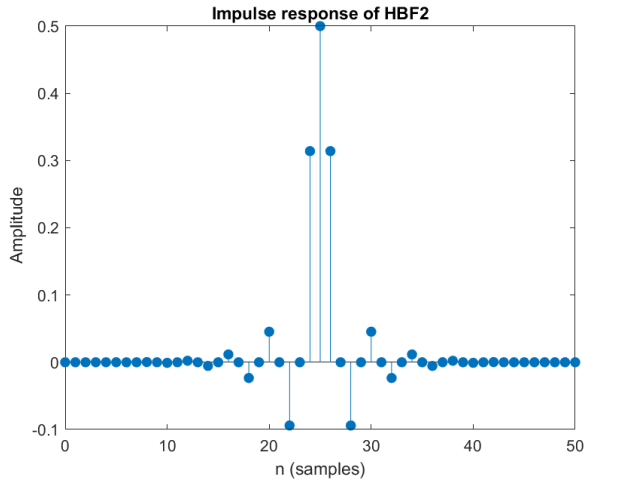


Fig. 8. SQNR analysis of noise transfer function (NTF), peak SQNR = 123.762 dB.



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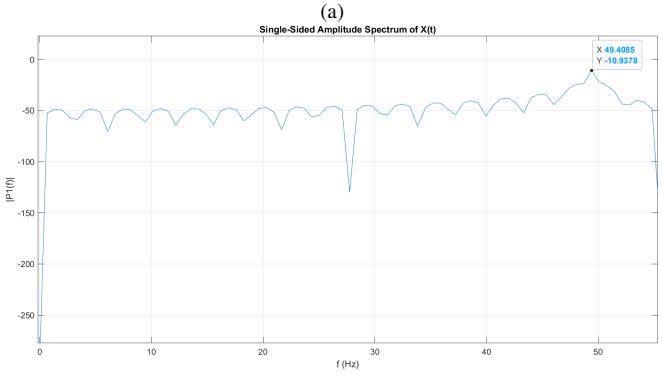

(b)

Fig. 7. Impulse response and FFT analysis of second half band filter (HBF2) at 50Hz input frequency.

Modulator output. The blue line is a combination of the peak of input sinusoid and some high frequency noise. The high frequency noise is one of the desirable properties of the Delta Sigma Modulator as it shifts the quantization noise to higher frequencies, away from our interest band.

The oversampling of the DSM was reduced and the data rate was brought down to Nyquist rate with the help of digital filtering. This is can be observed in the impulse response of HBF2 as shown in figure 7.

Ideal SNR after digital filtering, can be given by equation 1. The use of digital filtering to the output of ADC adds a correction factor, called process gain to the SNR equation. This results in the increase in SNR from the expected 98 dB to 125 dB.

Substituting N=16, fs= 220,000 Hz and BW= 215 Hz Ideal SNR= 125.169 dB. From the NTF-SQNR analysis, peak SQNR obtained is 123.762 dB as shown in figure 8. This is close to the ideal 125.169 dB. An ideal, stable second order DSM was designed in matlab.

III. LTSPICE SIMULATION

Based on design considerations and gain realization in MATLAB, the circuit level simulation of second order Sigma-delta Modulator has been done in LTSpice. Table III depicts the design parameter for the design of second order high resolution Sigma delta Modulator.

TABLE III
DESIGN PARAMETER VALUE

Parameter	value
Order	2
Oversampling ratio	512
Vdd	3.0V
Vcm	1.5V
Input frequency	5Hz,10Hz,20Hz,50Hz,100Hz

A clock rate of 1MHz yields an oversampling ratio of 512 []. The ideal SQNR for 1 -bit quantizer at an oversampling ratio of 512 is about 125dB. This has been achieved in MATLAB. The input voltage is taken as 1.2V to simplify the circuit design.

A. Circuit design

The LTspice circuit is realized using the simulink block diagram drawn in MATLAB. This is done in LTSPice with the use of a switched capacitor circuit design. First,the swing of each integrator output is determined and each stage is scaled so that the Simulink output is within the anticipated range of the operational amplifier in LTspice. From figure (simulink), all the cofficients a1, a2, b1, c1 except c2 play a part to determine the capacitance ratio. Switched capacitor topology of second

order delta sigma modulator circuit is shown in figure 9 and an associated timing diagram topology is shown in figure 10.

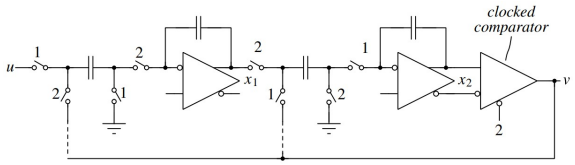

Fig. 9. Circuit design topology of second order sigma-delta modulator [7]

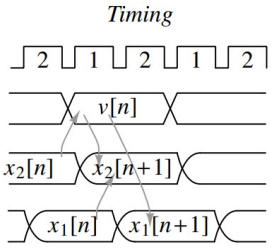

Fig. 10. Timing diagram topology of second order sigma-delta modulator [7]

Subsequent difference equation of first and second operational amplifier is shown in equation 6 and 7. Difference equation of voltage after first operational amplifier is given by vx1[n+1] and Vx2[n+1] as shown in equation 9.

$$x_2[n+1] = x_2[n] + c_1 + x_2[n] + a_2[n] \tag{6}$$

$$x_1[n+1] = x_1[n] + b_1 * u[n] - a_1 * v[n] \tag{7}$$

$$vx_1[n+1] = vx_1[n] + \frac{Cs1}{Ci1} * vu[n] - \frac{Cs1}{Ci1} * V[n] \tag{8}$$

$$vx_2[n+1] = vx_2[n] + \frac{Cs2}{Ci2} * vx_1[n] - \frac{Cs2}{Ci2} * V[n] \tag{9}$$

It can be seen that x1[n+1] is dependent on v[n] because x1[n+1] is produced when v[n] is present. Vx1[n] difference equation is given in equation 8. The output of equation 7 is scaled to the normalized Simulink model and entered into equation 8. From this Cs1 and Ci1 relation can be defined as shown in equation 10.

$$\frac{Cs1}{Ci1} = b_1 = \frac{10000}{1131} \approx \frac{1}{9} \tag{10}$$

Conclusively if Cs1 value is taken as 1pF then Ci1 value must be 9pF. These values of capacitances are ideal and the absolute value of capacitance must be calculated taking into consideration, the thermal noise constraints as shown in equation 11 and 12. The absolute value of capacitances is defined within classically accepted tolerances of noise when implemented in real time circuits. There are switches made of CMOS transistors which generate some noise when implemented in practical circuits [7]. However, here the chosen oversampling ratio is very high so, in band thermal noise of circuit gets decreased due to a higher gain at the first stage [7]. The gain of first stage operational amplifier is 17.101 dB . It can be calculated with the help of equation 13. So, noise constrain at second stage is not important. So, Cs2 and Ci2 will be less affected by noise due to higher oversampling ratio. The LTspice circuit is designed in two phases as shown in figure 11. The phase operation is shown in Table IV. In phase 1 Cs1 is charged to the input voltage, and at the same time Cs2 is grounded so, all the charge from Cs2 will be transferred to Ci2. In phase 2, Cs1 is grounded and the operational amplifier gain is infinity so, the charge from Cs1 is shifted to Ci1 and at the same time Cs2 gets charged with the output voltage from first operational amplifier.

TABLE IV
CIRCUIT OPERATION IN PHASE 1 AND PHASE 2

Phase	Switching mode	Operation of capacitance
Phase 1	(S1,S4), (S6,S7) is closed (S2,S3), (S5,S8) is opened	Cs1 charges to input voltage and Cs2 charge is transferred to Ci2
Phase 2	(S1,S4), (S6,S7) is opened (S2,S3), (S5,S8) is closed	Cs1 charges to input voltage and Cs2 charge is transferred to Ci2

$$v_n^2 = \frac{(vdd/2)^2/2}{10^(SNR/10)} \tag{11}$$

$$v_n^2 = \frac{KT}{OSR * C1} \tag{12}$$

$$A > \frac{OSR}{\pi} * \frac{Cs1}{Ci1} - 1 \tag{13}$$

$$A > 17.101dB \tag{14}$$

Cs2 can be selected as small value to minimize power with adequate accuracy. Cs1 and Ci2 are selected as 1pF and 9pF respectively to equalize the gain of the first stage and second stage operational amplifiers. The capacitance values of the designed circuit are shown in table V.

TABLE V
CIRCUIT PARAMETER CAPACITANCE VALUE

Stage	Capacitance	value
Stage 1	Cs1	1pF
Stage 1	Ci1	9pF
Stage 2	Cs2	1pF
Stage 2	Ci2	9pF

After generating vx2, it is compared with the help of another comparator that has it's saturation voltage as Vdd. Output vx2 is compared with Vcm at the non-inverting terminal. A clocked

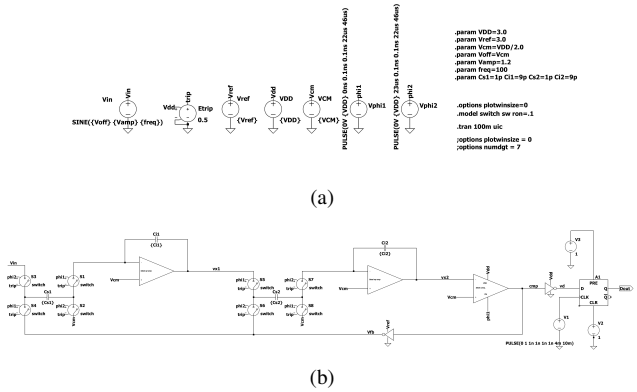

Fig. 11. Circuit level design of second order sigma-delta modulator.

comparator is attached after this to investigate the effect of the input supply voltage. The signal is then passed through a D-Flip flop to store the incoming PWM analog to digital converted signal.

B. Simulation Result

Transient analysis is performed after designing circuit, output voltage is taken as Vvd. Output data is extracted as text from LTspice and analyzed in MATLAB as shown in figure 12.

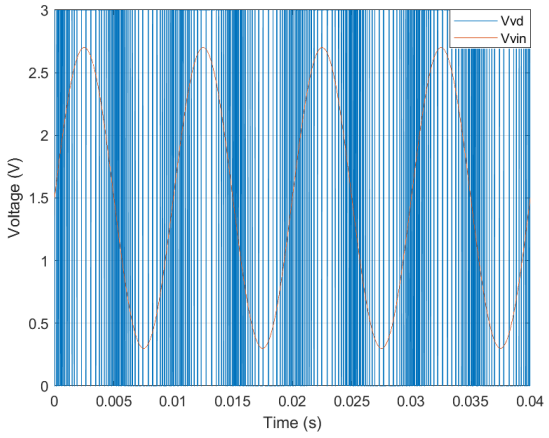

Fig. 12. Simulated output result of modulator.

FFT of the signal is plotted in LTspice after generating an output signal. Hanning window is often applied on random data because of it's moderate effect on the accuracy of amplitude, and resolution of frequency. The data generated to plot the FFT is very large, so two changes need to be added in the spice directive. First command 'options plotwinsize' is set to 0 so that data in transient analysis is not compressed. Second command 'options numdigit' is set to 7. For numprecision value greater than 6, LTspice uses double precision to read data [5].

A Linear FFT is drawn to measure the amplitude of output voltage at peak operating frequency as shown in figure 13.

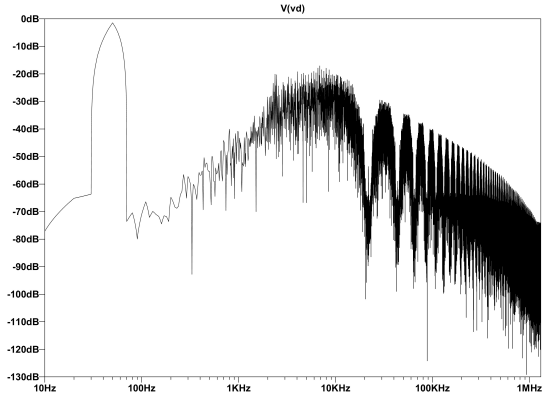

Fig. 13. FFT output (dB) of modulator at input frequency 50 Hz.

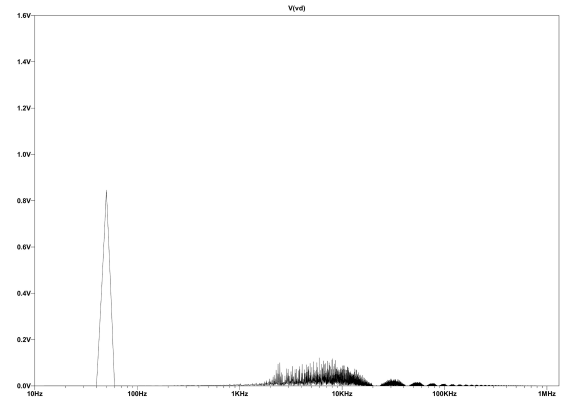

Fig. 14. Linear FFT output (V) of modulator at input frequency 50 Hz (Amplitude = 835mV)

Number of samples for 100Hz input frequency LTspice data in matlab is 412392. The corresponding voltage of different samples is extracted and FFT analysis id performed in matlab. Frequency bin of above data is 13 as shown in figure 15.

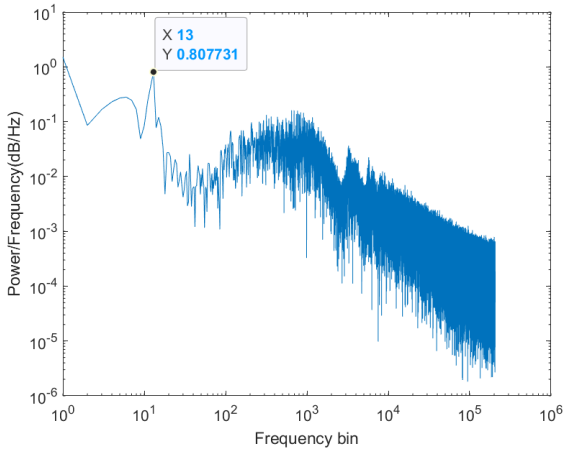

Fig. 15. Frequency bin plot of modulator at input frequency 50 Hz (LTspice data)

So, with the help of equation 15-18. Frequency resolution can be calculated as 7.692. So, sampling frequency of LTspice

for 100Hz input signal can be calculated as 3.172 MHz.

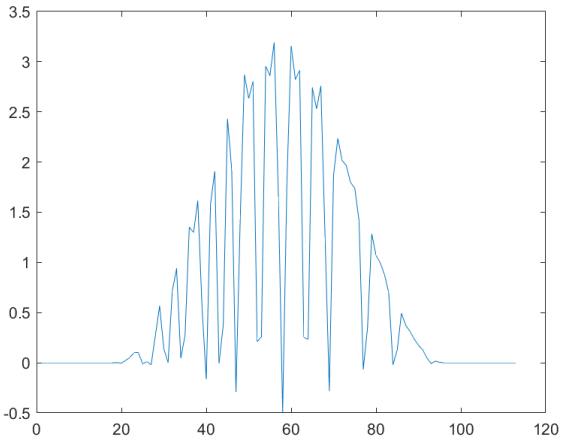

Fig. 16. Dessimated output of LTspice data,

$$Frequency\ bin = 13 = \Delta K_f = \frac{100}{\Delta f} \tag{15}$$

$$\Delta f = Frequency\ resolution = 7.692 \tag{16}$$

$$Frequency\ resolution = 7.692 = \Delta f = \frac{f_s}{412392} \tag{17}$$

$$Sampling\ frequency = f_s = 3.1722\ MHz \tag{18}$$

The high sampled frequency of LTspice data can not be realized using FFT so, decimation filter is applied on LTspice data to for downsampling. It can be seen the high sampling frequency output of sigma delta modulator sampled at 3.172 MHz in figure 12 is downsampled at lower frequency range shown in figure 16.

IV. Analysis using ADS1115

A. Components

ADS1115 is a 16-bit, low power, high precision analog to digital converter with four analog channels. It operates on a single power supply from 2V to 5.5V. It has programmable data rate ranging from 8 to 860 samples per second (SPS). It is compatible with the I2C serial interface. Both positive and negative values of voltage can be measured by ADS1115. Among the 16 bits, one bit is assigned for positive and negative number. So, out of 16 bits, 15 bits are used to measure magnitude of voltage, and the resolution of analog to digital converters (ADC). There is an on-board programmable gain amplifier (PGA) available that offers input range from supply voltage to ±256 mV with which both large and small signals can be measured [1].

BitScope Micro is dual channel oscilloscope with 20MHz bandwidth [8]. It is a digital to analog signal capture device and it is usually configured as the mixed signal oscilloscope. It offers 8 logical and 2 analog channels. A waveform generator and clock generator are included. In addition, it can function as logic, protocol and spectrum analyzer [8].

ESP8266 is a system on chip (SoC) which is manufactured by Chinese company Espressif. It consists of L106 32-bit Reduced Instruction Set Computer (RISC) microcontroller unit and a Wi-Fi transceiver [2]. It has an analog input and 17 General Purpose Input Output (GPIO) pins. It has several interfacing options like SPI, I2C, UART and I2S.

B. Procedure to measure ADC values

Firstly, ADS1115 is connected with ESP8266 through GND and 3.3V. After this, the SDA (Serial data) and SCL (serial clock) pins of ESP8266 are connected with the corresponding pins of ADS1115 converter. The input sinusoidal signals at different frequencies are then provided with the help of dual channel Bit Scope Micro. I2C interfacing is used between the ESP8266 and ADS1115 to collect the output ADC values [5]. The circuit diagram for connection of ADS115 with ESP8266 is shown in figure 17.

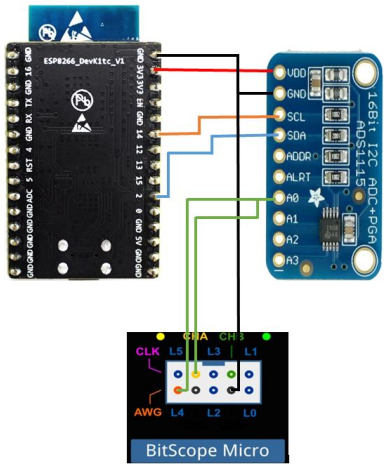

Fig. 17. Connection of ADS1115 with ESP8266.

C. Programming and data acquisition

Micro-Python firmware, Thonny IDE is used to program ESP8266. Firstly, the MicroPython firmware .bin file is loaded onto ESP8266 device to flash the device. The library of ADS1115 and I2C communication is now added to the device. Since I2c is being used, SCL and SDA are connected as minimum, the address pin (addr = 72) is set to low, and the baud rate is set to 400000. After setting the baud rate, the class of ADS1115 is defined to interpret different parameters such as Gain, I2C and Address. After this, a pair of methods for a time optimized sequential reading, 'adc.set_conv()' and adc.read_rev() are triggered with time is now used to collect adc values at different input frequency tones of 5Hz, 10Hz, 20Hz, 50Hz and 100Hz. The results are stored in myTestFile.

D. ADS1115 Result

FFT is used to convert discrete time domain data to discrete frequency domain data. Since the FFT is designed to be used

with discrete time domain data. It is common to convert ADC data from the time domain to frequency domain. So, for n number of time domain points, FFT will produce frequency domain points. The mathematics behind FFT assumes that time domain signal continues to infinite time [10]. Data generated from ADS1115 is decimated data. The sampling frequency of ADS1115 varies between 8Hz to 860Hz so, FFT alias region is half of sampling frequency and it is normally hidden. The hidden alias region in ADS1115 data is 426Hz to 860Hz [6]. So, in this case FFT output is between 8Hz to 426Hz. The frequency resolution of FFT is shown in equation 19. It is the minimum change in frequency that an FFT can detect. In this case the number of samples (N) is 2048. Translating the time domain sine wave to frequency domain will create a component in a frequency bin. This frequency bin is determined by dividing input frequency by the frequency resolution as shown in equation 20.

$$Frequency\ resolution = \Delta f = \frac{f_s}{N} \tag{19}$$

$$Frequency\ bin = \Delta K_f = \frac{f_{in}}{\Delta f} \tag{20}$$

The data collected from ADS1115 varies from 5Hz to 100 Hz. There are different input frequency so signals at different frequency will be sampled by ADS1115 at different sampling frequency [5]. To determine the sampling frequency at particular input frequency first frequency bin is calculated with the help of matlab. At first it is operated at 5Hz input frequency the frequency bin peak comes at 69 as shown in figure 18.

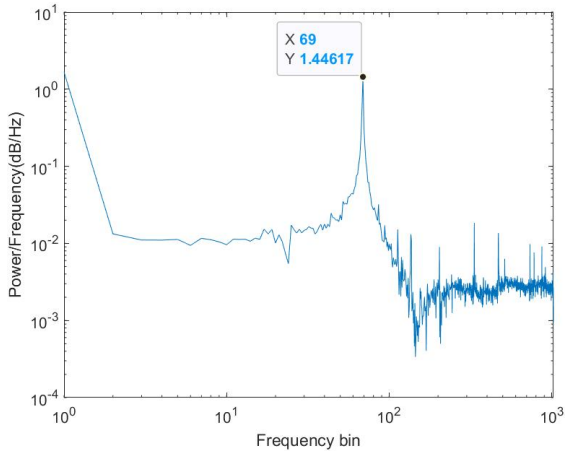

Fig. 18. Frequency bin in periodogram power spectral density estimate at 5Hz.

$$Frequency\ bin = 69 = \frac{5Hz}{\Delta f} \tag{21}$$

$$\Delta f = 0.07246 \tag{22}$$

Putting frequency resolution value in equation 19 sampling frequency of ADS1115 at input frequency of 5Hz data can be calculated as 148.405 Hz.

$$f_s = 148.405\ Hz \tag{23}$$

The corresponding sampling frequency of ADS1115 is calculated at different frequency input data and it can be referred from table VI. After knowing sampling frequency FFT can be drawn. FFT drawn with help of 5Hz input frequency data at sampling frequency of 148.405 Hz is shown in figure 19.

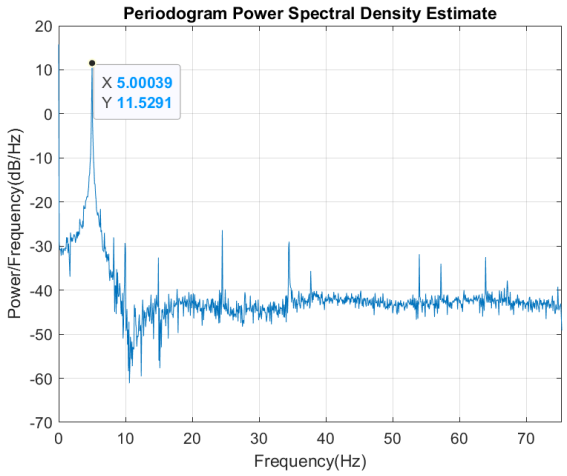

Fig. 19. FFT, periodogram power spectral density estimate at input frequency 5Hz.

Same procedure is adopted for other input frequency data, the power spectral density plotted at 10 Hz input frequency with frequency resolution 0.0719, frequency bin 139 and sampling frequency of ADS1115 at 147.338 is shown in figure 20.

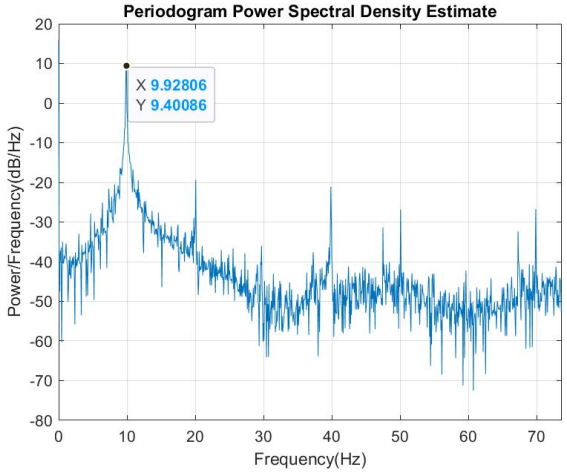

Fig. 20. FFT, periodogram power spectral density estimate at input frequency 10Hz.

The power spectral density plotted at 20 Hz input frequency with frequency resolution 0.07246, frequency bin 276 and sampling frequency of ADS1115 at 148.405 is shown in figure 21.

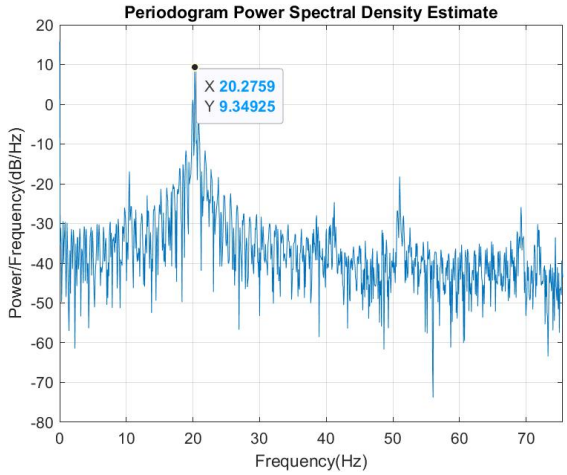

Fig. 21. FFT, periodogram power spectral density estimate at input frequency 20Hz.

The power spectral density plotted at 50 Hz input frequency with frequency resolution 0.07256, frequency bin 689 and sampling frequency of ADS1115 at 148.405 is shown in figure 22.

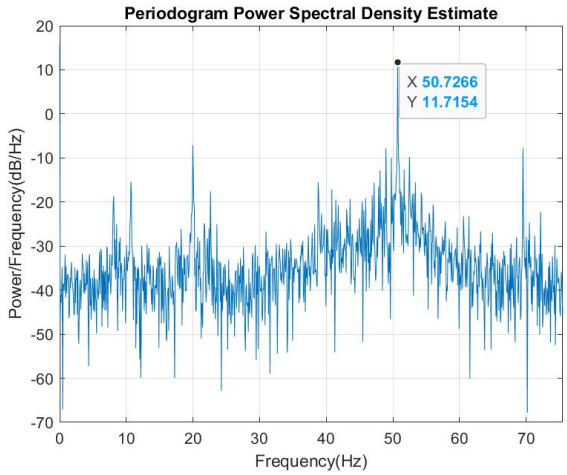

Fig. 22. FFT, periodogram power spectral density estimate at input frequency 50Hz.

The power spectral density plotted at 100 Hz input frequency with frequency resolution 0.148, frequency bin 674 and sampling frequency of ADS1115 at 303.857 is shown in figure 23.

It can be seen from FFT at different input frequency, when input frequency is less i.e 5Hz, power spectral density is achieved and 5Hz. It can be seen that frequency component near 5 Hz peak are not producing peak, so the noise contributed by these frequencies at lower frequencies are less. As input frequency keep on increasing from 5 Hz , 10 Hz to 50Hz and 100Hz it can be seen in 100 Hz power spectral density curve that frequencies nearby peak frequency is also having higher amplitude. So, if this system is used at lower input frequency there will be less noise in the system than at

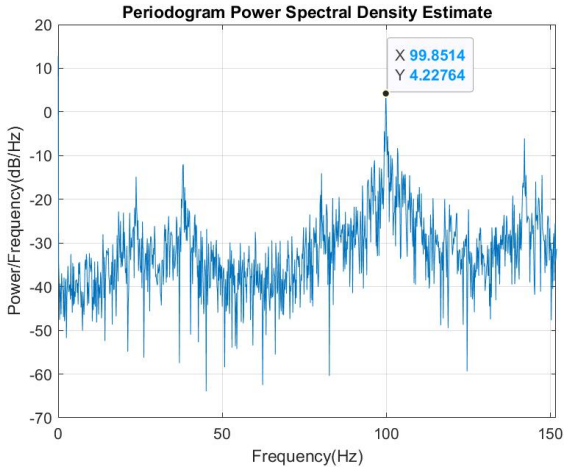

Fig. 23. FFT, periodogram power spectral density estimate at input frequency 100Hz.

TABLE VI
SAMPLING FREQUENCY OF ADS1115 AT DIFFERENT INPUT FREQUENCY

Input frequency (f_{in})	Frequency bin (ΔK_f)	Frequency resolution (Δf)	Sampling frequency (f_s)Hz
5 Hz	69	0.0724	148.405
10 Hz	139	0.0719	147.338
20 Hz	276	0.07246	148.405
50 Hz	689	0.07256	148.405
100 Hz	674	0.148	303.857

higher frequency like 100Hz. This make this system perfect for lower frequency industrial application usage in process control industry for measurement purpose.

V. DISCUSSION

A stable second-order sigma delta modulator was designed in 2 specified levels, MATLAB, and LTSpice and tested in the hardware level, ADS1115. The sigma delta modulator designed works well in the required operating bandwidth of Electric Energy meters from 40 Hz to 2000 Hz. The desired SQNR for a 1-bit quantizer with an oversampling ratio of 512 is 126 dB. Upon the SQNR analysis of the generated noise transfer function, it was observed that a peak SNR of 123.76 was obtained. Using equation 1, the effective number of bits (ENOB) can be calculated as 16. This proves that a comparatively higher resolution output can be obtained from a lower resolution (1 bit) ADC. Another point that can be proved is the improvement in SQNR upon doubling of the sampling rate. For a bandwidth of 125 Hz, the peak SQNR obtained was 107 dB. Upon doubling of that, the SQNR increases to 123 dB, providing nearly a 16 dB increase in SQNR for doubling the sampling rate. The digital filtering setup in MATLAB performs its desired function of reducing the data rate of the incoming signal and outputting a signal at the Nyquist rate. The LTSpice data upon post-processing shows that similar to MATLAB, it is operating at a high sampling frequency of 3.172 MHz and it tracks the given sinusoidal input wave.

Switching capacitors values are calculated with the help of coefficients of b1 extracted from matlab. It was observed that if b1 balue is less than 0.25 than the voltage given to clocked comparator was in desired range and it will not burn. Also, to consider some moderate desired gain (greater than 10dB) of first stage and second stage operational amplifier value of b1 must be less than 0.25. On observation of output FFTs from ADS1115, it can be seen that the sigma delta modulator works best at lower frequencies with lesser quantization noise. However, on the whole, the sigma delta modulator pushes away the noise from the desired band of interest and a peak is obtained at the specified input frequency.

VI. Conclusion

A sigma delta modulator is extremely useful for lower power consumption, high-resolution applications. With the use of oversampling, noise shaping, digital filtering and decimation, a comparatively lower resolution 1 bit ADC was made to produce a high-resolution output. Oversampling enables us to achieve high-resolution outputs, noise shaping helps shape the noise out of the desired frequency range, digital filtering filters out the unwanted noise and decimation filter brings back the oversampled data down to Nyquist rate. Fast Fourier Transform was performed on the data of ADS1115 to analyze the discrete-time domain data in the frequency domain. A stable, second-order sigma delta modulator for the given specifications was designed and analyzed in the 3 different levels

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