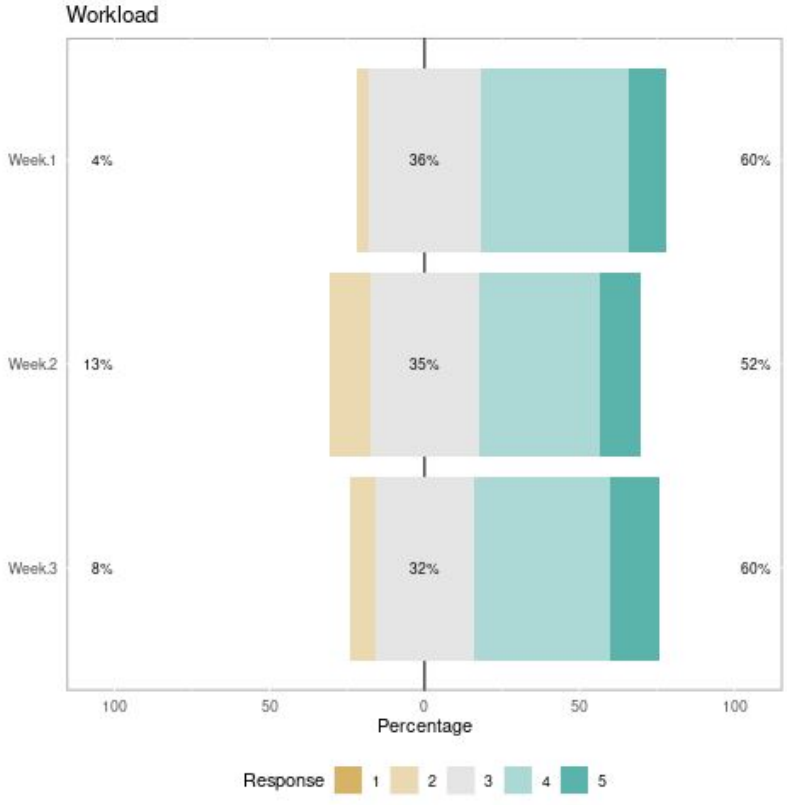
0x06 - Modern VLSI Flows

ENGR 3410: Computer Architecture

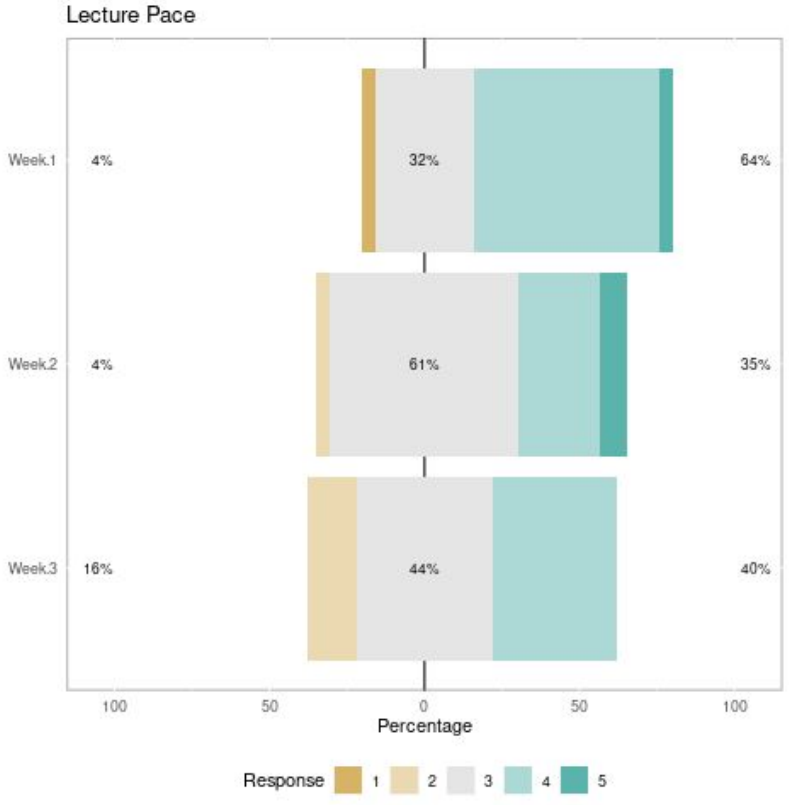
Jon Tse

Fall 2020

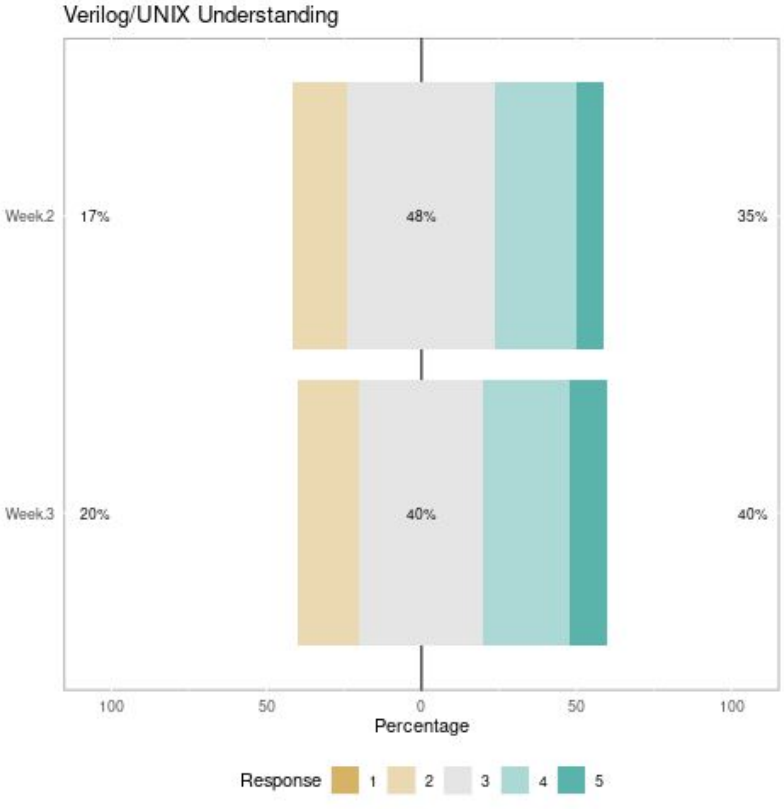
Feedback - Workload



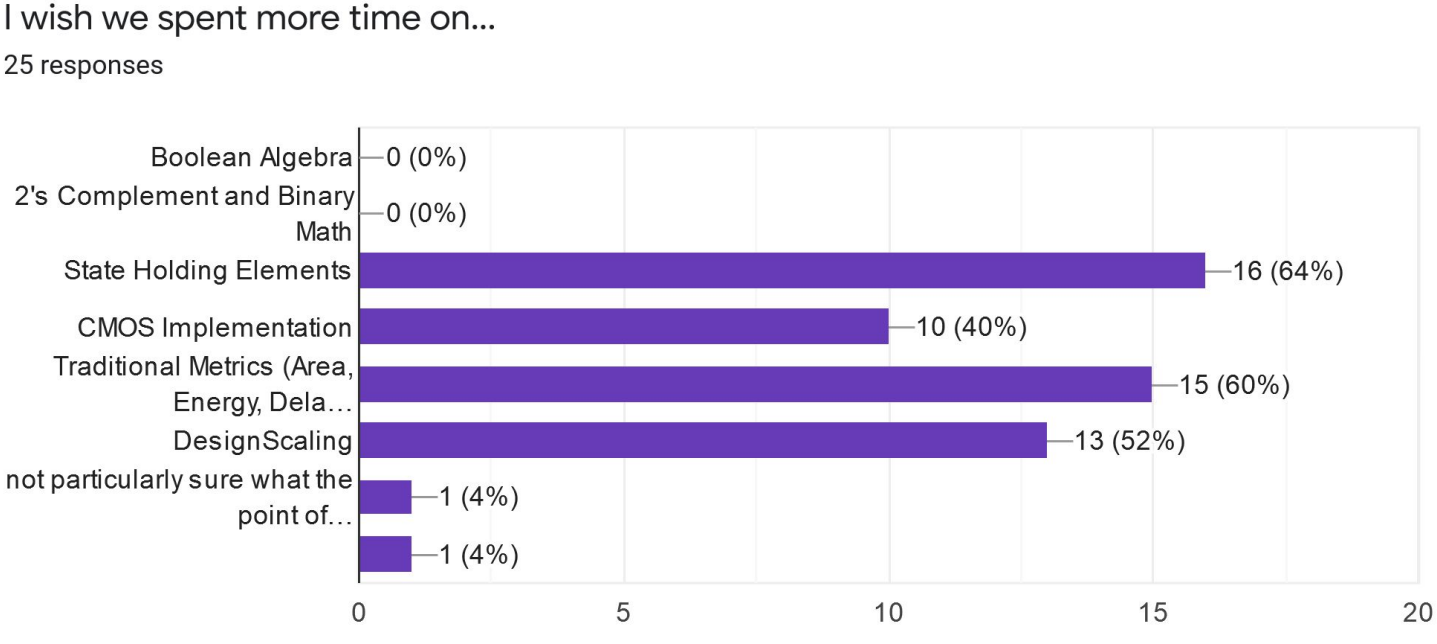
Feedback - Pace



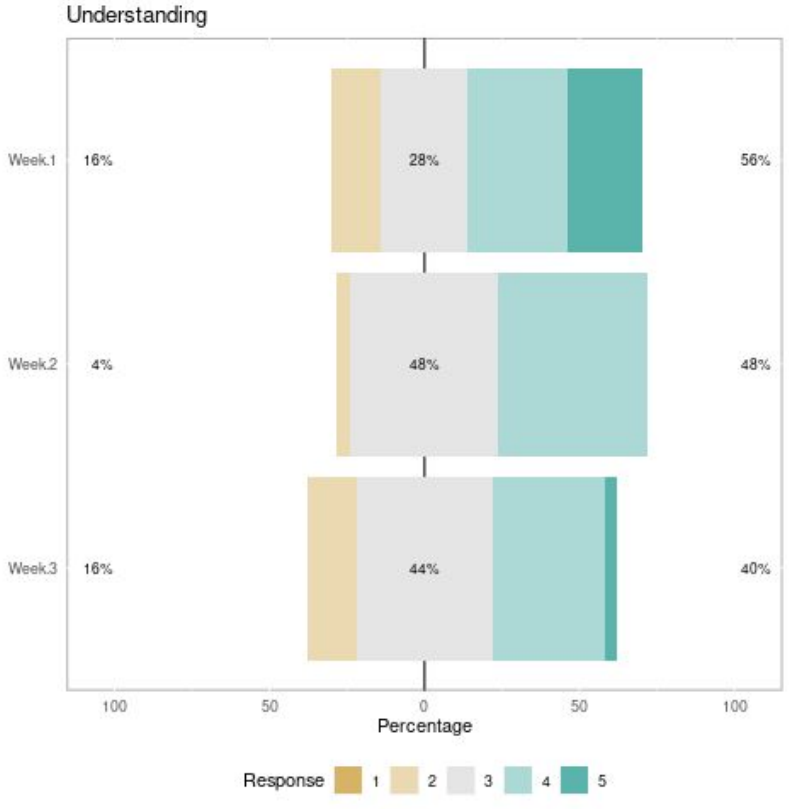
Feedback - Verilog



Feedback - More Time



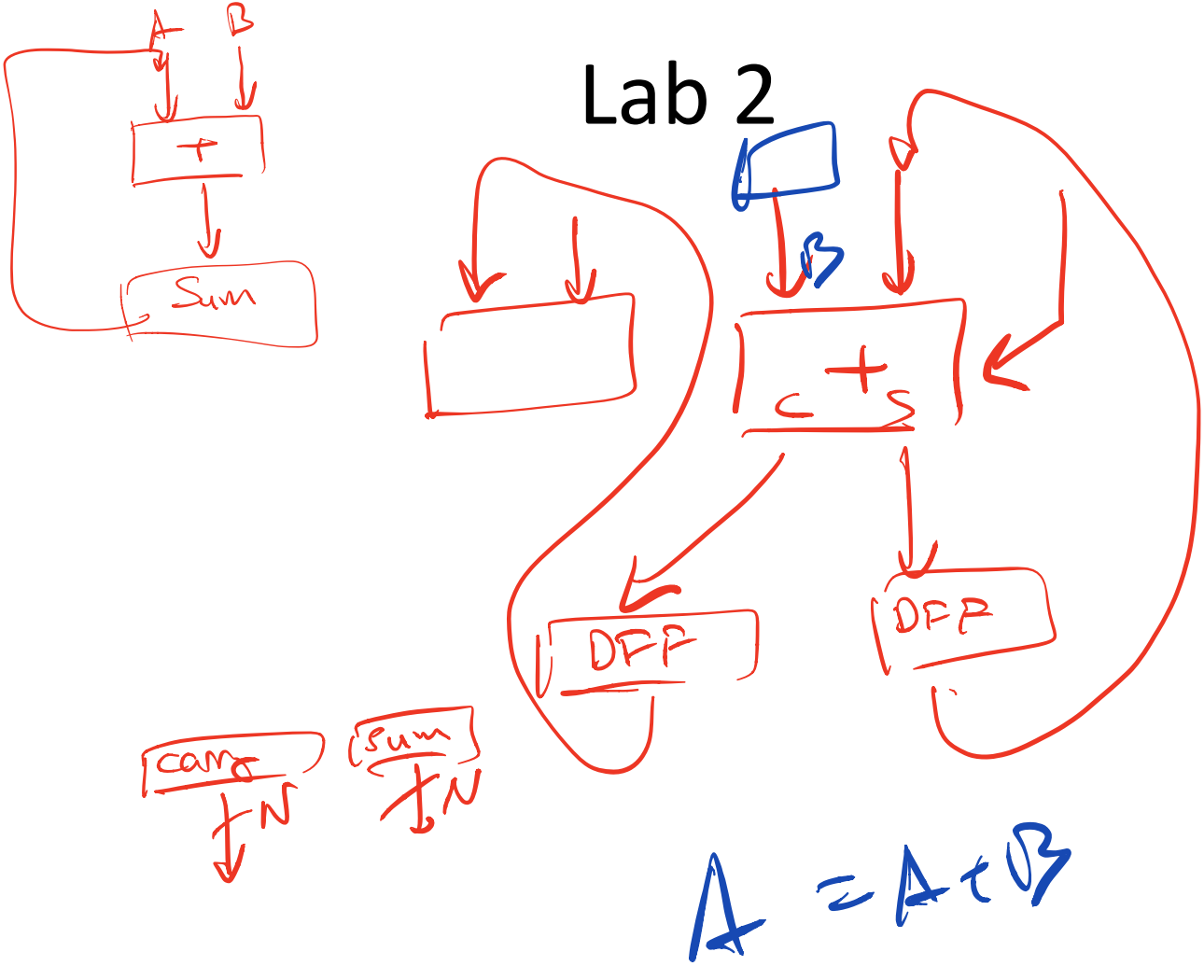
Feedback - Understanding



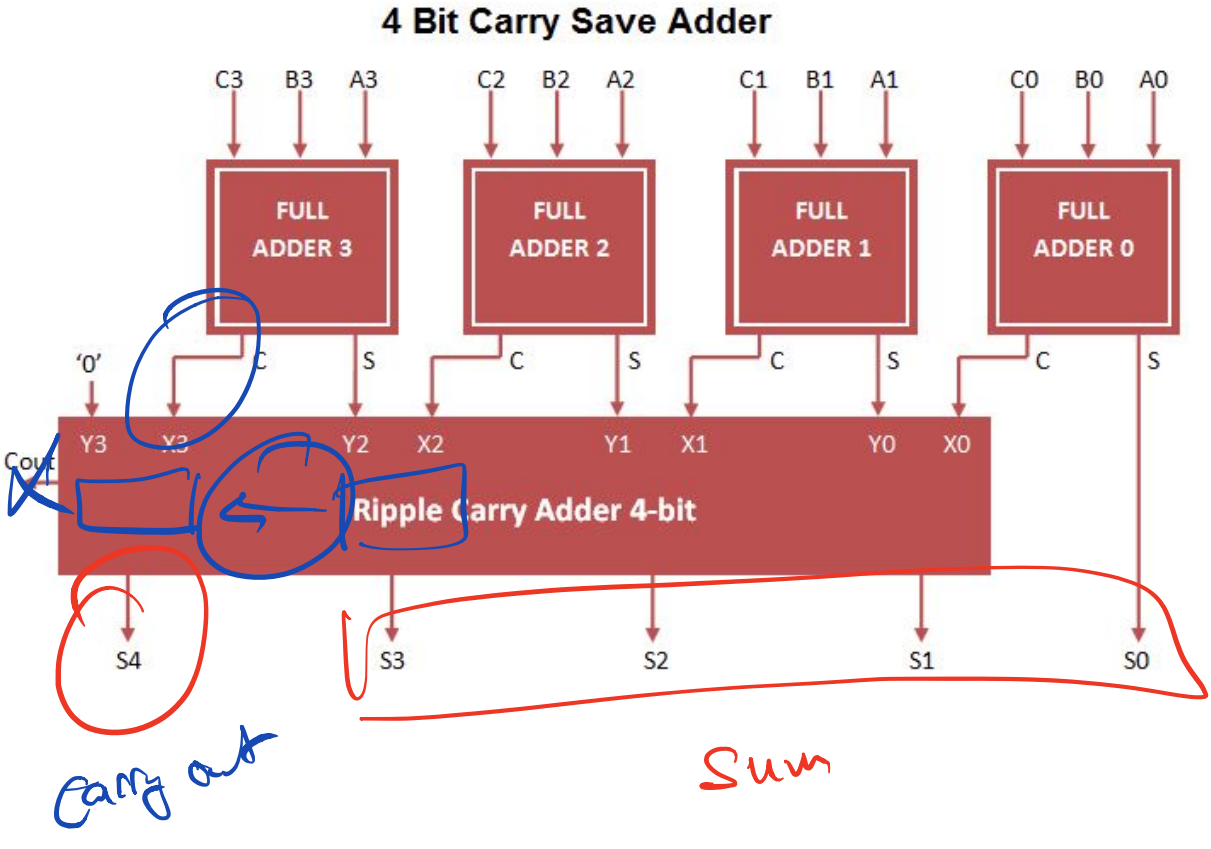
Housekeeping

- Feedback Discussion
- Review HW3
- Discuss HW4
- Discuss Lab 2

Lab 2

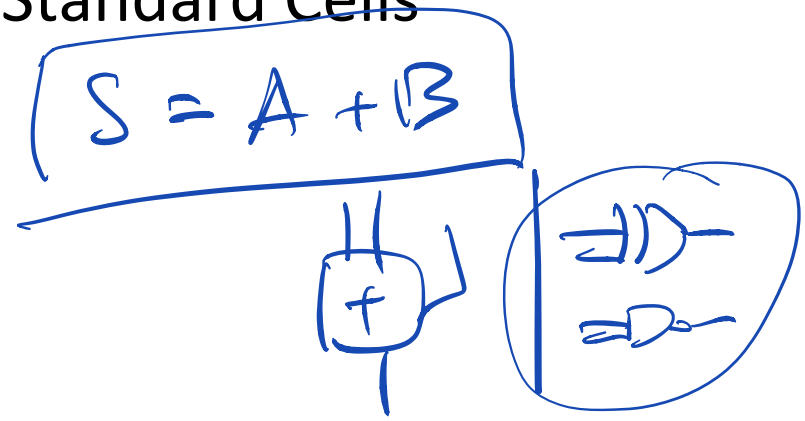


Lab 2

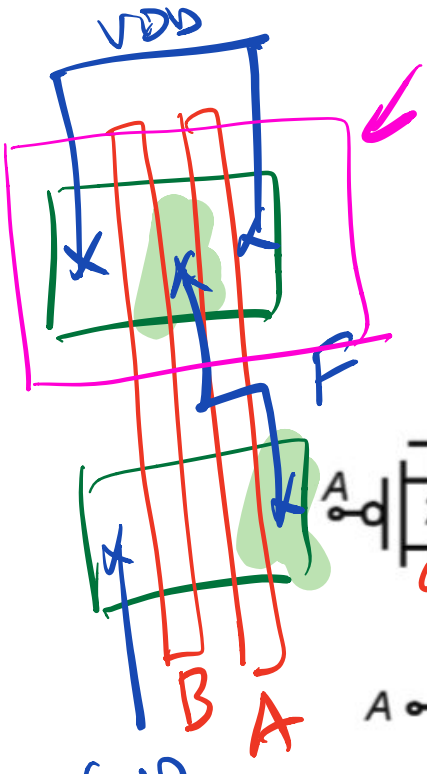

4 Bit Carry Save Adder
C3
B3
A3
C2
B2
A2
C1
B1
A1
C0
B0
A0
FULL ADDER 3
FULL ADDER 2
FULL ADDER 1
FULL ADDER 0
'0'
C
S
Y3
Y2
X2
Y1
X1
Y0
X0
Cout
Ripple Carry Adder 4-bit
S4
S3
S2
S1
S0
Carry out
Sum

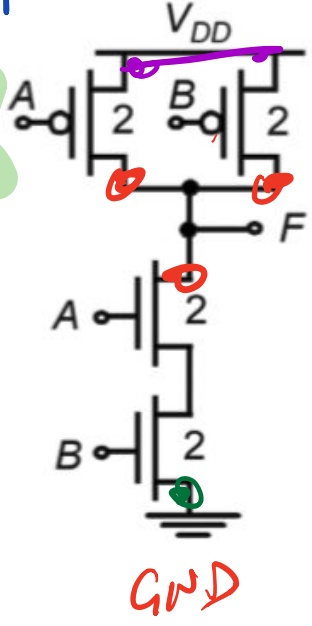
Modern VLSI Flows

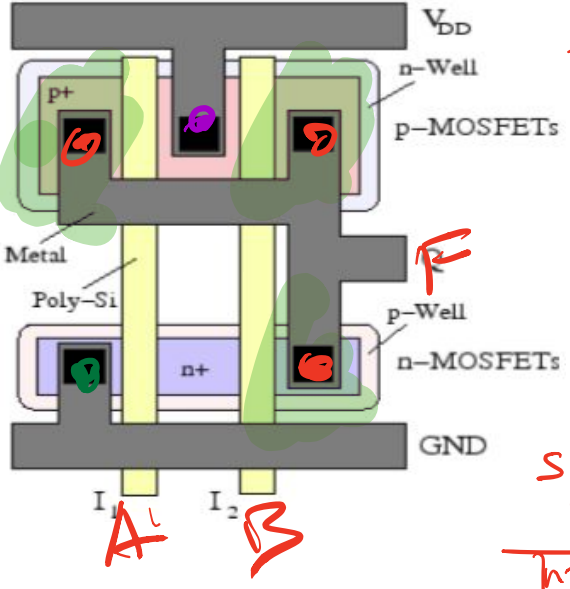
- Build a Standard Cell Library (Gates)
- Write a Design Spec
- Design the Micro Architecture
- Write RTL (Verilog)
- Synthesize Verilog -> Standard Cells
- Place and Route Standard Cells
- Close Design



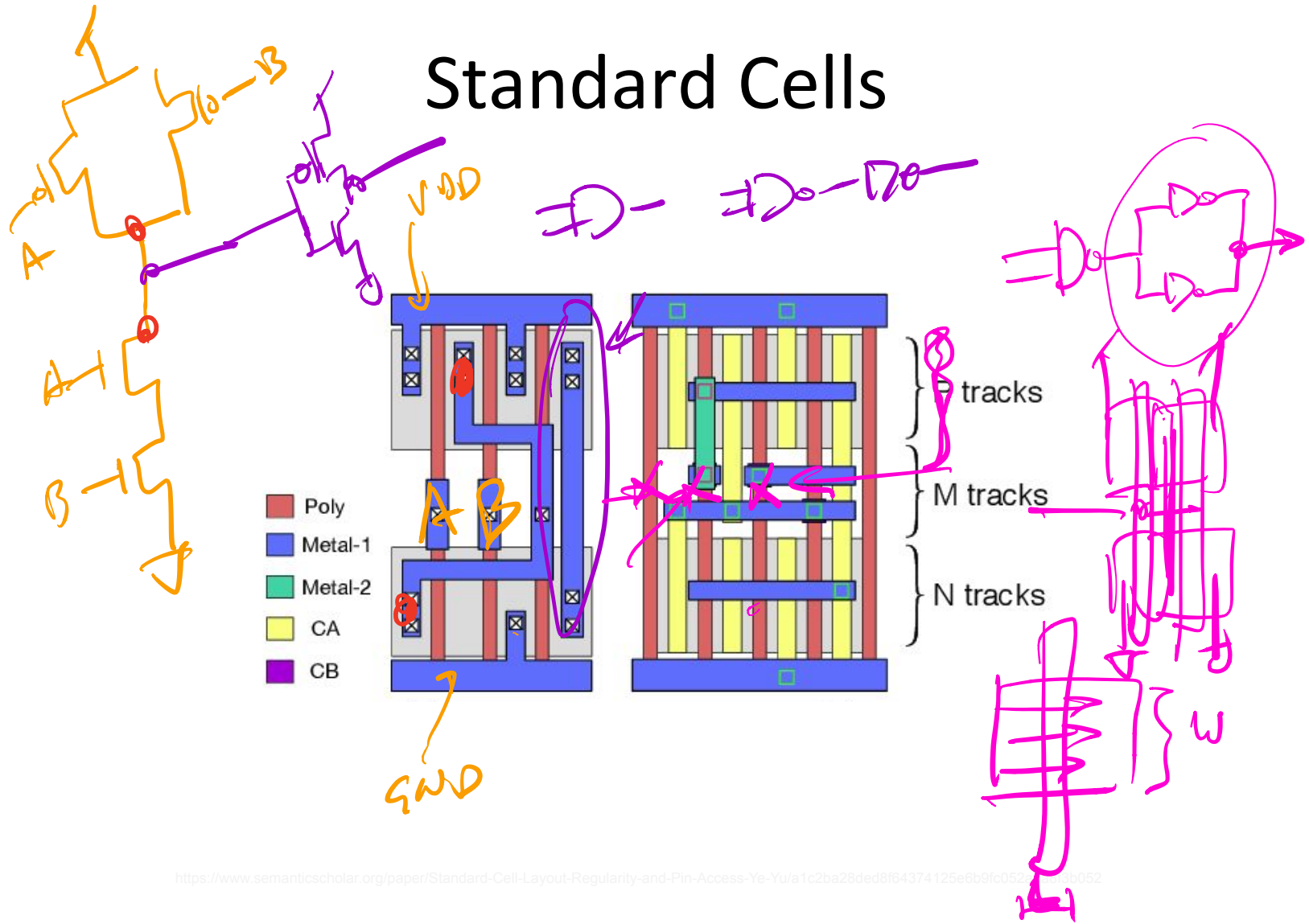
NAND Gate







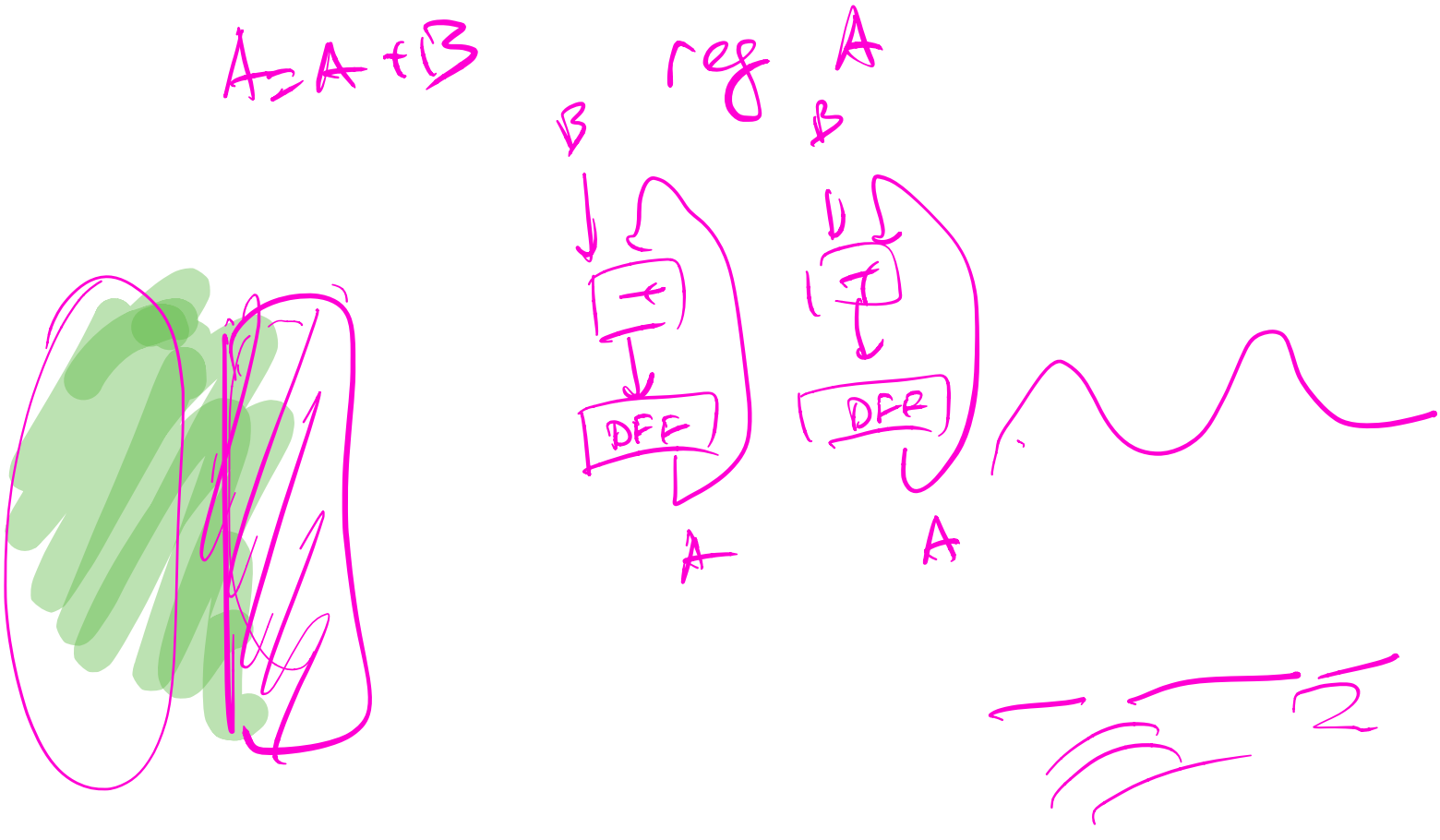
Standard Cells



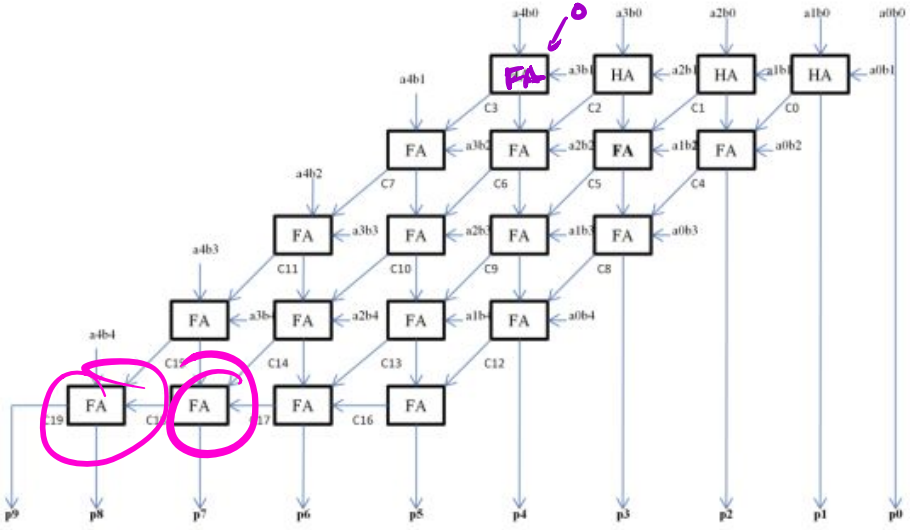
Spec and RTL for Multiplier

```
module mult (
   input [W-1:0] A,B,
   output [2*W-1:0] C
);

C = A*B

endmodule
```

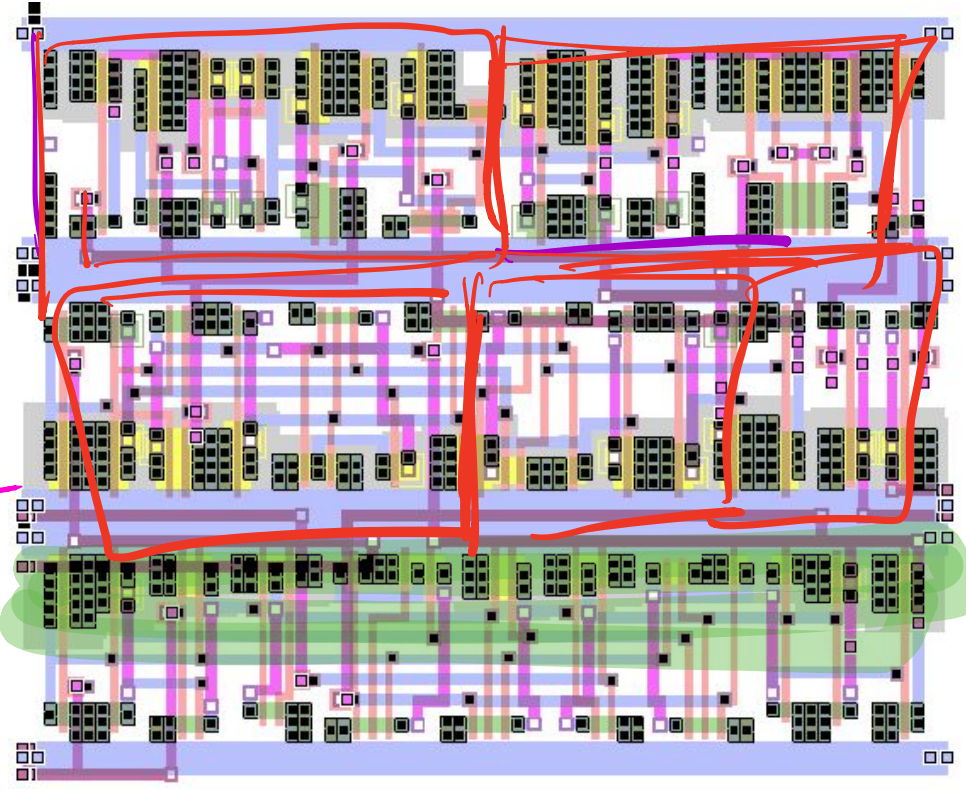
Microarchitecture?



Synthesize RTL



Place and Route



http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_s00/Project/STANDARD%20CELL%20TEMPLATE%20DEFINITIONS_.htm

Close Design