0x14 - Introduction to Async

ENGR 3410: Computer Architecture

Jon Tse

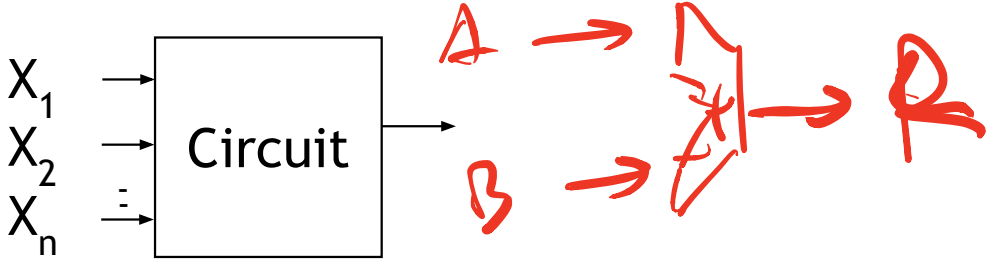
Fall 2020

Housekeeping

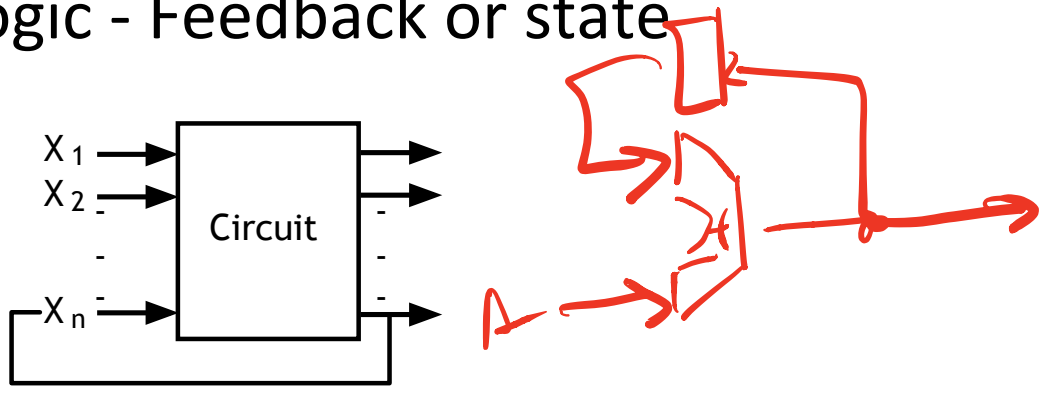
- NINJAs to have grading done by end of Nov
- Project Proposal feedback ASAP

Review

- Combinational Circuits - No feedback, no state

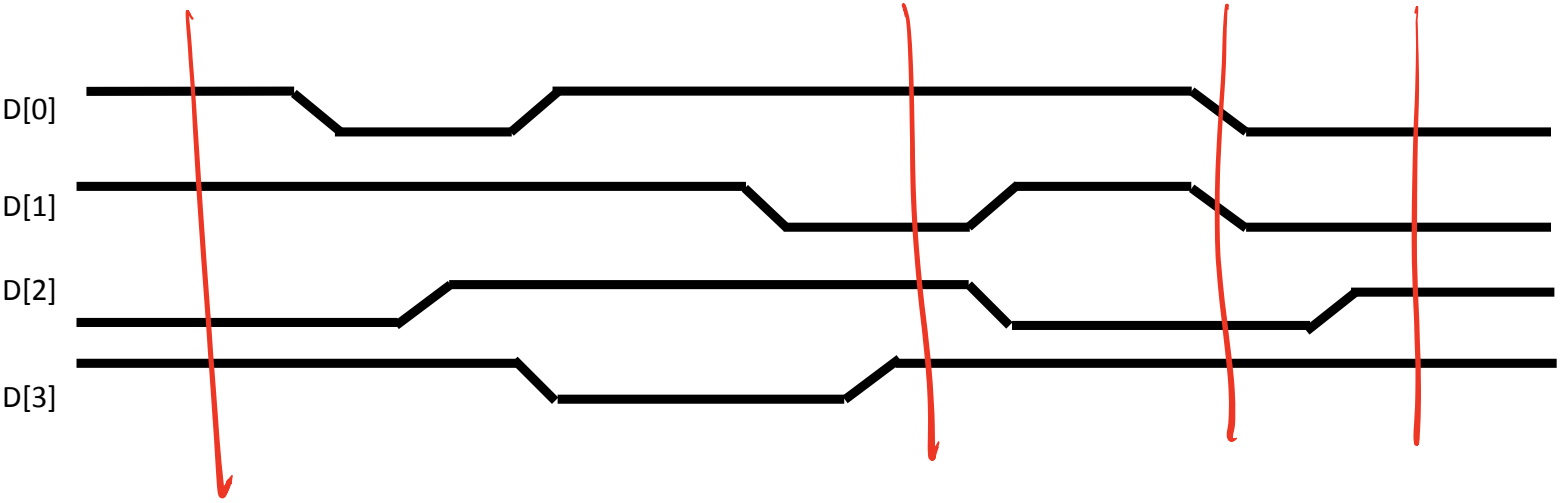


- Sequential Logic - Feedback or state



Representing Data

Time as the differentiator...



Representing Data

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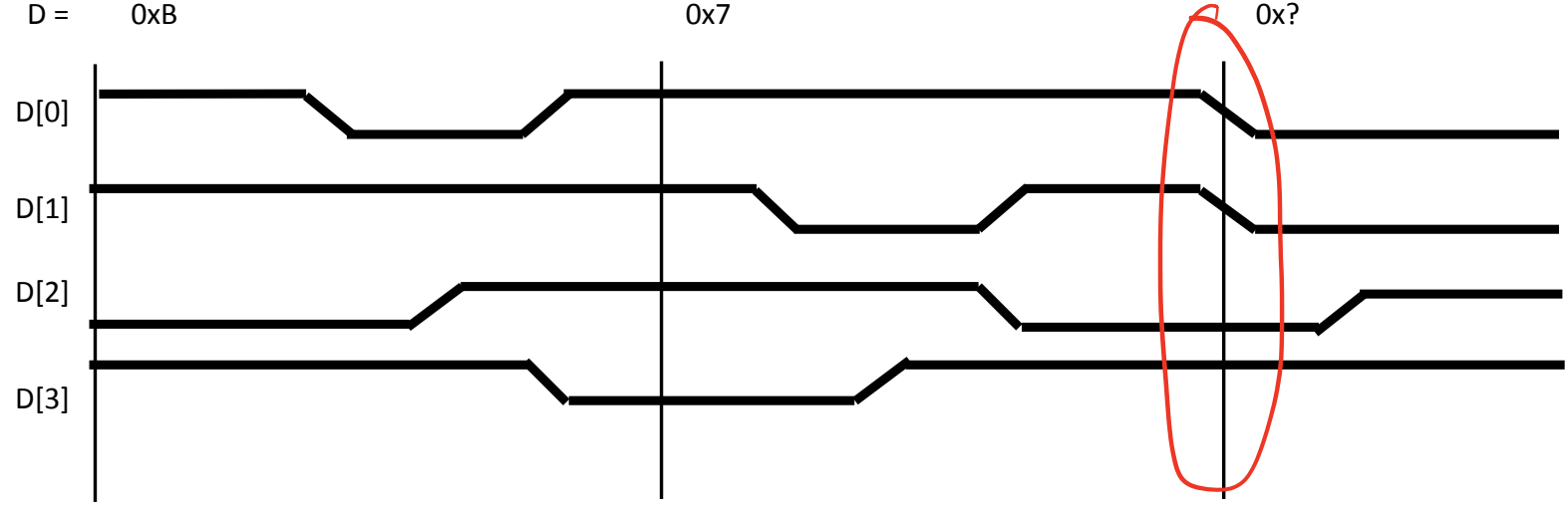
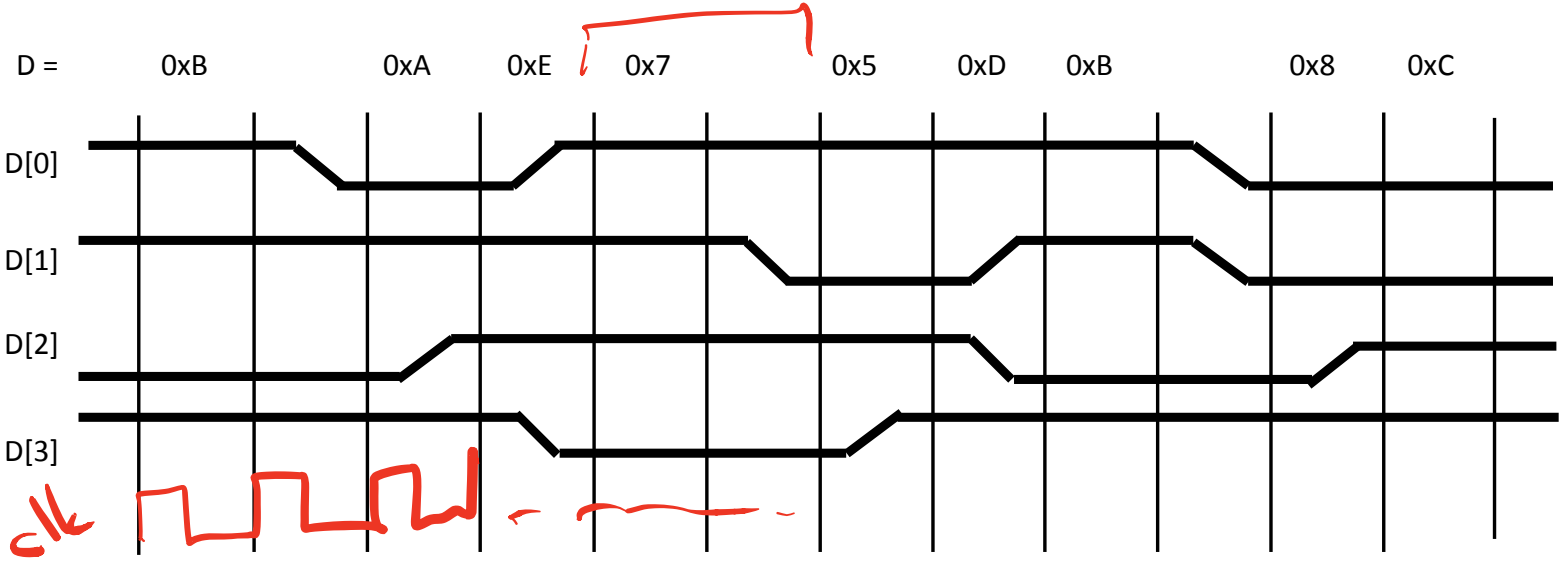
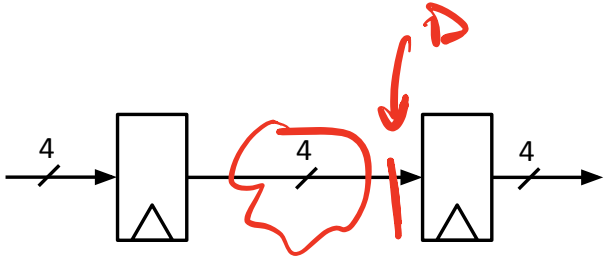


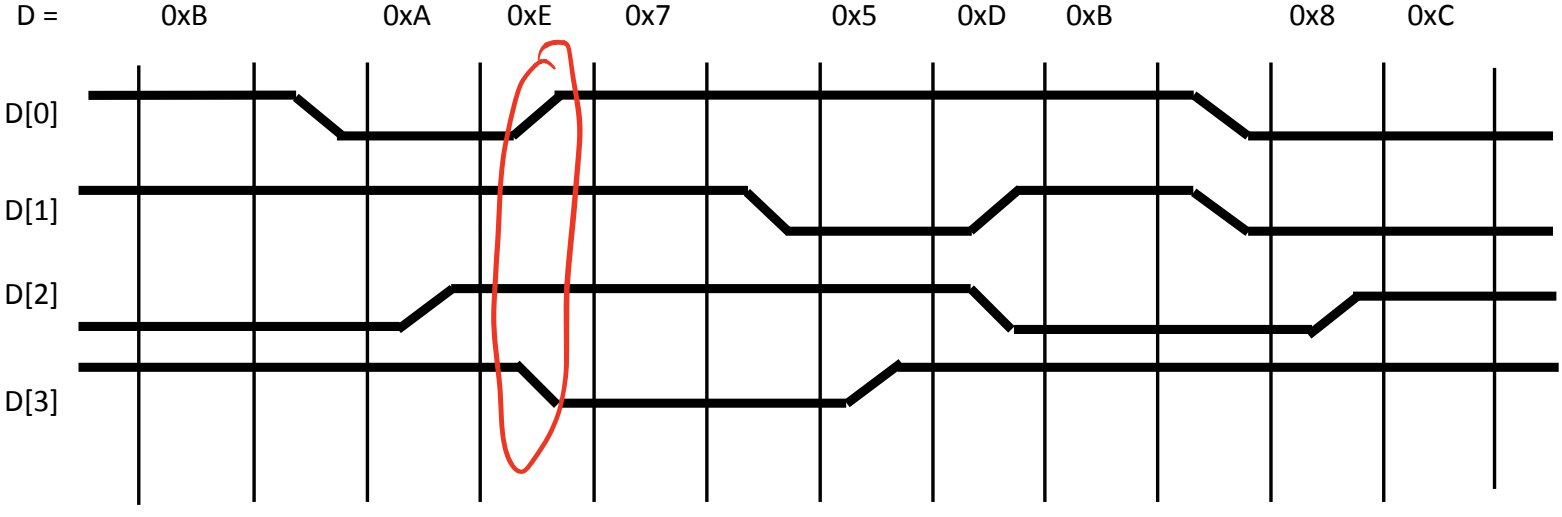
Representing Data

Time as the differentiator...

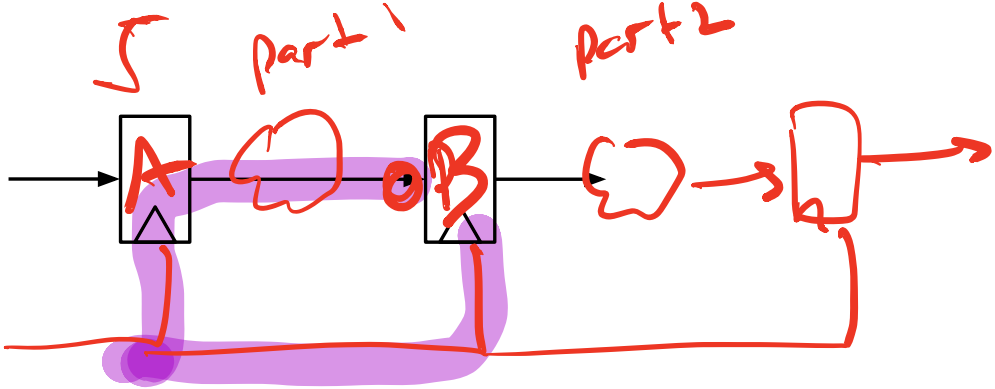


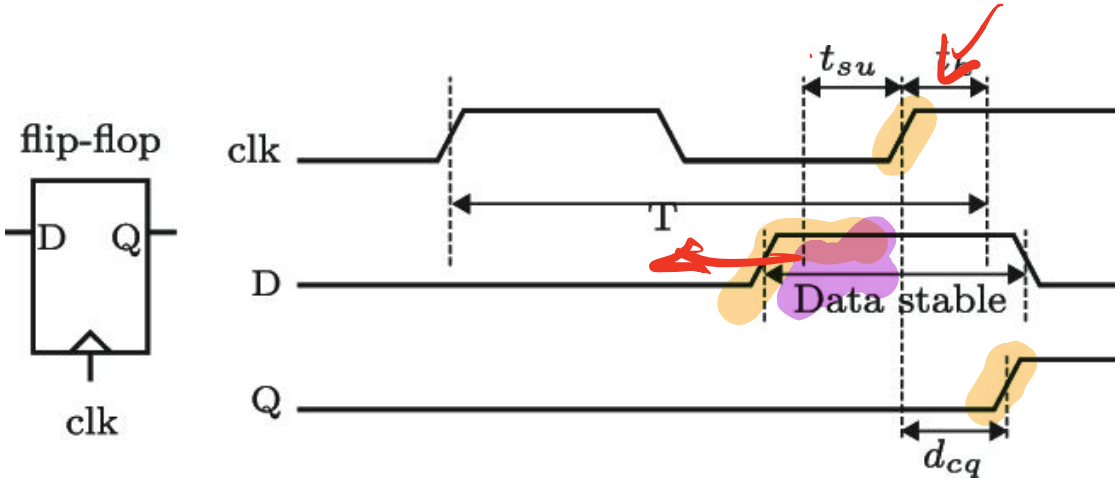
Sampling Data





Setup and Hold





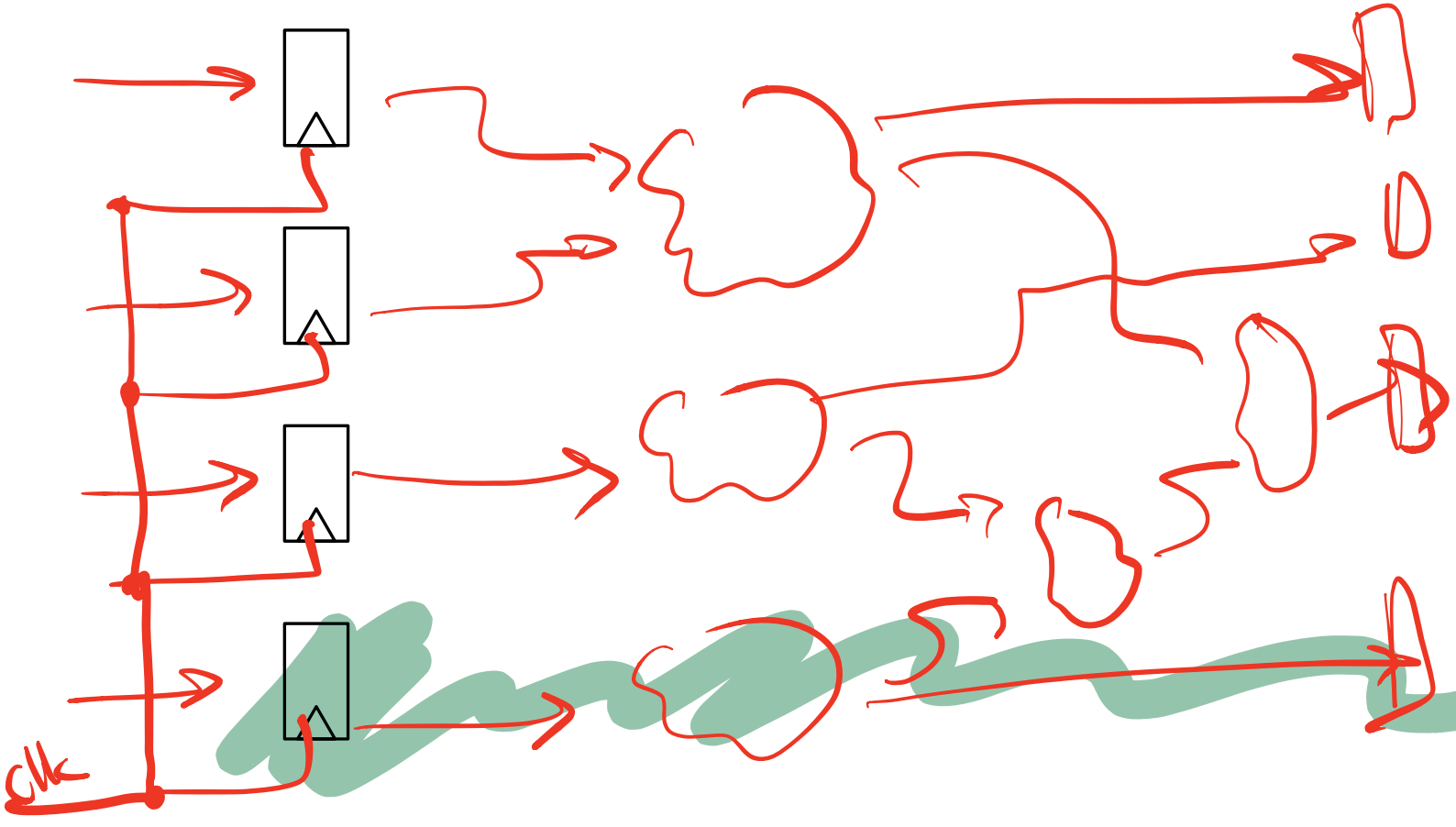
https://www.researchgate.net/figure/Setup-time-t-su-hold-time-t-h-and-clock-to-q-delay-d-cq-of-a-flipflop_fig2_323349911

Clocks are Important

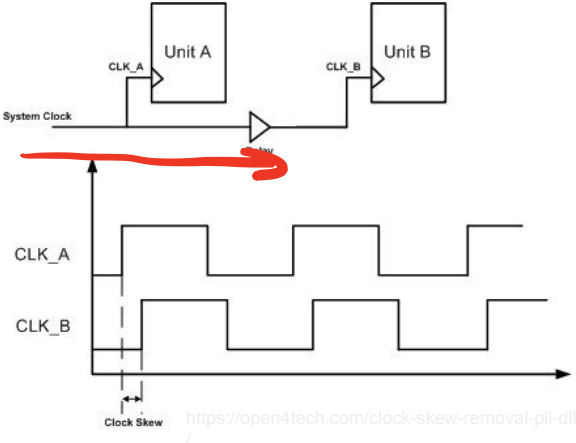
- Grant validity to data
- Allow us to synchronize circuits
- Grant us some noise immunity

$E = \frac{1}{2} C V^2$ $P = \frac{1}{2} f C V^2$

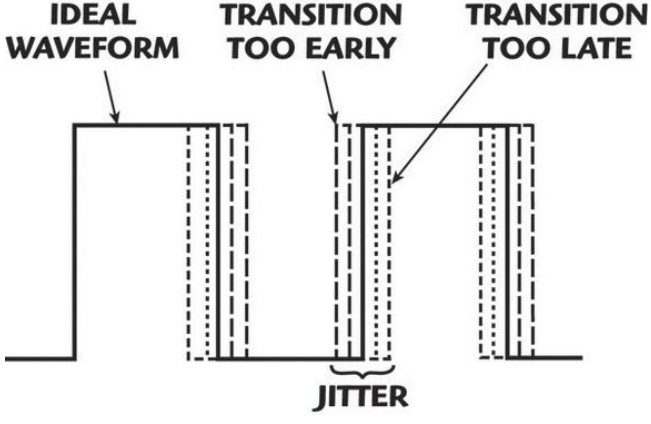
But… they always switch



and they're not perfect....

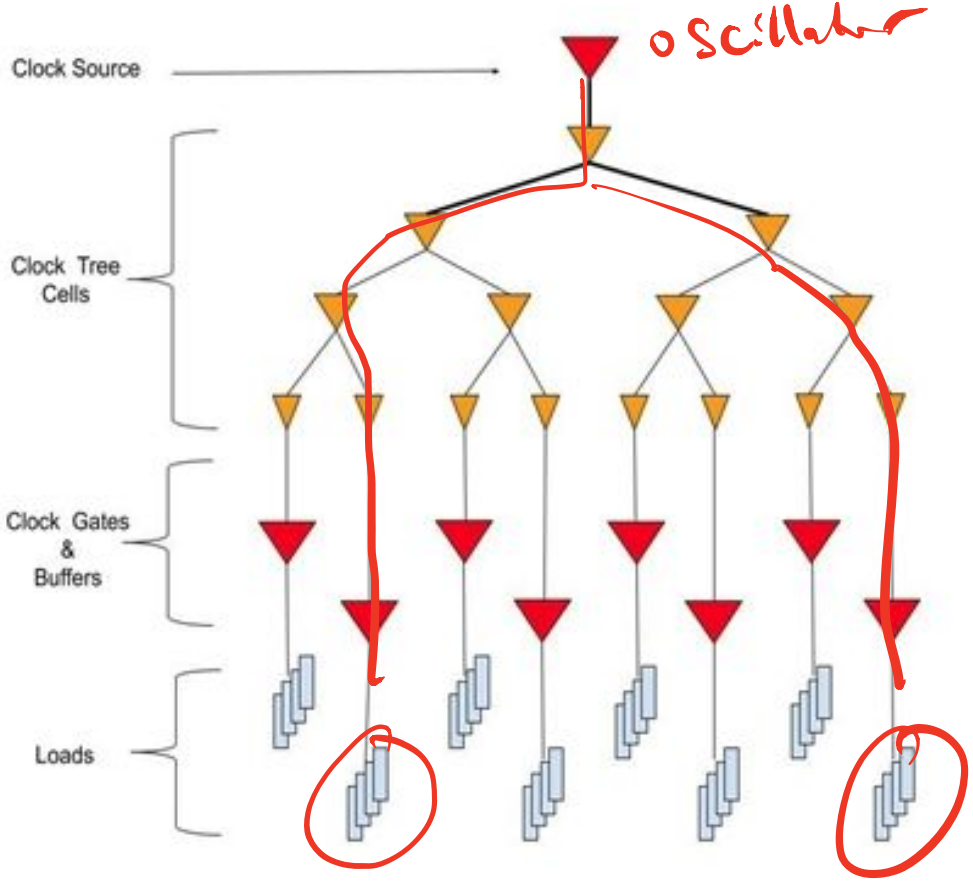


Clock Skew



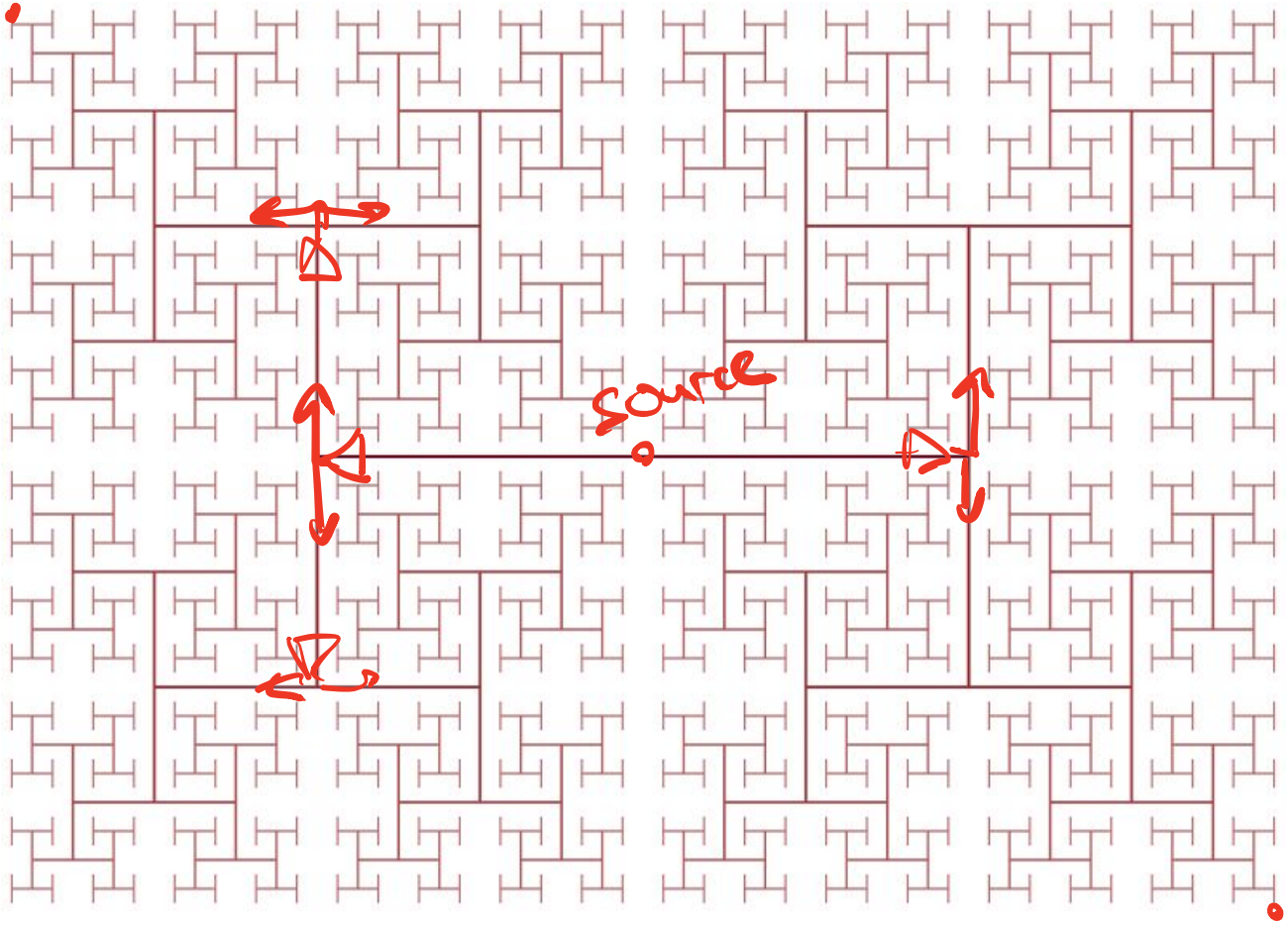
Clock Jitter

Solving Skew: Clock Tree



https://www.semiconductor-digest.com/2020/02/04/clock-tree-optimization-methodologies-for-power-and-latency-reduction/

Spatial Layout: H-Tree



https://en.wikipedia.org/wiki/H_tree

Clock Gating to Save Power

Recirculating register output:

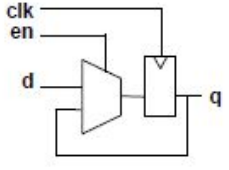


Figure 1a: Feedback MUX

Verilog:
always @(posedge clk)
if (en) q <= d;

Clock-gated output:

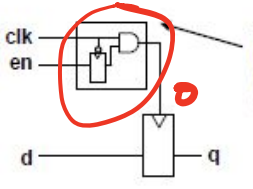
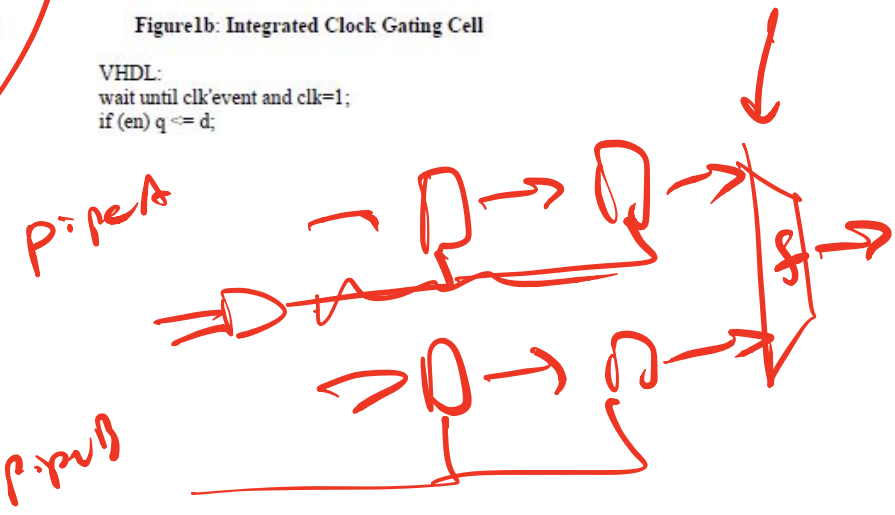


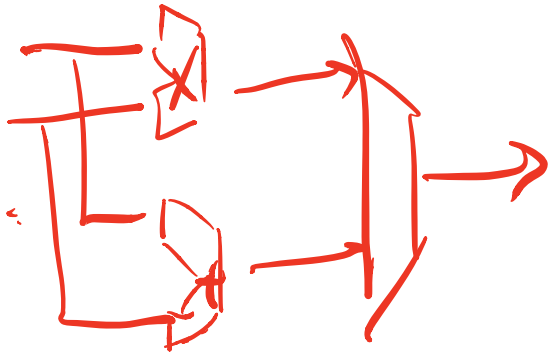
Figure1b: Integrated Clock Gating Cell

VHDL:
wait until clk'event and clk=1;
if (en) q <= d;



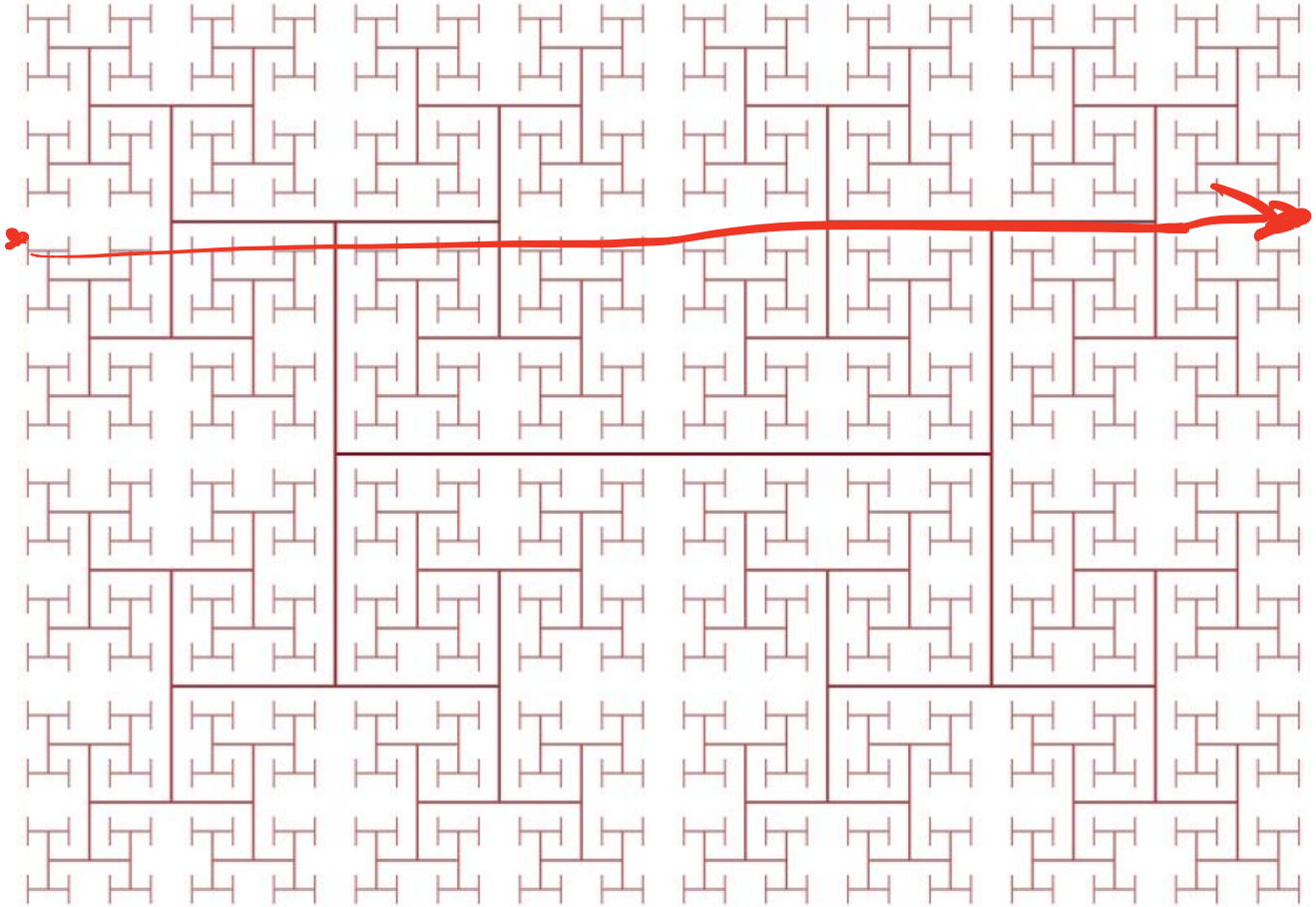
Seems Inelegant...

- Clocks define when data is valid
- Lots of special casing requiring control circuits
  - Clock gating
  - Clock skew/jitter
  - Multi-cycle
  - Pipeline stalls



- Need to close timing on the whole chip

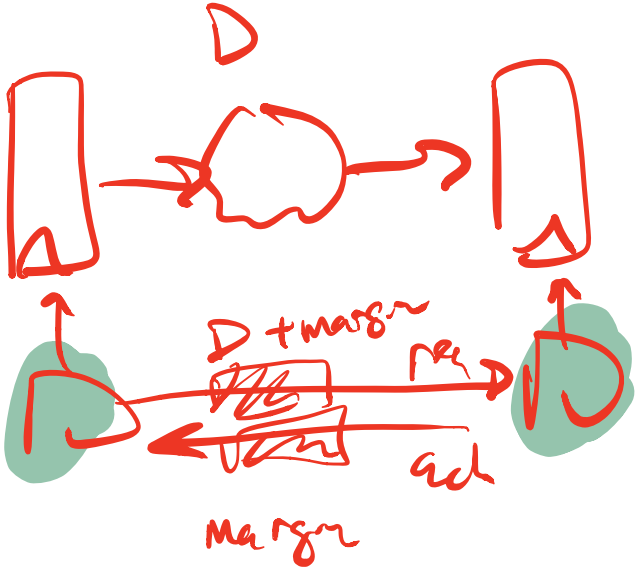
Transmit Data from W to E

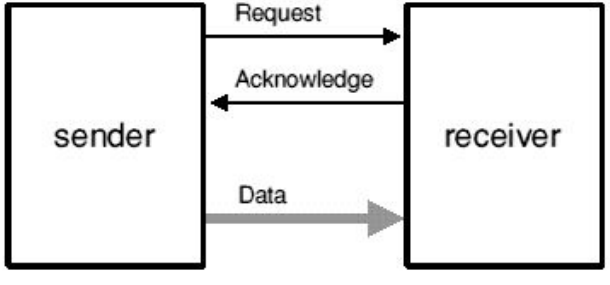


There must be a better way!

https://kitschcornell.wordpress.com/2018/01/08/aesthetics-of-late-night-infomercials/

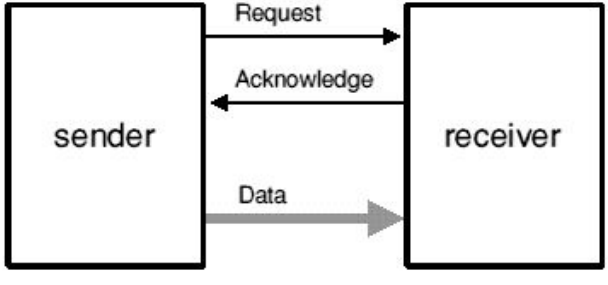
What if “valid” was explicit?



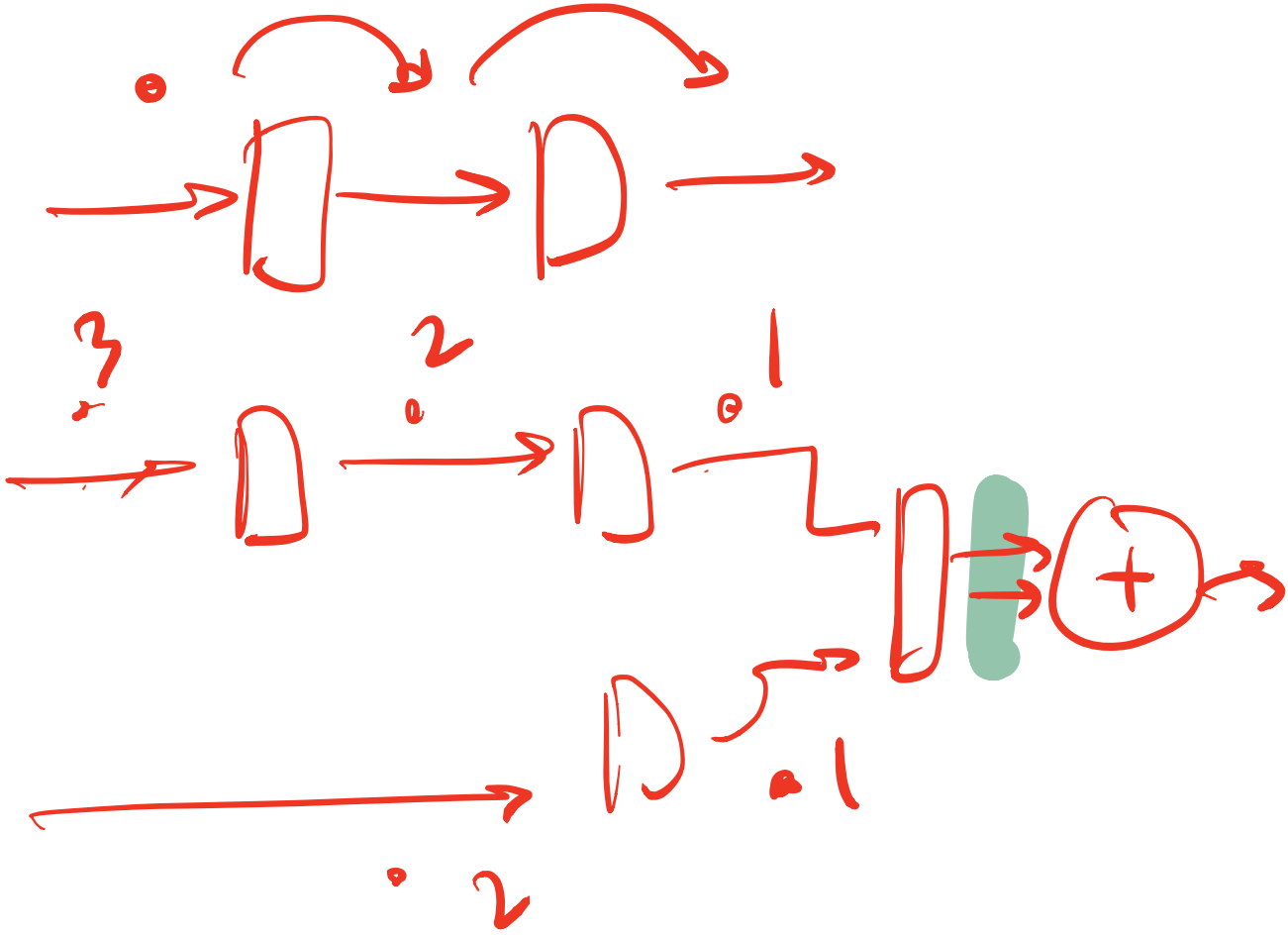


Implications?

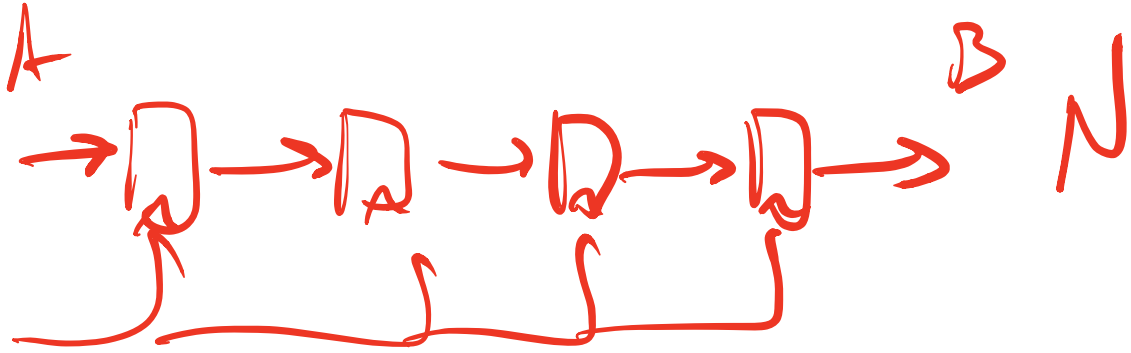
- If there is no new data, no active power!
- What happens if a stage stalls?

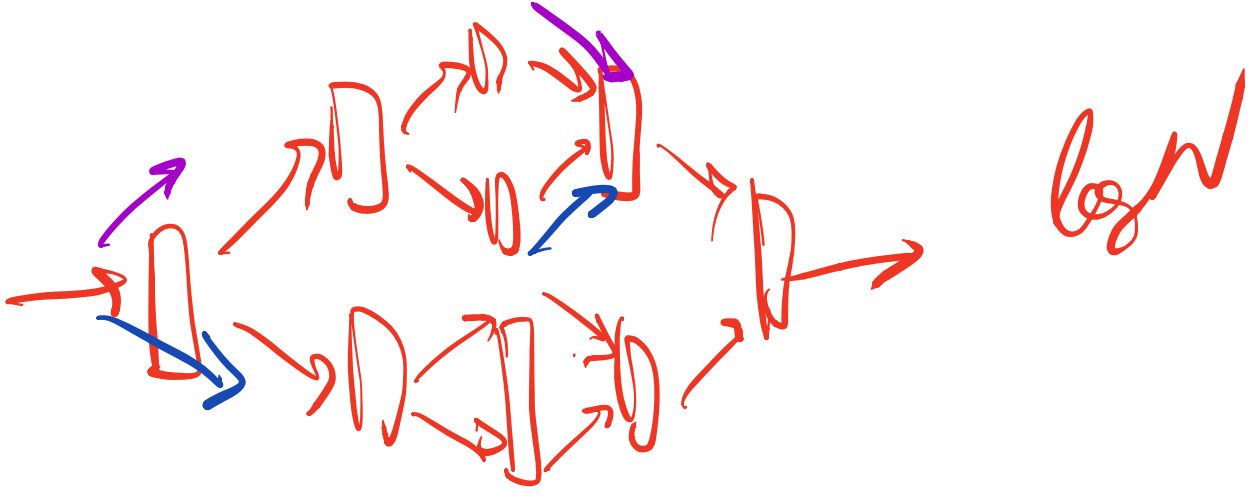


Pipelining

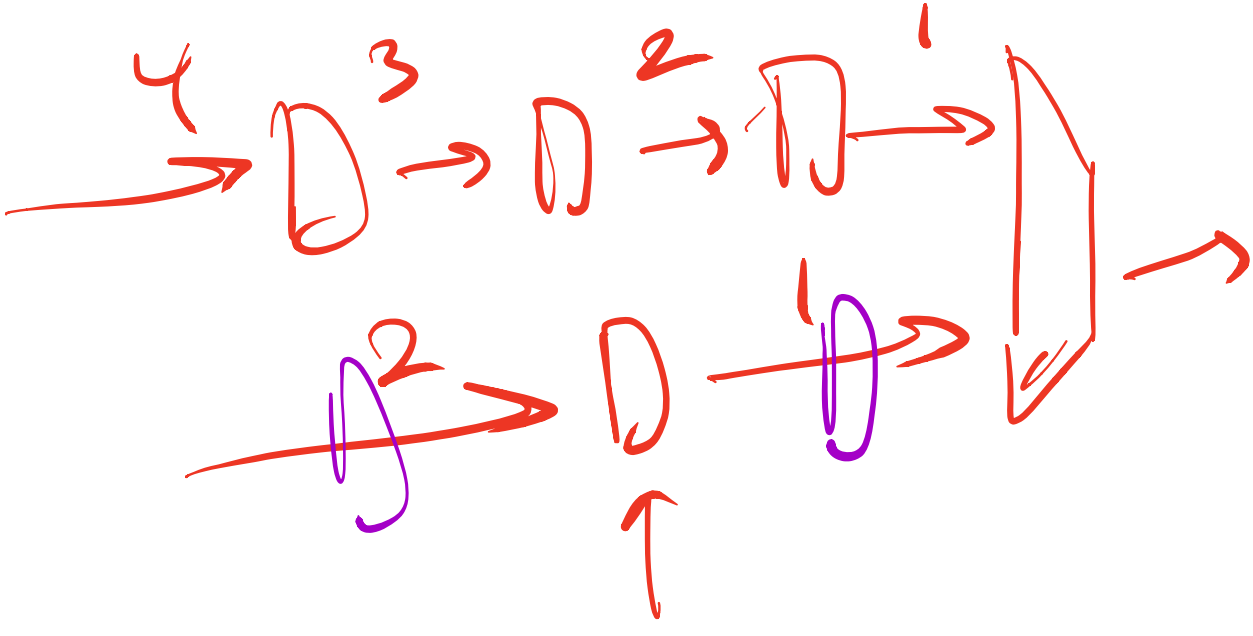


Tree FIFO

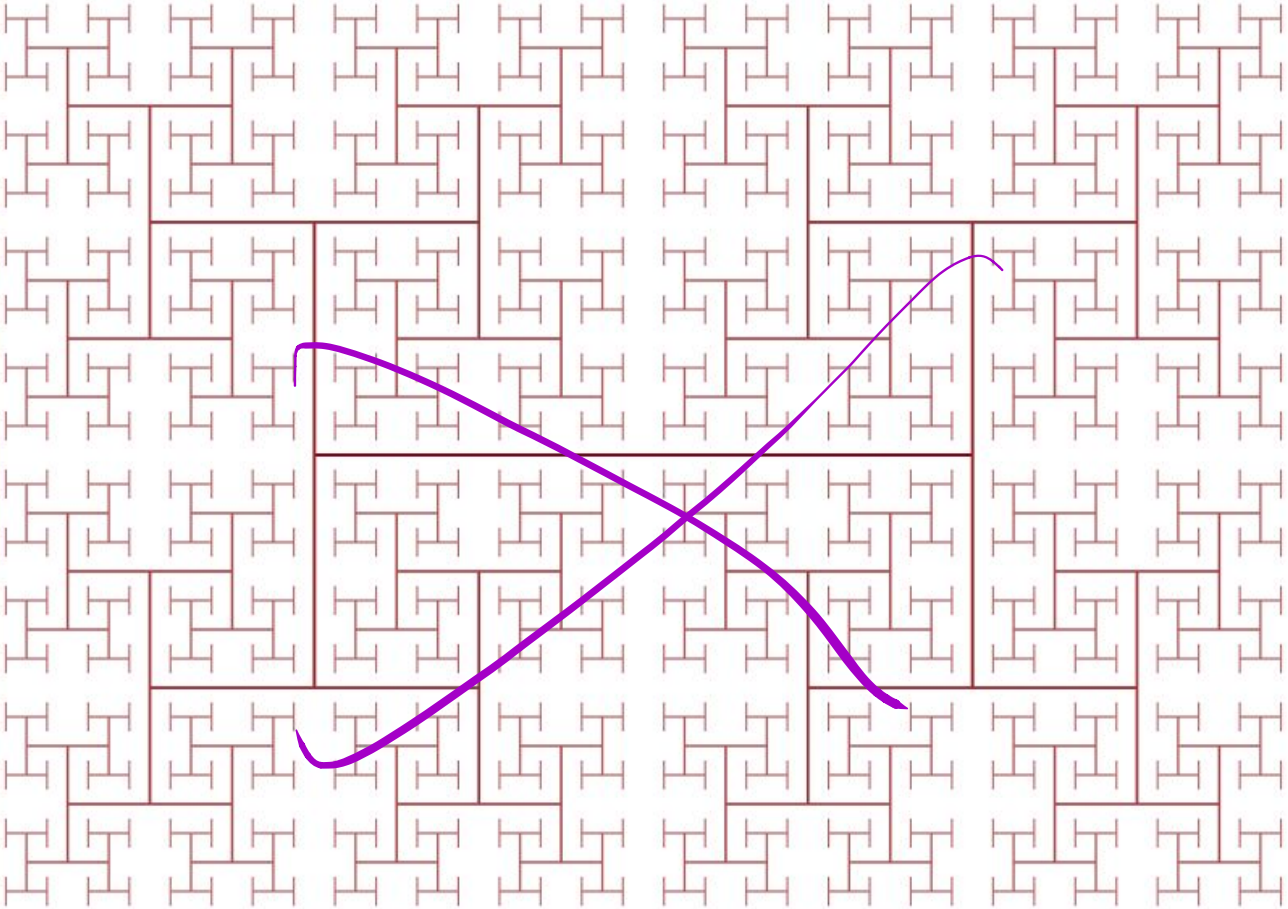




Slack Matching

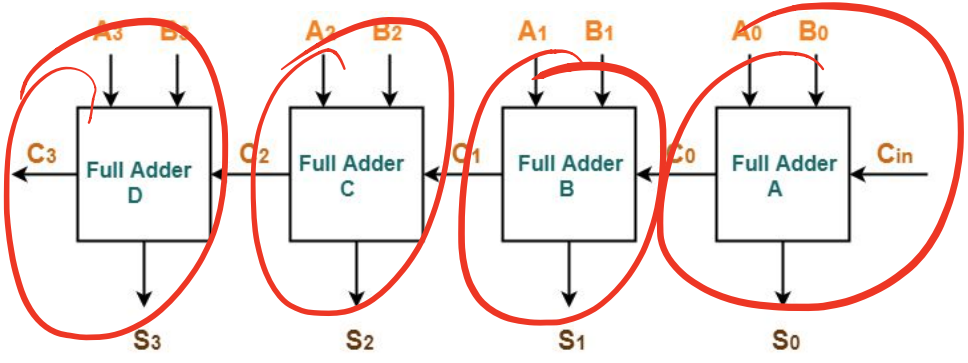


Transmit Data from W to E

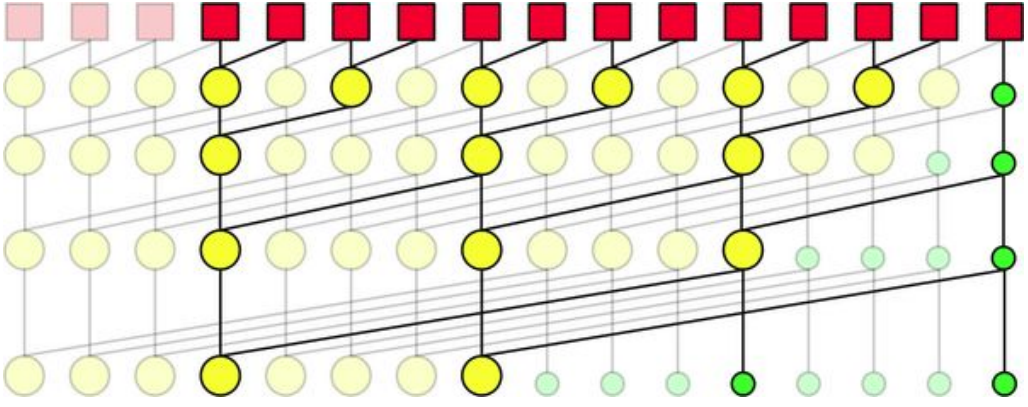


Transmit Data from W to E

Average Case Behavior



4-bit Ripple Carry Adder



https://www.gatevidyalay.com/ripple-carry-adder/
https://en.wikipedia.org/wiki/Kogge%E2%80%93Stone_adder

Average Carry Length

```
Average Carry Length for 16-bit adds is 5.1 bits over 10000 samples
        bucket   |                                                                                                  Total Counts
[0        ,    1) | ######                                                                                           111
[1        ,    2) | ########################                                                                         443
[2        ,    3) | ##########################################################                                       1088
[3        ,    4) | ##########################################################################################       1603
[4        ,    5) | ##########################################################################################       1593
[5        ,    6) | ###############################################################################                  1422
[6        ,    7) | ##################################################################                               1151
[7        ,    8) | ###########################################                                                      789
[8        ,    9) | ##################################                                                               602
[9        ,   10) | ######################                                                                           401
[10       ,   11) | #############                                                                                    249
[11       ,   12) | ###########                                                                                      190
[12       ,   13) | ########                                                                                         136
[13       ,   14) | ####                                                                                             78
[14       ,   15) | ###                                                                                              58
[15       ,   16) | ####                                                                                             86
```

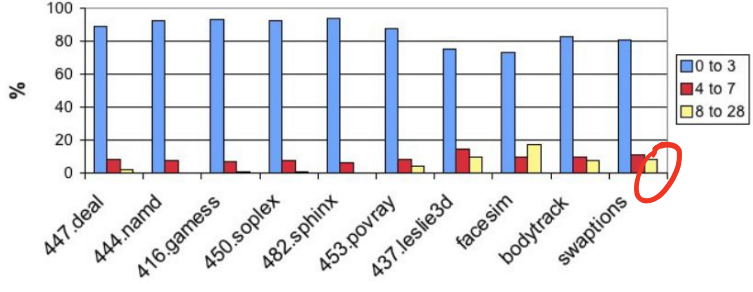
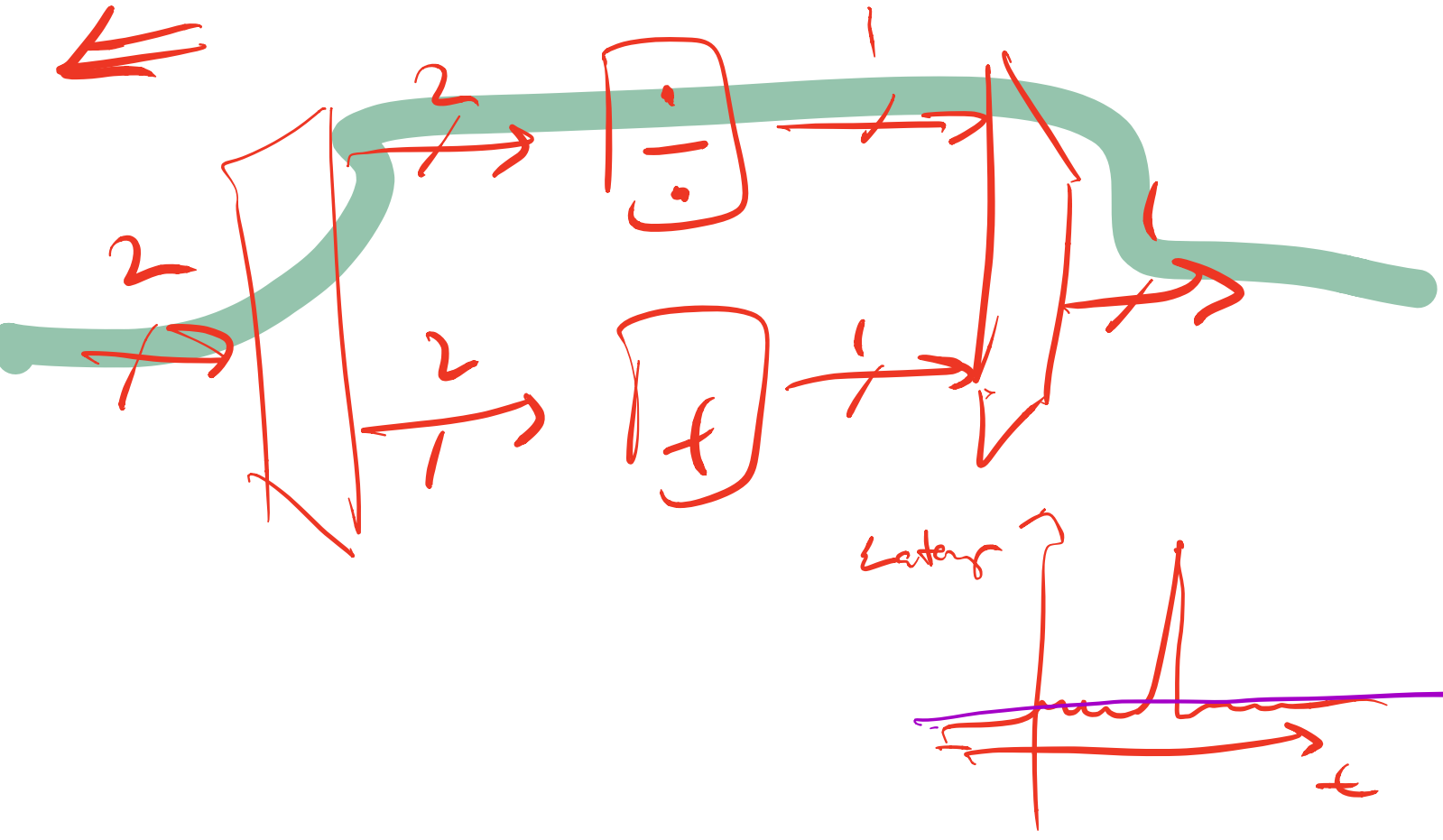


Fig. 4. Radix-4 Ripple-Adder Carry-Length

https://avlsi.csl.yale.edu/~rajit/ps/fpa.pdf

Multi-Cycle ALU



ULSNAP Teaser

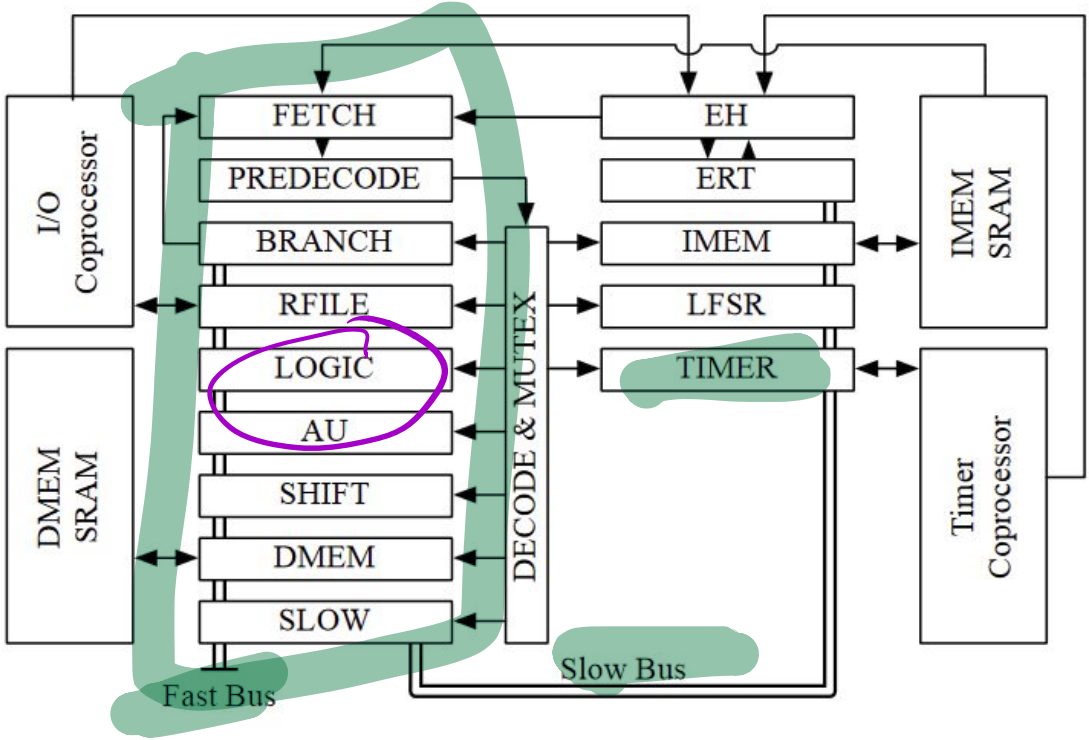


Fig. 2: ULSNAP Architecture

https://www.jontse.com/papers/files/2014_snap.pdf

Problem Pushing

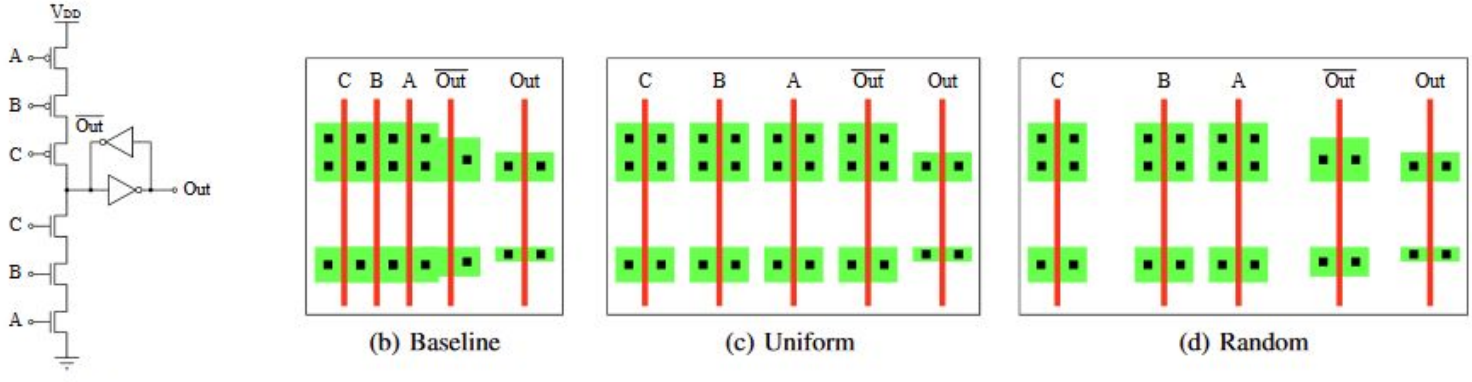
- Synchronous
  - Whole chip timing
  - Lots of complexity and special cases
  - Some noise immunity
  - Lots of power lost to clock

- Asynchronous
  - Localized timing considerations
  - Reduced control complexity (by a lot)
  - Noise is an issue depending on circuit family
  - No active power when idle!

Some Cool Ideas

- Obfuscated Silicon
- Easy to Design Processors
- Neural Network Processors

Obfuscated Silicon

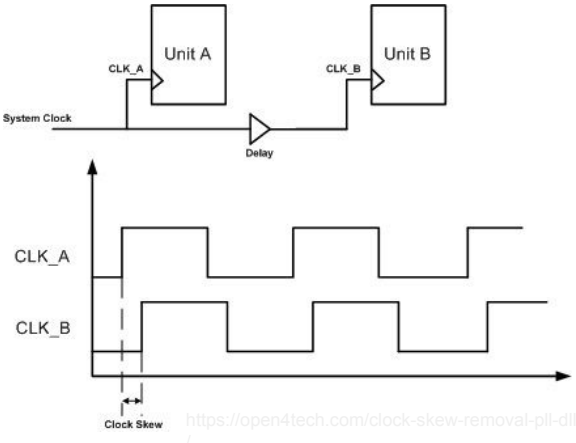


(a) Schematic (b) Baseline (c) Uniform (d) Random

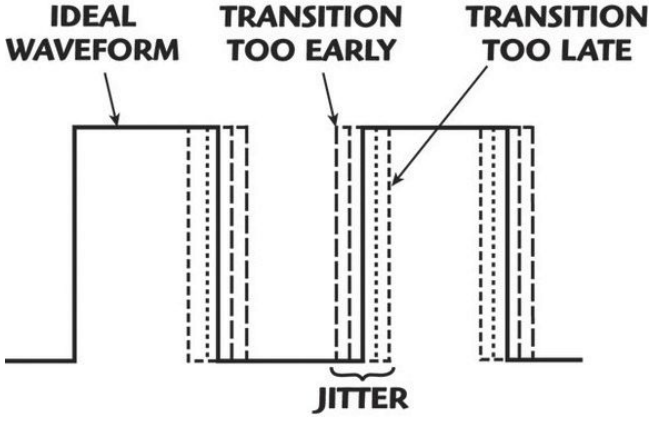
Fig. 1: 3-Input C-Element FEOL

https://www.jontse.com/papers/files/2015_obfuscation.pdf

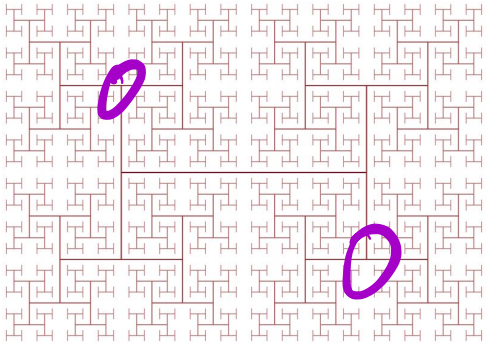
PVT Variation Robustness



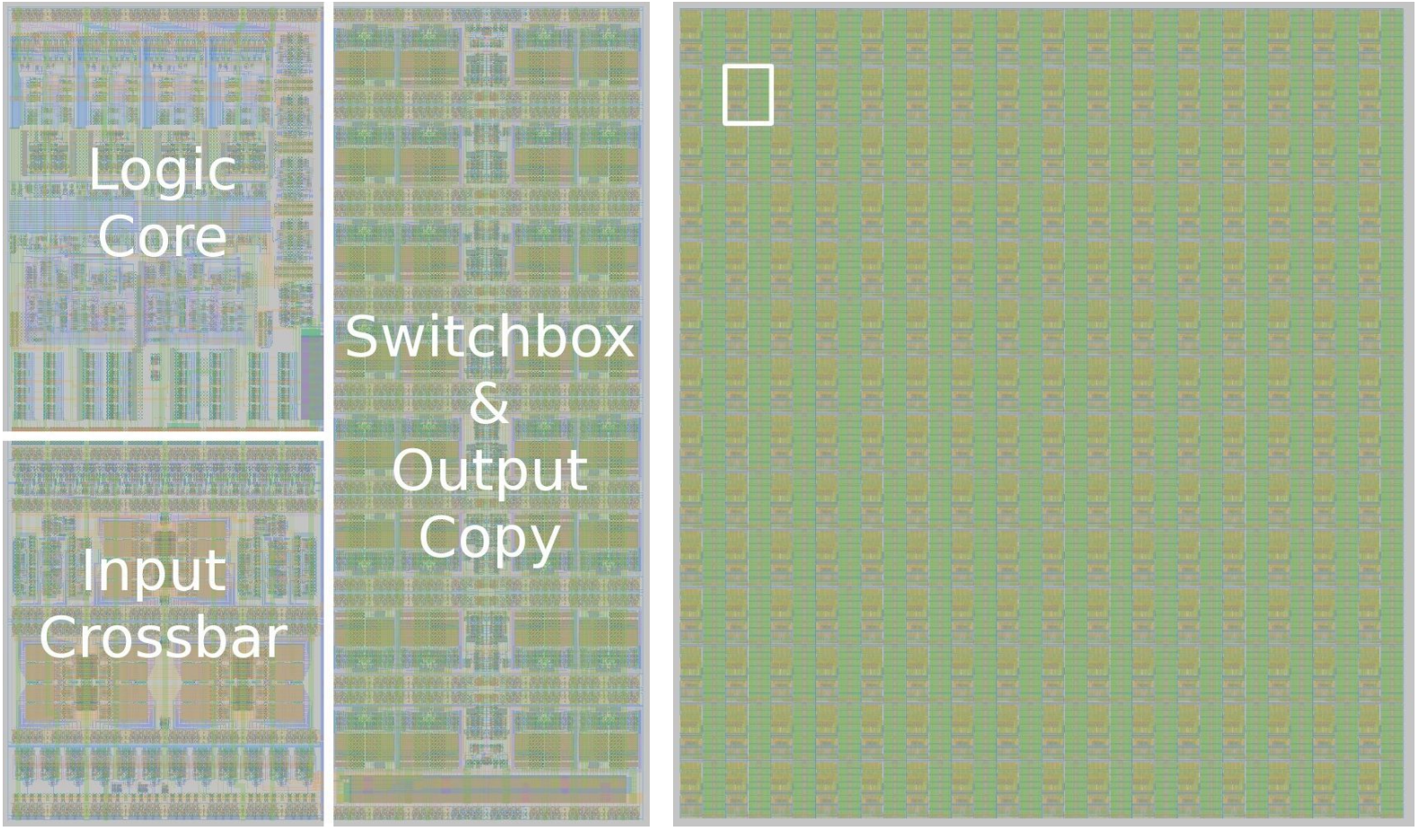
Clock Skew



Clock Jitter



FPGA



FPGA Pipelining

7 Chips, 7 Years