Computer Organization and Architecture Laboratory

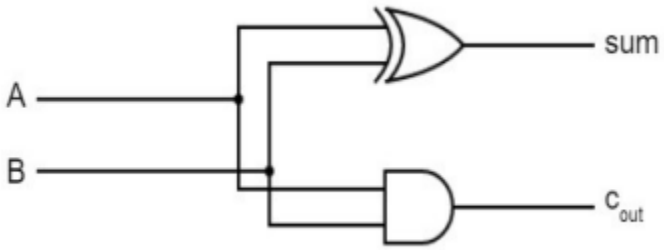
Assignment-3

Group members (Group - 56):

1. **Utsav Mehta (20CS10069)**
2. **Vibhu (20CS10072)**

Design of an Ripple Carry Adder (RCA) :-

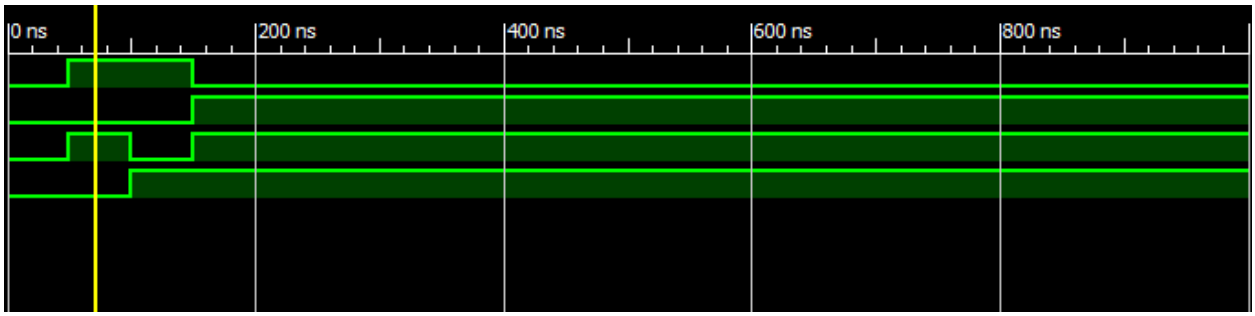
A. Half - adder:
   a. Takes two input bits ‘a’ and ‘b’
   b. Produces two output bits ‘sum’ and ‘carry’
   c. Values of the output bits can be derived from the input bits as -
      i. sum (or s) = a ^ b (bitwise - xor operation)
      ii. carry (or c) = a & b (bitwise - and operation)
   d. The logic circuit for half adder is:



   e. The truth table for half - adder is as shown -

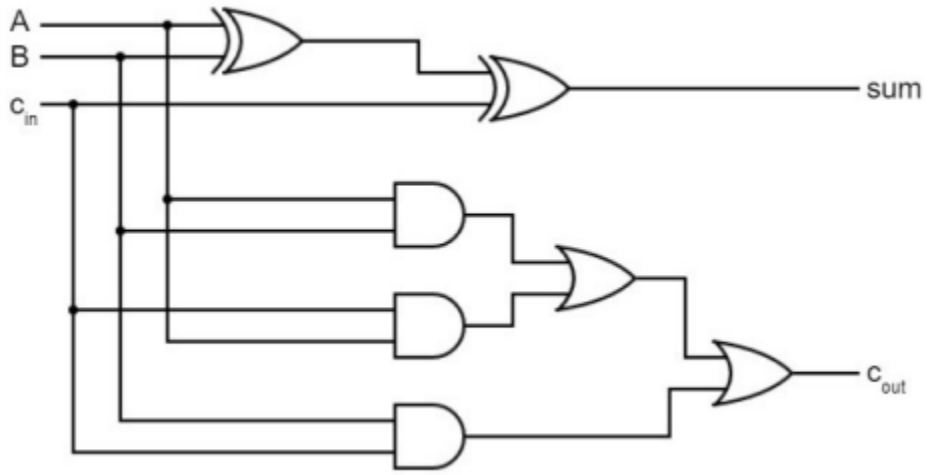
Truth Table (for half adder)			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

   e. The graph observed is as shown -



Relevant files: half_adder.v, tb_half_adder.v

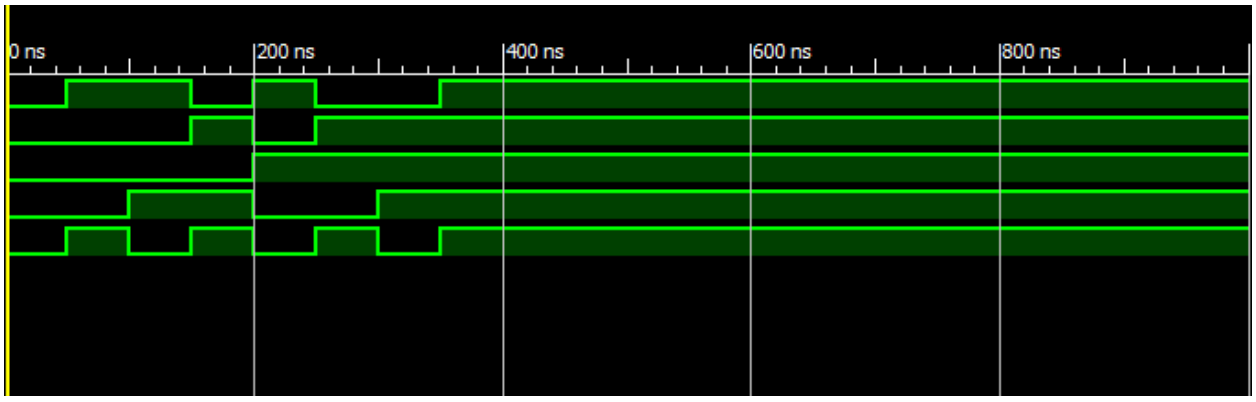
B. Full - adder:
   a. Takes three input bits ‘a’, ‘b’ and ‘carry0’
   b. Produces two output bits ‘sum’ and ‘carry1’
   c. Values of the output bits can be derived from the input bits as -
      i. temp_sum = a ^ b
      ii. temp_carry0 = a & b
      iii. sum = temp_sum ^ carry0
      iv. temp_carry1 = temp_sum & carry0
      v. carry1 = temp_carry0 | temp_carry1
   d. The logic circuit for full adder is as shown:



   e. The truth table for full - adder is as shown -

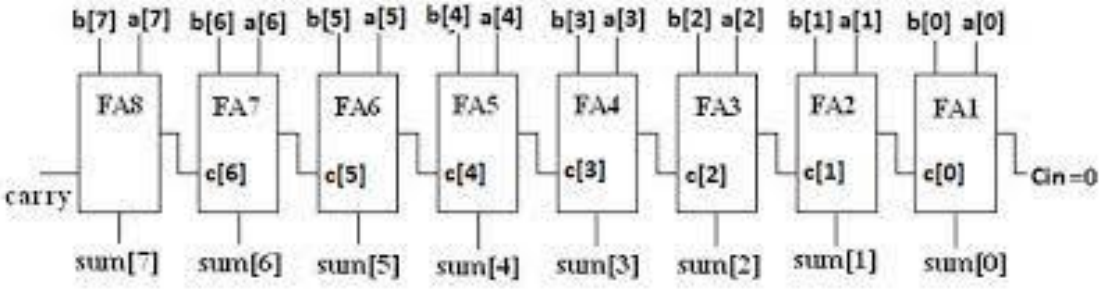
Truth Table (for Full Adder)				
Inputs			Outputs	
A	B	Carry0	Sum	Carry1
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

f. The graph observed is as shown -

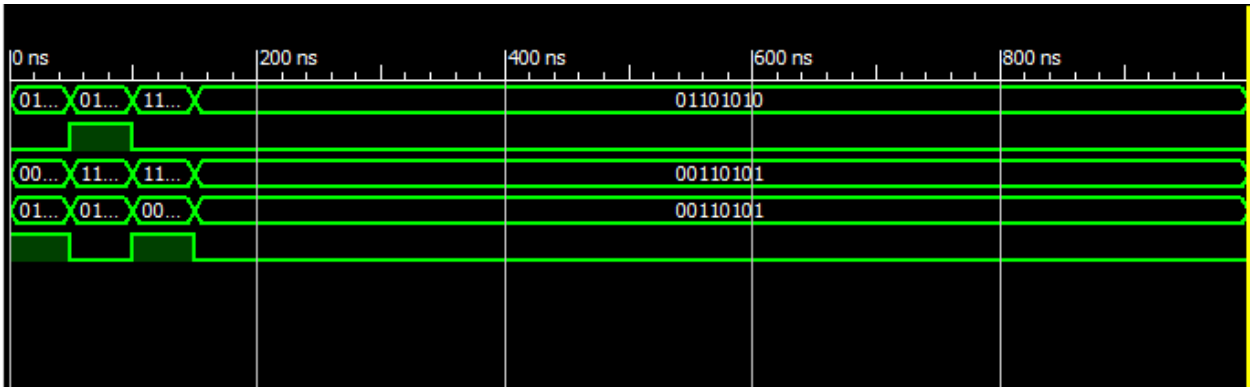


Relevant Files: full_adder.v, tb_full_adder.v

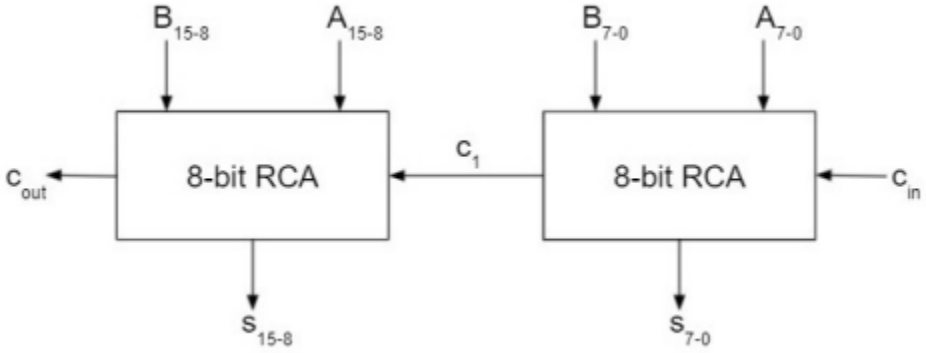
C. Ripple Carry Adders:
   a. 8-bit adder - Take 8 full adders and connect them in cascading fashion



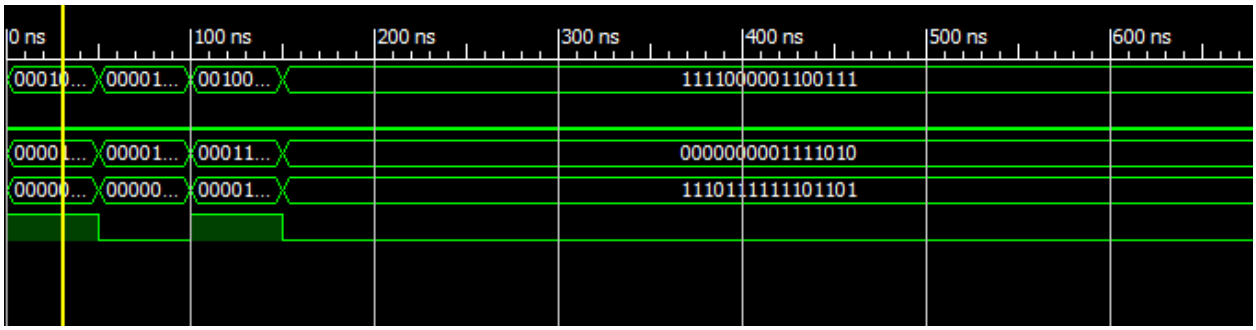
The graph observed for 8-bit ripple carry adder is as shown -



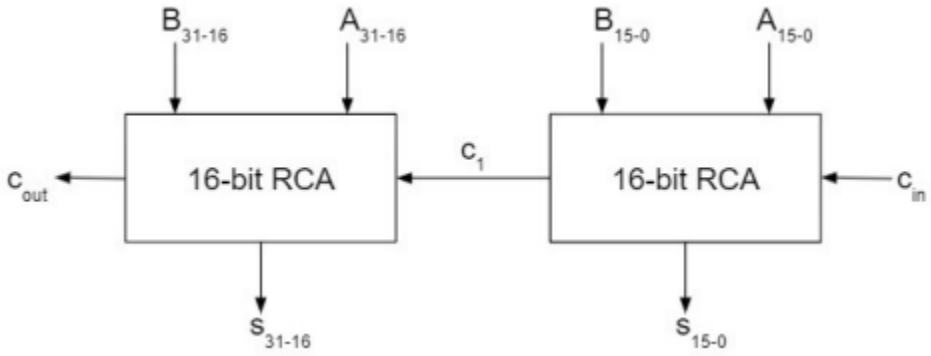
b. 16-bit adder - Take 2 eight bit adders and connect them in cascading fashion



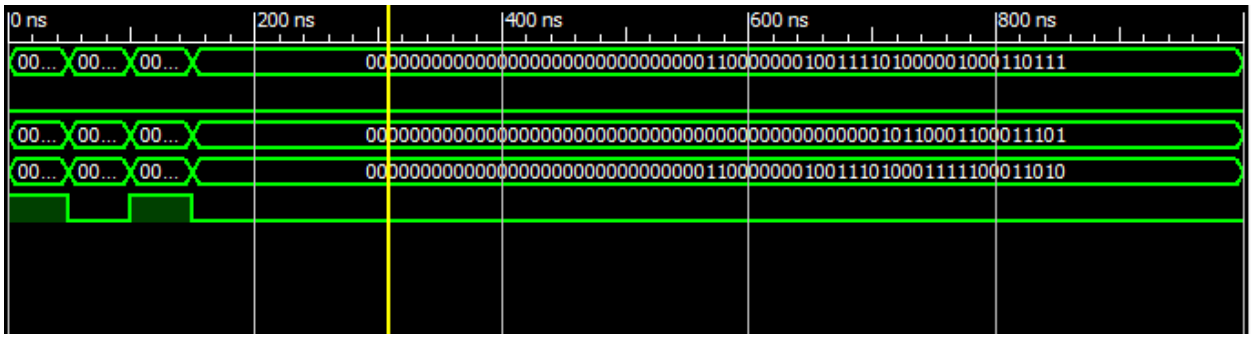
The graph observed for 16-bit ripple carry adder is as shown -



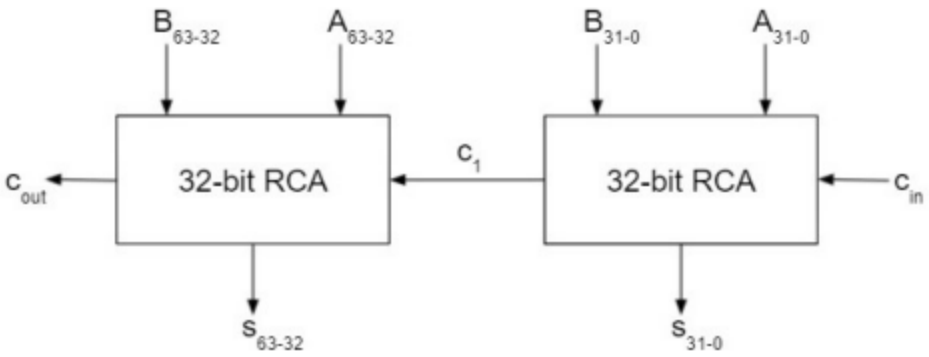
c. 32-bit adder - Take 2 sixteen bit adders and connect them in cascading fashion



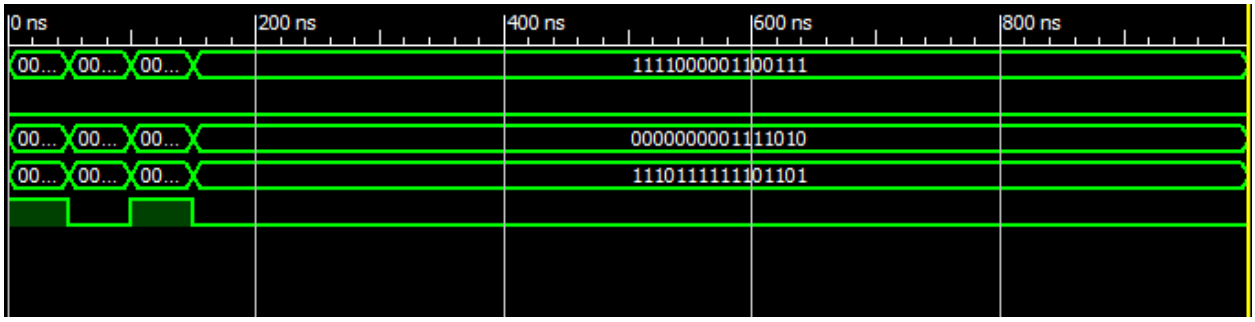
The graph observed for 32-bit ripple carry adder is as shown -



d. 64-bit adder - Take 2 thirty two bit adders and connect them in cascading fashion



The graph observed for 64-bit ripple carry adder is as shown -



The synthesis report (denoting the longest delays in the circuits is):-

Synthesis report	
Ripple carry adder	Longest delay
Half bit adder	1.066
Full bit adder	1.246
8-bit RCA	3.471
16-bit RCA	6.167
32-bit RCA	11.559
64-bit RCA	22.343

Relevant Files:

s8_bit_adder.v, tb_8_bit_adder.v

s16_bit_adder.v, tb_16_bit_adder.v
s32_bit_adder.v, tb_32_bit_adder.v
s64_bit_adder.v, tb_64_bit_adder.v

D. Using the above circuit for calculating differences:

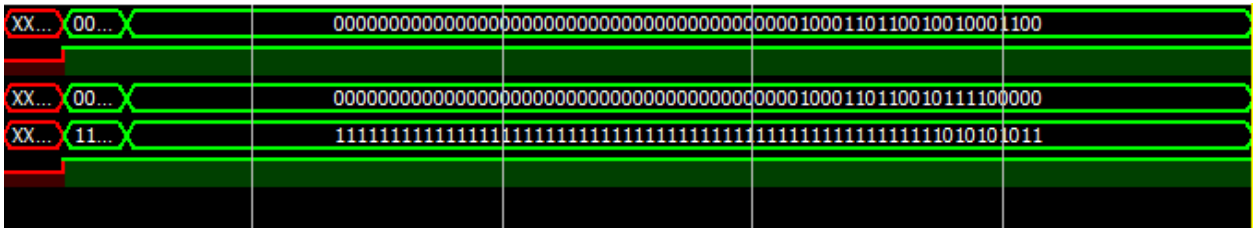
Let the input integers be A and B, and we want to calculate the value of A-B using the ripple carry adders generated above.

The equation can be re-interpreted as A + (-B).
The value of -B can be computed from B by the following steps:

1. Take the two's complement of B
2. Add 1 to the value computed above

Thus, we can add the generated value and A to compute the difference between A and B.

The graph observed for 64-bit ripple carry adder (used as a subtractor) is as shown -



Relevant Files:

substractor.v, s64_bit_adder.v