Digital-to-Analog Converter for FSK

Master Thesis Performed at Lund University, Sweden and Electronics System Department of Linköping University, Sweden

By

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Master Thesis
Electronic Systems
Department of Electrical Engineering
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This thesis demonstrates a low-power, ultra wide band 10 bit DAC with an update frequency of 24 MSPS(Mega Samples Per Second). The DAC uses a L-fold linear interpolation architecture. It includes a 16-tap voltage controlled delay line and a 10 bit binary-weighted DAC with a time interleaved structure. The linear interpolation technique improves the attenuation of mirror components and also reduces the glitch. This helps to relax the analog filter requirements and sometimes an off chip capacitor is enough as low pass filter. The attenuation of image components is doubled in decibels(dB) compared with that of conventional DAC.

In this work various DAC architectures are studied. The current-steering DAC is chosen due to its high speed and high resolution. A binary weighted architecture is chosen to reduce the digital circuits. This helped in reducing the power consumption.

The design and simulation is done with help of Cadence. The layout is done in Cadence Virtuoso and the DDS is integrated with the DAC. The chip is to be manufactured in 130 nm CMOS process.

Keywords
DAC, FSK, 10-bit, layout, 130 nm, Digital-To-Analog , CMOS, Common centroid

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1 Introduction

1.1 Background

Data Converters are one of the main fields of research where a lot of effort and time is spent. Why is it so important ? The answer is many of the natural occurring signals are analog or continuous. Humans can feel only the analog signals. In the modern world of electronics most of the signal processing is carried out in the digital domain with 0s and 1s. The advantages of digital systems are that they can easily be duplicated and do not depend on strict component tolerances and system responses do not drift with temperature. Digital systems are easy to design and have scaled down considerably in size for years. Now billions of transistors are compressed into a small area due to the growth of the digital technology.

So information has to be converted back and forth into analog and digital modes. Here comes the importance of Data Converters. Data Converters are of two types. Analog-to-Digital (ADC) and Digital-to-Analog (DAC). ADC converts the naturally occurring signals to Digital signals and DAC's are interfaces between the digital world and analog real life.

Embedded data converters are becoming a new trend where data conversion interfaces along are integrated along with DSPs (Digital Signal Processing). The trend to put digital and analog circuits together in a single chip to provide efficient and portable frequency systems creates new challenges. Main challenges are feasibility of integrating sensitive analog functions in technologies optimized for digital performance, down scaling of supply voltage, spurious signal pick-up from on-chip digital circuitry and low power consumption.

Much research is going in the field of Data Converters to create low-power, precise devices like Mobile Phones and Audio/Video devices. The spectral purity of the output signal is one of the primary issues associated with data converters. In this work the emphasis is on Digital To Analog conversion process.

Now in this new era digital communication is having a very rapid growth. DAC's have become a integral part of digital communication. DAC's are used in Transceivers where the digital signal is converted to analog signal to be transmitted over a channel or as electromagnetic waves. In the receiver side modern techniques like Direct Conversion de-modulation processes uses DAC's for the demodulation process.

1.2 Objective Of This Thesis

This thesis is one part of an overall task of designing a module for FSK to be used in an UWB system. The FSK system will be used in a transceiver for digital communication. The FSK system has a DDS and two DACs. The DACs differential current signals are directly fed to a RF unit that generates the UWB RF signal. The focus of this thesis is on DAC while the DDS is developed in VHDL as another thesis work. Following tasks are carried out in this thesis :

- Study of different DAC architectures
- Design and implementation of a 10-bit DAC based on the L-fold linear interpolation architecture for low power and with a good spectral purity
- Implemented the DAC at the layout level in UMC 130 nm CMOS process
- Integrated the DAC with DDS which is created through VHDL(Very High Speed Integrated Circuit Hardware Description Language)
- Finally assembled the chip with pads to be mounted in JLCC(J-Leaded Chip Carrier)

1.3 Organization Of Chapters

Chapter 2 gives a brief description of the FSK and FSK system. All the input/output , control signals and interfacing of the the DAC and DDS are discussed.

Chapter 3, a detailed description of basic theory and properties of digital to analog conversion is given.

In Chapter 4, different types of DAC implementation and architectures are described.

Chapter 5 describes the figure of merits associated with digital to analog conversion.

In Chapter 6, the basic theory of Linear interpolation and L-fold DACs are discussed. The benefits of using linear interpolation are discussed. The circuit implementation is discussed here.

In Chapter 7, the implementation of L-fold linear interpolation at the layout level is discussed.

Chapter 8 gives the results and conclusions.

2 FSK based Transceiver

2.1 Introduction

As the work on this thesis is a part of a FSK based UWB transceiver system, this chapter gives a brief introduction to Frequency Shift Keying (FSK). The operation of the FSK based transceiver system and the architecture of the FSK used in this thesis is also discussed.

2.2 Frequency Shift Keying

Frequency-shift keying is a form of frequency modulation in which the modulating signal shifts the output frequency between predetermined values. The instantaneous frequency is shifted between two discrete values termed the mark frequency and the space frequency. This technique is used for digital communication where different frequencies in the carrier signal are used to represent the binary states of 0 and 1. For example using FSK, a modem converts the binary data from a computer into a binary form in which logic 1 is represented by an analog waveform at a specific frequency and logic 0 is represented by a wave at a different specific frequency. Figure 2.1 shows the data signal and transmitted signal. Frequency measurements of the FSK signal are stated in terms of shift, deviation and center frequency. Shift is the frequency difference between mark and space frequencies. Center frequency is defined as the halfway between the mark and space frequencies. Deviation is defined as the absolute value of the difference between the center frequency and the mark or space frequency.

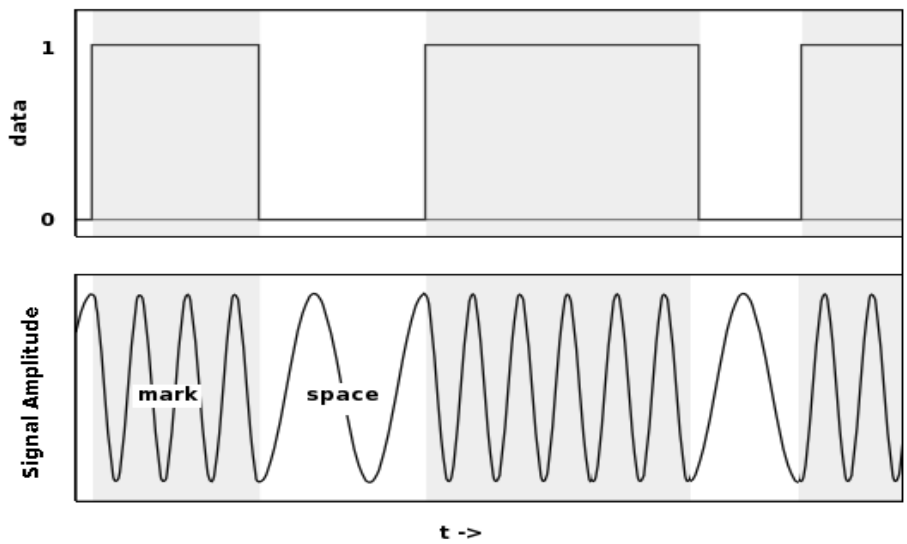

Figure 2.1 FSK modulation

2.3 The Transceiver

A block diagram for the UWB transceiver is shown in Figure 2.2. In the transmitter in the upper part of the figure, a binary data stream $d_{in}(t)$ is generated by the application module, which is the input to the subcarrier generation module. A triangular wave $m(t)$ is generated by the subcarrier module. The subcarrier signal $m(t)$ is the input signal to the RF unit that generates the UWB RF signal $V_{TX}(t)$. The receiver in the lower part of the figure is receiving a UWB signal $V_{RX}(t)$, which is amplified and demodulated to the signal $m(t)$. The wanted output data signal $d_{out}(t)$ is filtered out using a direct-conversion architecture. A received signal strength information (RSSI) signal is also provided to the application module.

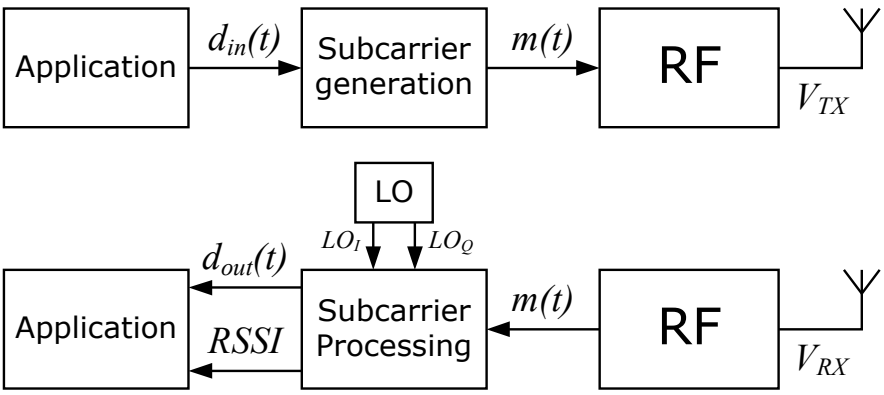

Figure 2.2 Transceiver block diagram

The focus here is to design a single chip containing parts of the transceiver architecture. In the transmitter, the subcarrier generation is the target and in the receiver, the local oscillator (LO) generation is the objective. Both parts are based on a direct digital synthesizer (DDS) and a digital-to-analog converter (DAC). In the transmitter, a frequency shift keying (FSK) architecture is used for the subcarrier generation. Basically the same architecture, can be used for the LO signal generation, but without the input signal d.

2.2 The FSK Architecture

Figure 2.3 shows the architecture of the transceiver. It has both the transmitter and receiver in it. Since the transmitter will be quiet when signals are received and vice versa, the same physical modules can be used by both the transmitter and the receiver. The transmitter needs one DDS for the FSK generation and one DAC to finally generate the subcarrier signal. The receiver is based on one DDS and two DACs for the quadrature signal generation. The transmitter and receiver are sending and receiving on different subcarrier frequencies. When switching between the send and receive mode a control signal TX is used. That signal will then switch between the preloaded values N_{TX} and N_{RX} for the different send and receive frequencies.

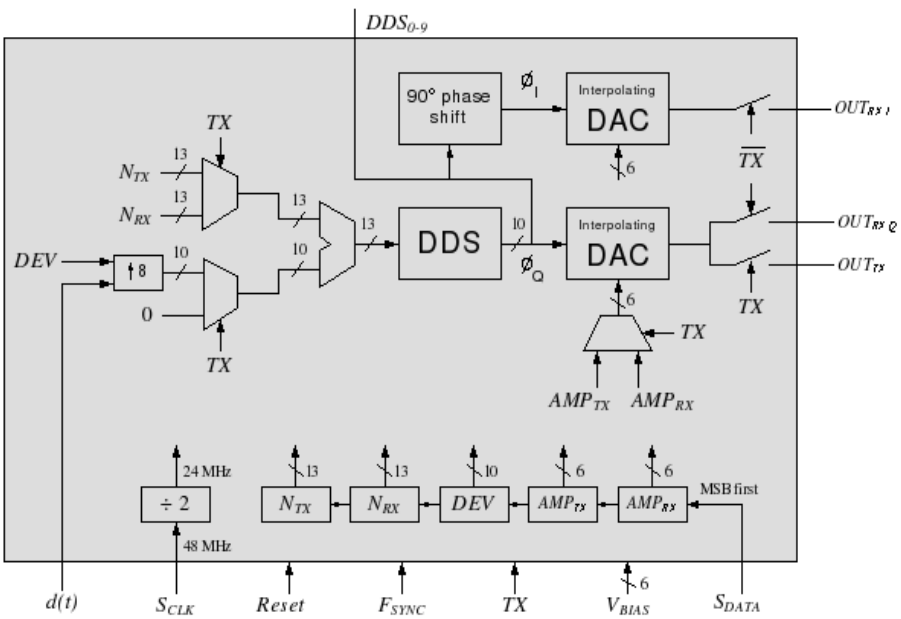

Figure 2.3 Overview of the chip

A preloaded frequency deviation DEV is used for the FSK signal in the transmitter and a zero signal is used in the receiver. Amplitude information, AMP_{TX} and AMP_{RX}, for the DAC is also preloaded. All preloaded values are received serially from the input pin S_{DATA}.

2.3 System Characteristics

The system is designed for low data rates, typically 100 kbps. The input signal is modulated to an FSK signal with a center frequency f_{sub} between 1 and 2 MHz. Table 1 gives some characteristics of the chip.

Table 1. Some characteristics for the FSK chip

Clock frequency f_{clk}	24 MHz (divided from 48 MHz)
Input frequency d_{in}	Typically 100 kHz, Max 125 kHz
Amplitude resolution A	10 bits
Output frequency f_{sub}	1 – 2 MHz
Supply voltage	1.2 V
Power consumption, DDS	100 uW (target)
Power consumption, DAC	100 uW (target)

2.4 Operation Modes and Control Signals

A control signal, T_X, determines the operation mode of the DDS as shown in Table 2. The transmitter and receiver may use different sub-carrier frequencies, f_{sub} that are down loaded and stored in registers to avoid continuous reprogramming when shifting mode. It is important to keep the mode switching times as short as possible. The TX and RX may also require different sub-carrier amplitude levels, which also are included in the programming.

Table 2. State of different parameters during transmit and receive mode

Parameter	TX = 0 Receive mode	TX = 1 Transmit mode	Bits
FSK modulation	Disabled	Enabled	
Quad. output	Enabled	Disabled	
Phase step	N_{RX}	N_{TX}	13
Phase deviation	0	DEV	10
O/P amplitude	AMP_{RX}	AMP_{TX}	6

There are many control signal for the chip. Table 3 gives an overview of the control signals.

Table 3. Overview of the control signals

Control signal	Description
S_{CLK}	24 MHz clock divided from 48 MHz sys-clk
S_{DATA}	48 bit word for programming
F_{SYNC}	Low when programming S_{DATA}
TX	Transmit/receive mode (high for transmit)
Reset	
The Programming (S_{DATA})	
N_{TX}	Transmitter phase step
N_{RX}	Receiver phase step
DEV	Transmitter deviation from the phase step
AMP_{TX}	Transmitter output amplitude
AMP_{RX}	Receiver output amplitude

3 Digital to Analog Conversion

3.1 Basic Ideal Operation

The DAC fundamentally converts finite-precision numbers into a physical quantity, usually an electrical voltage or current or charge as shown in Figure 3.1. A DAC is fed many such numbers at a rate in terms samples per second normally in Mega Samples Per Second (MSPS). This causes the output signal from the DAC to recreate the signal that the samples were measured from with some margin of error. Normally the output signal is a linear function of the input number. The input numbers are written to the DAC, along with a clock signal that causes each number to be latched in sequence. The DAC output signal changes rapidly from the previous value to the value represented by the currently latched number. The effect of this is that the output signal is held in time at the current value until the next input number is latched resulting in a piecewise constant output. This is equivalently a zero hold operation and has an effect on the frequency response of the reconstructed signal.

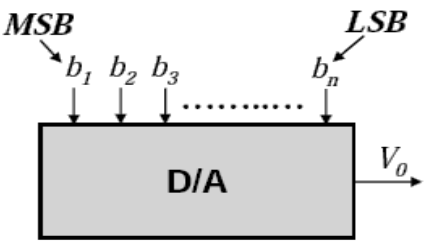

Figure 3.1 DAC basic function

Figure 3.2 shows the ideal sampling of an analog signal and Figure 3.3 shows the reconstruction.

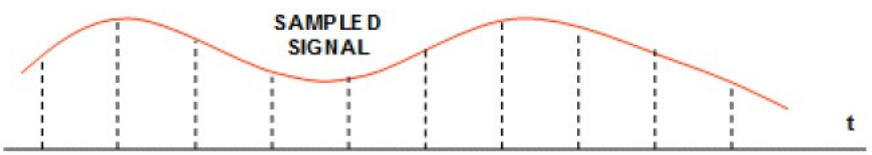

Figure 3.2 Ideally sampled signal

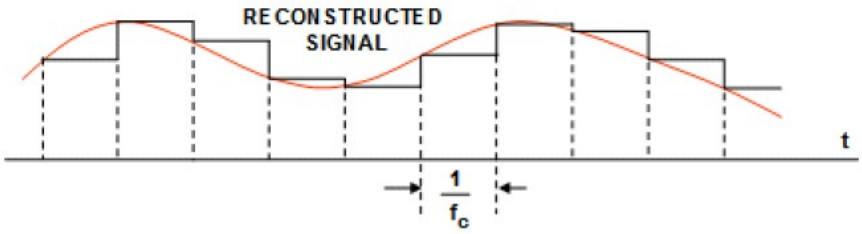

Figure 3.3 Piecewise constant signal typical of a practical DAC output.

Practical DACs do not output a sequence of Dirac impulses which if ideally low-pass filtered, results in the original signal before sampling. But the zero-hold operation instead output a sequence of rectangular pulses, so there is an inherent effect of the zero-hold error on the effective frequency response of the DAC resulting in a mild roll-off of gain at the higher frequencies. This zero-order hold effect is a consequence of the hold action of the DAC and is not due to the sample and hold that might precede a conventional analog-to-digital converter as is often misunderstood. The digital input to a DAC has a limited amplitude resolution because of the limited number of bits. Due to discrete-amplitude there will be quantization noise at the output. Therefore, some information will be lost and this error is called quantization noise.

3.2 DAC Frequency Response

In order to perform any form of processing by digital computers, the signals must be reduced to discrete samples of a discrete-time domain. The operation that transforms a signal from the continuous time to the discrete time is called sampling, and it is performed by picking up the values of the continuous-time signal at time instants. When an analog signal is sampled before applying to a Analog-to-Digital converter the spectrum of sampled signal will be the periodic replication at interval f_s the sampling frequency. This is shown in Figure 3.4 and Figure 3.5.

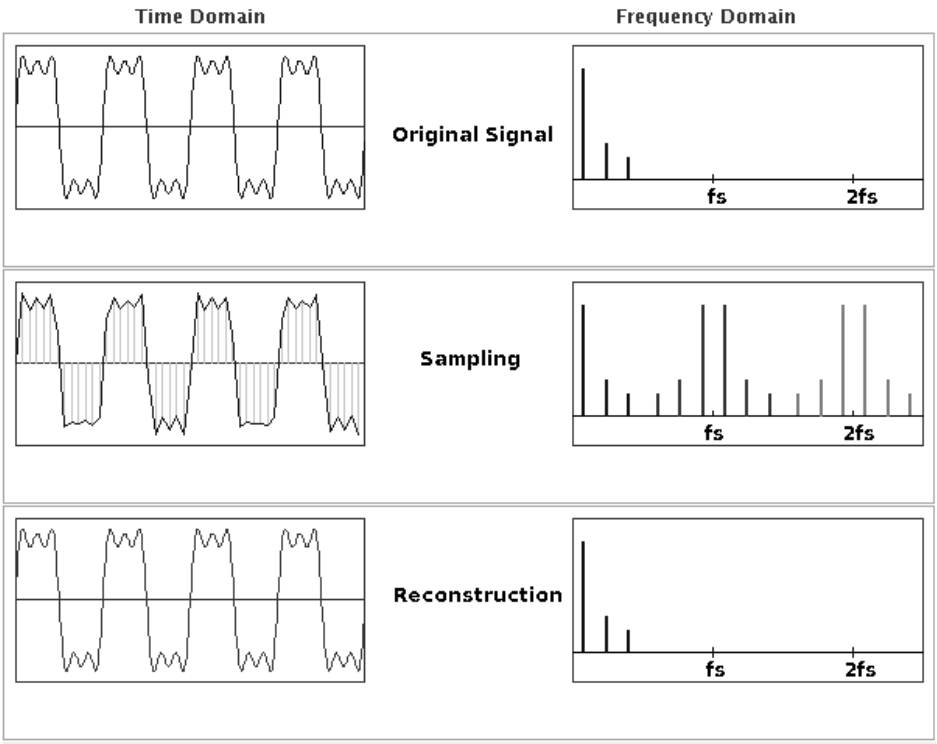

Figure 3.4 Spectrum replication due to sampling

The output spectrum is given by the eq (3.1) and as shown in Figure 3.4.

$$\vec{X}(\omega)=\frac{1}{T}.\sum_{k=-\infty}^{\infty} X(\omega T-k.2\pi) \qquad (3.1)$$

Where $T = 1/f_s$, $\vec{X}(\omega)$ is the output spectrum and $X(\omega)$ is the input signal spectrum.

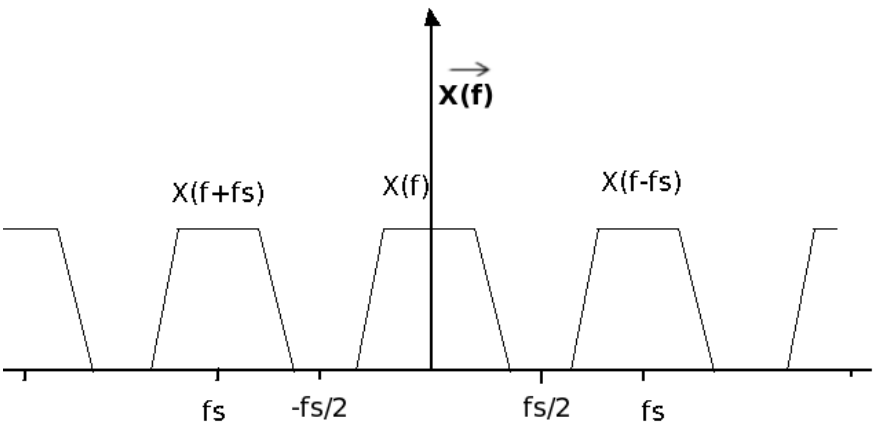

Figure 3.5 Spectrum replication due to sampling

In order to eliminate the mirror components we need a system whose frequency response is

$$P(\omega) = \begin{cases} 1 & |\omega| \le f_u.\pi \\ 0 & |\omega| \ge f_u.\pi \end{cases} \qquad (3.2)$$

The time domain realization of this type of filter is a sinc function as in eq (3.3) and shown in Figure 3.6.

$$p(t) = \sin(t)/t \qquad (3.3)$$

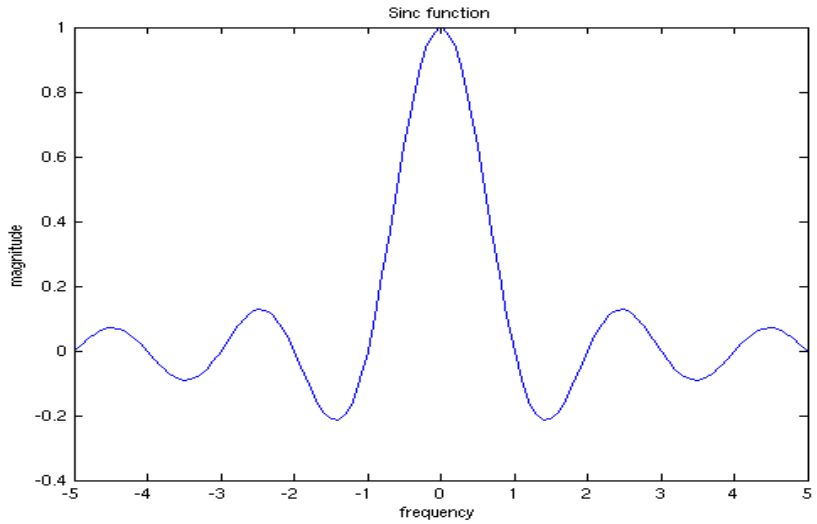

Figure 3.6 The *sinc* function

The *sinc* function is an ideal one with infinite temporal extension on both sides of time axis. Reconstruction by this procedure cannot be practically implemented. So we have to choose a zero-order hold function instead.

$$p(t) = \begin{matrix} 1 & 0 \le t < T \\ 0 & else \end{matrix} \quad (3.4)$$

Thus the output becomes sample and hold during one update period. In the frequency domain this corresponds to a sinc as

$$P(w) = \frac{\sin(wT)}{wT} \quad (3.5)$$

According to Poisson's formula[2], the spectrum of the the analog output signal of a DAC is

$$X(\omega) = \frac{1}{T} . \sum_{k=-\infty}^{\infty} X(\omega T - k.2\pi) . P(\omega T) \quad (3.6)$$

where $T=1/f_u$. f_u is the update frequency, X(w) is the spectrum of the original signal. P(w) is the DAC output spectrum.

This implies that the images of the output spectrum which repeats at the multiples of clock frequency is not completely removed. A low pass filter or image rejection filter is needed at the output to attenuate the images.

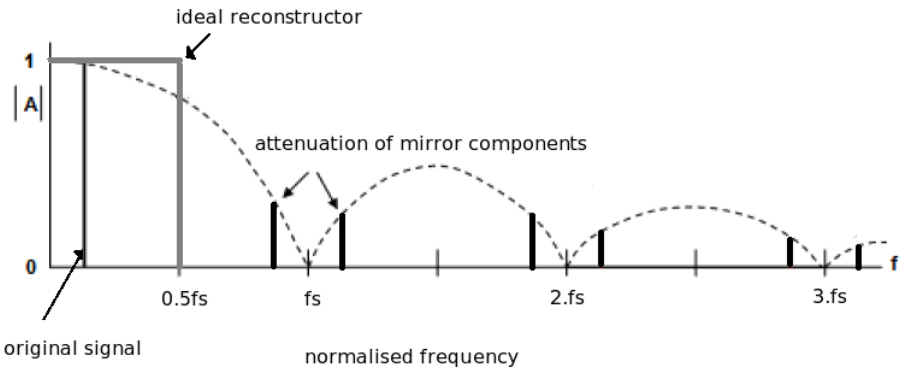

Figure 3.7 Spectrum of the DAC showing both *sinc* type attenuation as dashed line and ideal attenuation as solid line.

Figure 3.7 shows the attenuation due to the sinc function. The mirror components are not removed completely. The dashed line indicates the characteristics of the sinc in the frequency domain and solid line indicates the desired filtering function of an ideal Low Pass filter. For a normal DAC a good analogue low pass filter is mandatory. We will see in a later section how the attenuation of the mirror component is increased by linear interpolation and how analog filter requirements are scaled down**.**

3.3 Transfer Function

For an ideal DAC the analog output signal A_{out} is related to the digital signal as shown in equation (3.7)

$$A_{out} = \sum_{k=1}^{N} \omega_k . b_k \quad (3.7)$$

where ω_k is the weight for the k-the bit b_k and N is the number of bits. Table 4 shows the different type of weight used in different DAC concepts.

Table 4. Different DAC Types and corresponding weights

DAC Types	Weights
binary offset	$\omega_k = 2^{k-1}$ for k= 1, ..., N
signed-digit	$\omega_k = (-1)^{W_N} . 2^{k-1}$ for k= 1, ..., N-1
thermometer	$\omega_k = 1$ for k= 1, ..., N
linear code	$\omega_k = k$ for k= 1, ..., N
2's complement	$\omega_k = 2^{k-1}$ for k= 1, ..., N-1 and $W_N = -2^{N-1}$

Normally the weights are implemented through analog components like current sources or resistors. This is discussed in later section. For binary code N bits there will be 2^N different input codes. The output LSB step compared to full scale (FS) output is called the resolution of DAC. If Δ is the analog output change corresponding to one LSB change in the input signal and if FS is the full scale voltage then resolution R is defined as:

$$R = \frac{FS}{\Delta}$$

for a binary DAC the resolution in bits

$$R = \log_2 (2^N.\Delta / \Delta) = N \quad (3.8)$$

4 DAC Architectures

4.1 Introduction

This chapter discusses briefly the most common types of DAC architectures. There are many different architectures of DAC available and the factors that distinguish them are discussed.

4.2 Classifications Of DACs

The DACs can be classified based on different factors which are discussed below

4.2.2 Classification Based On Mode Of Operation

The main factor that distinguish one DAC from others are their implementation modes namely *voltage mode, current mode* and *charge-redistribution mode*. In voltage mode a reference voltage is divided into a number of different voltage levels using elements like resistor-strings. In current mode the different output levels are obtained by increasing or decreasing the output current controlled by the input bits. In charge-redistribution mode the different output levels are obtained by charge-redistribution among a set of capacitors and uses switched capacitor(SC) techniques. The selection of mode depends upon the need, for example current-mode technique is used for high speed applications.

4.2.3 Classification Based On Bit Weights

Once the operation mode is selected the transfer function distinguishes one DAC from other. Most of them are implemented in a binary weighted format or thermometer code format. The Table 4 in previous chapter is based on this classification.

4.2.3 Classification Based On Sampling Frequency

One classification is based on the clock frequency of the sampling clock. If sampling frequency is slightly greater than the bandwidth of the signal then it is called **Nyquist DAC**. If the sampling frequency is much greater than the bandwidth of the signal then it called an **Oversampled DAC**.

4.3 Current Source DAC- Binary Weighted

Figure 4.1 shows a current steering DAC of binary weighted type. The reference elements are current sources and sum elements are only wire connections. As shown we can get the complementary outputs. The switches are normally MOS transistors. The switches are controlled by the input bits. The k-th bit current source is formed by connecting 2^{k-1} current sources in parallel. This approach of using unit elements improves matching of current sources after layout is done. The output current is given by eq (4.1)

$$I_{out} = b_0.I_{unit} + b_1.2^1.I_{unit} + ... + b_{N-1}.2^{N-1}.I_{unit} \qquad (4.1)$$

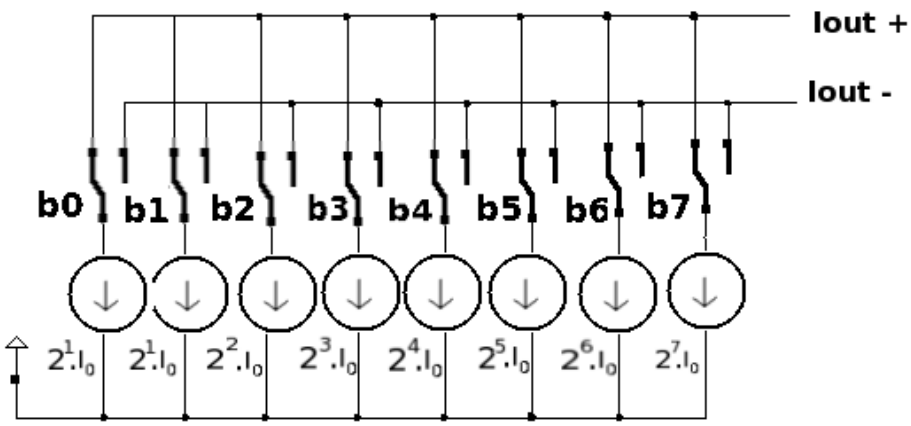

Figure 4.1 Binary weighted current steering DAC

4.4 Current Source DAC - Thermometer Coded

The thermometer coded DAC contains an equal resistor or current source segment for each possible value of DAC output. A 10-bit thermometer DAC would have 1023 segments, i.e 2^N-1 thermometer bits, corresponding to N binary bits. The input binary code is encoded into thermometer code as shown in the figure 4.2. This is the fastest and highest precision DAC architecture but at the expense of high cost, due to additional area and encoding circuits needed. Since elements are of equal size the matching becomes much simpler than a binary DAC. This is used for low resolutions since otherwise the encoding circuits become circuits too large.

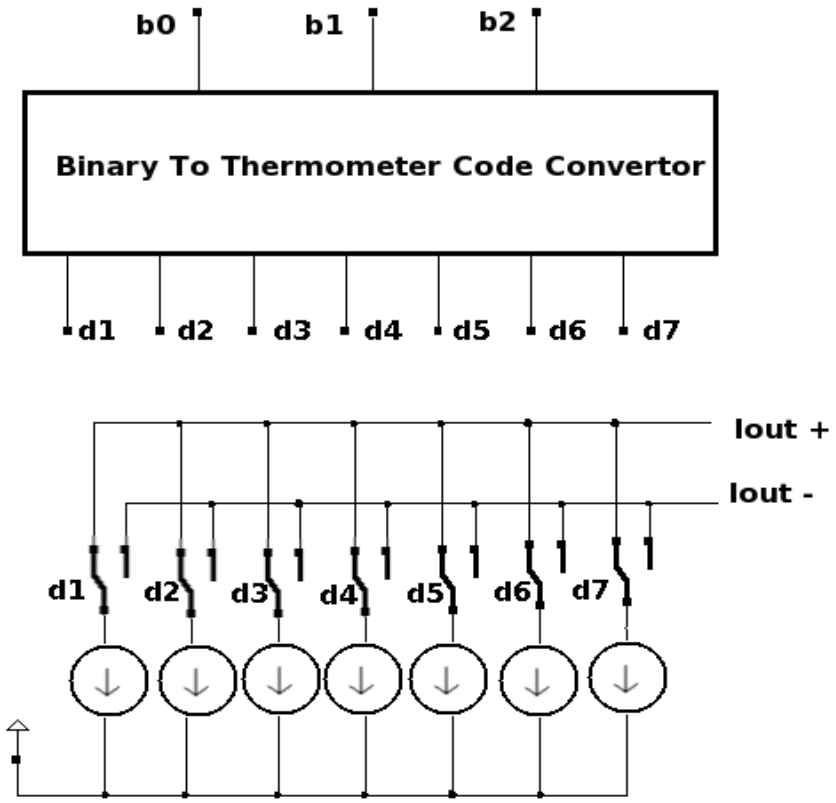

Figure 4.2 Thermometer coded DAC

4.5 Charge Redistribution Switched Capacitor DAC

The basic architecture of a switched-capacitor based on charge distribution is shown in the Figure 4.3. Samples of charge proportional to the unit capacitor value C, the reference voltage V_{ref}, and the digital input word are sampled into an array of input capacitors during one phase. During next phase, charge from input capacitors are integrated onto the integrating capacitor, Ci, to generate an output proportional to the input code.

The limitations of these converters are matching of capacitors, the switch on-resistance, the finite bandwidth of amplifier and *KT/C* noise. Monotonicity depends on element matching. The output voltage is given by eq(4.2)

$$V_{out} = \frac{\sum_{k=0}^{N-1} b_i 2^i}{2^N} . V_{ref} \quad (4.2)$$

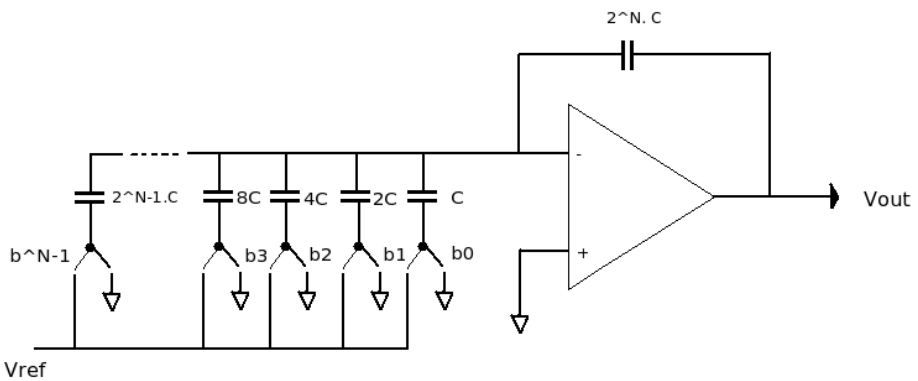

Figure 4.3 Charge Redistribution DAC

4.6 R-2R Ladder DAC

The R-2R DAC is a binary weighted DAC that uses a repeating cascaded structure of resistor values R and 2R as shown in Figure 4.4. This improves the precision due to the relative ease of producing equal valued matched resistors. However, wide converters performs slowly due to increasingly large RC-constants for each added R-2R link. The resistances are nonlinear and contains signal-dependent capacitance, which yield distortion. The output voltage is given by eq(4.3)

$$V_{out} = \frac{R_f}{R} . V_{ref} . [\frac{b0}{16} + \frac{b0}{8} + \frac{b0}{4} + \frac{b0}{2}] \quad (4.3)$$

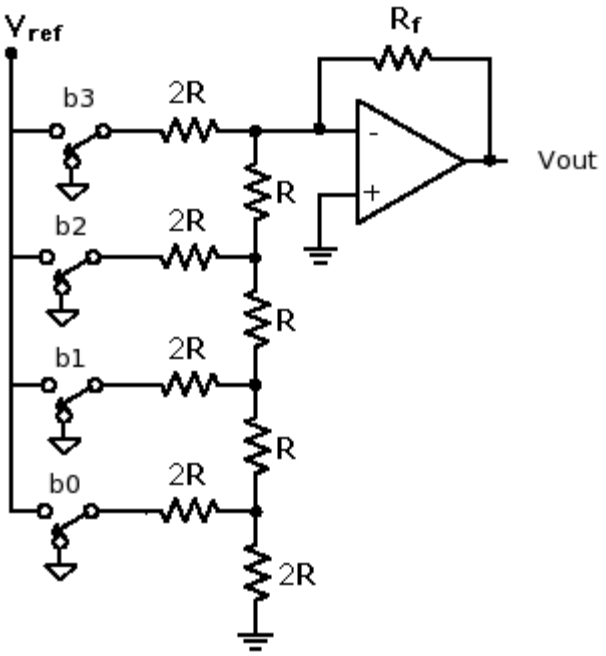

Figure 4.4 A 4-bit R-2R ladder DAC

4.7 Resistor String DAC

The resistor string DAC is a voltage based technique [4]. As shown in Figure 4.5 2^N resistors of equal sizes are needed, which generates 2^N equally spaced voltages. This takes the full advantage of the availability of almost perfect switches in MOS technologies. It is fast and inherently monotonic. The disadvantages are it needs 2^N resistors and 2.2^N switches. For more than 10 bit of resolution the settling time increases significantly.

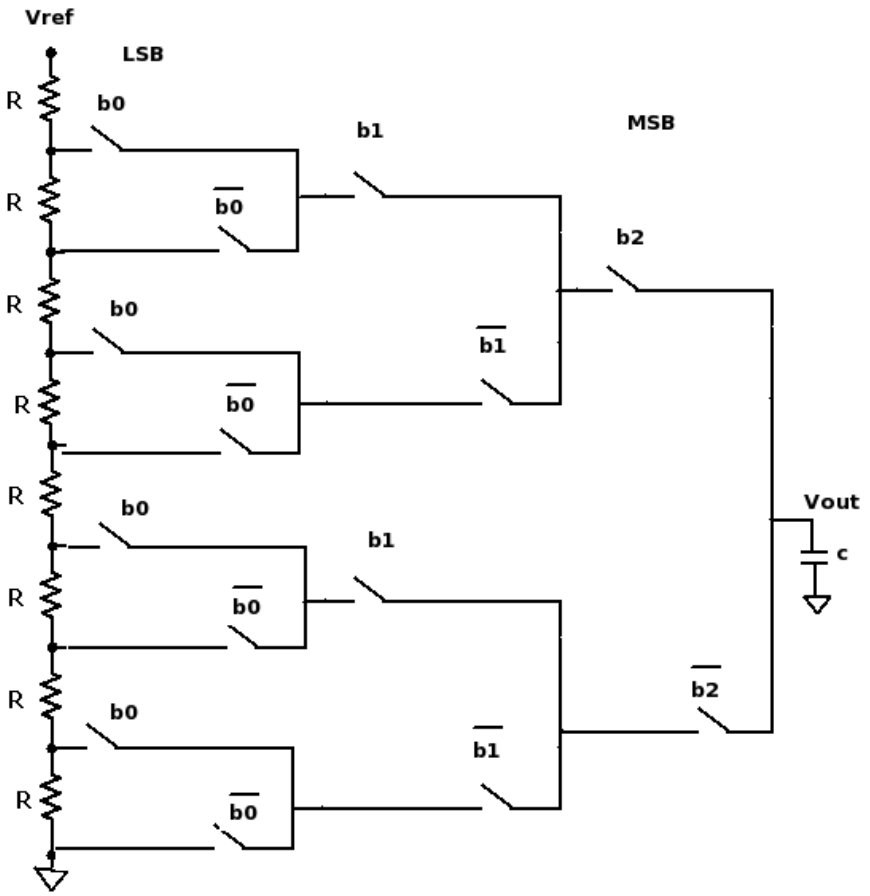

Figure 4.5 Resistor -String DAC

4.8 Oversampling DACs

Oversampling DACs uses interpolation technique to reduce the analog circuits. This is preferred when high linearity is required over high bandwidth. Majority of the circuit is implemented with digital circuits. Therefore many of the analog matching problems associated with other type of DAC are less here. It uses a negative feedback loop, in a technique called delta-sigma modulation. This results in an effective high-pass filter acting on the quantization noise, thus steering this noise out of the low frequencies of interest into the high frequencies of little interest, which is called noise shaping. The quantization noise at these high frequencies are removed or greatly attenuated by use of an analog low-pass filter at the output (sometimes a simple RC low-pass circuit is sufficient). Most very high resolution DACs (greater than 16 bits) are of this type due to its high linearity and low cost. Higher oversampling rates can either relax the specifications of the output low-pass filter and enable further suppression of quantization noise.

4.9 Linear Interpolation DAC

The linear interpolation DAC combines the digital FIR filter and DAC function. The design of such a DAC is relatively easy, and the digital part can be scalable. The required chip area is small and power consumption is low. This is the architecture used in the thesis and it will be discussed in later sections in detail.

4.10 Hybrid Architectures

Hybrid DACs, use a combination of the more than one techniques in a single converter. Most DAC integrated circuits are of this type due to the difficulty of getting low cost, high speed and high precision in one device. The Segmented DAC, which combines the thermometer coded principle for the most significant bits and the binary weighted principle for the least significant bits is a popular architecture. In this way, a compromise is obtained between precision (by the use of the thermometer coded principle) and number of resistors or current sources (by the use of the binary weighted principle).

5 DAC Figures of Merit

5.1 Introduction

Different applications have different performance requirements. To preserve the sound quality in audio, for example, the preeminent target is to have a high dynamic range with little or no distortion. For video systems, instead, the DAC linearity is the crucial parameter to ensure a good picture quality. Hence selecting the right DAC for a particular application needs the knowledge of the performance requirements this device has to meet. Consequently the identification of the basic DAC performance parameters and their definition become absolutely necessary. Different performance measures can be used to characterize the quality and performance of DACs. DACs performance can be divided into three types: static performance, frequency domain performance and time domain performance.

5.2 Static performance

Static performances describe how well the output matches the input digital code under DC conditions. The static non-linearities dominate distortion at lower output frequencies. The main static performance measures are quantization noise, gain and offset error, differential nonlinearity (DNL), and integral nonlinearity (INL).

5.2.1 Quantization Noise

A DAC itself does not generate quantization noise when the number of bits or resolution of the DAC is same or higher than that of the input digital signal. The quantization is caused due to finite number of input bits and the DACs static and dynamic nonlinearity. Normally this appears as white noise in the output spectrum. The rms value of this error is[2] :

$$P_q = \frac{\Delta^2}{2} \qquad (5.1)$$

where Δ = LSB step. When a sine wave is used to calculate the SNR, the maximum amplitude of the sine wave output without causing saturation is $\Delta.2^{N-1}$ and the average signal power is:

$$P_s = \frac{(\Delta . 2^{N-1})^2}{2} \qquad (5.2)$$

Therefore the SNR of an ideal converter is

$$SNR = \frac{P_s}{P_q} = \frac{(\Delta . 2^{N-1})^2/2}{\Delta^2/2} = \frac{3}{2}.2^{2N} \quad (5.3)$$

This can be expressed in terms of dB by the well known formula:

$$\mathbf{SNR_{dB} = 6.02.N + 1.76\ dB} \quad (5.4)$$

So, a 10-bit ideal DAC should have a SNR not less than 62 dB, but normal working circuits has an average SNR of 58 dB.

5.2.2 Offset error and Gain error

Offset is the difference between an ideal and actual DAC output when zero digital code applied to the input. Gain error is the difference between an ideal and actual output when full scale digital code is applied to the input. These are shown in the Figure 5.1.

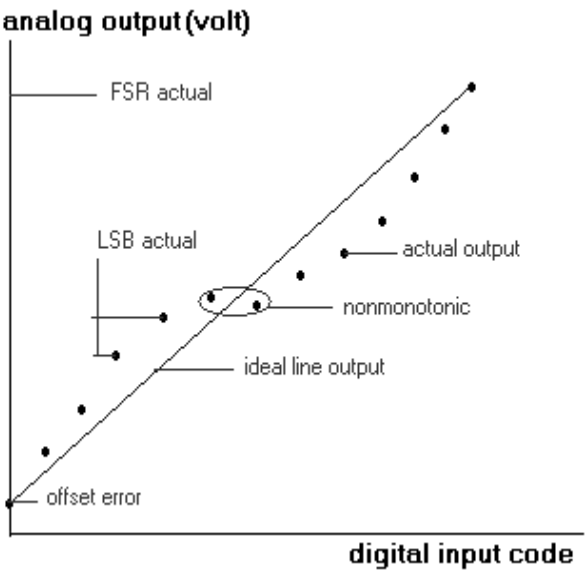

Figure 5.1 DAC offset error and gain error

The offset and gain error depend on which DAC transfer curve is used as a reference. Offset and gain errors do not degrade the performance unless some clipping happens.

5.2.3 DNL and INL

DNL (Differential Non-Linearity) shows how much two adjacent code analog values deviate from the ideal 1 LSB step. INL (Integrated Non-Linearity) shows how much the DAC transfer characteristic deviates from an ideal one. The ideal characteristic is usually a straight line; INL shows how much the actual voltage at a given code value differs from that line, in LSBs (1 LSB steps). Figure 5.2 shows the INL and DNL.

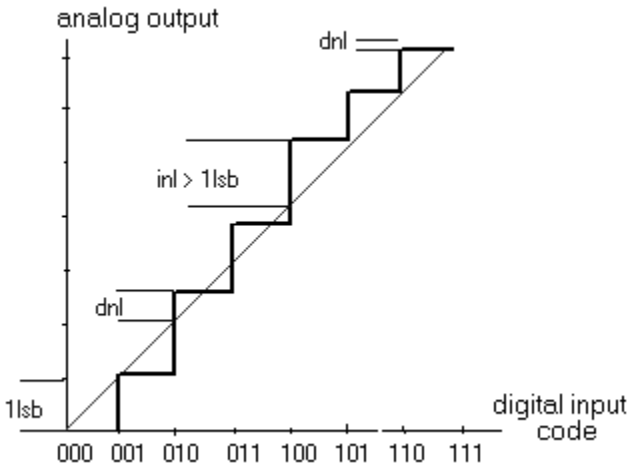

Figure 5.2 INL and DNL

Which of these two parameters is more important depends on the application. Normally the worst case DNL and INL are reported in terms of fractions of LSB. In Figure 5.1 if we observe that the different inputs are producing the same output values. They are in the same LSB/2 decision range. So this is a non-monotonic behavior. A non monotonic behavior is normally found at the MSB transitions in binary weighted DACs. Monotonicity is guaranteed if the deviation from best-fit line is less than half an LSB. This implies that DNL must be less than one LSB [7] as shown in eq(5.4):

$$\begin{aligned} \left|(INL_k)\right| &\le 0.5\,LSB,\ K=0,1,\ldots,2^N-1 \\ \left|(DNL_k)\right| &\le 1\,LSB,\ K=0,1,\ldots,2^N-1 \end{aligned} \tag{5.4}$$

5.3 Dynamic Performance

Dynamic specifications describe how the DAC responds to transitions between different output levels, and to digital switching. The dynamic errors dominate the DAC performance at higher signal levels and higher signal and clock frequencies. The common specifications are settling time, rise time and glitch energy.

5.3.1 Settling Time, Rise Time and Fall Time

The importance of settling time in a data conversion system is that certain analog operations must be performed in sequence, and one operation may be accurately settled before the next operation can be initiated. In DACs this parameter gives information about the time required by the converter to meet the right output value after a change in the input code. The settling time has many components as shown in Figure 5.3. The delay time is very small and during this interval there is no output change. During slew time, instead, the output amplifier moves at its highest possible speed towards the final value or the output capacitance gets charged. Ring time defines the region where the amplifier recovers from slewing and ceases movement within some defined error band.

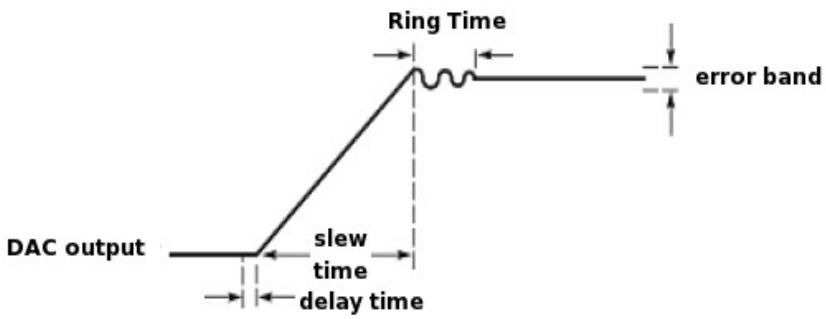

Figure 5.3 The different components of settling Time

The settling time, the rise time and fall time becomes code dependent then it can introduce distortion.

5.3.2 Glitch Energy

DAC glitch can arise from two mechanisms: capacitive coupling of digital transitions to the analog output, and effects of some switches in the DAC producing temporary spurious outputs since they operate more quickly than others. Capacitive coupling frequently produces roughly equal positive and negative spikes which more or less disappear in the longer term. The glitch produced by switch timing differences is generally unipolar, much larger, and of greater concern. The glitch area is the time integral of the analog value of the glitch transient. The maximum specified glitch area refers to a specific worst-case code change.

Finally, the glitch energy is the time integral of the electrical power of the glitch transient. The power of the glitch typically spread over the frequency range as noise. Further description on glitches with respect to Linear Interpolation is treated in a later section. Figure 5.4 shows a typical glitch in a DAC.

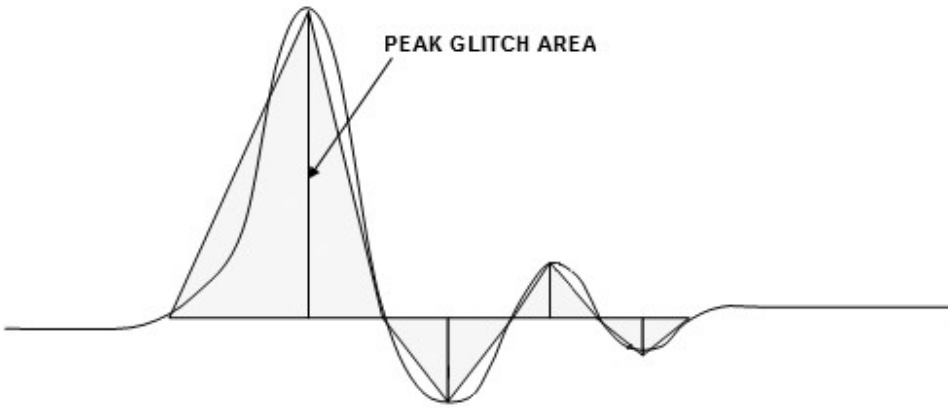

Figure 5.4 Glitch in DAC

5.4 Frequency domain performance

The DAC's frequency domain performance is often evaluated by single tone and multi-tone tests within a certain frequency band. The most common specifications are SFDR (Spurious Free Dynamic Range) which indicates in dB the ratio between the powers of the converted main signal and the greatest undesired spur. SNR (Signal to Noise) indicates ratio of the power of the fundamental and the total noise power within a certain frequency band. SNDR (Signal to Noise and Distortion Ratio) indicates in dB the ratio between the powers of the converted main signal and the sum of the noise and the generated harmonic spurs. THD (Total Harmonic Distortion) is the ratio of the total harmonic distortion power to the power of fundamental signal. Figure 5.5 shows the SFDR measurement.

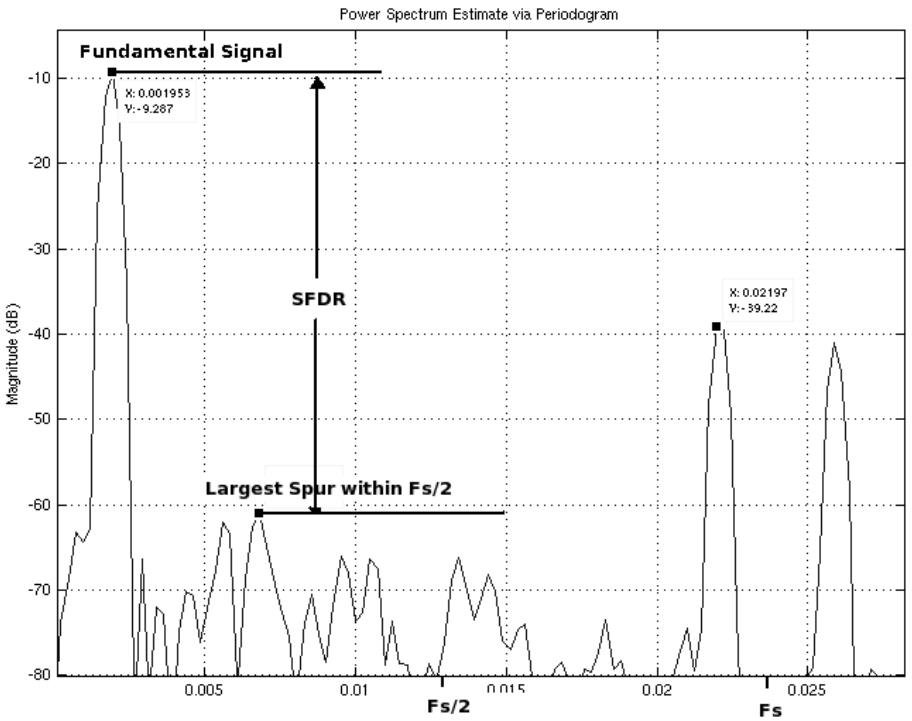

Figure 5.5 SFDR measurement

6 Linear Interpolation DAC

6.1 Introduction

As stated previously a normal DAC is a zero-order-hold converter whose frequency response is a *sinc* function. The analog filter required to remove the mirror components should be of good performance. Implementing a analog filter in a CMOS process is expensive and difficult. In this thesis, the binary-weighted linear interpolation DAC [1] using a time-interleaved structure is used. The frequency response of the presented linear interpolation DAC is approximately a square of sinc function. This causes the attenuation to be doubled for the mirror components. The analog filter is completely removed or only an off chip capacitor is sufficient to filter out the unwanted signal**.**

6.2 Principle of Linear Interpolation

The zero-order hold effect of DAC due the hold action of the DAC gives a sinc response. This sinc transfer function will add distortion to the baseband signal which cannot be neglected for wide-band application. A good reconstruction can be obtained by connecting the samples with straight lines. This is the principle behind linear interpolation. The impulse response of the linear interpolation is

$$h(t) = \begin{cases} t/T & for \quad 0 \le t < T \\ 2 - t/T & for \quad T \le t < 2\mathrm{T} \\ 0, & elsewhere \end{cases} \quad (6.1)$$

The Figure 6.1 shows the impulse response of the zero order holder and linear interpolation

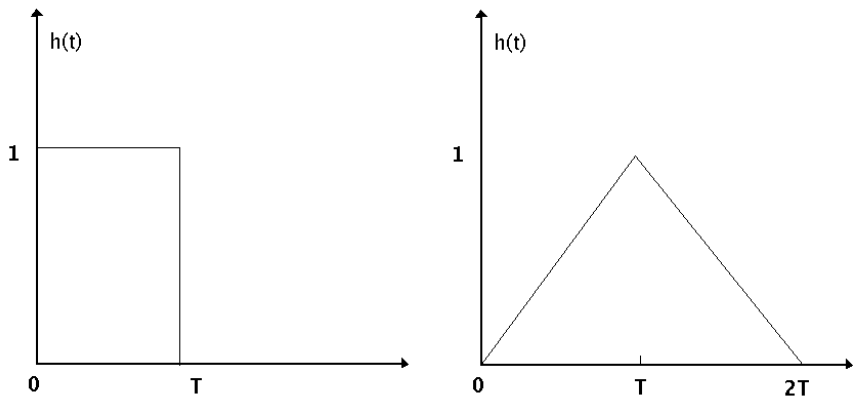

Figure 6.1 Shows impulse response of ZOH and Linear Interpolation

Figure 6.2 shows the frequency response of ZOH and Linear interpolation. The frequency response is given by eq (6.2) [1]

$$H(f) = T.e^{-j2\pi fT}[sinc(fT)]^2 \quad (6.2)$$

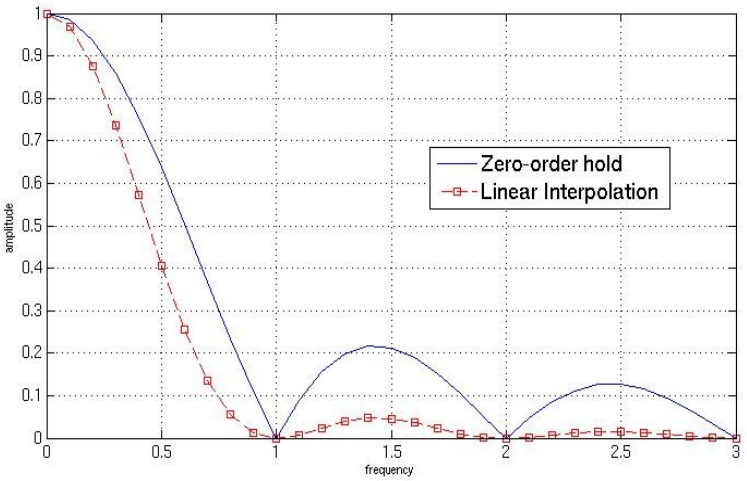

Figure 6.2 Frequency response of ZOH and Linear Interpolation function

As shown in the frequency response linear interpolation provides high attenuation to the image signals. Compared with the zero-order-hold, the attenuation in (dB) is doubled. The low pass filter can be completely removed or filter requirements become less stringent.

The realization of Linear interpolation is difficult to realize with ordinary circuit elements. A L-fold linear interpolation [1] can be used to approximate the linear interpolation. This approach achieves almost the same performance as linear interpolation and is used in this work.

6.3 L-fold linear interpolation

6.3.1 Basic Principle

The basic principle of L-fold implementation is that the clock signal is further divided by L times and the skewed clocks sequentially triggers different bits. The L-fold linear interpolation approximates the linear interpolation and achieves a frequency response close to the square function. The Figure 6.3 show the L-fold response in time domain compared with the original signal, zero-order hold and linear interpolation.

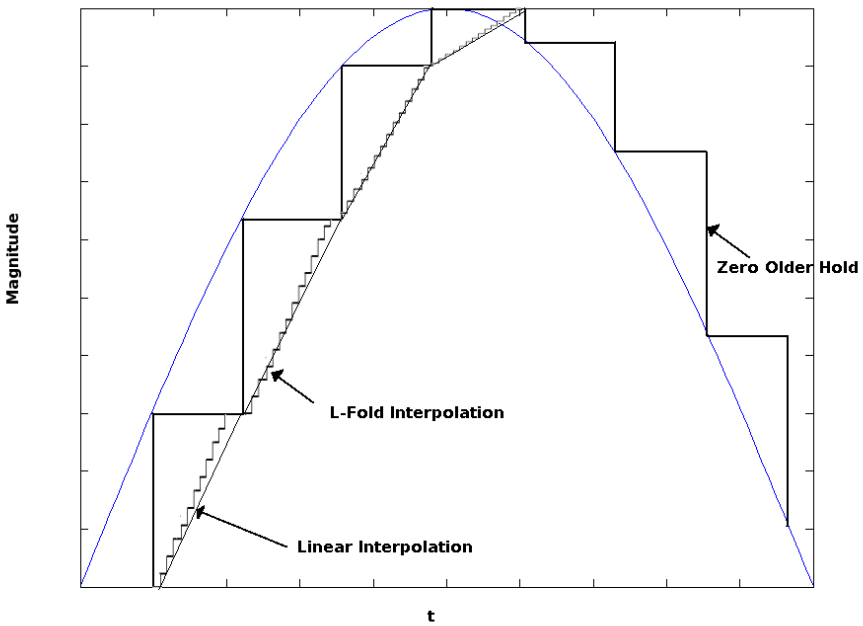

Figure 6.3 L-fold linear interpolation

In frequency domain, the L-fold linear interpolator realizes the FIR interpolation filter. DACs effective frequency is increased by Lfs. The frequency response is obtained by multiplying the FIR interpolation filter's frequency response by the frequency response of zero-order hold whose clock frequency is Lfs.

$$H(f)=L.\left|\frac{sinc(\frac{f}{fs})}{sinc(\frac{f}{Lfs})}\right|^2.sinc(\frac{f}{Lfs}) \qquad (6.3)$$

When L is large, $sinc(\frac{f}{Lfs})\approx 1$

$$H(f) \approx L.\left|sinc(\frac{f}{fs})\right|^2 \qquad (6.4)$$

This linear interpolation DAC combines the functions of linear interpolation FIR filter and the DAC.

6.4 Architecture

The L-fold linear interpolation DAC used in this thesis uses a current steering binary weighted architecture [1]. It includes a 16-tap voltage controlled delay line and a 10-bit binary-weighted DAC with a time interleaved structure. The Figure 6.4 shows the structure.

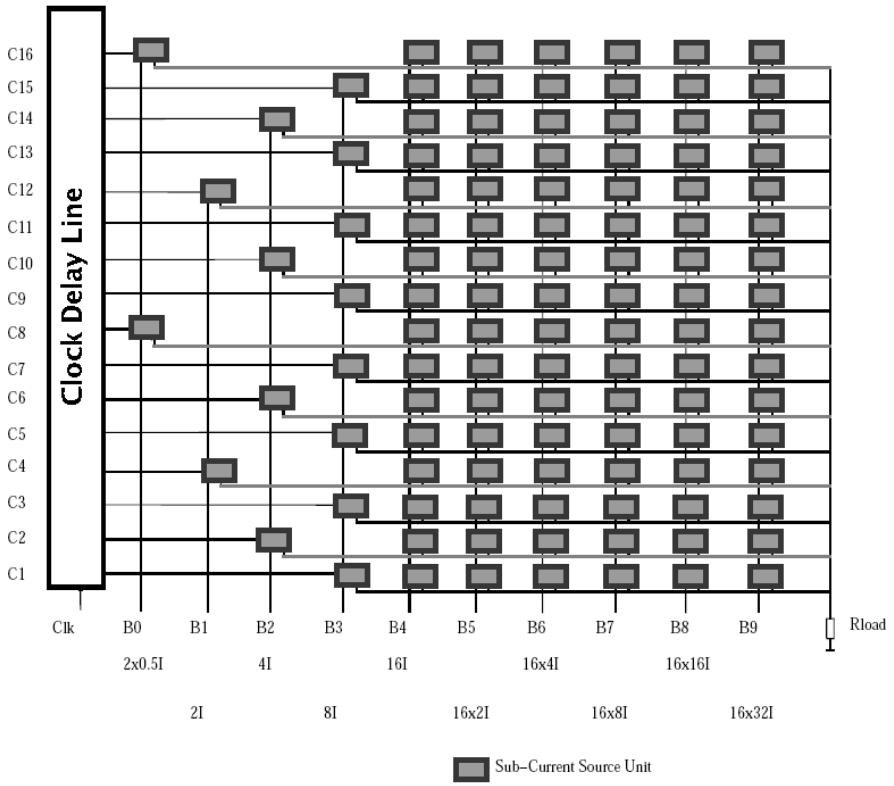

Figure 6.4 10-bit, 16 tap linear interpolation DAC

As shown in the figure the binary-weighted current source of each bit is divided into 16 identical sub-current source units. The input clock is skewed into 16 sub-clocks at equal intervals by a voltage-controlled delay line. The sub-current sources units are sequentially triggered by the sub-clocks according to the value of each bit, and the L-fold linear interpolation is realized. For example, the bit B9 which should have $2^9 = 512$ unit current sources is divided into 16 parts of 32 unit current sources. Each of the 16 part is switched on sequentially. By this way, the effective clock frequency is increased to 16 times the clock frequency.

6.5 Glitch In DACs

There are two sources of glitches namely due to capacitive coupling of signal and the sampling jitter between different bits. The later type are of major concern especially for current-steering DACs. Timing errors like this will add current spikes to the output signal. The settling behavior will also be affected in a non-linear way since the start value of the settling vary dramatically. The switching time instants of different bit depends upon the matching errors in switches, driver circuits, time skew between switching signal etc.

For example during the transition from 01 1111 1111 -> 10 0000 0000 there will be a intermediate code 11 1111 1111 present if MSB is switching faster than LSB. This will gives a full scale output for a short time and hence a large glitch. This glitch is thus a signal dependent error or distortion and degrades the dynamic performance.

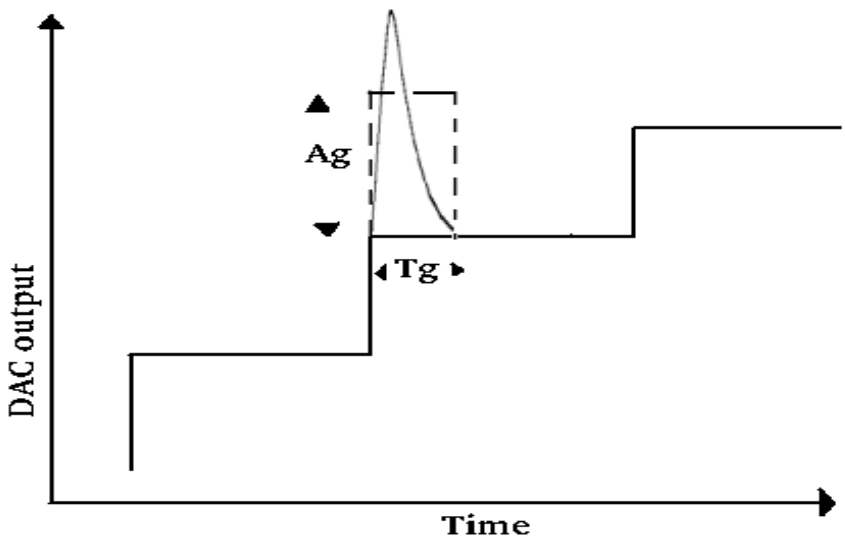

Figure 6.5 DAC output glitch

Figure 6.5 shows the glitch at the DAC output. The glitch can be modeled as a triangle wave, but in the figure it is modeled as rectangular pulse shown in dashed line to estimate the worst case behavior. This pulse has a magnitude of Ag and time duration of Tg. The glitch energy is defined as

$$E_g = A_g^2 . T_g \qquad (6.5)$$

We can characterize glitch energy by comparing to energy of the 0.5 LSB transition. This can be used to find the glitch duration and we can try to minimize the glitch so that the energy induced is not large to degrade the SNR.

As we have discussed the worst case glitch for binary DACs has got a full scale amplitude [2]. So $A_{g,max} = 2^{N-1}.\ \Delta$

$$E_{gmax} = A^2_{g,max}.\ T_g \qquad (6.6)$$

The LSB energy during one update period T_u is

$$E_{LSB} = \Delta^2\ .\ T_u \qquad (6.7)$$

For less glitch energy induction we have

$$E_{gmax} < E_{LSB}/2$$

So the upper limit on Tg is

$$Tg < \frac{Tu}{2^{(2N-1)}} \qquad (6.8)$$

In this thesis an update frequency of 24 MHz is used and N = 10 , Tg = 8 *fs* which is hard to achieve. Normally the glitches from simulations are in picoseconds range. So specific de-glitching circuits are required. But in Linear Interpolation DACs this is not needed as we discuss below.

6.5.1 Glitch Reduction In Linear Interpolation DACS

Let us see how the glitch can be reduced in L-fold DACs. The Figure 6.6 shows a part of the 10-bit L-fold structure. Let us consider for simplicity that it is a 4-bit DAC. Let us see what happens during the following transition

0111 -> 1000

As we can see from Figure 6.6 the total current for 0111 is 7 LSB and when it is 1000 it should be 8 LSB. For a normal DAC a glitch with value 1111 can happen. But in the case of L-fold DAC when the C1 is active 1.LSB of B3 turns on giving a net increase in 1LSB to total DAC current. When C2 becomes active 1 LSB of B2 is reduced from total current. So now the net change is zero. If we analyze further we see that a net increase is 0.5.LSB when c8 becomes active since b0 are half LSB cells. Then C16 is active the LSB increase of 1 LSB is completed. So we can see that the maximum change during the transition from 0111 -> 1000 is only 1.LSB against a full scale for the normal DAC. In this way the glitch is reduced wonderfully. This is shown in the pictorially in Figure 6.7.

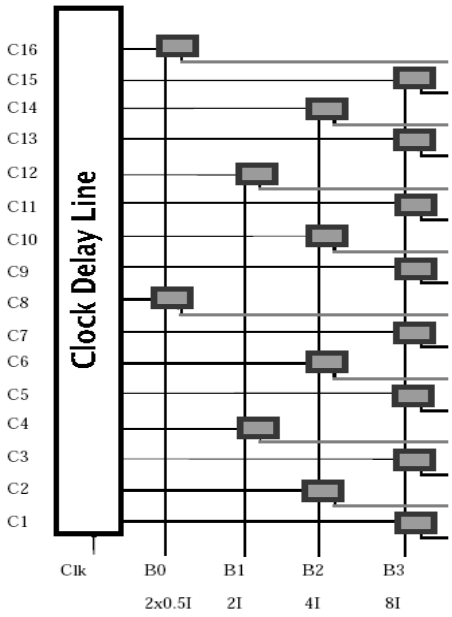

Figure 6.6 A section of the L-fold Linear Interpolation Structure

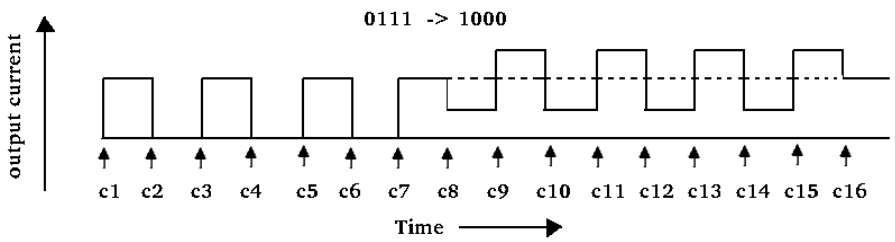

Figure 6.7 Output current activity during the transition from 0111 -> 1000

6.6 Current Source Cell

The sub current source unit has different number of unit current sources as shown in below Figure 6.8. The number of unit current sources depends upon the position of bit. For binary weighting, bit B9, B8, B7, B6, B5, B4, B3, B2, B1, B0 has 32, 16, 8, 4, 2, 1, 1, 1, 1 unit current sources respectively. Bit B0 use two half current source cells for making the layout symmetrical.

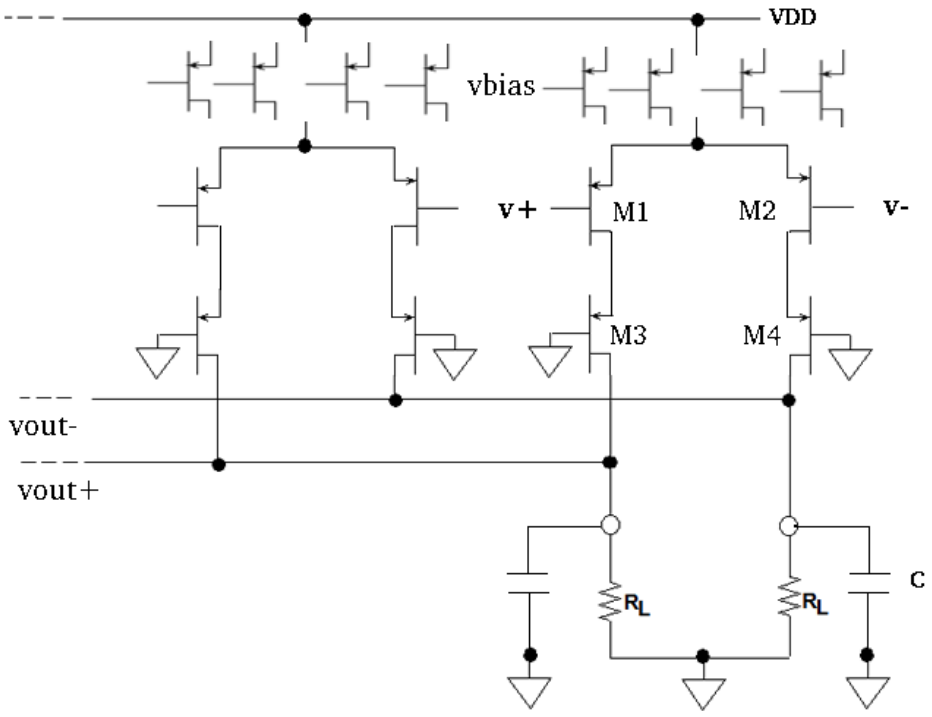

Figure 6.8 Current source with switches and isolation transistors

The Figure 6.8 shows the PMOS current sources, the switching transistors and isolation transistors. In order to reduce the coupling from the clock signal to the output through the parasitic capacitance of the switch transistors, isolation transistors are used [6]. The current source is switched to either of the differential outputs depend upon value of each bit. The V_{bias} can be used to adjust the DAC output of each unit current source cell. The v+ and v- is derived from a differential driving stage. In order to speed up the settling and minimize the the voltage fluctuation differential current switches are used not to be turned off simultaneously.

6.7 Unit Current Source

The unit current source can be designed with PMOS, NMOS or cascode connection. Usually when high linearity performance is required a cascode structure is used to implement the DAC current sources. In this case the low supply voltage of 1.2 V does not allow the use of this structure else the transistors would not be working in the saturation region. The distortion effect due to the finite output impedance of the sources is reduced by using different switch sizes for different bits. PMOS current sources are used since it gives a lower 1/f noise due to lower mobility of holes but the thermal noise is high. 1/f noise dominates at low frequencies and additonal switching-circuits are necessary to reduce it[7].

The output voltage swing requirement is 100mV with a 1 KΩ termination resistance. Therefore the FS current is 100 uA and for a 10-bit DAC, the LSB current I_u is

$$I_u = \frac{100 * 10^{-6}}{2^{10} - 1} = 97.75\, nA \quad (6.9)$$

For high output impedance the transistor should operate in saturation region hence unit current is

$$I_u = \frac{\mu C_{ox}}{2} . \frac{W}{L} . Veff^2 \quad (6.10)$$

where μ is the mobility, Cox is the capacitance per gate area, W/L the transistor size aspect ratio and V_{eff} is the effective gate voltage.

For choosing the length and width we have to take many things into considerations. In next section we find out the minimum area required for the unit current source taking matching errors into account. Once this is done we have the choice of selecting both width and length to be equal. But the channel length is normally kept larger since the output impedance of the current source is

$$R_{out} = \frac{1}{\lambda . I_u} \quad (6.11)$$

$$\lambda \approx 1/L$$

So the output impedence is proportional to L and also long channel reduces the channel length modulation. Normally W is chosen smaller than L since the poles of the system depends upon the gate drain overlap capacitance of the current sources which is proportional to W [2].

6.8 Matching And Transistor Sizing

When we start with design of a DAC, the first question in our mind will be how much size we can use for the current source transistor. The natural choice is to start with minimum size. But the matching errors during fabrication force us to start with much larger size than the natural choice since the performance of the DAC strongly depends upon the matching of the current sources. Distance mismatch is mainly influenced by systematical effects, like gradients over chip lengths or across a wafer due to process features. Once this size is fixed, smart layout techniques should adopted to further reduce the matching errors. This section gives a description of how to choose the minimum area of transistors .

6.8.3 Selection Of Proper Transistor Size

As technology goes into deeper submicron we will have a feeling that the size of the unit current source can be reduced to a great extend to reduce the net area of the DAC, but this is not correct. In fact new technologies reduce the size of the digital circuits and hence the power consumption due to low supply voltages and less parasitic capacitance. But analog circuits do not have much benefits from scaling of technolgoy. Certainly the matching properties will improve as we go into submicron technologies.

With the use of Monte Carlo Simulations we can obtain the allowed mismatch between the current source transistors so as to achieve an expected error smaller than 0.5*LSB. The Figure 6.9 shows the the relation between allowed deviation of the LSB current and the INL error for a 10-bit DAC.

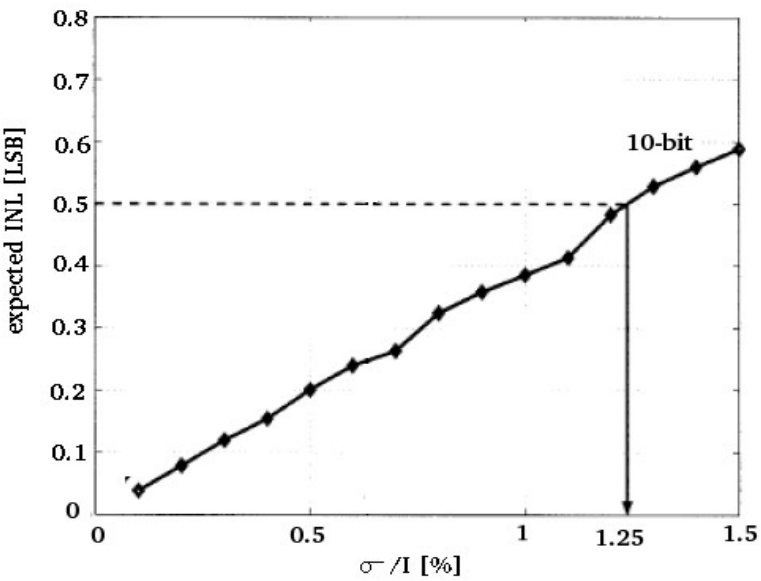

Figure 6.9 Allowed deviation of LSB current against expected INL [5]

From Figure 6.9 we can see that for a 10-bit D/A converter for getting an INL error less than 0.5 LSB , the allowable $\frac{\sigma}{I}$ is 1.25 %. Now Pelgrom equations eq(6.7) can be used to calculate the minimum size of transistors :

$$2 * \left(\frac{\sigma}{I}\right)^2 = \frac{A_\beta^2}{WL} + \frac{4A_{vt}^2}{WL(V_{GS} - V_t)^2}$$
$$WL = \frac{1}{2\left(\frac{\sigma}{I}\right)^2}\left[A_\beta^2 + \frac{4A_{vt}^2}{(V_{GS} - V_t)^2}\right] \quad (6.12)$$

where A_β, A_{vt} are technology parameters.

For he current-steering DAC, performance is based on matched current sources. Matching is also proportional to the process parameters A_{vt} and A_β . A_β remains almost constant as technology scales down while A_{vt} scales down. But since power supply also scales down the over drive voltage $V_{GS} - V_t$ scales down. So there is not much decrease in minimum area.

In this thesis we use a 1.2V, 130nm CMOS technology. For this we have A_β, A_{vt} as 2 % µm and 4 mVµm respectively. Since the LSB current is about 100nA and supply voltage is 1.2V, the overdrive voltage is nearly 80mV with V_t of 250mV. We get the value of WL_{unit} = 33 µm^2. So we choose a transistor size of W=3 µm and L=10 µm. Special layout techniques are needed to achieve the desired performance. Later section describes the layout techniques used.

6.9 Digital Switching

During switching phase a significant voltage variation will occur at the drain of the PMOS current source causing it go out of saturation region. This can cause the unit current to change and cause glitch related distortion. Differential switching is used to avoid large voltage fluctuations at the drain during switching. The current source is always on, supplying current to one of the two differential outputs. Thus in order to speed up settling and minimize voltage fluctuations at the drain of the current sources, the differential current switches are designed not to turn off simultaneously. The Figure 6.10 shows the required gate voltage non-overlapping waveforms for the differential switches of PMOS type.

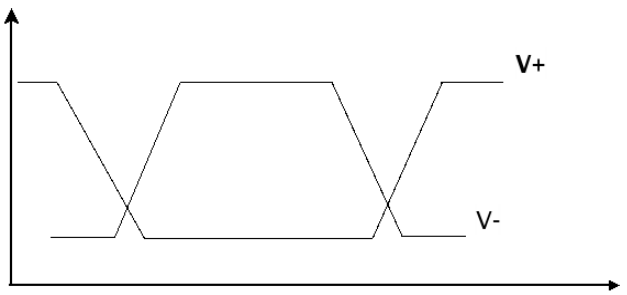

Figure 6.10 Switch signal for differential switches

6.10 Clock Feed Through And Isolation Transistors

Minimum size transistors are used for the switches to reduce clock feed through reduced gate capacitance. The width of switching transistors are increased for bit 8 and bit 9 for to reduce drop at the drain of the PMOS current source through reduced resistance. This improved the performance of DAC significantly. Different techniques were tried to reduce the clock feed through. Transmission gates and dummy transistor techniques can be used to reduce the clock feed through. But these were not implemented since it increased the wiring and additional clock signal requirements.

The voltage variation at the DAC output due to the clock feed through is

$$\Delta V = \frac{nC_{gd}}{(C_L + C_{dtotal}).} \Delta V_g \qquad (6.13)$$

where ΔVg is the control voltage swing, C_{dtotal} is the total parasitic drain capacitance of the switching transistor and nCgd is the total gate-drain capacitance of n switching transistors at the output of the DAC. When n is very large as for the 10-bit case the glitch at the DAC output will be very large. ΔVg can be reduced by reducing the voltage swing of control swings. But the circuits which implements this reduced swing controls are not optimal in turns of power or complexity [8]. In this thesis cascaded [6] transistors are used with same dimension as that of the switching transistors to reduce the glitches to the output. For a 1-to-0 transition of the control signal, when the PMOS switching transistor forms the conducting channel, the cascaded transistor are off so the output node is isolated and coupling is avoided. When the switching transistors are turning off some coupling exists at the beginning, but since the switching transistor cuts off very rapidly the voltage at the source of the cascade transistor drops, turning it off, and isolating the output node for the remaining of the transition of the control signals. The remaining glitch energy was small and the off chip capacitance effectively removed these glitches.

6.11 Driving Stage

The non-overlapping waveforms are generated by a driving stage as shown in Figure 6.11. Each unit source current cell shown in Figure 6.4 has a driving stage. Each driving stage is a falling edge triggered flip-flop, formed by a D-latch and a clocked SR flip-flop.

6.11.1 RS flip flop

The dimensions of the SR flip-flop are properly selected to generate the non-overlapping signals for PMOS switches. Q and Qbar are the outputs of D latch. The clk signal is one of the 16 clocks generated by the voltage controlled clock delay circuit and D is the one of 10 inputs of the DAC. The D latch and RS flip flop makes it sure that its active for one clock cycle after it is triggered.

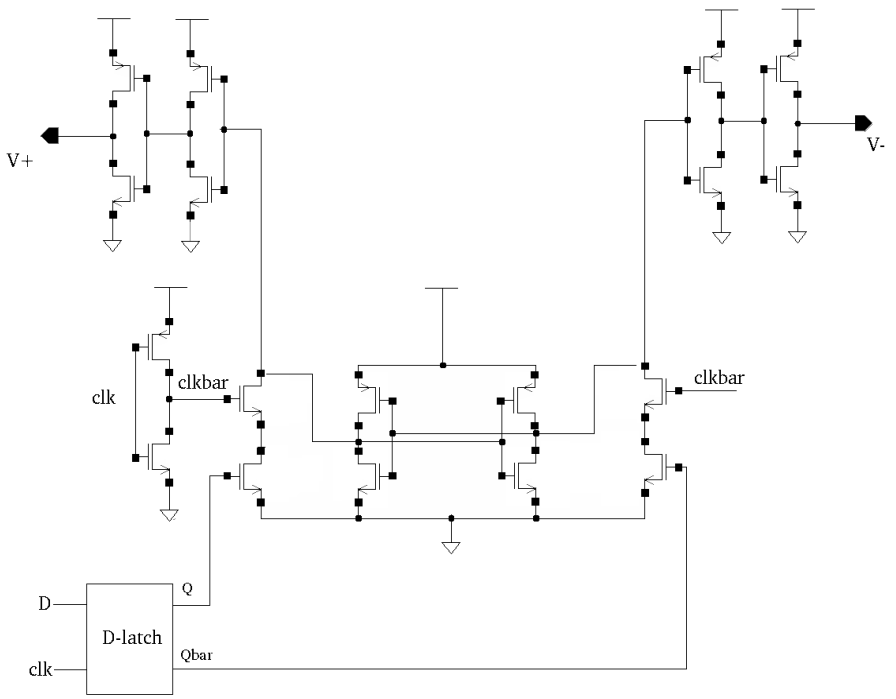

Figure 6.11 Driving Stage

6.11.2 D - Latch

The Figure 6.12 shows the NAND gate implementation and Figure 6.13 shows the CMOS implementation of the same.

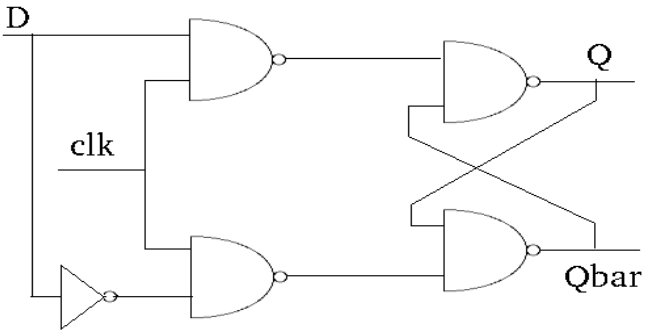

Figure 6.12 D- Latch

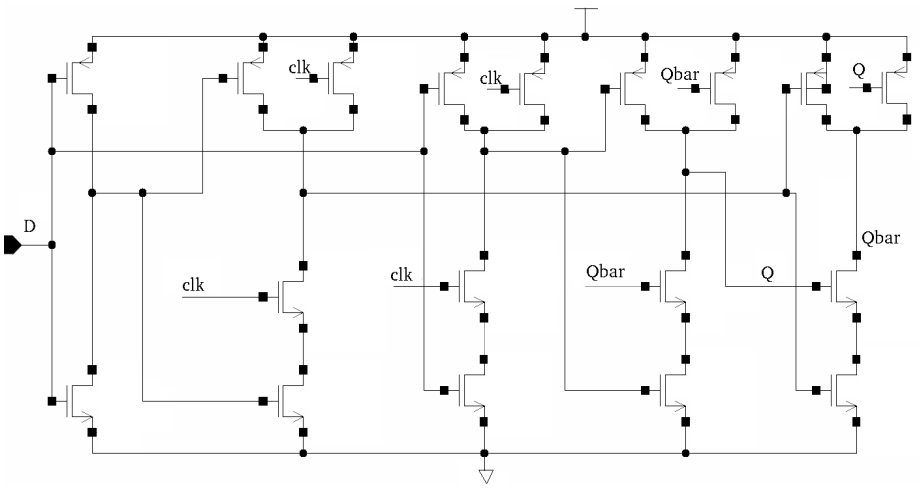

Figure 6.13 D-Latch CMOS implementation

6.12 Voltage controlled delay

The Figure 6.14 shows the block diagram of the voltage controlled delay line. The output from this is fed to the driving stage along with data bits. The V_{ctrl} signal ensures that the clock frequency can be adjusted. The Unit Delay block is implemented by a current starved inverter as shown in the below Figure 6.15.

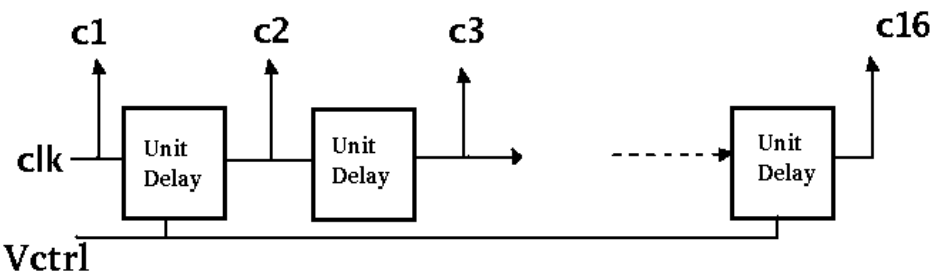

Figure 6.14 Delay Line

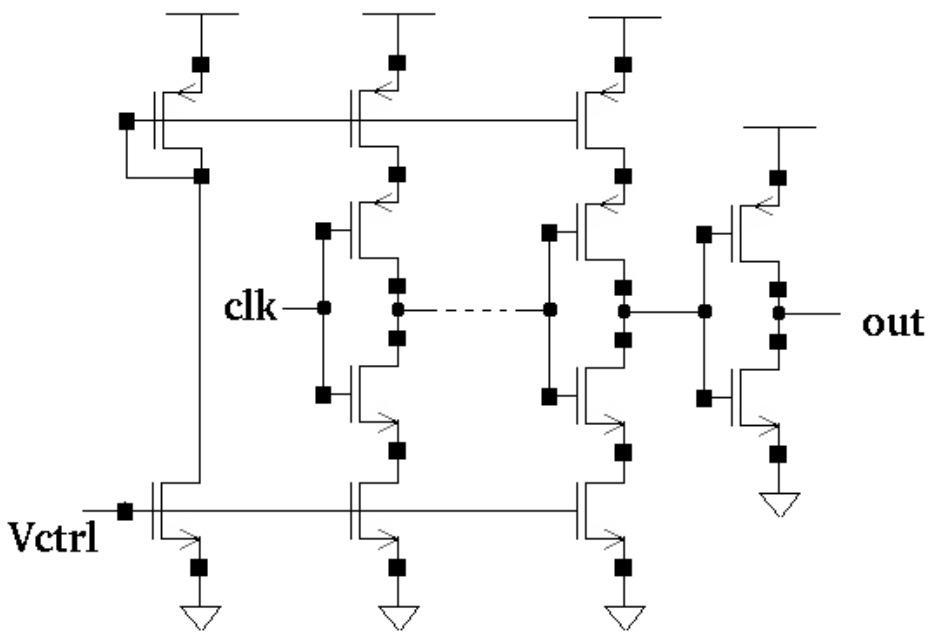

Figure 6.15 Current Starved Inverter

6.13 Digital Control of Biasing

A six bit control is provided for the DAC to control the biasing of the current sources. This controls the current and thus output amplitude. This is provided since the receiver and transmitted amplitude are different for the transceiver. Figure 6.16 shows the circuit implemented.

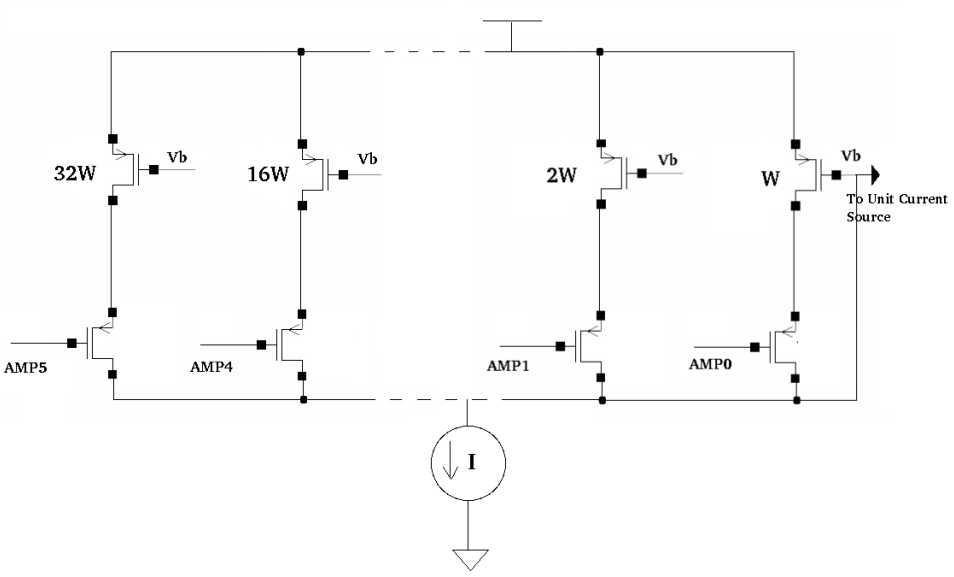

Figure 6.16 Current Starved Inverter

The lower PMOS transistors work as switches. All switches are of minimum size. The upper PMOS act as current sources that are switched on and off by controlling the switches. The DDS sends the digital signals AMP0 ... AMP5, which are in binary format. So the sizes of the current sources are also increased from AMP0, ... AMP5 in a binary way. The magnitude of the digital signal will be different for transmission and reception.

7 Layout

7.1 Introduction

The layout is of utmost importance in order to achieve the best static and dynamic performances for DACs. Therefore, some implementation details are pertinent. In this chapter some of the factors that affect the analog circuit in a mixed signal circuit at the layout level is discussed. This chapter also describes some of good layout practices and layout rules used in this thesis.

7.2 Substrate Noise

Mixed signal circuits have both digital and analog circuits on same substrate so all the digital noises injected into substrate are received by the analog part and the performance is affected since analog design performances are sensitive to electrical disturbance [7,9,10]. Disturbance in the substrate should be minimized as much as possible. There are three main sources that disturbs the substrate namely inductive noise, capacitive noise and noise due to minority carriers**.**

7.2.1 Inductive Noises (L di /dt)

Inductive Noises are created through bonding wires that create a large di/dt on power supplies and non-ideal power supplies connecting directly to the substrate. Figure 7.1 shows the inductive noise injection through bond wire.

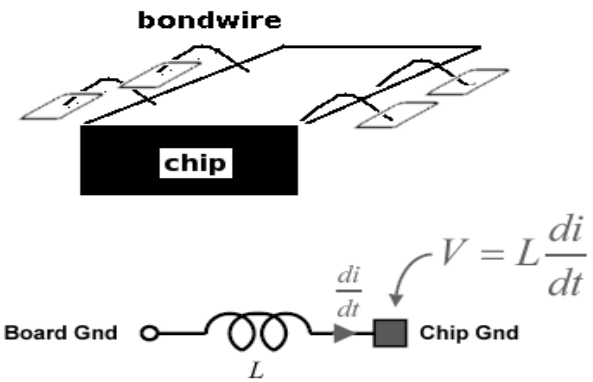

Figure 7.1 Bond Wire and Inductive Injection

Inductive noise can reduced by choosing a better package and regulated power supplies.

7.2.2 Capacitive Coupling (dv/dt)

Capacitive coupling is caused due to interconnect capacitance to substrate and junction capacitances in the substrate as shown in the Figure 7.2.

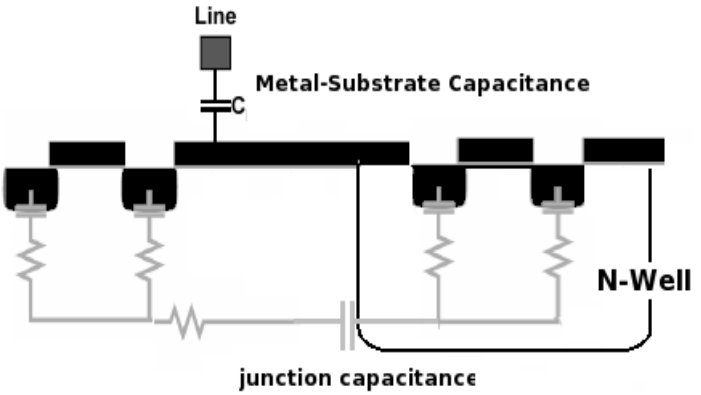

Figure 7.2 A parasitics capacitances in the chip which causes substrate noise

Capacitance coupling can be avoided by shielding of the analog signal from digital part with a ground signal. Analog ground should be used for shielding since digital ground contains much activity from the switching of digital circuits. Switching of large capacitive nodes should be avoided. The guard rings are effective mechanism to avoid coupling as shown in a later section. Digital high switching pins should be kept far away from analog outputs, inputs and bias signal. Slow rise, fall times and lower voltage swing of digital signal also reduces noise coupling.

7.2.3 Injection Of Minority Carriers

Normally for NMOS substrate is connected to the least potential and PMOS N-well is connected to the highest potential. Some times the source potential or the drain potential of NMOS comes down below the substrate potential and the source potential or the drain potential of PMOS goes above the N-well potential. This may be due to an inductive ground path that causes the ground in the substrate to bounce or resistive power and ground path from the power pins to the substrate and the N-well or due fast switching signal with significant overshoot.

7.3 Guard Rings

To reduce disturbances through the substrate, we can use a guard ring which is a metal substrate contact. This is effective for low-ohmic substrates and different techniques have to be used for high-ohmic substrates. For low-ohmic substrates the noise tends to spread in a horizontal direction and guard rings are effective. For high-ohmic substrate the noise spread in the vertical direction to bottom end of substrate and spread to other part of substrate from there [2]. For high-ohmic substrate there should be a separate quiet supply for the substrate.

A guard ring can be used in the following way. Surround NMOS in the p-substrate with N-well guard ring. Tie the N-well guard ring to VDD. The N-diffusions from the NMOS could inject stray electrons into the substrate. These stray electrons could be collected efficiently by the N-well guard ring that is biased to VDD to attract the electrons. Surround the PMOS in the N-well with a P-diffusion guard ring. Tie the P-diffusion guard ring to ground. P-diffusions from the PMOS inject stray holes into the N-well. These stray holes could be collected efficiently by the P-diffusion guard ring that is biased to ground to attract the holes. For the guard rings to be effective, the resistance in the path from the straying minority carrier to the guard ring and then to the voltage source must be kept as low as possible. Hence, the minority carrier noise guard rings are made wider so as to decrease its resistance. Ideally, the guard rings should be placed as closely to the likely noise sources as possible. The guard rings are also placed around the critical transistors to minimize stray electrons and stray holes from affecting the critical transistors. We can use a guard ring around the digital circuit and analog circuit as shown in Figure 7.3 to give more protection.

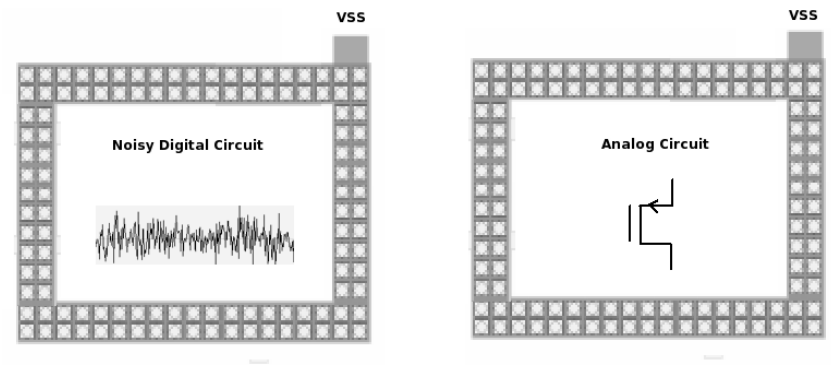

Figure 7.3 Guard Rings

7.4 Major layout rules techniques used

Some of the layout techniques used are mentioned below

- A symmetry is maintained for better matching.
- The current sources are put very close to each other and are arranged as a matrix.
- Dummy current sources are arranged around the current sources.
- The matrix is kept in a big N-well and guard rings are used between current source and digital part to prevent the noise coupling via the substrate.
- The current sources for various bits are spread over the matrix for better matching.
- The current sources for different bits are arranged in a common centroid way.
- The supply and ground lines for analog part and digital parts are different.
- Minimum wire length for the clock is used to avoid skew and also prevent less noise injection into the digital part.
- Ground lines are put in between places where analog and digital signals cross each other in different metal layers.
- Symmetry is maintained at different levels as shown in floor plan figures.
- Decoupling capacitors, which act as batteries, are provided for supply lines.
- Decoupling capacitors are provided for the V_{ctrl} signal of the voltage controlled delay.
- For Digital circuits cell rows are mirrored for a compact layout.

7.5 Layout floor plan

The entire floor plan of the DAC is shown in Figure 7.4**.**

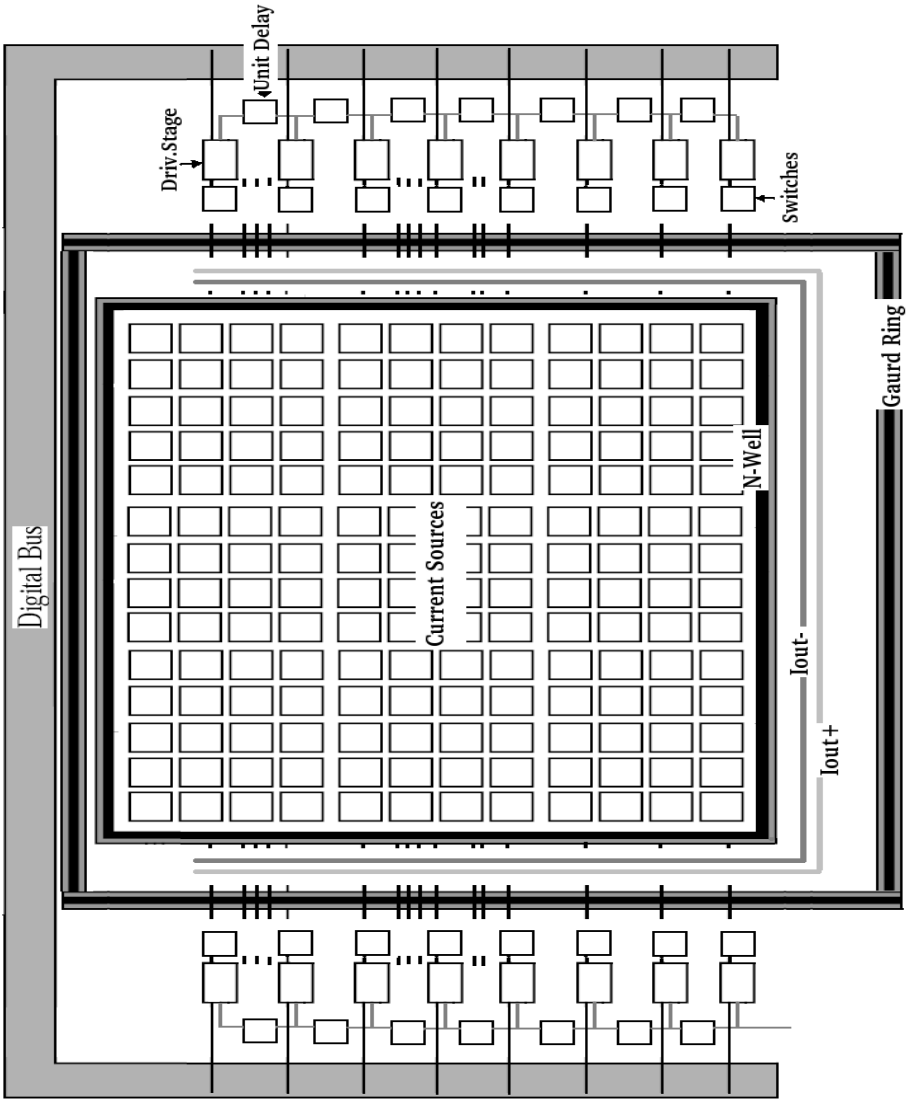

Figure 7.4 Floor Plan of the DAC

At the middle of the layout lies the current source array. This is put in a N-well and surrounded by a guard ring connected to ground. The digital signals are kept away from analog signal as far as possible. The analog signals are shielded where ever they cross the digital signals.

7.6 Current Source Array

The Figure 7.5 shows the arrangement of the current sources. A common centroid approach is followed here, with center occupied by current sources which are trigerred by the bits b0, b9. There are 64 rows and 16 columns altogether amounting to 1024 transistors. The center grayed ones are the 4 transistors for the b0 and b1 bits. The dark ones are the current sources associated with the b9 bit. Since b9 has $2^9 = 512$ unit sources it occupies half the area of the total matrix. The whole array is divided into 4 quadrants for clarity and as we can see one of the quadrant is completely filled with bit b9 source arrays. The other quadrants are filled like stair cases. Each stair case has transistor for bit 9 associated with a particular clock phase of the 16 skewed clock signal. For example the first stair case has b9 transistor sources associated with clock c1 and next stair case has b9 current sources associated with clock c2. All the bits starting from b8 to b2 are spread in a similar manner.

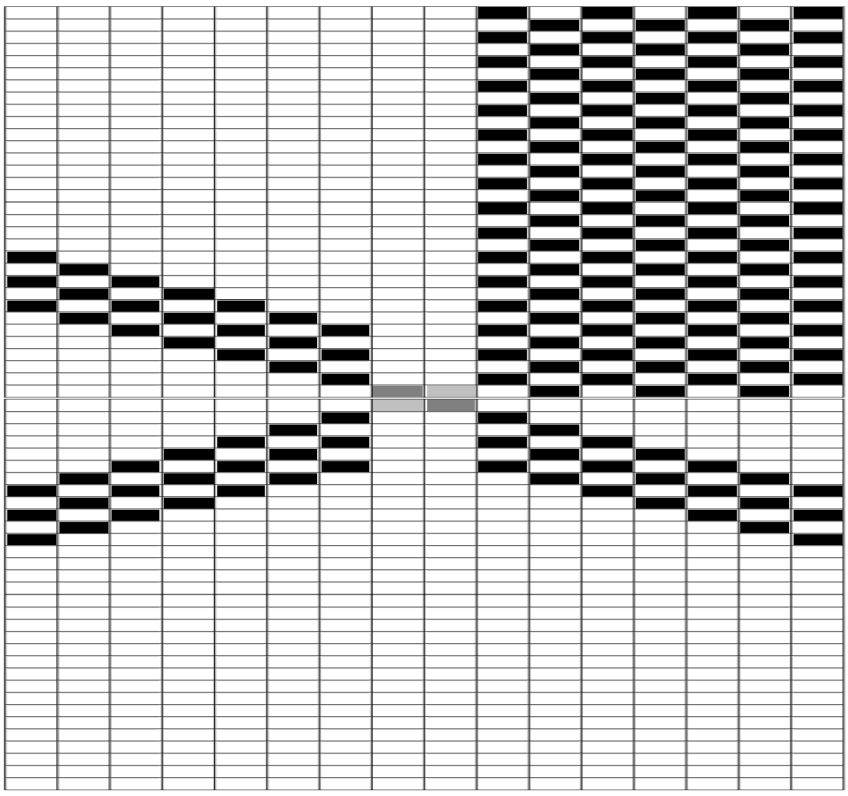

Figure 7.5 The positions of bit b9 in the transistor array

7.7 Layout

This section shows some of the layout figures used in this work. Figure 7.6 shows a single unit delay at the bottom and buffers at the top.

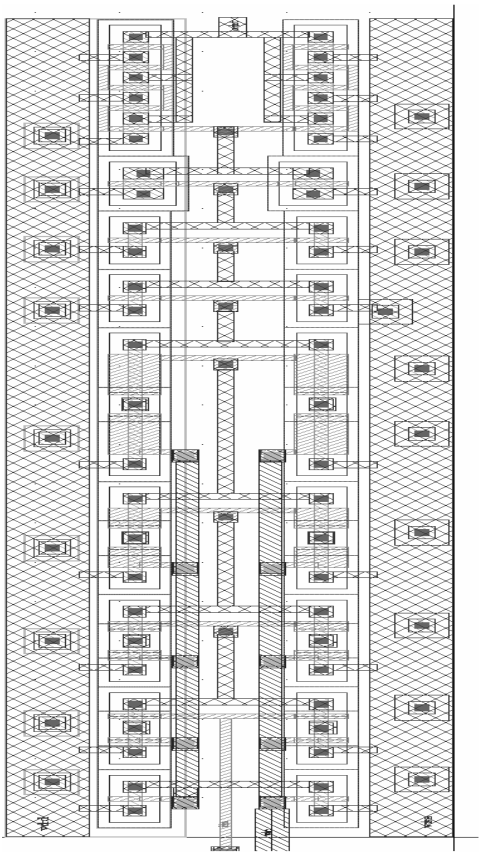

Figure 7.6 Layout of Unit Delays and Buffers

The Figure 7.7 shows the compact layout of isolation transistors at the top and bottom and switches in the middle.

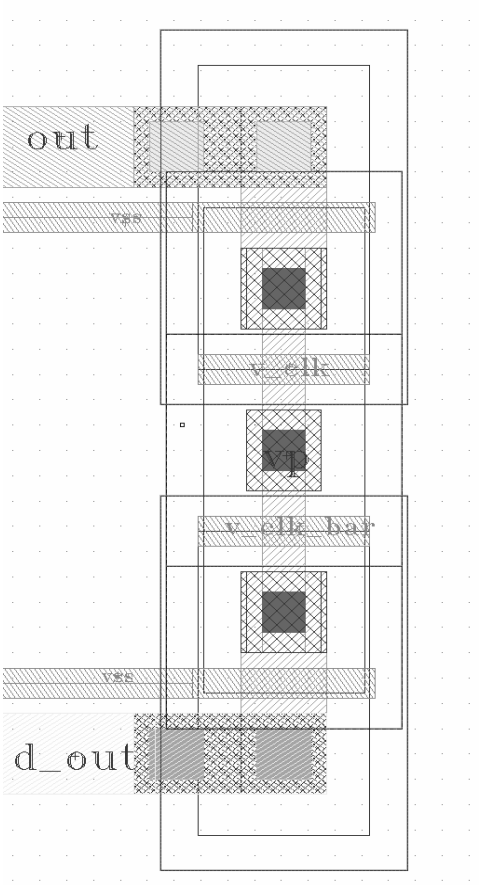

Figure 7.7 Switches and Isolation Transistors

Figure 7.8 shows the driving stage. It has the D latch at the bottom and the RS-flip-flop at the top.

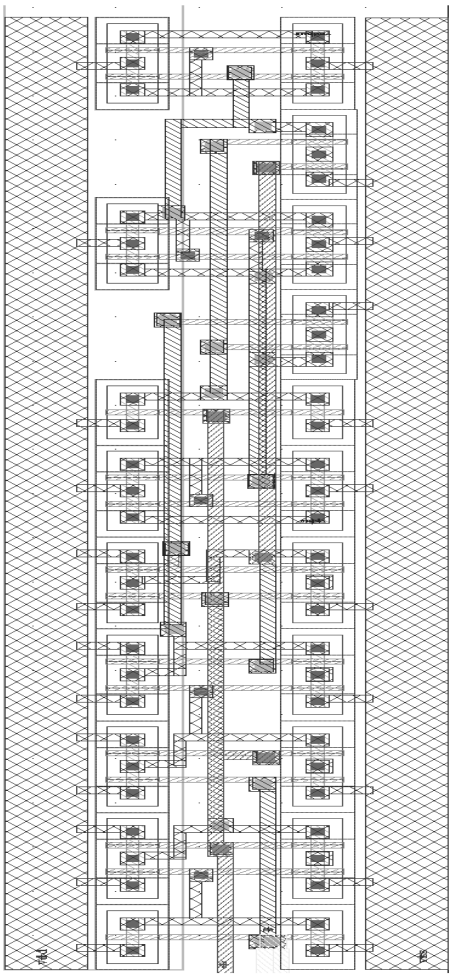

Figure 7.8 Driving Stage Layout

Figure 7.9 shows the whole FSK chip with the DDS and the two DACs. The DDS is kept far away from the DACs to reduce the noise injection.

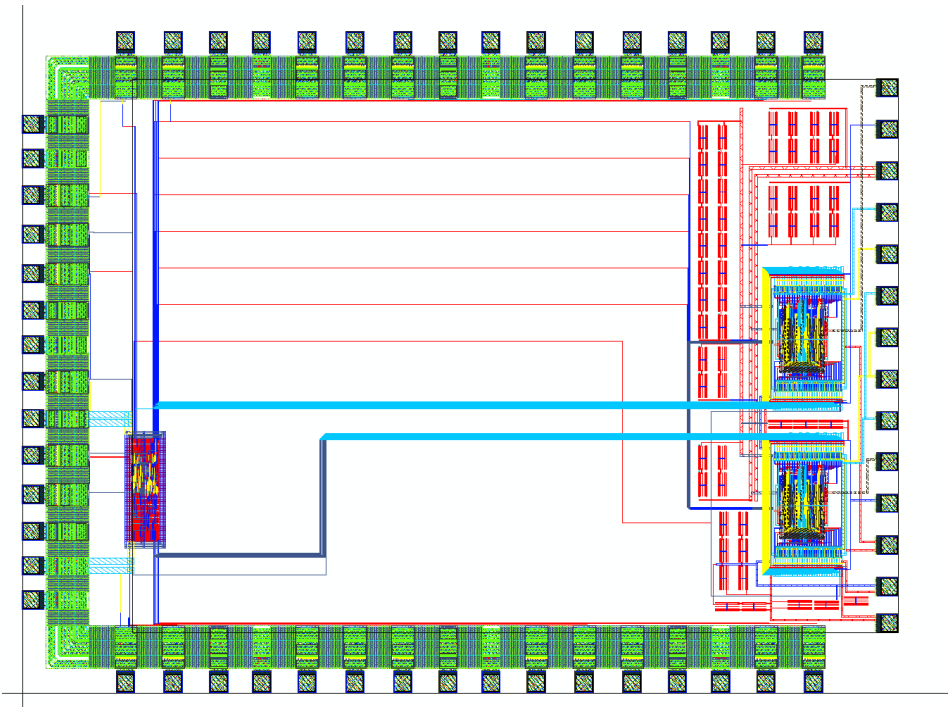

Figure 7.9 The FSK chip layout

The layout of the DDS part is done by automatic place and route tool Cadence Encounter. The layout of the DAC section including the pads are manually done.

8 Results and Conclusions

8.1 Introduction

This chapter describes the simulation results and conclusion. For comparing with normal DAC performance, a 10-bit normal DAC is also constructed and stimulated. The spectrum of this DAC is compared with the L-fold linear interpolation DAC.

8.2 Spectrum of 10-bit Normal DAC

To compare the frequency domain performance of 10-bit normal DAC and L-fold linear interpolation DAC , the normal DAC was constructed and simulated. The Figure 8.1 shows the spectrum of the normal 10-bit DAC.

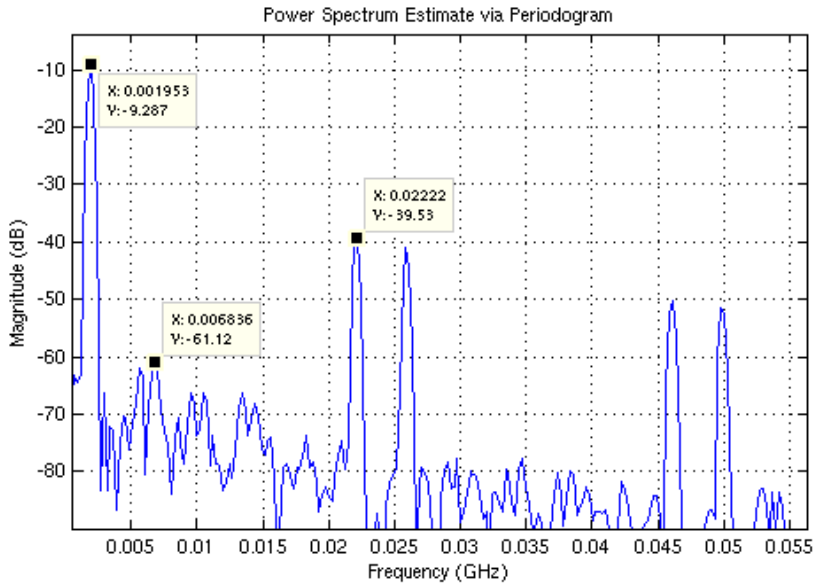

Figure 8.1 Spectrum of 10-bit normal binary weighted DAC

The SFDR is 52 dBFS and attenuation of the mirror component is 30 dBFS. The low value of SFDR is mainly due to the code transition glitches associated with binary DACs. The mirror component attenuation can be compared with that in Figure 8.2.

8.3 Spectrum of 10-bit L-fold DAC

The Figure 8.2 shows the spectrum of the L-fold 10-bit DAC.

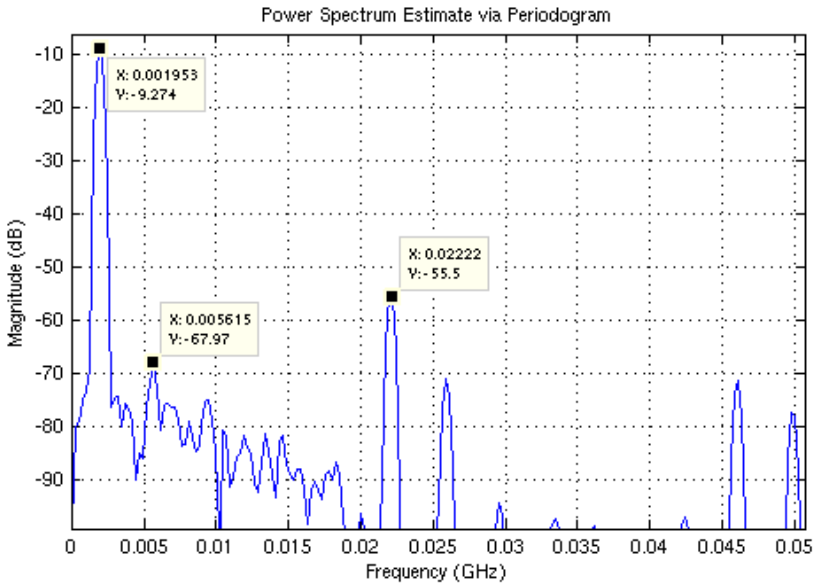

Figure 8.2 Spectrum of L-fold DAC

The SFDR is 58.5 dBFS and attenuation of the mirror component is 46.3 dBFS. The results shows that the SFDR and attenuation has improved compared to normal 10-bit binary weighted DAC.

8.4 INL of 10-bit L-fold DAC

Figure 8.3 shows the INL of the 10-bit DAC. The INL of the 10-bit DAC is 0.05 LSB.

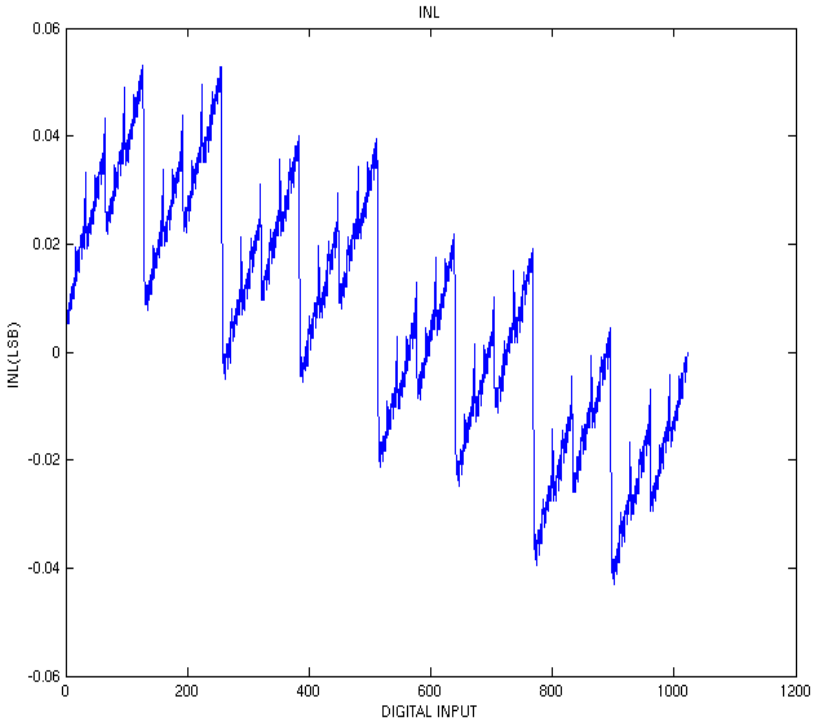

Figure 8.3 INL of L-fold DAC

The INL satisfies the condition for monotonicity.

8.5 DNL of 10-bit L-fold DAC

Figure 8.4 shows the DNL of L-fold DAC. The DNL is 0.04 LSB.

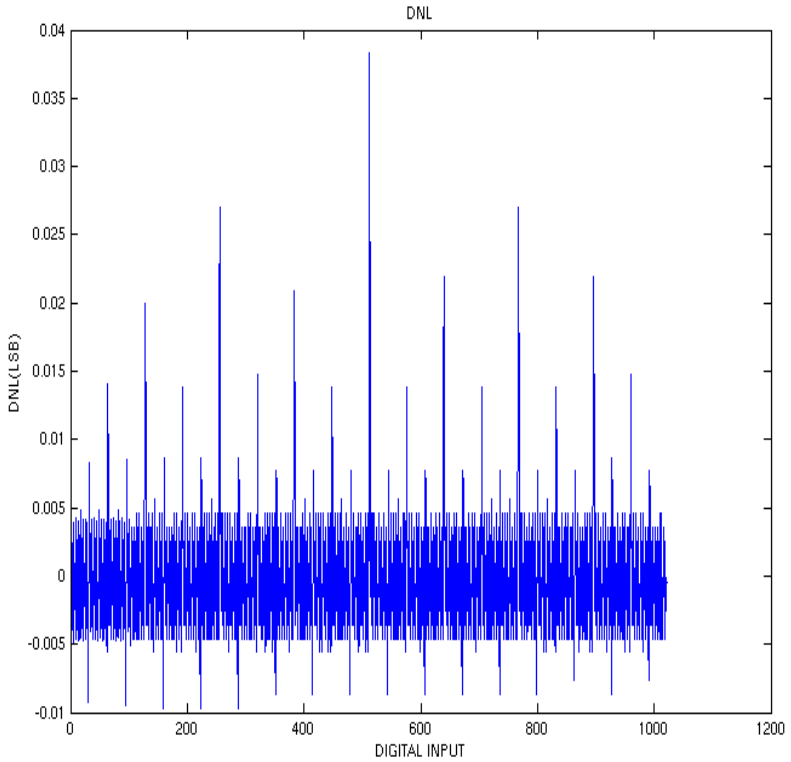

Figure 8.4 DNL of L-fold DAC

The DNL satisfies the condition for monotonicity.

8.2 Performance of 10-bit L-fold DAC

Table 5 shows the performance summary of the L-fold DAC

Table 5. Performance Summary

Resolution	10 Bit
Update	24 MHz
INL	+/- 0.05 LSB
DNL	0.04 LSB
Power @ 1.2 V	350 uW
SFDR	58.5 dB
Attenuation of Mirror component	46.3 dB

8.3 Conclusions

Different DAC architectures were studied. A 10-bit CMOS linear interpolation DAC has been designed and tested. The DAC has been implemented in a 1.2V, UMC 130 nm CMOS process. It uses linear interpolation technique to increase the attenuation of the image signal and reduce the glitch. The measured attenuation of image components presents a good agreement with the theory. The requirement for the LPF can be greatly relaxed, which is significant for system on chip design. The DAC is integrated with DDS and the FSK is implemented.

Common centroid approach was used for doing the layout to reduce matching errors. The chip is to be mounted in a 68 pin JLCC package. The power consumption of DAC is 350 uW. From the study of L-fold DAC it can be concluded that linear interpolation can reduce the glitches of binary weighted DACs and increase the attenuation of the image signals. Linear Interpolation can also simplify the design of the reconstruction filter and the DAC can be integrated with other circuits easily.

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