MASTER EQUATION BASED NUMERICAL SIMULATION USING MATLAB

INTRODUCTION TO NANOSCIENCE AND NANOTECHNOLOGY

ECE1006

FACULTY-PROF. SAKTHI SWARRUP J

GROUP MEMBERS:

RAKESH RANJAN GUPTA- 18BEC0651

UTSAB SUVRO BISWAS- 18BEC0914

ACKNOWLEDGEMENT:

We wish to express our sincere thanks and deep sense of gratitude to our project guide, **Professor. SAKTHI SWARRUP J**, for her encouragement and guidance offered to us throughout the course of this project.

We also take this opportunity to thank the School of Electronics Engineering and Vellore Institute of Technology for providing us the opportunity and infrastructure to perform the project.

PROJECT TITLE

MASTER EQUATION BASED NUMERICAL SIMULATION USING MATLAB

AIM

UNDERSTANDING THE I-V CHARACHTERISTICS OF A SINGLE ELECTRON TRANSISTOR

CONTENTS

ABSTRACT:

Recent modern fabrication technology allows us for the fabrication of nanometer-scaled devices, which is possible to observe single electronic or single electron tunneling phenomena.
The variety of possibility which is possible at nanoscale this project aims to understand the I-V characteristics at the nano scale to understand the electronic properties better.
Recent modern fabrication technology allows us for the fabrication of nanometer scaled devices in which it is possible to observe single electron tunnelling phenomena.
In mosfet on decreasing the channel length below 20nm there is a large statistical fluctuation of the threshold voltage.
Possible way is to use single electron devices for future VLSI because it will be low power consuming and more efficient.

INTRODUCTION:-

Recent modern fabrication technology allows us for the fabrication of nanometer-scaled devices, which is possible to observe single electronic or single electron tunneling phenomena
(Averin & Likharev, 1991; Likharev, 1988; Likharev, 1999; Hanna et al., 1991; Tucker, 1992). On
the other hand, MOSFET (metal-oxide-semiconductor field effect transistor) devices with channel length below 20 nanometer (nm) are no more properly operated because the downscaling
of MOS devices causes a large statistical fluctuation of the threshold voltage. A possible approach to overcome this problem is to use the single electron devices for future VLSI (very large scale integrated circuit) (Takahashi et al., 1995; Saitoh et al., 2001).
Nanometer scale single electron devices have the following features, i.e., low power consumption and small size. These are key features to realize ultra high density circuits. Single electron circuits with new architecture are also possible because the basic operation of single electron devices is quite different from that of conventional semiconductor devices. There are two major requirements for single electron tunneling phenomena (Coulomb blockade) to occur (Averin & Lhikarev, 1991; Likharev, 1988; Likharev, 1999). Firstly, thermal energy □□□ must be much smaller than elemental charging energy □□/□□. This ensures that the transport of charges is in fact governed by the Coulomb charging energy. This condition can be fulfilled either by lowering the temperature or by decreasing the capacitance which means to reduce the island size. Usually, experiments are performed at temperatures of a few mK and for structures with island sizes of a few hundred nanometers. Second requirement is related to tunnel resistance which must exceed the quantum resistance ($h/□□□ \approx □.□$ kΩ)

MATLAB CODE-

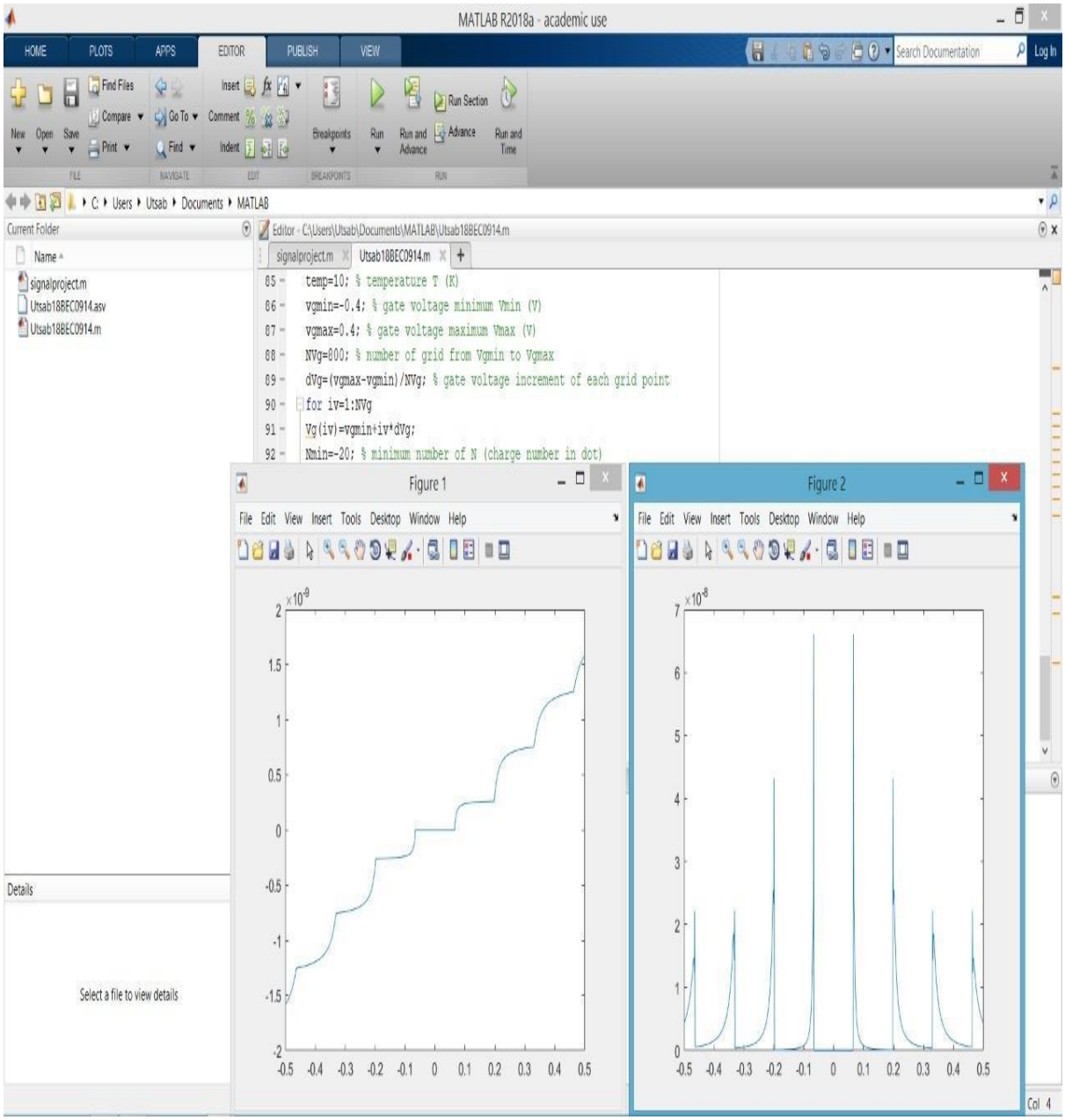
```
% Matlab program source for numerical simulation of Master
equation
% in single electron transistor
% This program code is made by Dr. Ratno Nuryadi, Jakarta,
Indonesia
clear all;
% Definition of Physical constant
q=1.602e-19; % electronic charge (C)
kb=1.381e-23; % Boltzman constant (J/K)
% Definition of Device parameters
c1=1.0e-20; % tunnel capacitor C1 (F)
c2=2.1e-19; % tunnel capacitor C2 (F)
cg=1.0e-18; % gate capacitor Cg (F)
ctotal=c1+c2+cg; % total capacitance (F)
mega=1000000; % definition of mega=10⁶
r1=15*mega; % tunnel resistance R1 (Ohm)
Vg=0; % gate voltage (V)
q0=0; % background charge q0 is assumed to be zero
temp=10; % temperature T (K)
vmin=-0.5; % drain voltage minimum Vmin (V)
vmax=0.5; % drain voltage maximum Vmax (V)
NV=1000; % number of grid from Vmin to Vmax
dV=(vmax-vmin)/NV; % drain voltage increment of each grid point
for iv=1:NV % loop start for drain voltage
V(iv)=vmin+iv*dV; % drain voltage in each grid point
% Note that loop end for drain voltage is located in the end of
this
program source
Nmin=-20; % minimum number of N (charge number in dot)
Nmax=20; % maximum number of N (charge number in dot)
for ne=1:Nmax-Nmin % loop start for N
n=Nmin+ne; % N charge number in dot
% Calculation of Δ☒ in equations (25a) and (25b)
dF1p=q/ctotal*(0.5*q+(n*q-q0)-(c2+cg)*V(iv)+cg*Vg);
dF1n=q/ctotal*(0.5*q-(n*q-q0)+(c2+cg)*V(iv)-cg*Vg);
dF2p=q/ctotal*(0.5*q-(n*q-q0)-c1*V(iv)-cg*Vg);
dF2n=q/ctotal*(0.5*q+(n*q-q0)+c1*V(iv)+cg*Vg);
% Noted that loop end for N is located after calculation of ☒
if dF1p<0
T1p(ne)=1/(r1*q*q)*(-dF1p)/(1-exp(dF1p/(kb*temp)));
% ☒ positive in equation (26a)
else
T1p(ne)=1e-1; % ☒ positive is assumed to be very small
end
if dF1n<0
T1n(ne)=1/(r1*q*q)*(-dF1n)/(1-exp(dF1n/(kb*temp)));
% ☒ negative in equation (26a)
else
```

```
T1n(ne)=1e-1; % ☒ negative is assumed to be very small
end
if dF2p<0
T2p(ne)=1/(r2*q*q)*(-dF2p)/(1-exp(dF2p/(kb*temp)));
% ☒ positive in equation (26b)
else
T2p(ne)=1e-1; % ☒ positive is assumed to be very small
End
if dF2n<0
T2n(ne)=1/(r2*q*q)*(-dF2n)/(1-exp(dF2n/(kb*temp)));
% ☒ negative in equation (26b)
else
T2n(ne)=1e-1; % ☒ negative is assumed to
be very small
end
end % loop end for N
p(1)=0.001; % ρ(Nmin) is assumed to be 0.01
p(Nmax-Nmin)=0.001; % ρ(Nmax) is assumed to be 0.01
sum=0; % sum=0 is initial value to calculate ρ
for ne=2:Nmax-Nmin
p(ne)=p(ne-1)*(T2n(ne-1)+T1p(ne-1))/(T2p(ne)+T1n(ne));
% calculation of ρ(N) in equation (28)
% The conditions below are used to avoid divergence of Matlab
calculation
if p(ne)>1e250
p(ne)=1e250;
end
if p(ne)<1e-250
p(ne)=1e-250;
end
% ----------------------
sum=sum+p(ne);
end
for ne=2:Nmax-Nmin
p(ne)=p(ne)/sum; % Normalization in equation (31b)
end
```

Finally, the current is computed as follows:

```
sumI=0; % sumI=0 is initial condition
for current calculation
for ne=2:Nmax-Nmin
sumI=sumI+p(ne)*(T2p(ne)-T2n(ne));
end
I(iv)=q*sumI; % I in equation (32b)
end % end of drain voltage loop
plot(V,I); % plot of I vs V
for iv=1:NV-1
dIdV(iv)=(I(iv+1)-I(iv))/dV; % calculation of dIdV
end
figure;
plot(V(1,1:NV-1),dIdV); % plot of dIdV vs V
```

SIMULATION RESULT



CONCLUSION

A numerical simulation of the single electron transistor using Matlab.
This simulation is based on the Master equation method and is useful for both educational and research purposes. Simulated results produce the staircase behavior in the current-drain voltage characteristics and periodic oscillations in current-gate voltage characteristics.

REFERENCES-

Amman, M.; Wilkins, R.; Ben-Jacob, E.; Maker, P.D.; & Jaklevic, R.C. (1991). Analytic
solution for the current-voltage characteristic of two mesoscopic tunnel junctions coupled in series, Phys. Rev. B, 43, pp. 1146-1149.
Averin, D.V. & Likharev, K.K. (1991). Mesoscopic phenomena in Solids, edited by B.L.
Altshuler, P.A. Lee, and R.A. Webb (Elsevier, Amsterdam), pp. 173-271.
Fonseca, L.R.C.: Korotkov, A.N.: Likharev, K.K.; & Odintsov, A.A. (1997). A numerical study of
the dynamics and statistics of single electron systems, J. Appl. Phys. 78 (5), pp. 3238-3251.
Hanna, A.E. & Tinkham, M. (1991). Variation of the Coulomb staircase in a two-junction
system by fractional electron charge, Phys. Rev. B, 44, pp. 5919-5922.
Kirihara, M.; Kuwamura, N.; Taniguchi, K.; & Hamaguchi, C. (1994). Monte Carlo study of
single-electronic devices, Proceedings of the International Conference on Solid State Devices and Materials, Yokohama, Japan, pp. 328-330.
Likharev, K.K. (1988). Correlated discrete transfer of single electrons in ultrasmall junctions,
IBM J. Res. Develop. 32(1), pp. 144-157.
Likharev, K.K. (1999). Single-electron devices and their applications, Proceedings of the IEEE,
87, pp. 606-632.
Lee, D.S.; Yang, H.S.; Kang, K.C.; Lee, J.E.; Lee, J.H.; Park, S.H.; & Park, B.G. (2009). Silicon-
Based Dual-Gate Single-Electron Transistors for Logic Applications", Jpn. J. Appl. Phys. 48, p. 071203.