1. Description

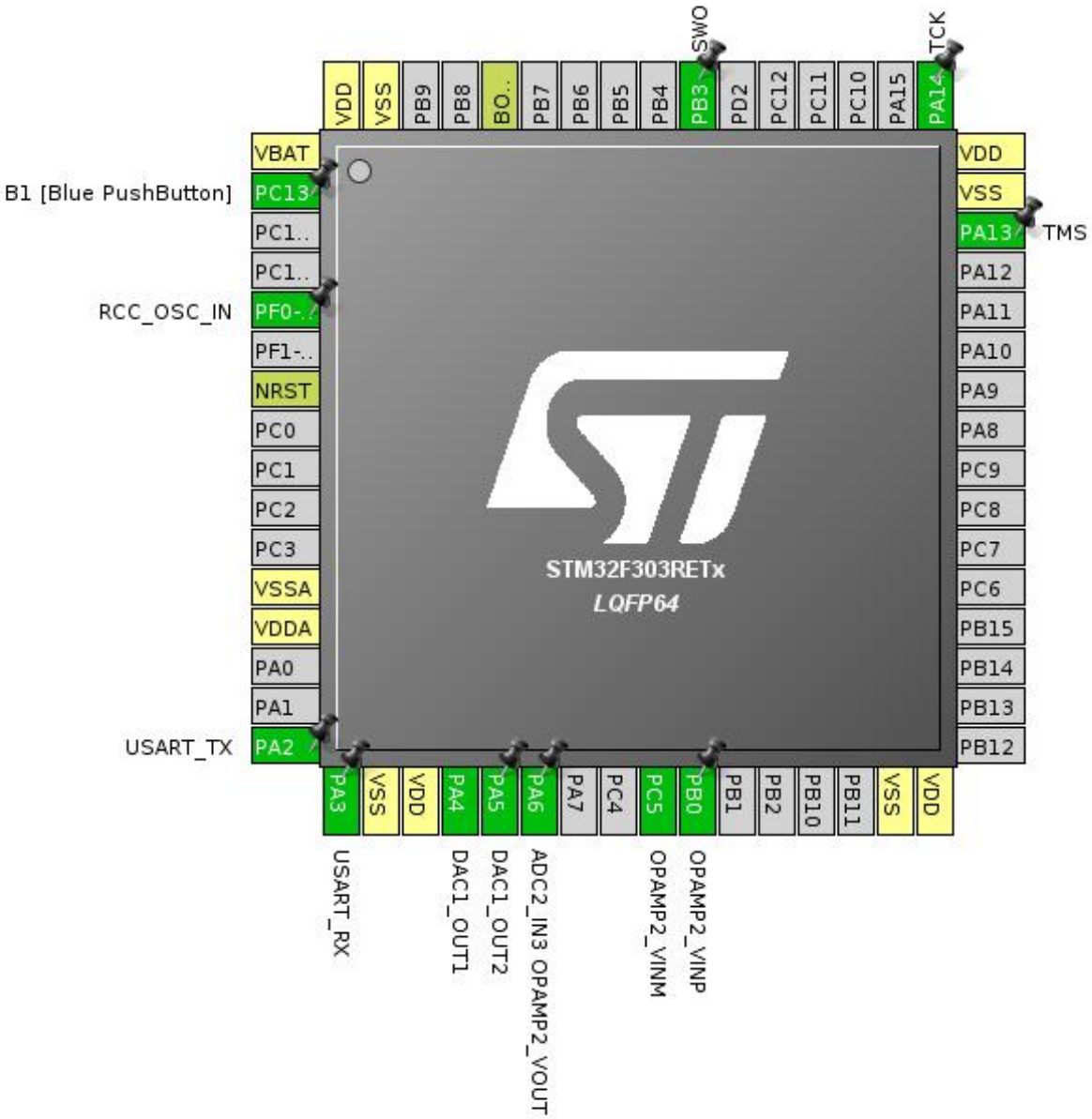
1.1. Project

Project Name	f3_nucleo_oscilloscope
Board Name	NUCLEO-F303RE
Generated with:	STM32CubeMX 4.21.0
Date	06/15/2017

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303RETx
MCU Package	LQFP64
MCU Pin number	64

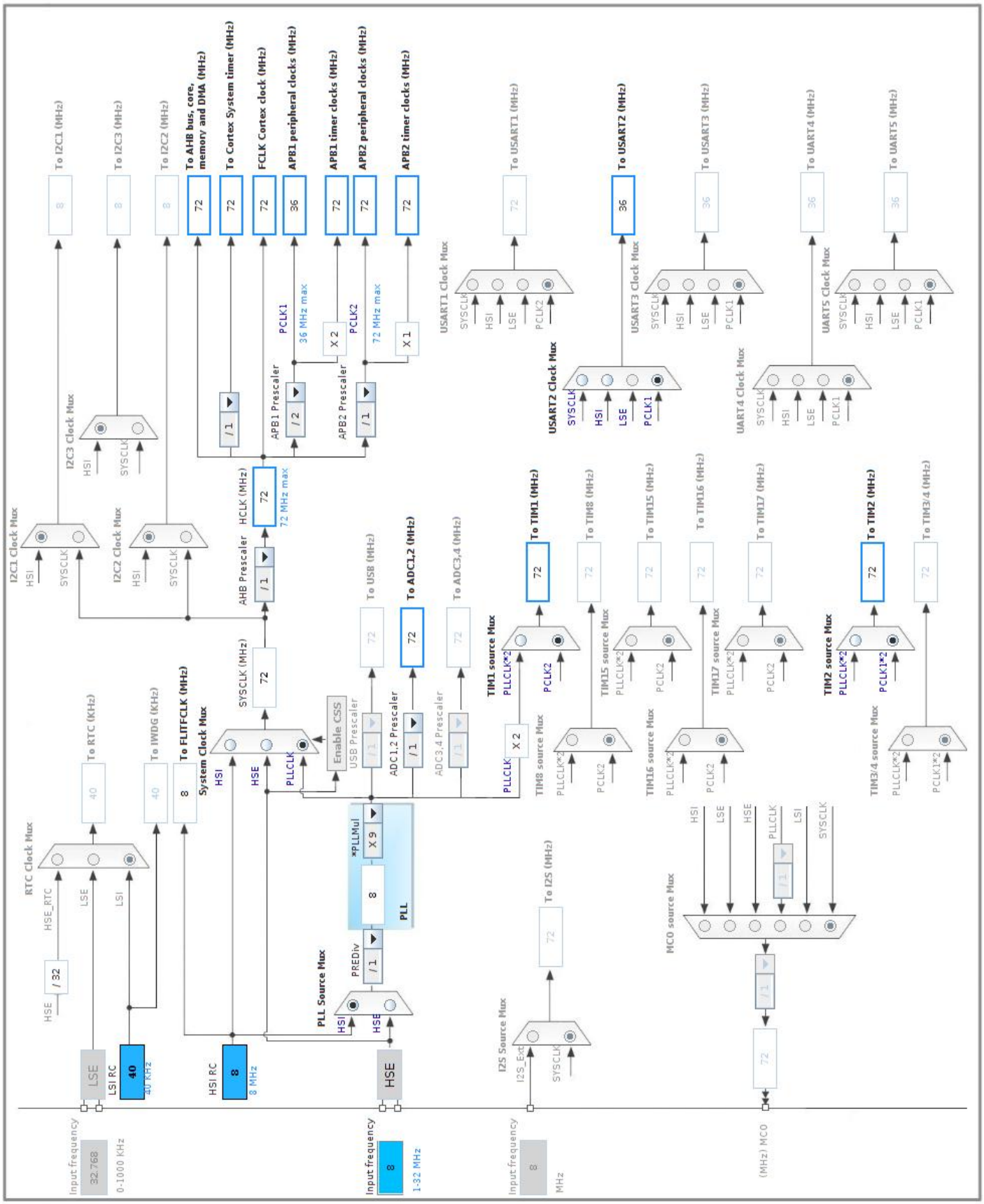
2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	DAC1_OUT1	
21	PA5	I/O	DAC1_OUT2	
22	PA6	I/O	ADC2_IN3, OPAMP2_VOUT	
25	PC5	I/O	OPAMP2_VINM	
26	PB0	I/O	OPAMP2_VINP	
31	VSS	Power		
32	VDD	Power		
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3	I/O	SYS_JTDO-TRACESWO	SWO
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC2

IN3: OPAMP2 Output Single-Ended
mode: VOPAMP2 Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 1 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 3
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0
Monitored by	None
ADC_Injected_ConversionMode:	
Enable Injected Conversions	**Disable ***
Analog Watchdog 1:	
Enable Analog WatchDog1 Mode	**true ***
Watchdog Mode	Single regular channel
Analog WatchDog Channel	Channel 3

High Threshold	**1000 ***
Low Threshold	0
Interrupt Mode	**Enabled ***

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	**true ***
High Threshold	**4095 ***
Low Threshold	**900 ***
Interrupt Mode	**Enabled ***

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. DAC1

mode: OUT1 Configuration

mode: OUT2 Configuration

5.2.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	**Disable ***
Trigger	**Timer 7 Trigger Out event ***
Wave generation mode	**Triangle wave generation ***
Maximum Triangle Amplitude	**255 ***

5.3. OPAMP2

Mode: PGA Connected

5.3.1. Parameter Settings:

Basic Parameters:

PGA Gain	**16 ***
User Trimming	Disable

5.4. RCC

High Speed Clock (HSE): BYPASS Clock Source

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.5. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

5.6. TIM1

Clock Source : Internal Clock

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**15 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	**Enable (sync between this TIM (Master) and its Slaves (through TRGO)) ***
Trigger Event Selection TRGO	**Update Event ***

Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

5.7. TIM2

Slave Mode: External Clock Mode 1

Trigger Source: ITR0

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1199 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	ETR mode 1

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	**Update Event ***

5.8. TIM7

mode: Activated

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**79 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

5.9. USART2

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**1152000 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC2	PA6	ADC2_IN3	Analog mode	No pull up pull down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull up pull down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull up pull down	n/a	
OPAMP2	PA6	OPAMP2_VOUT	Analog mode	No pull up pull down	n/a	
	PC5	OPAMP2_VINM	Analog mode	No pull up pull down	n/a	
	PB0	OPAMP2_VINP	Analog mode	No pull up pull down	n/a	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	SWO
USART2	PA2	USART2_TX	Alternate Function Push Pull	*	Low	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	*	Low	USART_RX
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull up pull down	n/a	B1 [Blue PushButton]

6.2. DMA configuration

DMA request	Stream	Direction	Priority
MEMTOMEM	DMA1_Channel1	Memory To Memory	Low
MEMTOMEM	DMA1_Channel2	Memory To Memory	Low
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low
DAC1_CH1	DMA1_Channel3	Memory To Peripheral	Low
ADC2	DMA2_Channel1	Peripheral To Memory	Low

MEMTOMEM: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Src Memory Increment:	**Enable ***
Dst Memormy Increment:	**Enable ***
Src Memory Data Width:	**Half Word ***
Dst Memormy Data Width:	**Half Word ***

MEMTOMEM: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Src Memory Increment:	**Enable ***
Dst Memormy Increment:	**Enable ***
Src Memory Data Width:	**Word ***
Dst Memormy Data Width:	**Word ***

USART2_TX: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

DAC1_CH1: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable

Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC2: DMA2_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
ADC1 and ADC2 interrupts	true	0	0
TIM2 global interrupt	true	0	0
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	true	0	0
TIM7 global interrupt	true	0	0
DMA2 channel1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
DMA1 channel1 global interrupt	unused		
DMA1 channel2 global interrupt	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger, commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
EXTI line[15:10] interrupts	unused		
TIM6 global interrupt and DAC1 underrun interrupt	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303RETx
Datasheet	026415_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	f3_nucleo_oscilloscope
Project Folder	/home/elmot/projects/f3_nucleo_oscilloscope
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F3 V1.8.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No