

1. Description

1.1. Project

Project Name	color_sensor
Board Name	NUCLEO-F446RE
Generated with:	STM32CubeMX 6.10.0
Date	04/25/2024

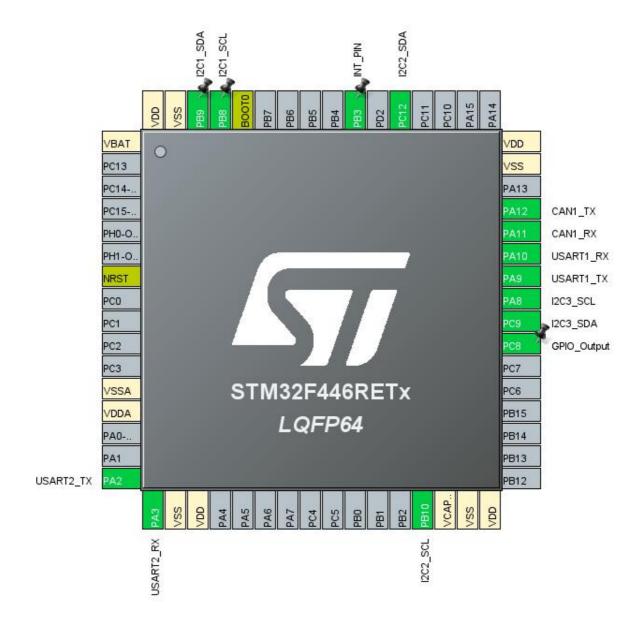
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

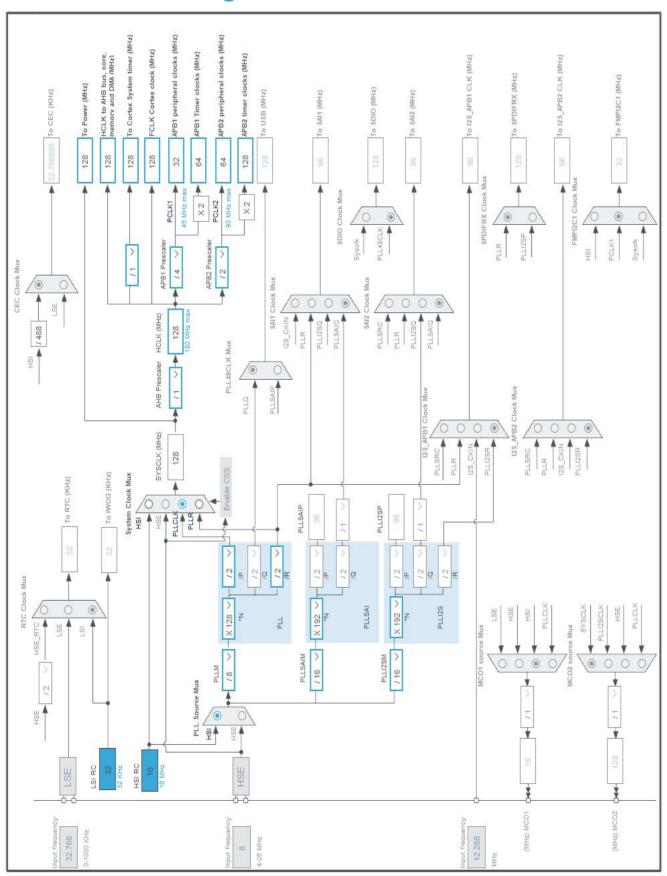


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
29	PB10	I/O	I2C2_SCL	
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
39	PC8 *	I/O	GPIO_Output	
40	PC9	I/O	I2C3_SDA	
41	PA8	I/O	I2C3_SCL	
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
44	PA11	I/O	CAN1_RX	
45	PA12	I/O	CAN1_TX	
47	VSS	Power		
48	VDD	Power		
53	PC12	I/O	I2C2_SDA	
55	PB3 *	I/O	GPIO_Input	INT_PIN
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value	
Project Name	color_sensor	
Project Folder	C:\Users\urtna\Downloads\color_sensor-20240420T012702Z-001\color_sensor	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.0	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART2_UART_Init	USART2
5	MX_I2C1_Init	I2C1
6	MX_USART1_UART_Init	USART1
7	MX_I2C3_Init	I2C3
8	MX_CAN1_Init	CAN1
9	MX_I2C2_Init	I2C2
10	MX_TIM12_Init	TIM12

color_sensor Project
Configuration Report

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	DS10693_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

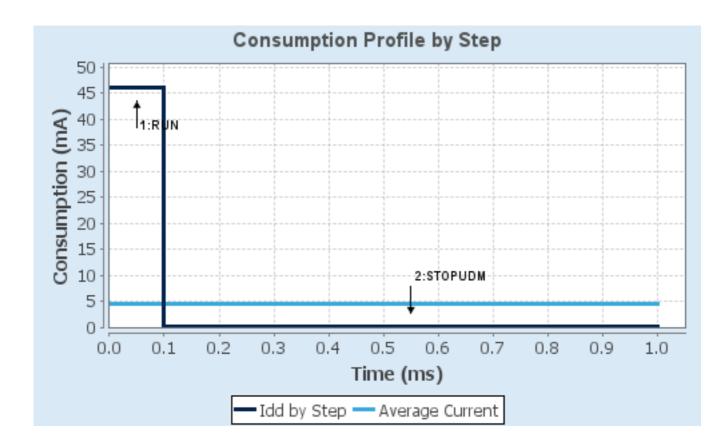
1.4. Sequence

	1	
Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/REGON/ART/P REFETCH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	55 μA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	98.02	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. CAN1

mode: Activated

2.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum) 2 *

Time Quantum 62.5 *

Time Quanta in Bit Segment 1 14 Times *

Time Quanta in Bit Segment 2 1 Time
Time for one Bit 1000

Baud Rate 1000000 *

ReSynchronization Jump Width 1 Time

Basic Parameters:

Time Triggered Communication Mode

Automatic Bus-Off Management

Disable

Automatic Wake-Up Mode

Automatic Retransmission

Disable

Receive Fifo Locked Mode

Disable

Transmit Fifo Priority

Disable

Advanced Parameters:

Operating Mode Normal

2.2. I2C1 I2C: I2C

2.2.1. Parameter Settings:

Master Features:

I2C Speed Mode Standard Mode

I2C Clock Speed (Hz) 100000

Slave Features:

Clock No Stretch Mode Disabled

Primary Address Length selection 7-bit

Dual Address Acknowledged Disabled

Primary slave address 0

General Call address detection Disabled

2.3. I2C2

12C: 12C

2.3.1. Parameter Settings:

Master Features:

I2C Speed Mode Standard Mode

I2C Clock Speed (Hz) 100000

Slave Features:

Clock No Stretch Mode Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

General Call address detection Disabled

2.4. I2C3 I2C: I2C

2.4.1. Parameter Settings:

Master Features:

I2C Speed Mode Fast Mode *

I2C Clock Speed (Hz) 400000

Fast Mode Duty Cycle Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0
General Call address detection Disabled

2.5. RCC

2.5.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 2

Power Over Drive Disabled

2.6. SYS

Timebase Source: SysTick

2.7. TIM12

mode: Clock Source

2.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 64000-1 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 2-1 *

Internal Clock Division (CKD)

auto-reload preload

Enable *

2.8. USART1

Mode: Asynchronous

2.8.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

2.9. USART2

Mode: Asynchronous

2.9.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

* User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN1	PA11	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA12	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
	PB9	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
	PC12	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INT_PIN

3.2. DMA configuration

DMA request	Stream	Direction	Priority
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte

Memory Data Width: Byte

Byte

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte
Memory Data Width: Byte

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0 0
Hard fault interrupt	true	0	0
·		0	0
Memory management fault	true		
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream5 global interrupt	true	0	0
DMA1 stream6 global interrupt	true	0	0
TIM8 break interrupt and TIM12 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CAN1 TX interrupt	unused		
CAN1 RX0 interrupt	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt		unused	
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		

3.3.2. NVIC Code generation

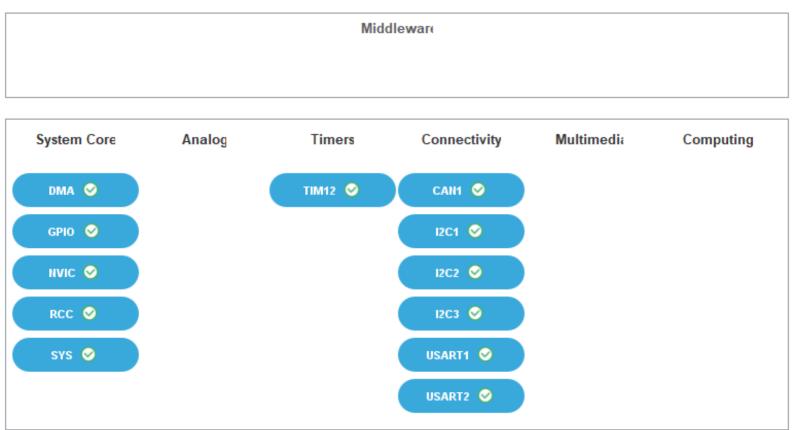
Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream5 global interrupt	false	true	true
DMA1 stream6 global interrupt	false	true	true
TIM8 break interrupt and TIM12 global interrupt	false	true	true

^{*} User modified value

4. System Views

- 4.1. Category view
- 4.1.1. Current



5. Docs & Resources

Type Link