

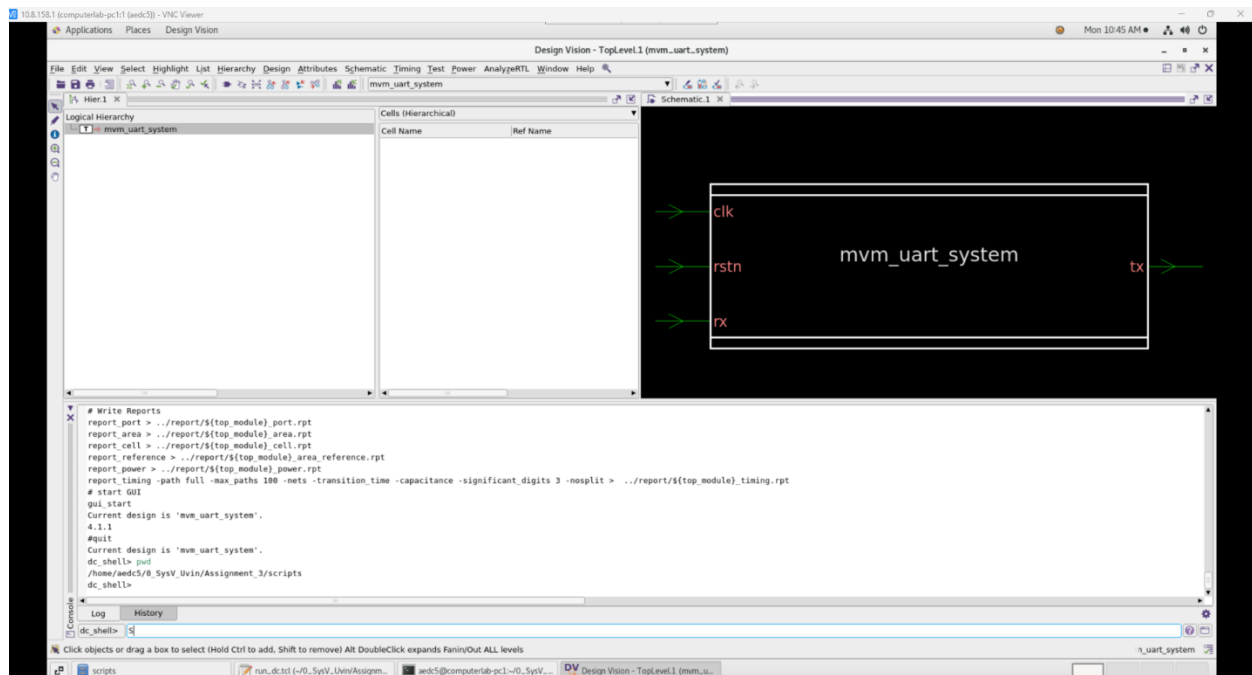
System Verilog for ASIC/FPGA Design & Simulation 2023 -In01

Assignment 3 – R.P.U.A. Pathirana

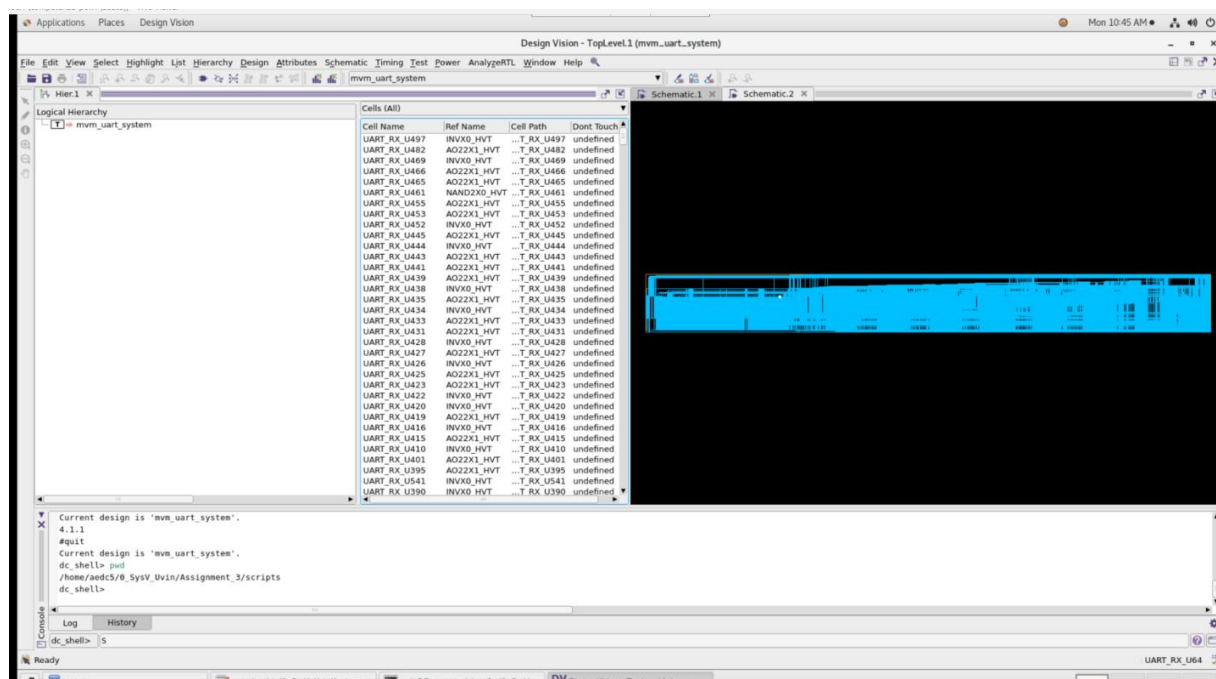
In this Assignment, Matrix Vector Multiplier UART System final verilog code was synthesized using the SAED 32nm EDK and Synopsys Design Compiler. Then the final layout was obtained after doing PnR using the Synopsys IC Compiler II. This report contains screenshots during the process.

Selected parameters : R=8, C=8, W_X=4, W_K=3

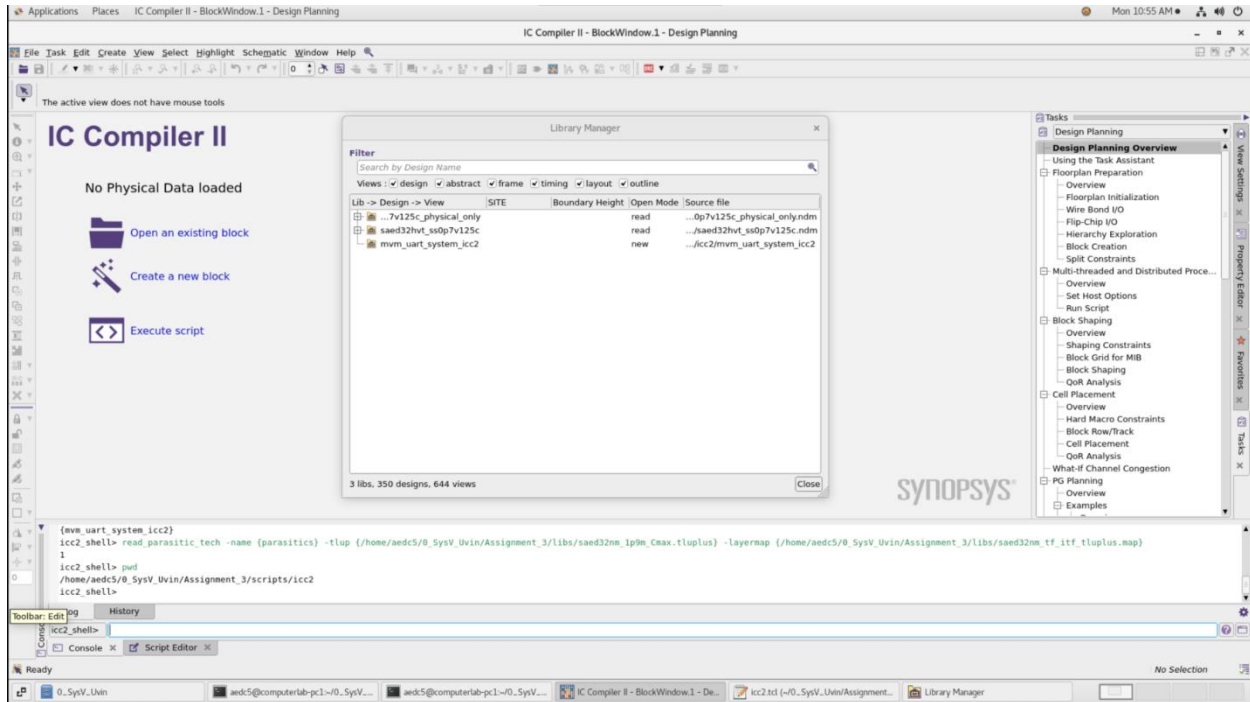
Top Level Module of the Design



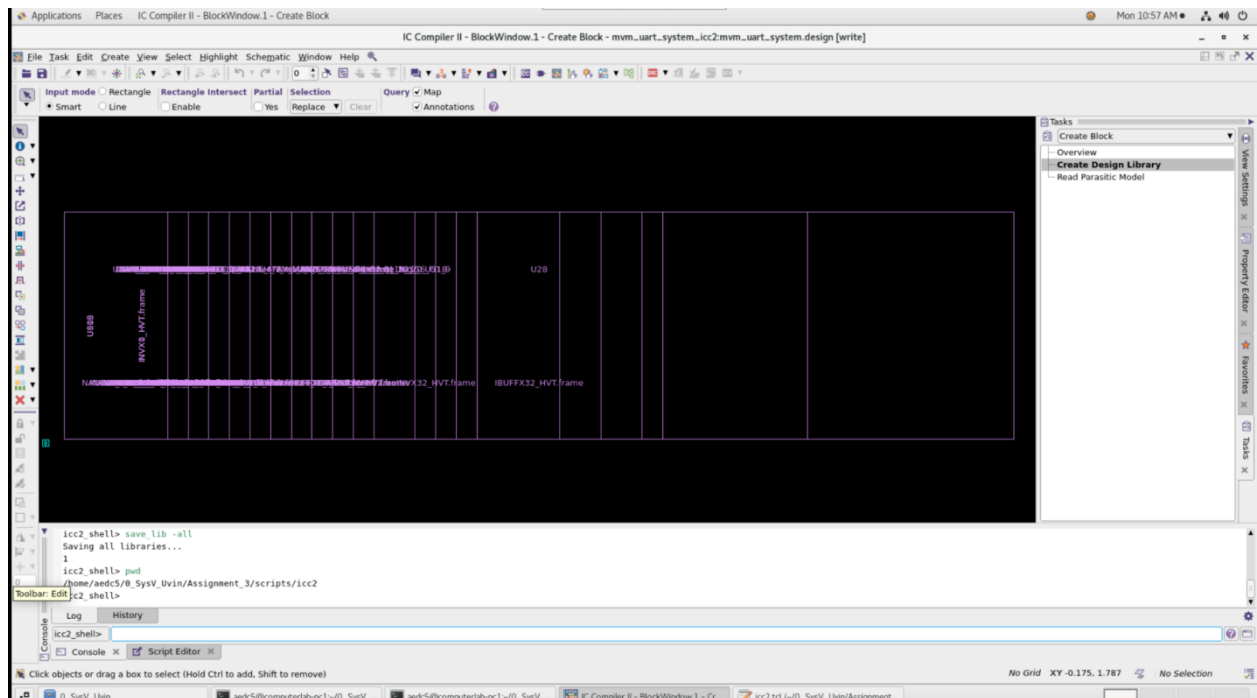
The synthesized RTL design schematic



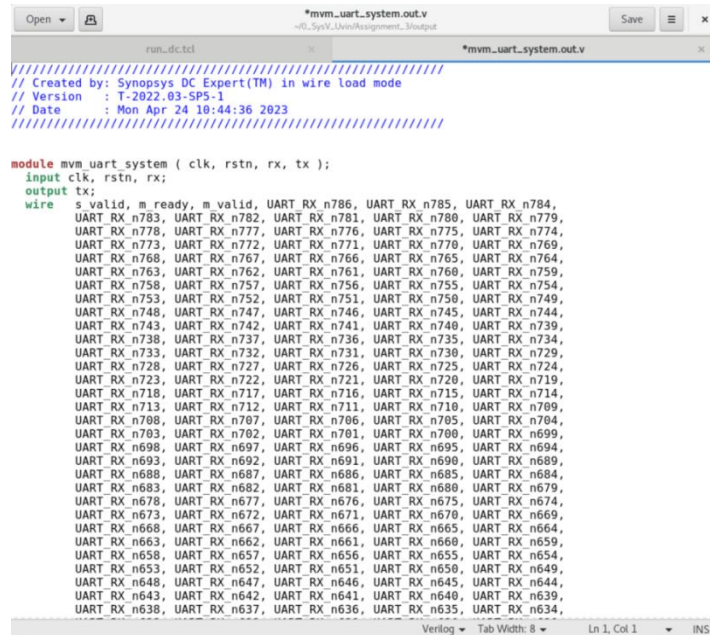
Creating a Library



Creating blocks



Synthesized output



```
Open  *mvm_uart_system.out.v  Save  x
~0_SysV_Uin/Assignment_3/output

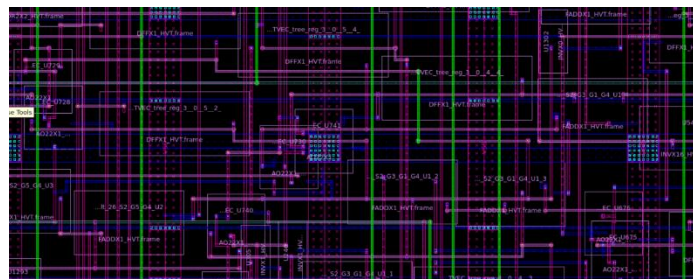
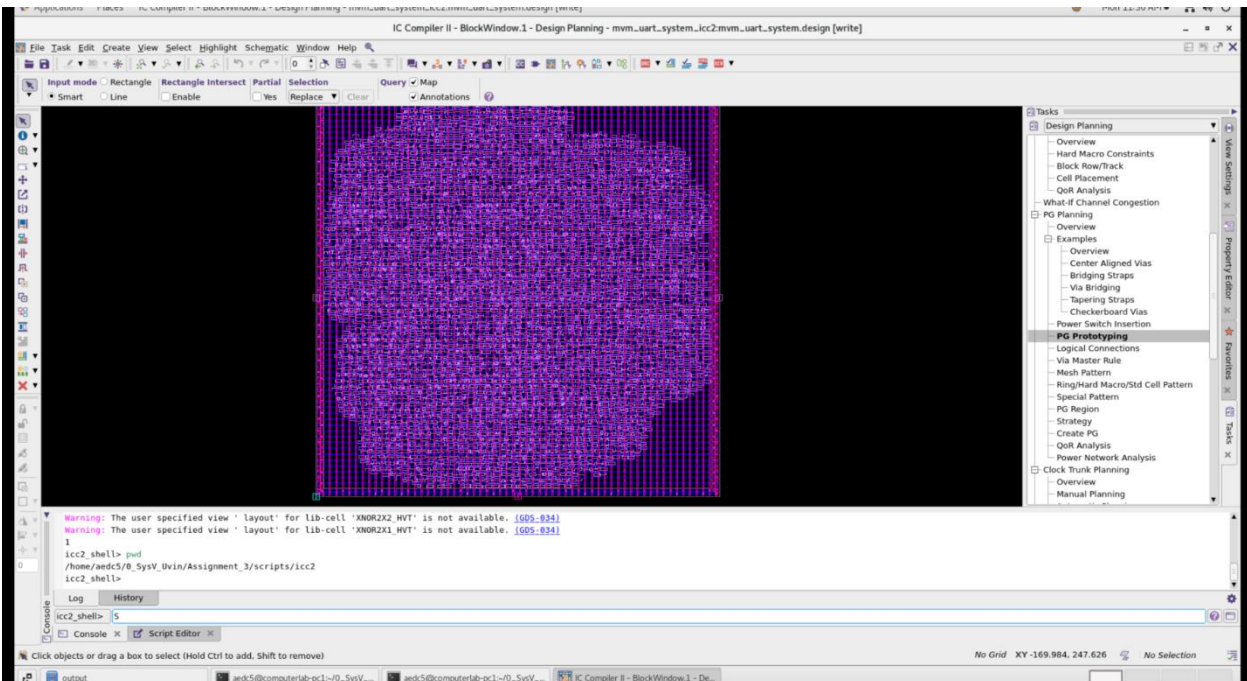
run_dct.tcl  *mvm_uart_system.out.v

/////////////////////////////////////////////////////////////////
// Created by: Synopsys DC Expert(TM) in wire load mode
// Version   : T-2022.03-SP5-1
// Date      : Mon Apr 24 10:44:36 2023
/////////////////////////////////////////////////////////////////

module mvm_uart_system ( clk, rstn, rx, tx );
input clk, rstn, rx;
output tx;
wire
s_valid, m_ready, m_valid, UART_RX n786, UART_RX n785, UART_RX n784,
UART_RX n783, UART_RX n782, UART_RX n781, UART_RX n780, UART_RX n779,
UART_RX n778, UART_RX n777, UART_RX n776, UART_RX n775, UART_RX n774,
UART_RX n773, UART_RX n772, UART_RX n771, UART_RX n770, UART_RX n769,
UART_RX n768, UART_RX n767, UART_RX n766, UART_RX n765, UART_RX n764,
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UART_RX n738, UART_RX n737, UART_RX n736, UART_RX n735, UART_RX n734,
UART_RX n733, UART_RX n732, UART_RX n731, UART_RX n730, UART_RX n729,
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UART_RX n23, UART_RX n22, UART_RX n21, UART_RX n20, UART_RX n19,
UART_RX n18, UART_RX n17, UART_RX n16, UART_RX n15, UART_RX n14,
UART_RX n13, UART_RX n12, UART_RX n11, UART_RX n10, UART_RX n9,
UART_RX n8, UART_RX n7, UART_RX n6, UART_RX n5, UART_RX n4,
UART_RX n3, UART_RX n2, UART_RX n1, UART_RX n0,
/////////////////////////////////////////////////////////////////

Verilog  Tab Width: 8  Ln 1, Col 1  INS
```

Completed PnR Layout



Reports

Open



mvm_uart_system_timing.rpt

Save



x

Report : timing

-path full

-delay max

-nets

-max_paths 100

-transition time

-capacitance

Design : mvm_uart_system

Version: T-2022.03-SP5-1

Date : Mon Apr 24 10:44:38 2023

A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: ss0p7v125c Library: saed32hvt_ss0p7v125c

Wire Load Model Mode: enclosed

Startpoint: AXIS_MVM_MATVEC_tree_reg_7_0_6_0

(rising edge-triggered flip-flop clocked by clk)

Endpoint: AXIS_MVM_MATVEC_tree_reg_7_1_3_9

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

mvm_uart_system 35000 saed32hvt_ss0p7v125c

Point Fanout Cap Trans Incr Path

clock clk (rise edge) 0.000 0.000

clock network delay (ideal) 0.000 0.000

AXIS_MVM_MATVEC_tree_reg_7_0_6_0 /CLK (DFFX1_HVT) 0.000 # 0.000 r

AXIS_MVM_MATVEC_tree_reg_7_0_6_0 /QN (DFFX1_HVT) 0.173 0.450 f

n309 (net) 1 0.549 0.000 0.450 f

U275/Y (OR2X1_HVT) 0.091 0.320 0.770 f

n182 (net) 1 0.751 0.000 0.770 f

U276/Y (INVX1_HVT) 0.083 0.103 0.872 r

AXIS_MVM_MATVEC_add_31_S2_G4_G1_G8_carry[1] (net) 1 1.341 0.000 0.872 r

AXIS_MVM_MATVEC_add_31_S2_G4_G1_G8_U1_1/C0 (FADDX1_HVT) 0.220 0.444 1.316 r

AXIS_MVM_MATVEC_add_31_S2_G4_G1_G8_carry[2] (net) 1 1.341 0.000 1.316 r

Plain Text Tab Width: 8 Ln 1, Col 1 INS

Open



mvm_uart_system_power.rpt

Save



x

Loading db file '/home/aedc5/libs/tsmc_32nm/SAED32_EDK/lib/stdcell_hvt/db_nldm/saed32hvt_ss0p7v125c.db'

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)

Warning: Design has unannotated primary inputs. (PWR-414)

Warning: Design has unannotated sequential cell outputs. (PWR-415)

Report : power

-analysis effort low

Design : mvm_uart_system

Version: T-2022.03-SP5-1

Date : Mon Apr 24 10:44:38 2023

Library(s) Used:

saed32hvt_ss0p7v125c (File: /home/aedc5/libs/tsmc_32nm/SAED32_EDK/lib/stdcell_hvt/db_nldm/saed32hvt_ss0p7v125c.db)

Operating Conditions: ss0p7v125c Library: saed32hvt_ss0p7v125c

Wire Load Model Mode: enclosed

Design Wire Load Model Library

mvm_uart_system 35000 saed32hvt_ss0p7v125c

Global Operating Voltage = 0.7

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000ff

Time Units = 1ns

Dynamic Power Units = 1uW (derived from V,C,T units)

Leakage Power Units = 1pW

Attributes

i - Including register clock pin internal power

Cell Internal Power = 9.7319 mW (99%)

Net Switching Power = 97.4868 uW (1%)

Total Dynamic Power = 9.8294 mW (100%)

Cell Leakage Power = 206.8400 uW

Power Group Internal Power Switching Power Leakage Power Total Power (%) Attrs

io_pad 0.0000 0.0000 0.0000 0.0000 (0.00%)

memory 0.0000 0.0000 0.0000 0.0000 (0.00%)

black_box 0.0000 0.0000 0.0000 0.0000 (0.00%)

clock_network 9.6557e+03 0.0000 0.0000 9.6557e+03 (96.21%) i

register 5.9658 0.8168 7.7732e+07 84.5462 (0.84%)

sequential 0.0000 0.0000 0.0000 0.0000 (0.00%)

combinational 70.2982 96.6694 1.2911e+08 296.0751 (2.95%)

Total 9.7320e+03 uW 97.4862 uW 2.0684e+08 pW 1.0036e+04 uW

1

Plain Text Tab Width: 8 Ln 30, Col 23 INS

```

*****
Report : port
Design : mvm_uart_system
Version: T-2022.03-SP5-1
Date   : Mon Apr 24 10:44:37 2023
*****

```

Port	Dir	Pin Load	Wire Load	Max Trans	Max Cap	Connection Class	Attrs
clk	in	0.0000	0.0000	--	--	--	
rstn	in	0.0000	0.0000	--	--	--	
rx	in	0.0000	0.0000	--	--	--	
tx	out	0.0000	0.0000	--	--	--	

1

```

*****
Report : area
Design : mvm_uart_system
Version: T-2022.03-SP5-1
Date   : Mon Apr 24 10:44:37 2023
*****

```

Library(s) Used:

saed32hvt_ss0p7v125c (File: /home/aedc5/libs/tsmc_32nm/SAED32_EDK/lib/stdcell_hvt/db_nldm/saed32hvt_ss0p7v125c.db)

```

Number of ports:          4
Number of nets:           8778
Number of cells:          7466
Number of combinational cells: 5314
Number of sequential cells: 2151
Number of macros/black boxes: 0
Number of buf/inv:        828
Number of references:      50

```

```

Combinational area:      16349.083457
Buf/Inv area:            2936.125674
Noncombinational area:   14598.285900
Macro/Black Box area:    0.000000
Net Interconnect area:   10333.727892

```

```

Total cell area:         30947.369356
Total area:               41281.097248
1

```

```

*****
Report : cell
Design : mvm_uart_system
Version: T-2022.03-SP5-1
Date   : Mon Apr 24 10:44:37 2023
*****

```

Attributes:

```

b - black box (unknown)
d - dont_touch
h - hierarchical
mo - map_only
n - noncombinational
r - removable
u - contains unmapped logic

```

Cell	Reference	Library	Area	Attributes
AXIS_MVM_MATVEC_U2	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	
AXIS_MVM_MATVEC_U3	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	
AXIS_MVM_MATVEC_U4	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	
AXIS_MVM_MATVEC_U5	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	
AXIS_MVM_MATVEC_U6	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	
AXIS_MVM_MATVEC_U7	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	
AXIS_MVM_MATVEC_U8	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	
AXIS_MVM_MATVEC_U9	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	
AXIS_MVM_MATVEC_U10	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	
AXIS_MVM_MATVEC_U11	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	
AXIS_MVM_MATVEC_U12	A022X1_HVT	saed32hvt_ss0p7v125c	2.541440	