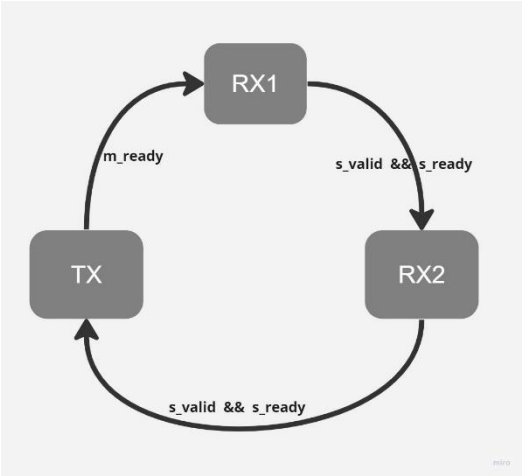
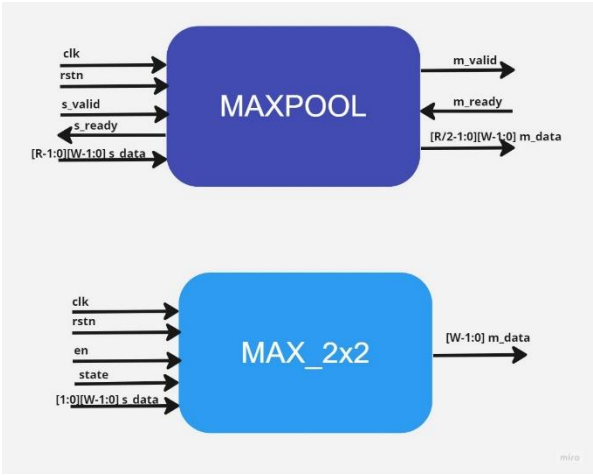
System Verilog for ASIC/FPGA Design & Simulation 2023 -In01

Assignmnet2 – R.P.U.A. Pathirana

The module is designed to do 2x2 max-pooling. It outputs the maximum element in every 2x2 window. Thus the output becomes 4 times smaller. There are two modules such as max pool and max_2x2. Maxpool acts as the top module and it handles the AXI stream of data. Max_2x2 module gets four W-bit wide values in two clock cycles and outputs its maximum value.

The state machine consists of three states such as RX1, RX2, and TX. State transition conditions are shown in the diagram.





RX1	Compare the two s_data values at clk1 and write the maximum to the max_1 register
RX2	Compare the two s_data values at clk2 and write the maximum to the max_2 register
TX	Compare max1 and max2 and write the maximum to the [w-1:0]m_data register