Task

1. Design a Verilog module to display the hexadecimal digits '0' to 'F' on a 7-segment display using Binary-Coded Decimal (BCD) to 7-segment conversion. The module should take a 4-bit BCD input and control the segments of the display to represent the corresponding hexadecimal digit.

2. Design a 3-bit ripple carry adder circuit that takes inputs from switches and displays the sum on a 7-segment display.
3. Design a configurable up-down counter circuit that can count either up or down based on the position of a control switch. When the control switch is in the '1' position, the counter should count upwards, and when the control switch is in the '0' position, the counter should count downwards. This counter is intended for applications where bidirectional counting capability is required, allowing the user to control the counting direction using a simple switch.

Home Task

4. Design a 2-digit counter in Verilog that counts from 0 to 99 and displays the digits on two 7-segment displays. Additionally, implement a clock divider circuit that slows down the counting speed, and when the counter reaches 10, 11, or 12, the corresponding two-digit number should be displayed on the 7-segment displays. This design aims to create a visual representation of the count while ensuring accurate digit display and proper clock division.