Córdova Pichardo Francisco Uziel

Practica 0

```
 1 library ieee;
 2 use ieee.std_logic_1164.all;
 3
 4 entity Practica0 is
 5 port(
 6     a,b,ref : in std_logic_vector(2 downto 0);
 7     sel : in std_logic;
 8     salida : out std_logic_vector(6 downto 0)
 9 );
10 end Practica0;
11
12 architecture APractica0 of Practica0 is
13 signal sensor,condicion : std_logic_vector(2 downto 0);
14     begin
15         --mux
16         sensor <= a when sel = '0' else b;
17         --comparador
18         condicion <= "001" when (sensor < ref) else
19         "010" when (sensor = ref) else "100";
20         --conv
21         salida <= "0000111" when (condicion = "100") else
22                   "0110001" when (condicion = "001") else
23                   "0110111";
24 end APractica0;
```

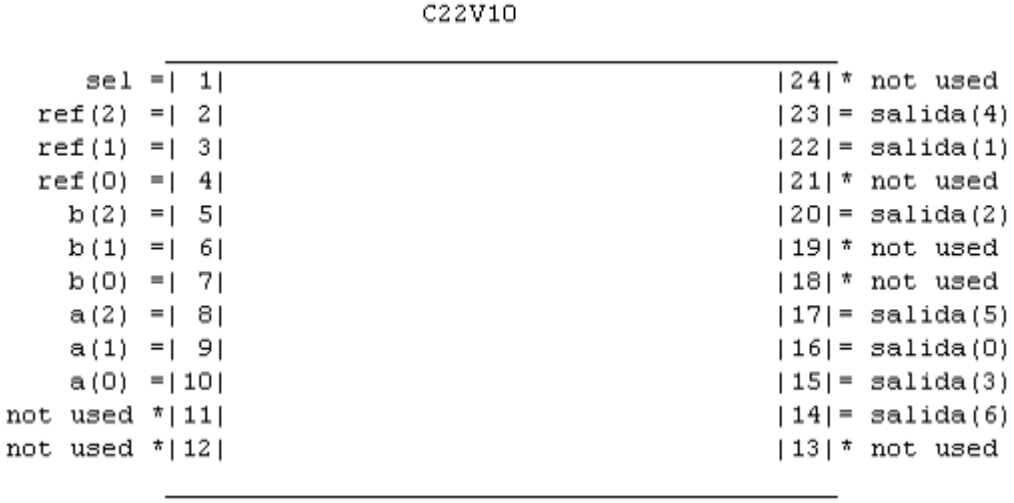
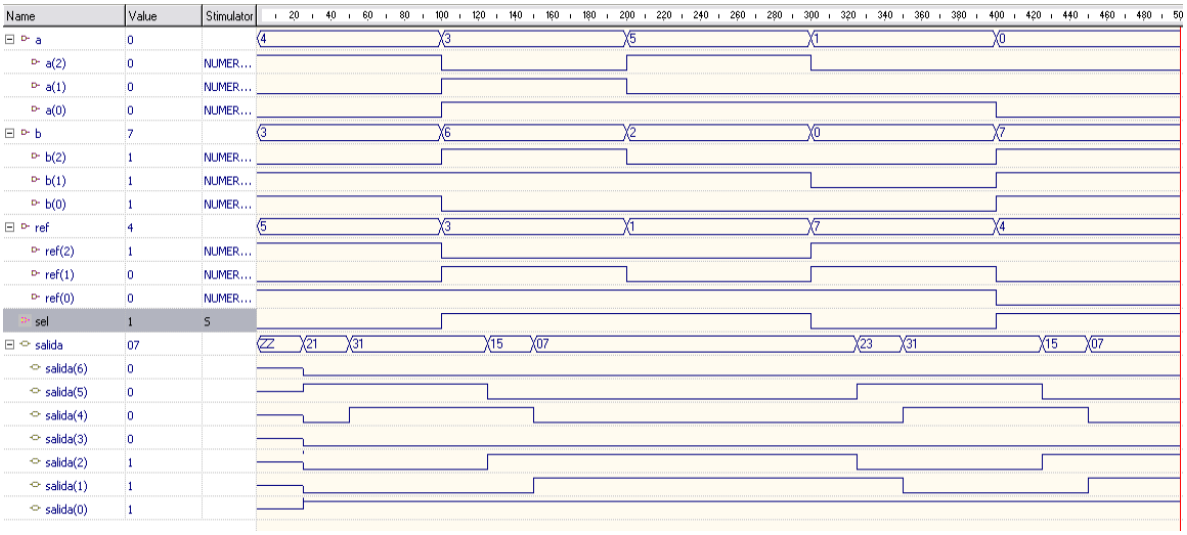


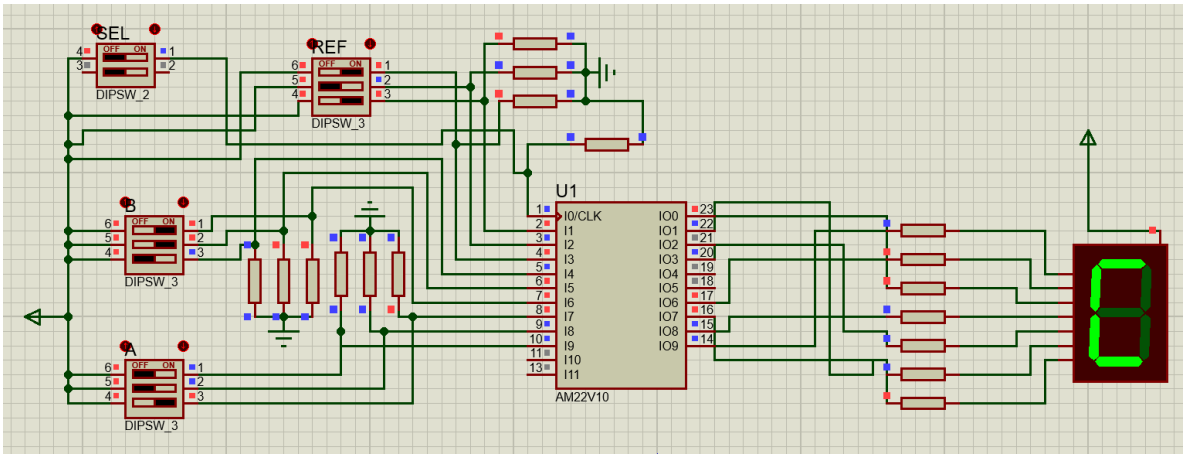
Tabla de pruebas realizadas

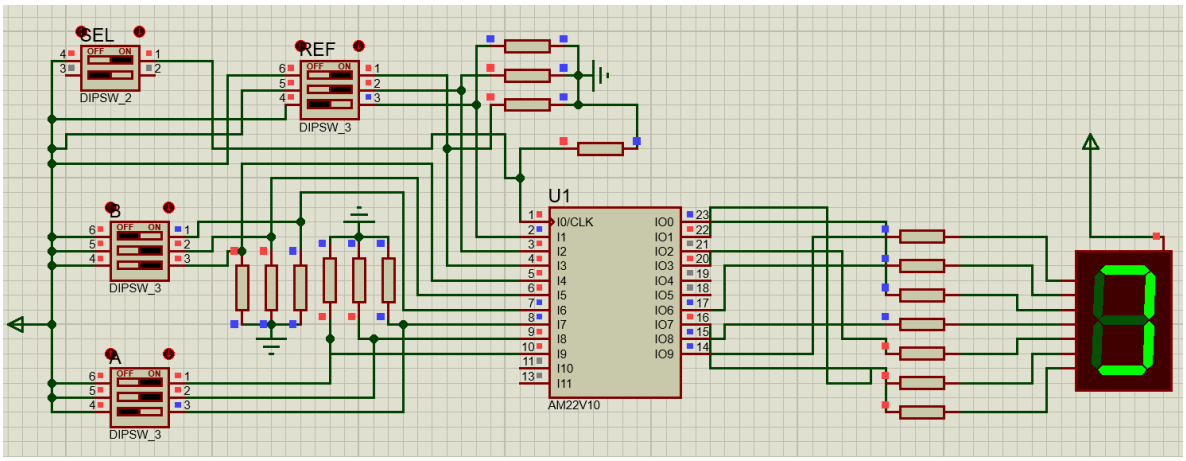
a	b	sel	ref
4	3	0	5
3	6	1	3
5	2	1	1
1	0	0	7
0	7	1	4

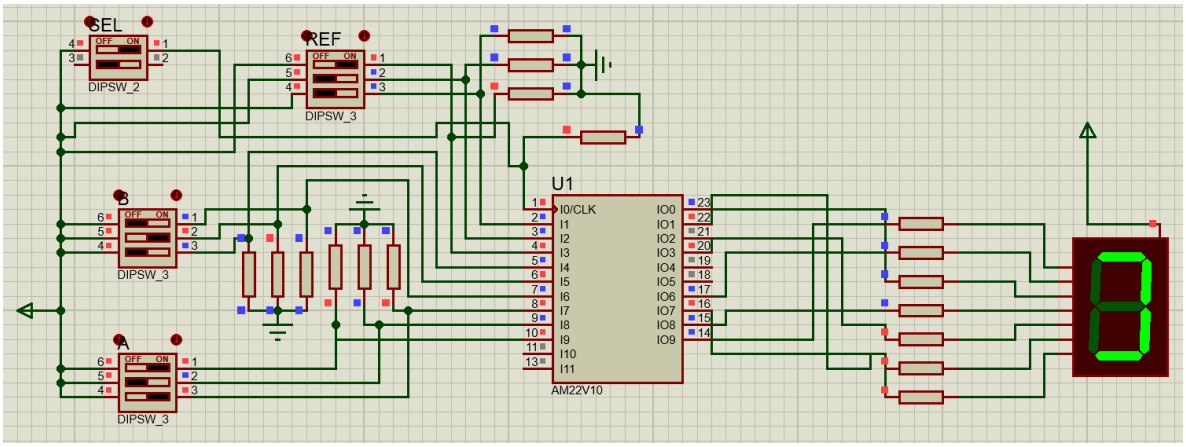
Simulación en galaxy

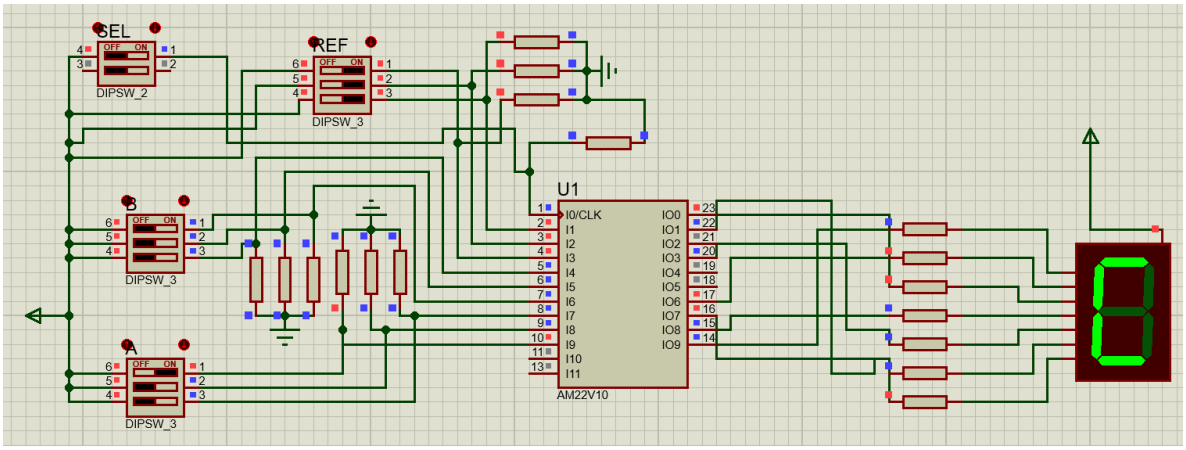


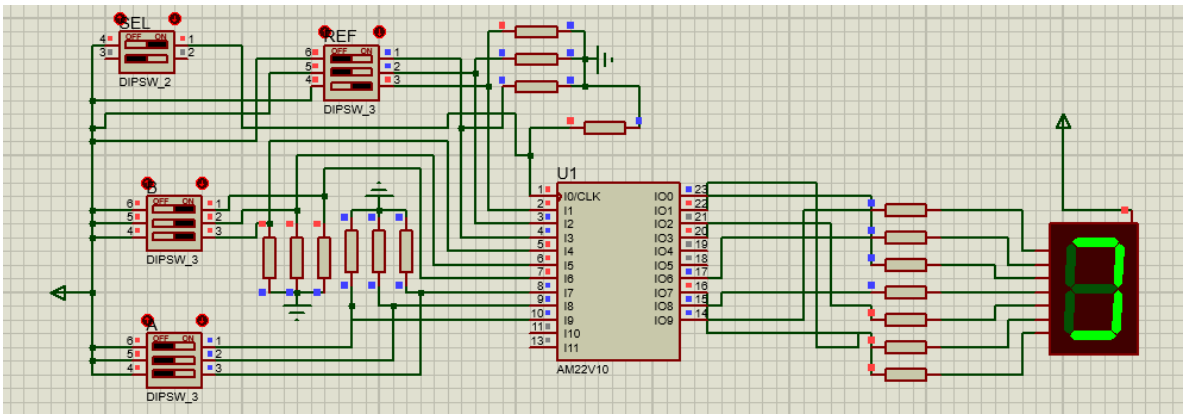
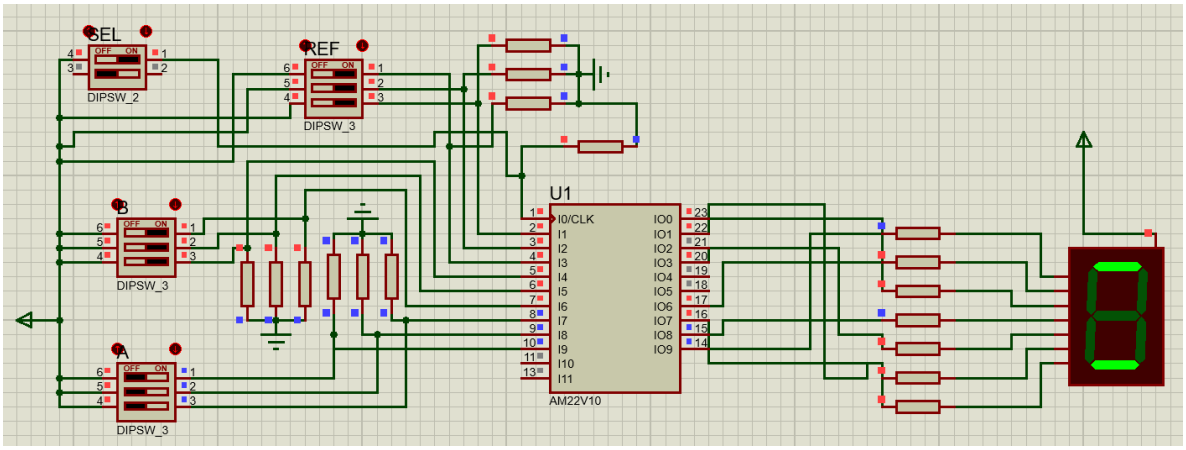
Simulación en Proteus




SEL
REF
B
A
DIPSW_2
DIPSW_3
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10


SEL
REF
B
A
DIPSW_2
DIPSW_3
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10


SEL
REF
B
A
DIPSW_2
DIPSW_3
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10



Esta es una prueba extra donde se muestra que pasa si las entrada seleccionada es igual a la referencia