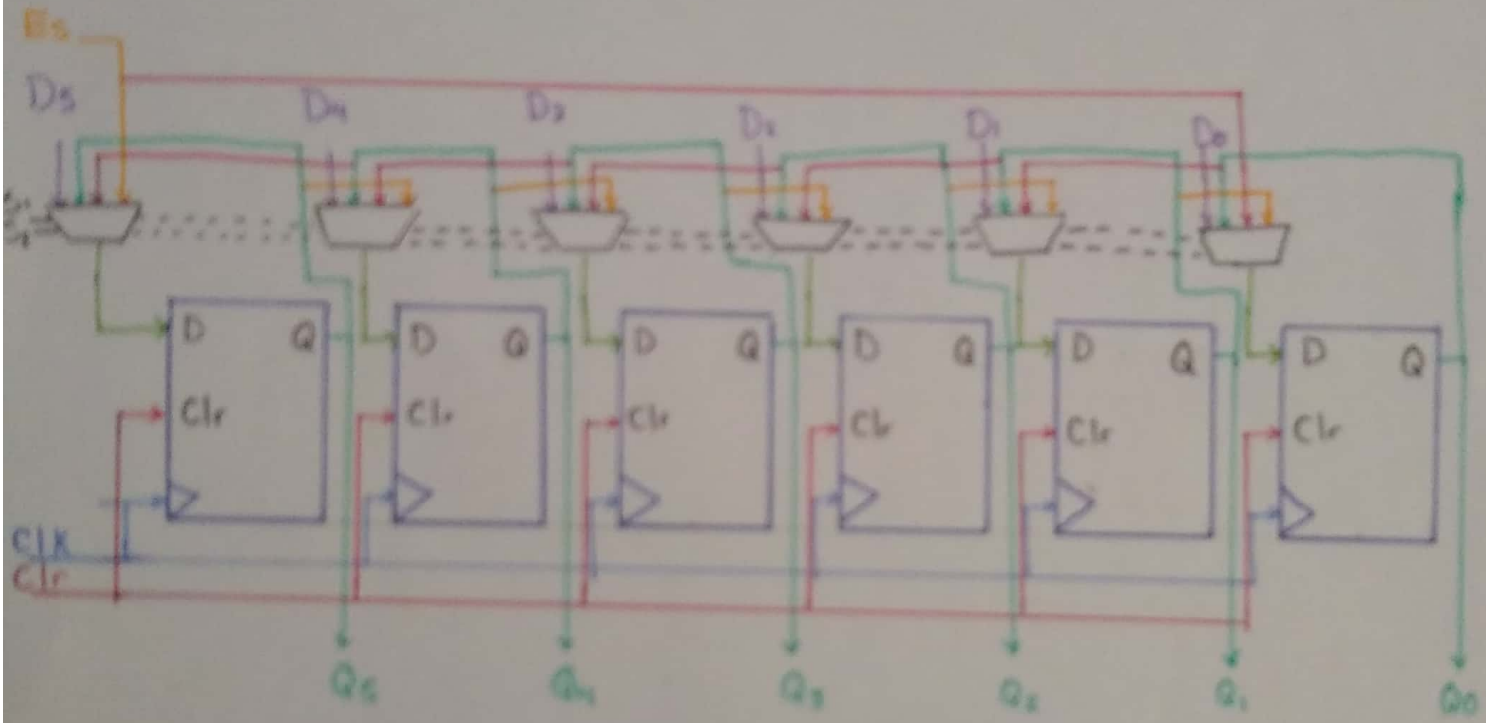
Córdova Pichardo Francisco Uriel

Registro generico de 6 bits



Córdova Pichardo Francisco Uziel

Practica 3

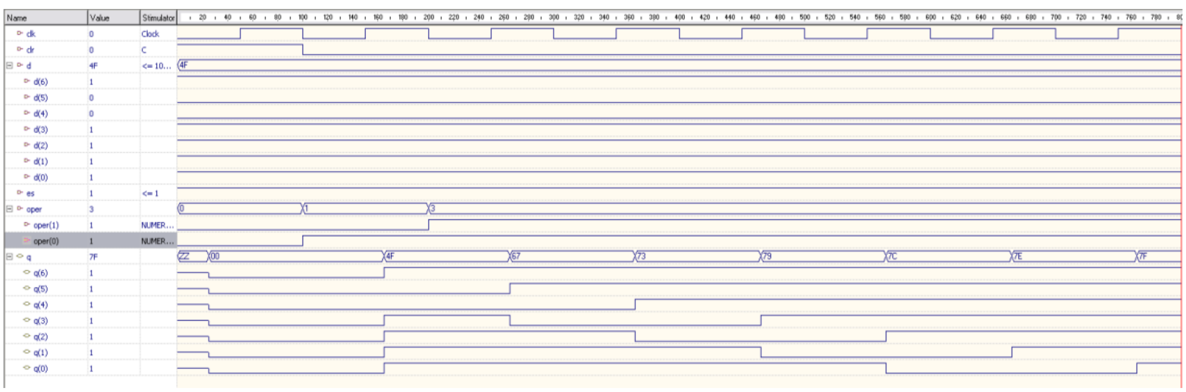
```
 1 library ieee;
 2 use ieee.std_logic_1164.all;
 3
 4 entity PRegistros is port
 5 (
 6     d : in std_logic_vector(6 downto 0);
 7     es, clk, clr : in std_logic;
 8     oper : in std_logic_vector(1 downto 0);
 9     q : out std_logic_vector(6 downto 0)
10 );
11 end PRegistros;
12
13 architecture ARegistros of PRegistros is
14 begin
15     process(clk, clr)
16     begin
17         if(clr = '1') then
18             q <= "0000000";
19         elsif (rising_edge(clk)) then
20             if(oper="00") then --retencion
21                 q<=q;
22             elsif(oper = "01") then --carga
23                 q <= d;
24             elsif(oper = "10") then --corrimiento ala izquierda
25                 for i in 0 to 6 loop
26                     if(i > 0) then
27                         q(i)<=q(i-1);
28                     end if;
29                 end loop;
30             elsif(oper = "11") then --corrimiento a la derecha
31                 for i in 0 to 6 loop
32                     if(i < 5)then
33                         q(i) <= q(i+1);
34                     else
35                         q(i) <= es;
36                     end if;
37                 end loop;
38             end if;
39         end if;
40     end process;
41 end ARegistros;
```

```
                         C22V10

                 ____________________________________________
          clk =|  1|                                      |24|* not used
           es =|  2|                                      |23|= q(5)
         d(6) =|  3|                                      |22|= q(3)
         d(5) =|  4|                                      |21|= q(1)
         d(4) =|  5|                                      |20|* not used
         d(3) =|  6|                                      |19|* not used
      oper(1) =|  7|                                      |18|* not used
      oper(0) =|  8|                                      |17|= q(0)
         d(2) =|  9|                                      |16|= q(2)
         d(1) =| 10|                                      |15|= q(4)
         d(0) =| 11|                                      |14|= q(6)
     not used *| 12|                                      |13|= clr
                 ____________________________________________
```

Entrada d= 1001111

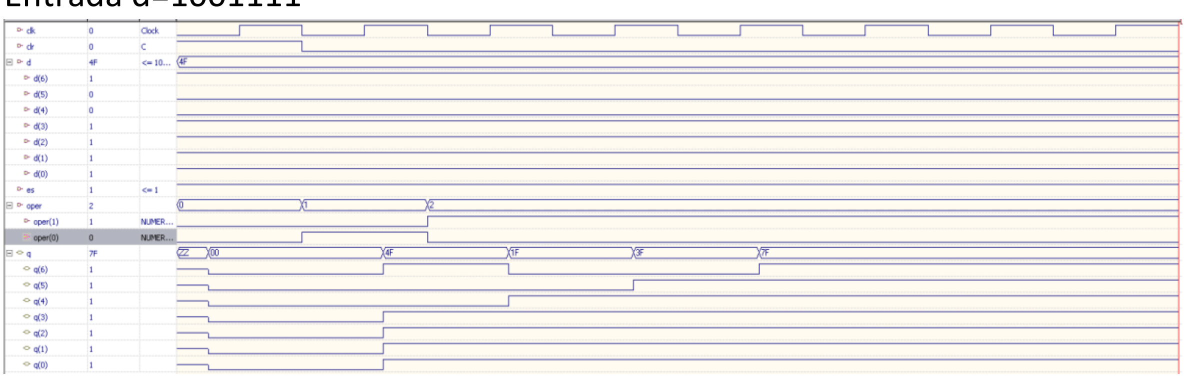
Corrimiento a la derecha



Salida q=1100111, 1100111, 1110011, 1111001, 1111100, 1111110, 1111111

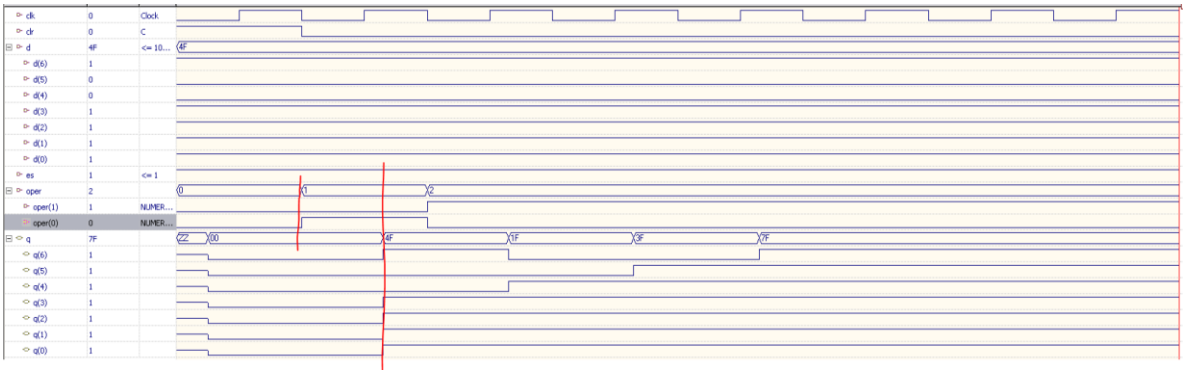
Corrimiento a la izquierda

Entrada d=1001111

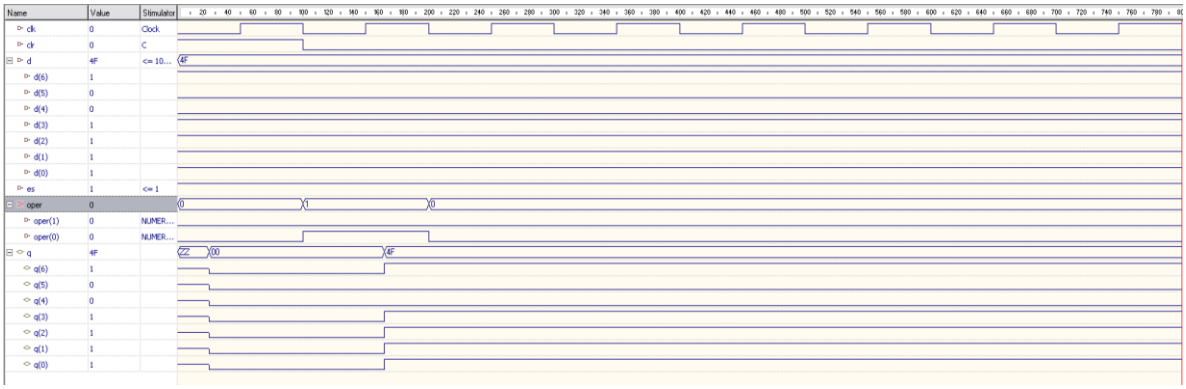


Salida q=1001111, 0011111, 0111111, 111111

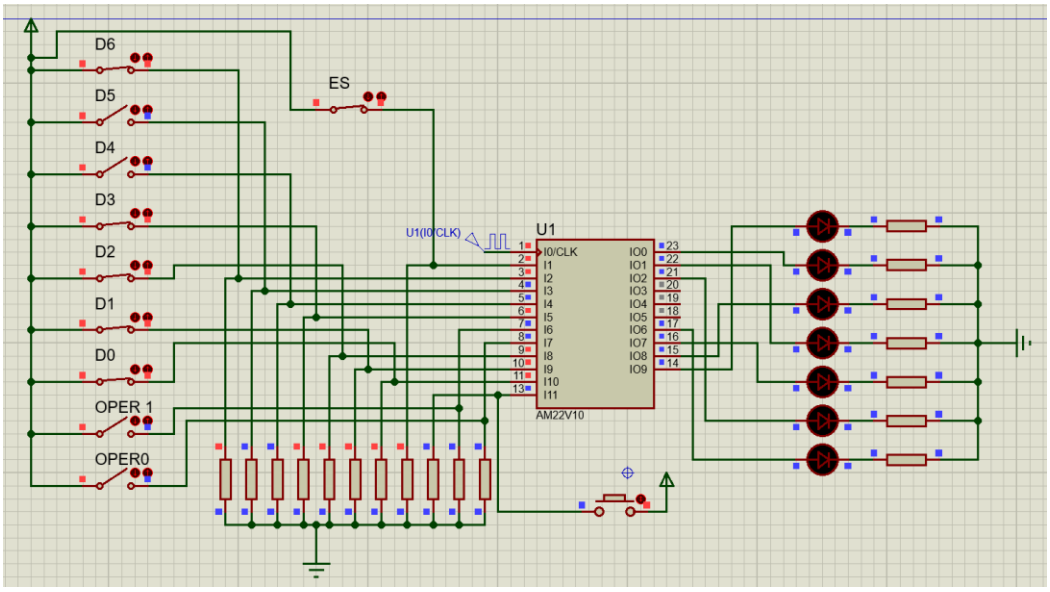
La carga de bits se ve en este punto en ambas simulaciones en el flanco de ascenso



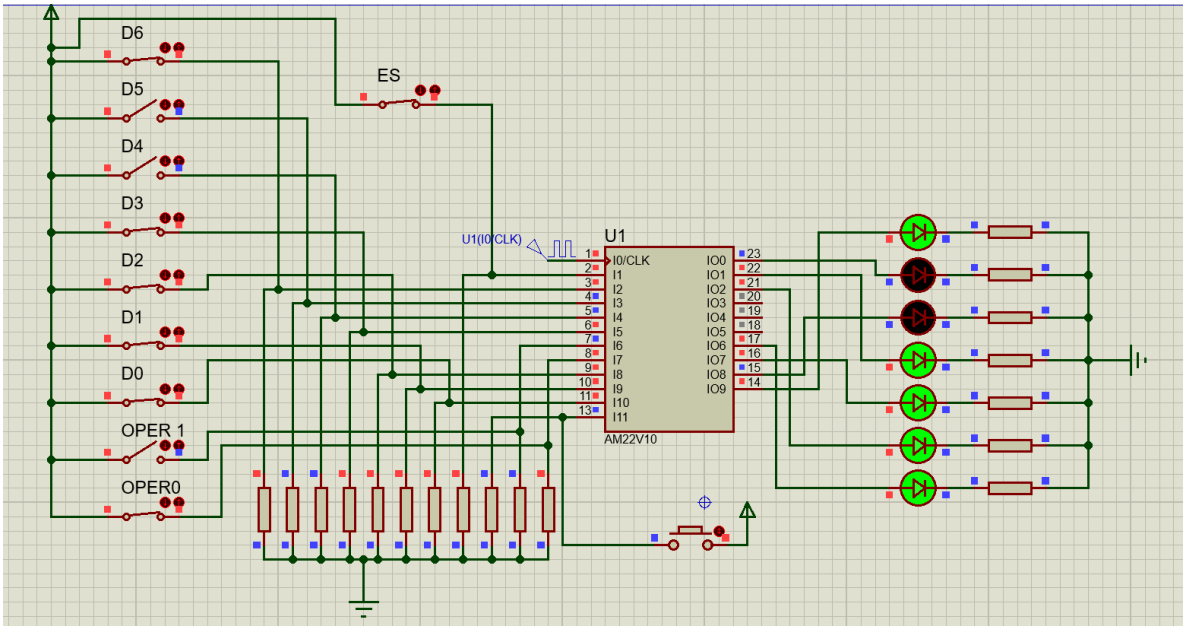
Retención de bits



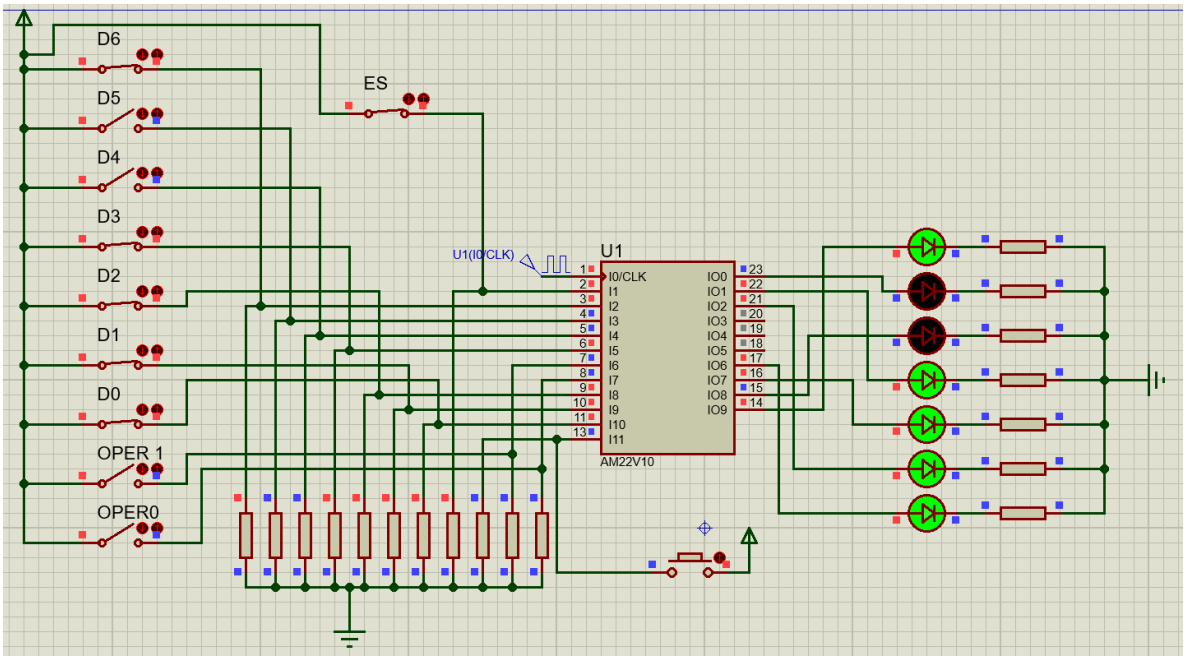
Simulación proteus



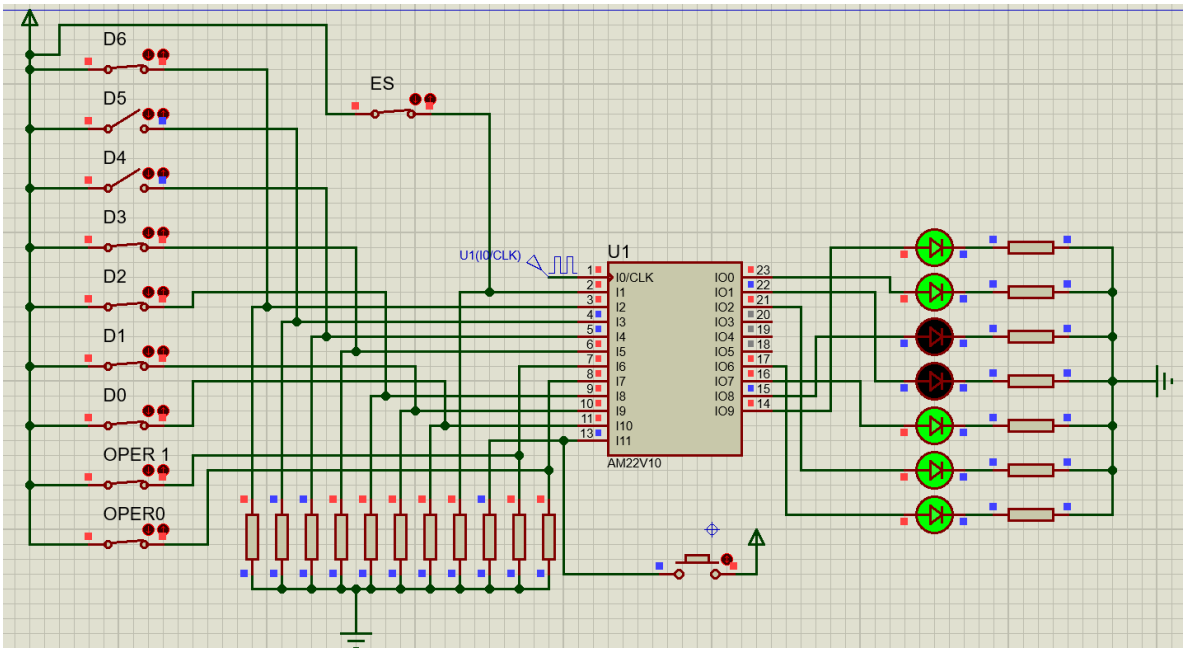
Carga de bits

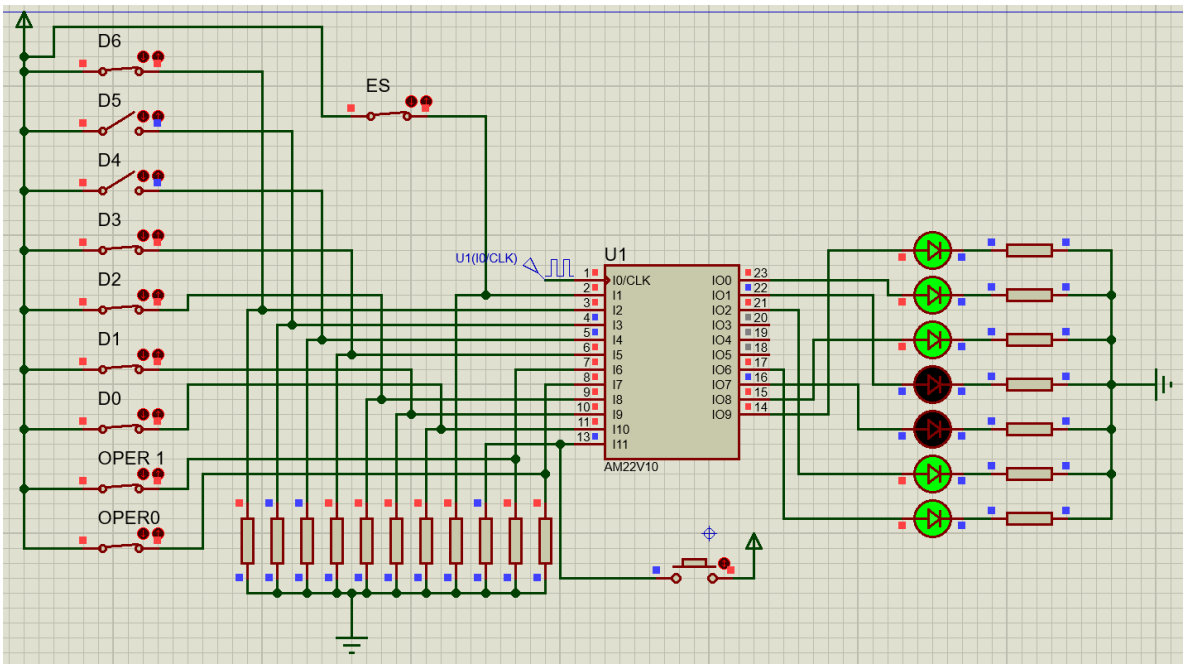


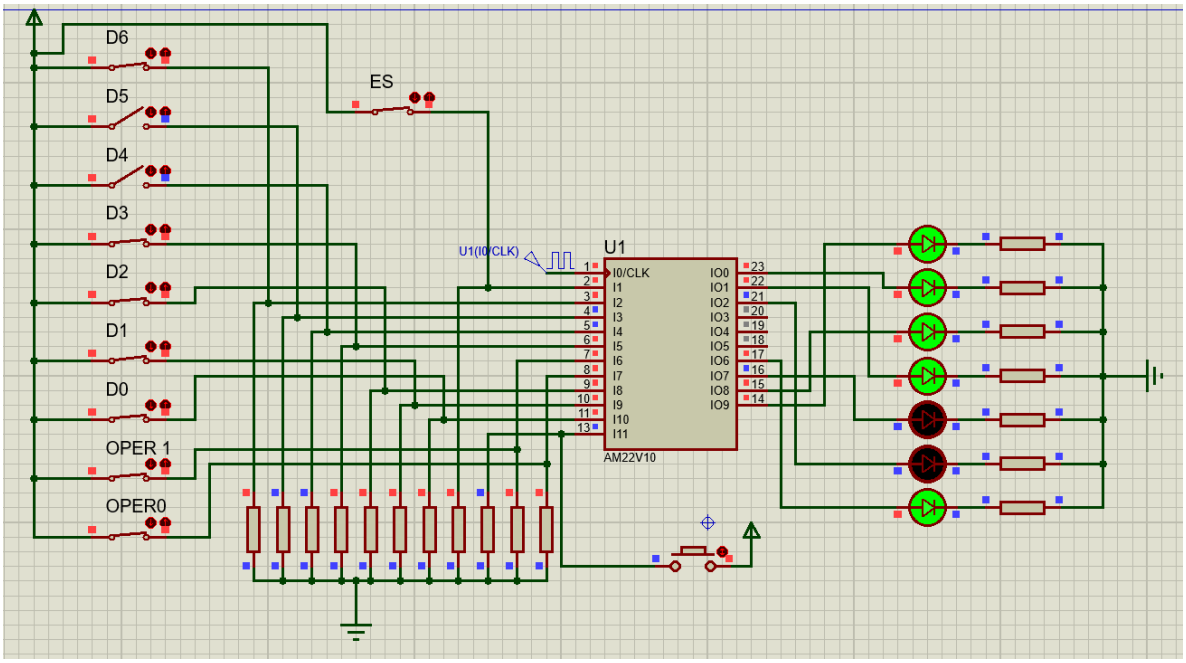
Retención de bits

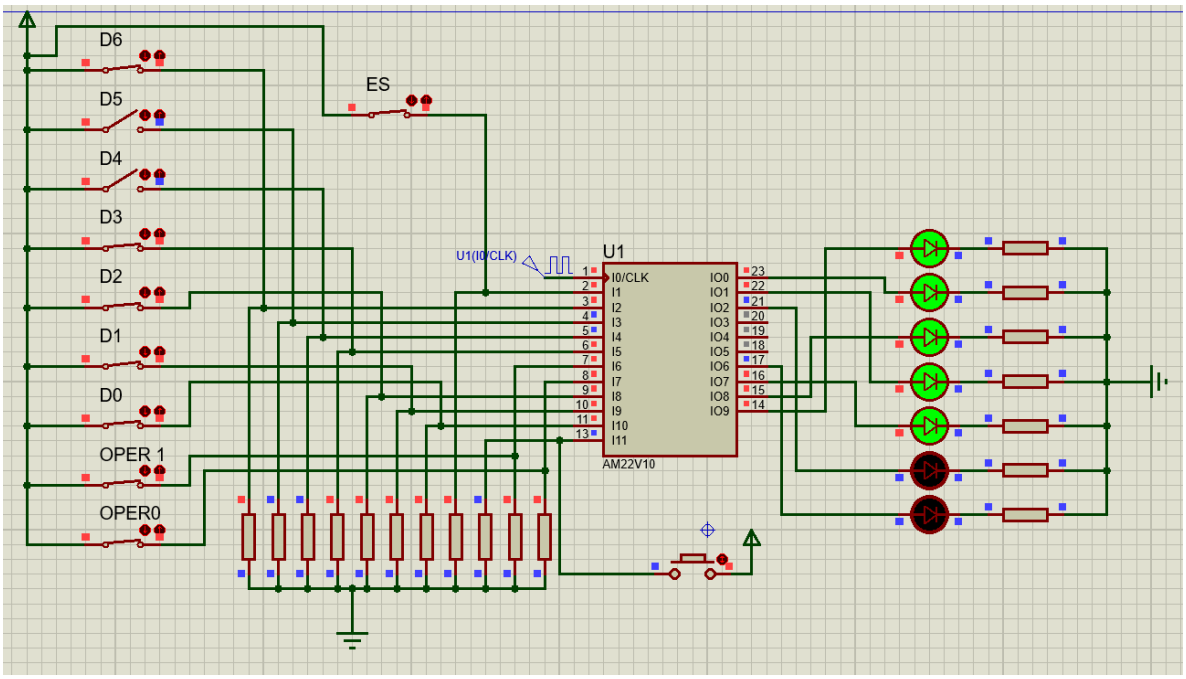


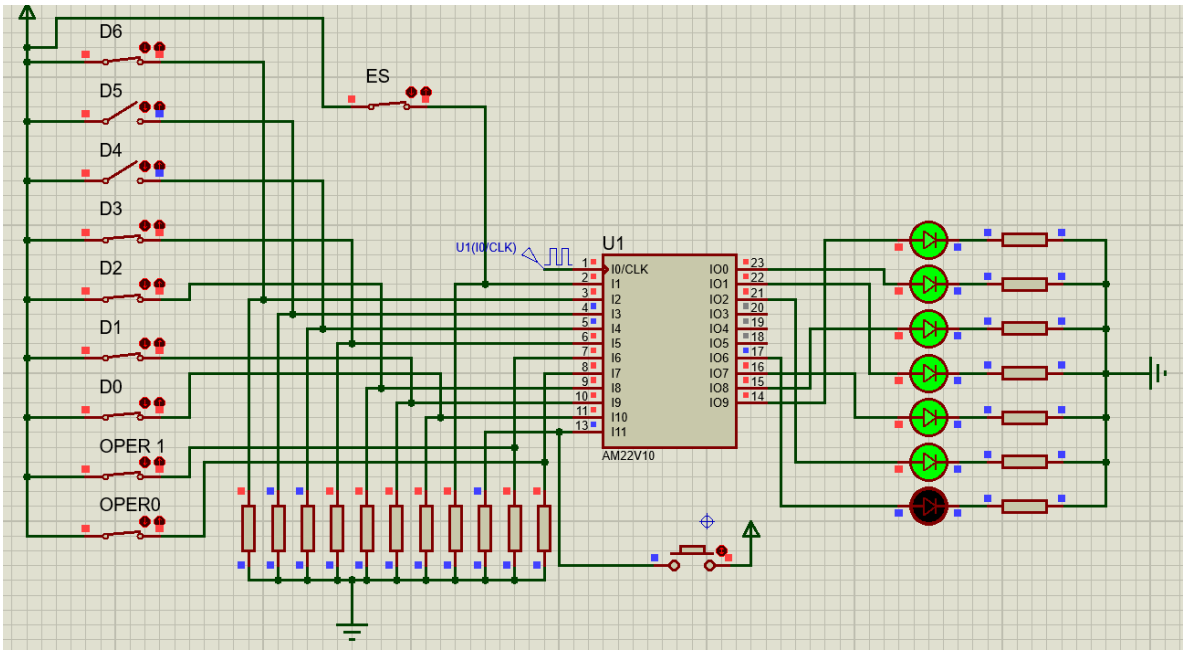
Corrimiento a la derecha

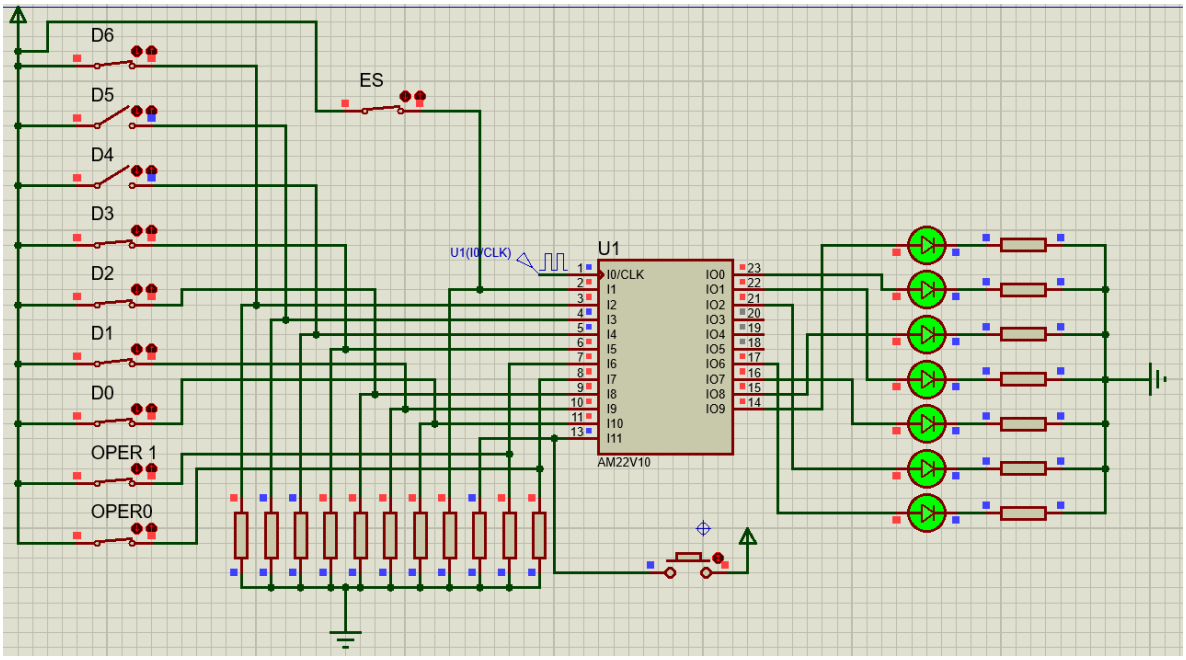




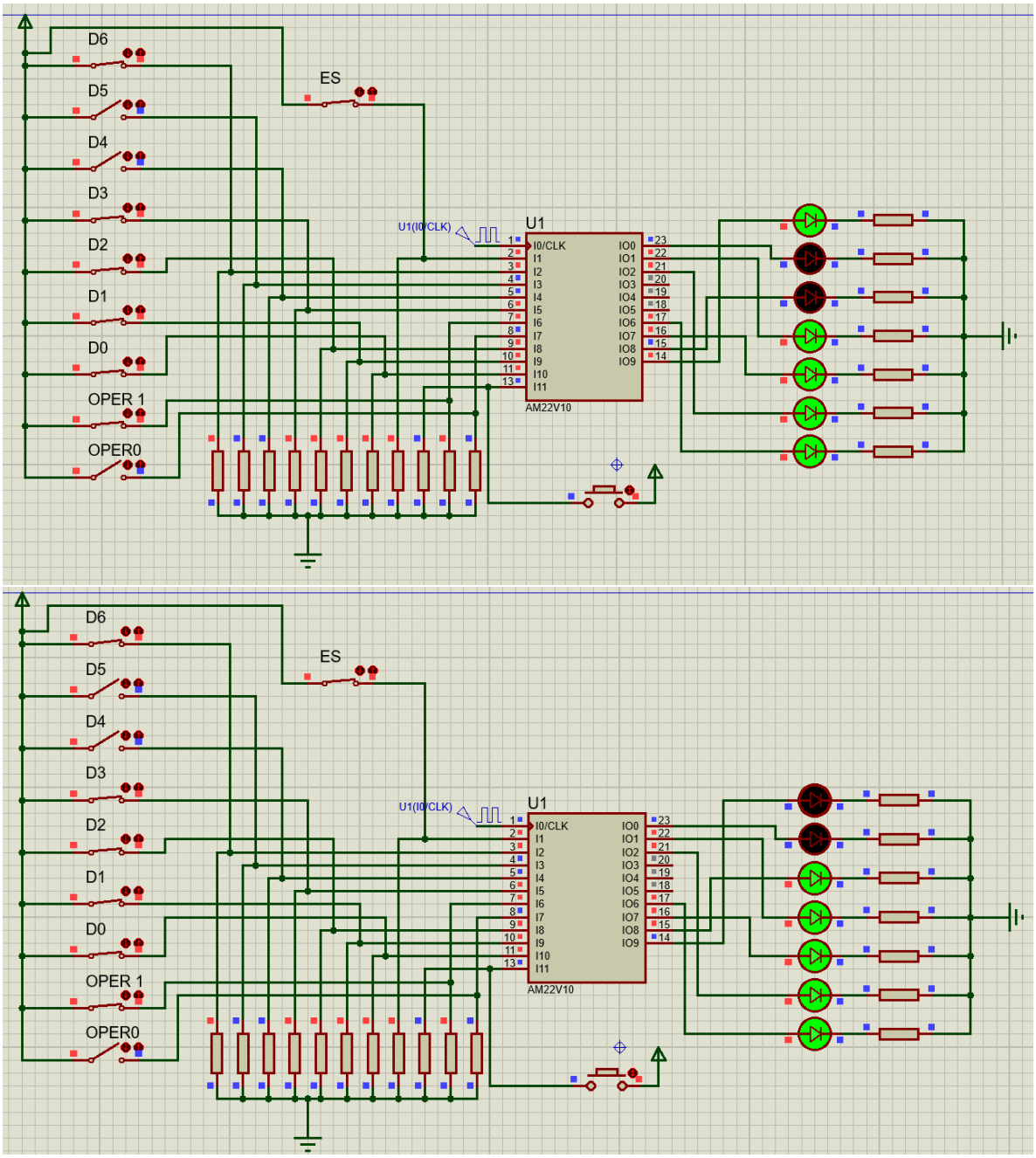

D6
D5
D4
D3
D2
D1
D0
OPER 1
OPER0
ES
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10

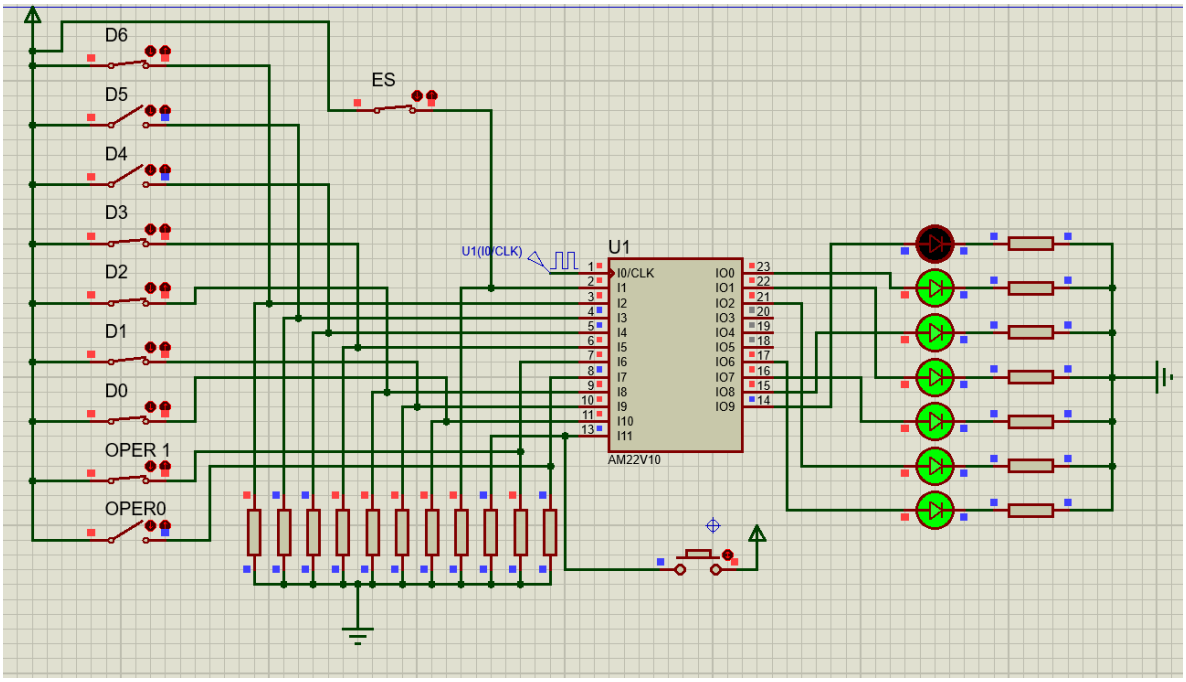

D6
D5
D4
D3
D2
D1
D0
OPER 1
OPER0
ES
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10

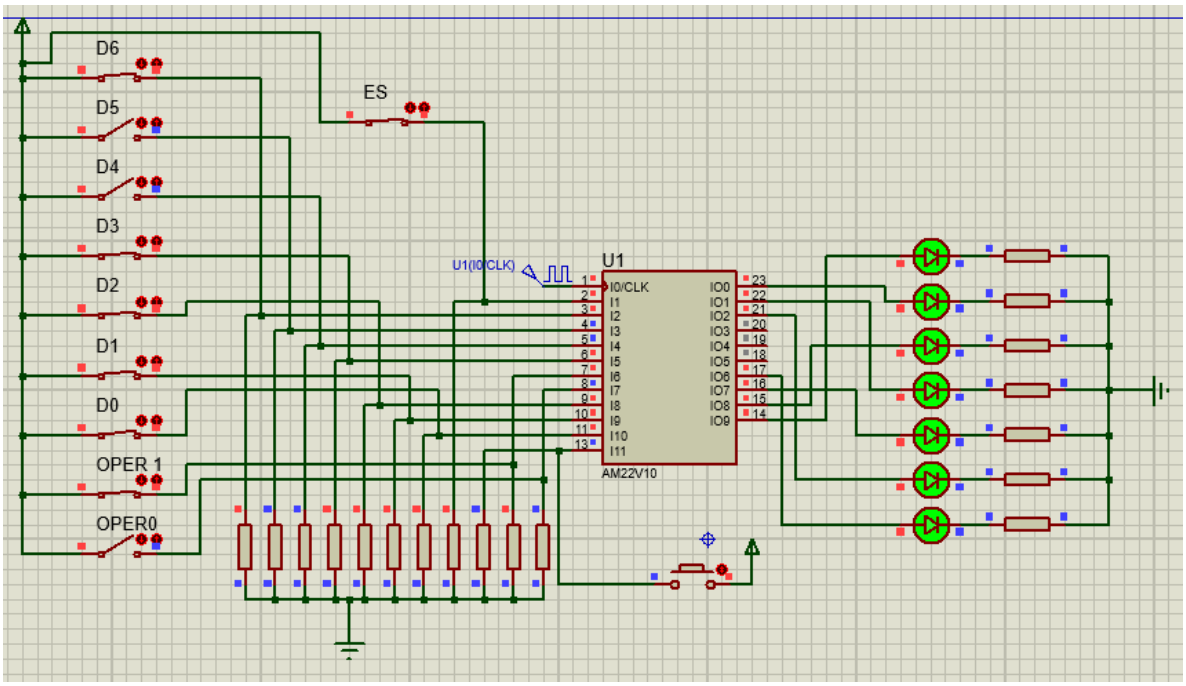

D6
D5
D4
D3
D2
D1
D0
OPER 1
OPER0
ES
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10


D6
D5
D4
D3
D2
D1
D0
OPER 1
OPER0
ES
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10

Corrimiento a la izquierda




D6
D5
D4
D3
D2
D1
D0
OPER 1
OPER0
ES
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10


D6
D5
D4
D3
D2
D1
D0
OPER 1
OPER0
ES
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10