

Córdova Pichardo Francisco Uziel

1- acd

2- c

3- a

4- b

5- bd

6- d

7- abc

8- d

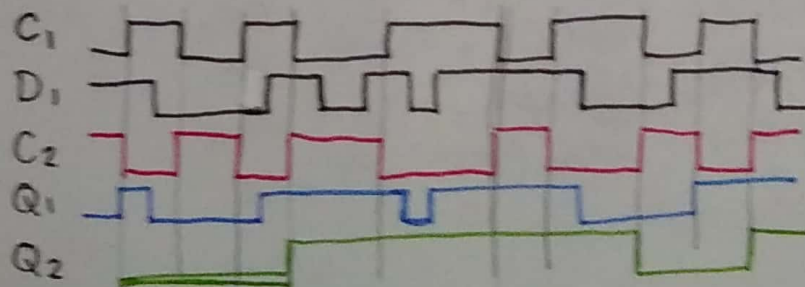
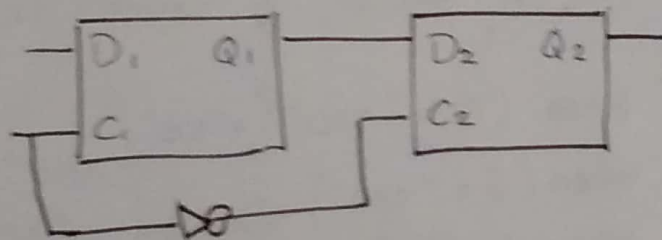
9- c

10- b

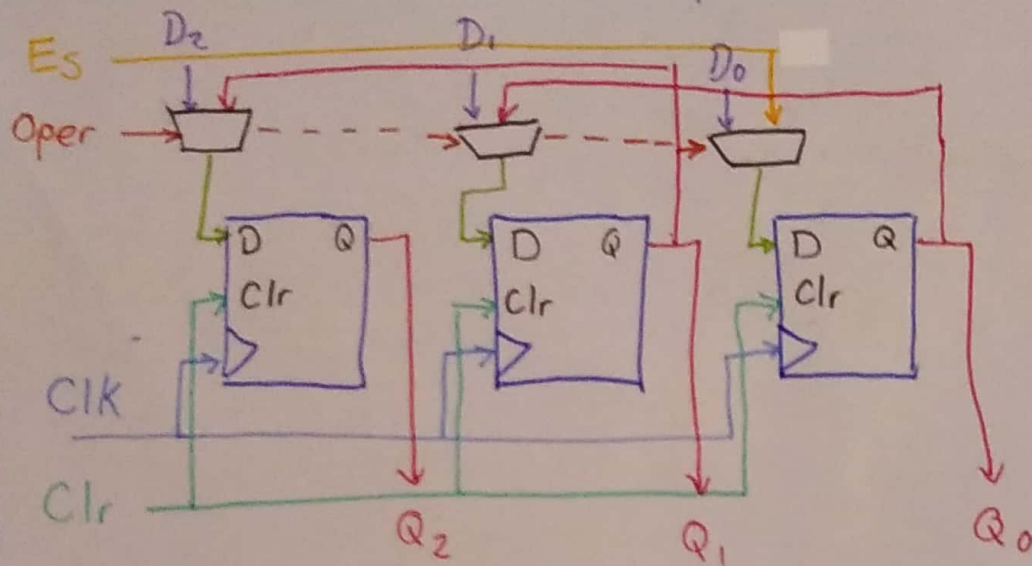
Q (5 pts) C₂

(b) Q₁

(c) Q₂



a) Operacion
 0 Carga
 1 Corrimiento a la izquierda



b) Convertidor de código Anodo si tomamos $Q : \text{std_logic_vector}(2 \text{ downto } 0)$

display <= "0000001" when (Q = "000") else

"1001111" when (Q = "001") else

"0010010" when (Q = "010") else

"0000110" when (Q = "011") else

"1001100" when (Q = "100") else

"0110100" when (Q = "101") else

"0100000" when (Q = "110") else

"0001111" when (Q = "111") else

"0000000";

```

library ieee;
use ieee.std_logic_1164.all;
entity Examen is port
(
  es Oper, clk, clr : in std_logic;
  D : in std_logic_vector(2 downto 0);
  display : out std_logic_vector(6 downto 0)
);
end Examen;

```

```

architecture A_Examen of Examen is
  signal Q : std_logic_vector(3 downto 0);
begin
  process (clk, clr)
  begin
    if (clr = '1') then
      Q <= "000";
    elsif (rising_edge(clk)) then
      if (oper = '0') then
        Q <= D;
      elsif (oper = '1') then
        for i in 0 to 2 loop
          if (i > 0) then
            Q(i) <= Q(i-1);
          end if;
        end loop;
      end if;
    end if;
  end process;
end architecture A_Examen;

```

-- Convertidor de código

-- Convertidor de Código

```
display <= "0000001" when (Q = "000") else  
"1001111" when (Q = "001") else  
"0010010" when (Q = "010") else  
"0000110" when (Q = "011") else  
"1001100" when (Q = "100") else  
"0110100" when (Q = "101") else  
"0100000" when (Q = "110") else  
"0001111" when (Q = "111") else  
"0000000";
```

end A Examen;