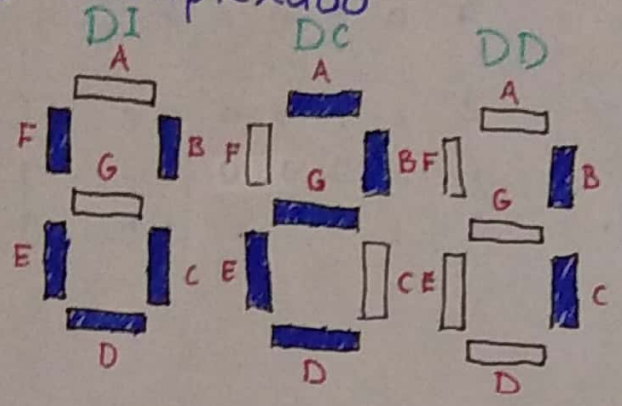
Practica 5 Córdova Pichardo Francisco Uziel

Mensaje multiplexado



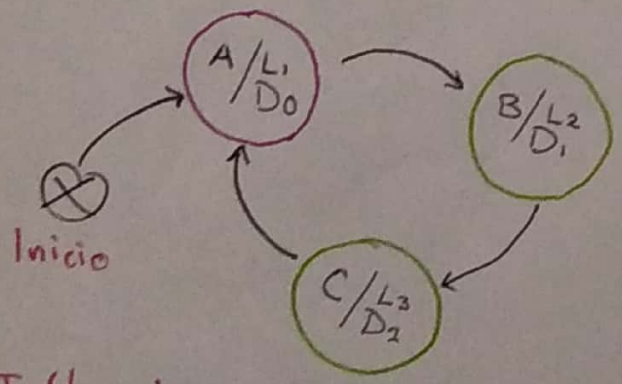
= UZI

F = 90 Hz

$L_1 = I$
$L_2 = Z$
$L_3 = U$

t_1	-	-	DD-L_1
t_2	-	DC-L_2	-
t_3	DI-L_3	-	-
t_4	-	-	DD-L_4

Diagrama de estados:



Edo_Act	Edo_Sig
A	B
B	C
C	A

Display

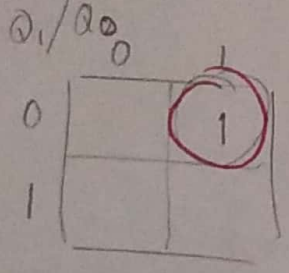
Tabla de estados: Nota: Catodo Comun enciende en 1 ∴ Catodo=0

Edo_ACT	Edo_SIG	DI	DC	DD	a	b	c	d	e	f	g
A	B	1	1	0	0	1	1	0	0	0	0
B	C	1	0	1	1	1	0	1	1	0	1
C	A	0	1	1	0	1	1	1	1	1	0

Tabla de estados codigo gray

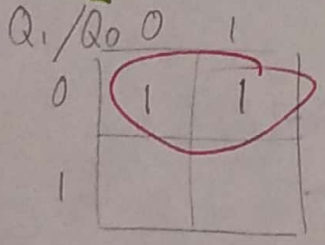
Edo_Act		Edo_Sig		DI	DC	DD	a	b	c	d	e	f	g	D_1	D_2
Q_1	Q_0	Q_1^+	Q_0^+												
0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	1
0	1	1	1	1	0	1	1	1	0	1	1	0	1	1	1
1	1	0	0	0	1	1	0	1	1	1	1	1	0	0	0

D_1

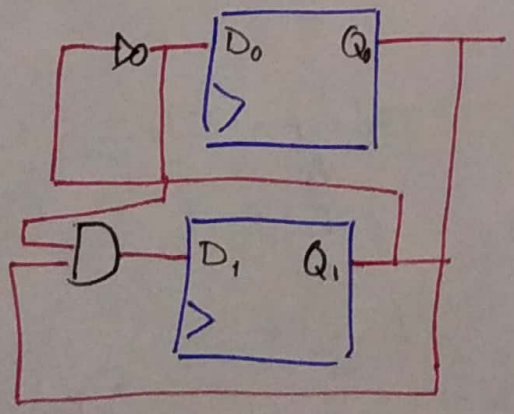


$D_1 = \overline{Q_1} Q_0$

D_2



$D_0 = \overline{Q_1}$

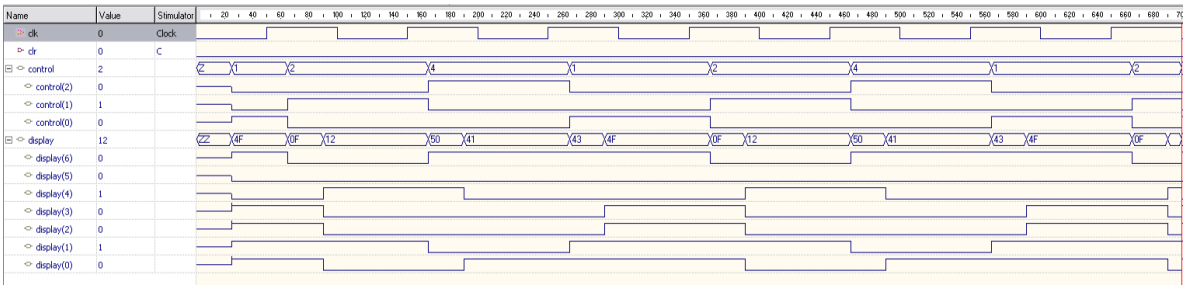


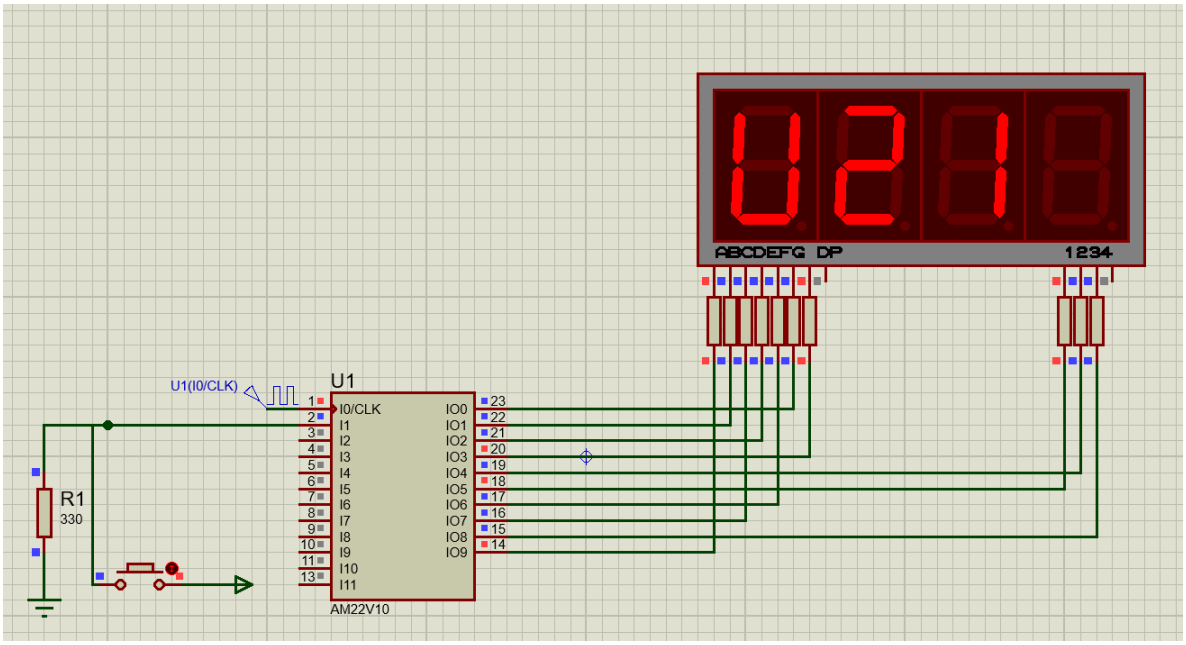
Practica 5

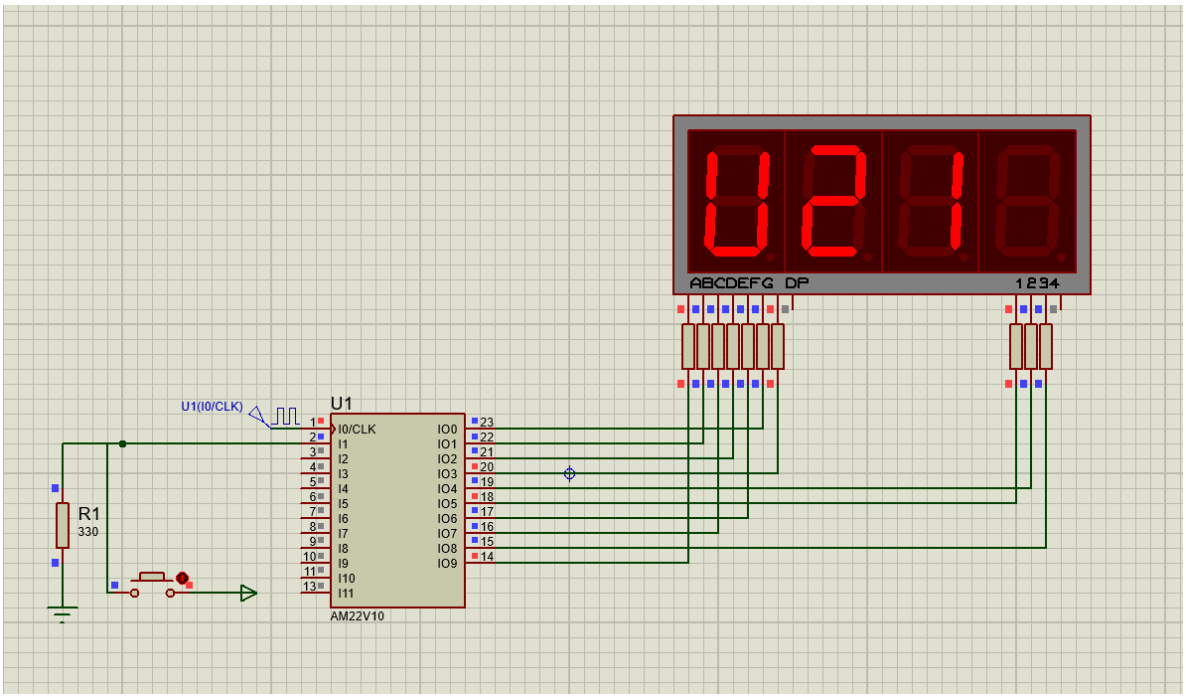
```
 1 library ieee;
 2 use ieee.std_logic_1164.all;
 3
 4 entity P5Mensaje is port
 5 (
 6     clk, clr : in std_logic;
 7     control : out std_logic_vector(2 downto 0);
 8     display : out std_logic_vector(6 downto 0)
 9 );
10 end P5Mensaje;
11
12 architecture AP5Mensaje of P5Mensaje is
13 signal aux : std_logic_vector (9 downto 0);
14 begin
15     process(clk, clr)
16     begin
17         if(clr = '1')then
18             aux <= "0011001111";
19         elsif(rising_edge(clk))then
20             case aux is
21                 when "0011001111" => aux <= "0100010010";
22                 when "0100010010" => aux <= "1001000001";
23                 when "1001000001" => aux <= "0011001111";
24                 when others => aux <= "0000000000";
25             end case;
26         end if;
27     end process;
28
29     control <= aux(9 downto 7);
30     display <= aux(6 downto 0);
31 end AP5Mensaje;
```

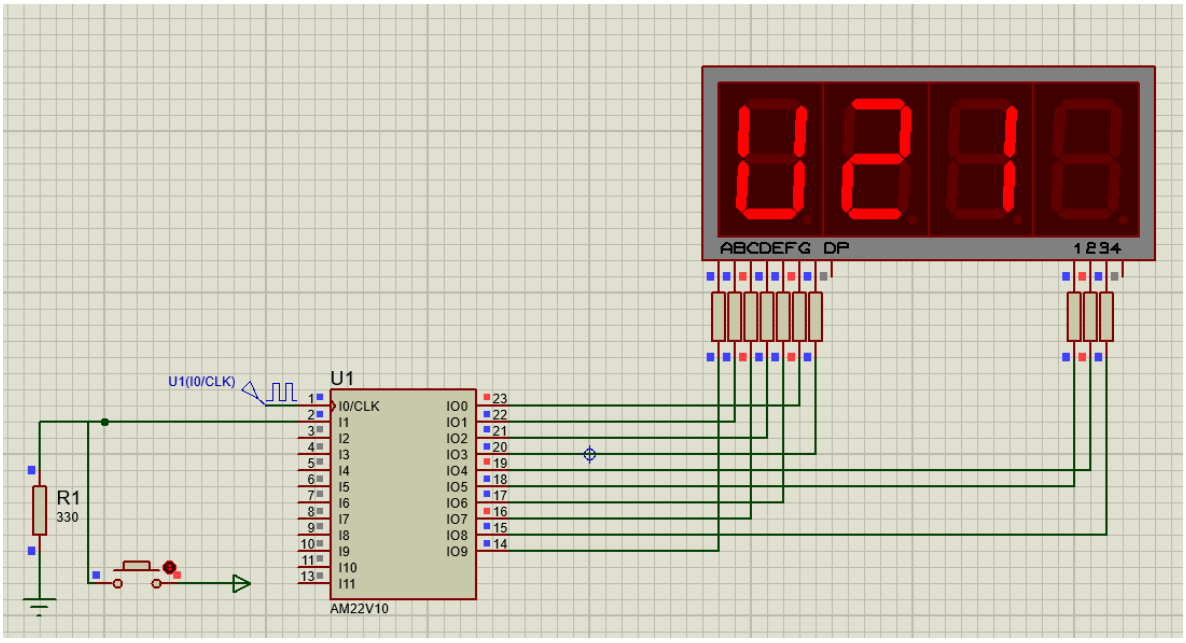
C22V10

```
      clk =|  1|                                    |24|* not used
      clr =|  2|                                    |23|= display(1)
not  used *|  3|                                    |22|= display(5)
not  used *|  4|                                    |21|= display(3)
not  used *|  5|                                    |20|= display(0)
not  used *|  6|                                    |19|= control(1)
not  used *|  7|                                    |18|= control(2)
not  used *|  8|                                    |17|= display(2)
not  used *|  9|                                    |16|= display(4)
not  used *|10|                                     |15|= control(0)
not  used *|11|                                     |14|= display(6)
not  used *|12|                                     |13|* not used
```






U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10
R1
330
ABCDEFG DP
1234


U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10
R1
330
ABCDEFG DP
1234