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## Practica 4

```
1 library ieee;
 2 use ieee.std logic 1164.all;
 3
 4 entity PDetector is port
 5 (
       E, clk, clr : in std logic;
 6
       display : out std logic vector(6 downto 0)
 8);
 9 end PDetector;
10
11 architecture ADetector of PDetector is
12 signal S : std_logic;
13 signal q : std_logic_vector (1 downto 0);
14 begin
       process(clk, clr)
16
      begin
           if(clr = '1') then
17
18
               q <= "00";
               s <= '0';
19
20
           elsif (rising edge(clk)) then
21
               q(0) \le ((not(q(1))) and(not(q(0))) and(E)) or((q(1)) and(not(q(0))) and(not(E)));
               q(1) \ \leftarrow \ ((not(q(1)))and(q(0))and(E))or((q(1))and(not(q(0))));
22
23
           end if:
24
      end process;
25
       S \ll q(1) and (q(0)) and (E);
       display <= "1001111" when (S='1') else
26
                   "0000001";
27
28 end ADetector;
```

## C22V10

```
|24| * not used
     clk =| 1|
       e = | 2|
                                                    |23| = (q 0)
     clr =| 3|
                                                    |22|= display(4)
not used *| 4|
                                                    |21|= display(2)
not used *| 5|
                                                    |20|= display(0)
not used *| 6|
                                                    |19| * not used
not used *| 7|
                                                    |18|= display(6)
not used *| 8|
                                                    |17|= display(1)
not used *| 9|
                                                    |16|= display(3)
not used *|10|
                                                    |15|= display(5)
not used *|11|
                                                    |14| = (q 1)
not used *|12|
                                                    |13|* not used
```















