

## Córdova Pichardo Francisco Uziel

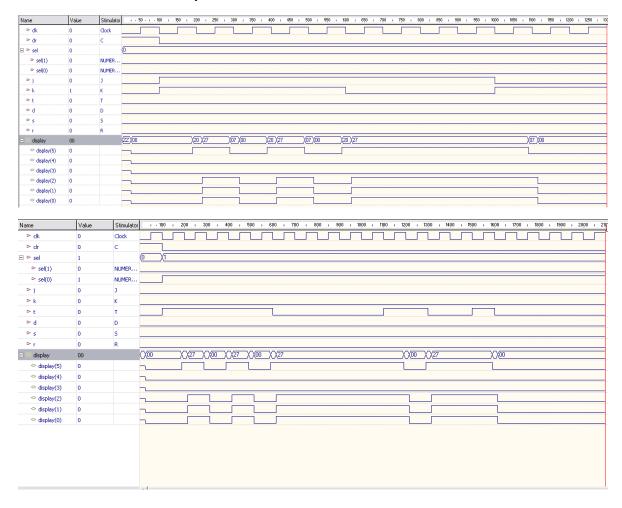
## Practica 2

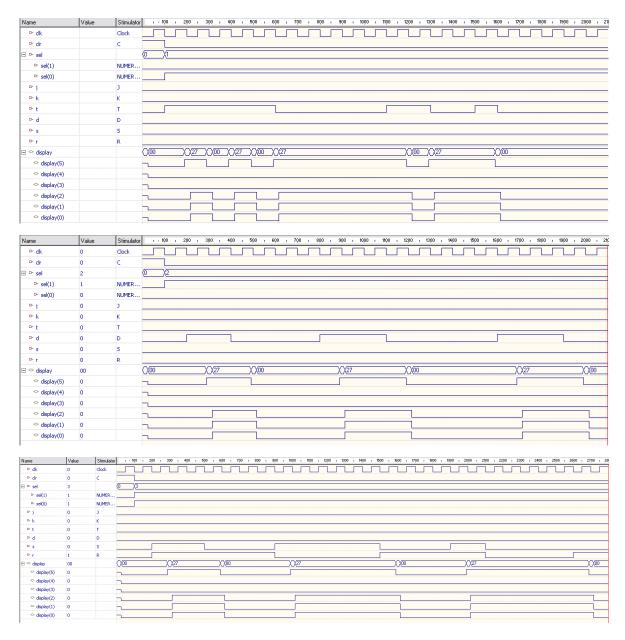
```
1 library ieee;
2 use ieee.std_logic_1164.all;
4 entity Practica2 is port
5 (
      j, k , t, d, s, r, clk, clr : in std logic;
      sel : in std logic vector(1 downto 0);
      display : out std logic vector (5 downto 0)
9);
10 end Practica2;
12 architecture APractica2 of Practica2 is
13 signal q, jk, tsalida, sr, mux : std logic;
14 begin
15 process(clk,clr)
16 begin
17 -- reset, señal de control asicrona
     if (clr = '1') then
18
          q <= '0';
19
          jk <= '0';
20
          tsalida <= '0';
21
22
          sr <= '0';
23
     elsif (clk'event and clk = '1') then
24
           q \ll d;
25
           jk <= ((not(k))and(jk))or((j)and (not(jk)));</pre>
26
          tsalida <= ((not(t))and(tsalida))or((not(tsalida))and(t));
27
          sr <= ((not(r))and(sr))or(s);</pre>
28
      end if:
29 end process;
30 -- Mux
31 mux <= jk when(sel = "00") else
      tsalida when (sel = "01") else
      q when (sel = "10") else
33
34
      sr;
35 -- Display
36 display <= "100111" when (mux = '1') else
37
                      "000000";
38 end APractica2;
```

## C22V10

clk	=  1	24 *	not used
t	=   2	23 =	(tsalida)
s	=  3	22 =	(jk)
r	=   4	21 =	display(4)
sel(1)	=  5	20 =	display(2)
sel(0)	=  6	19 =	display(0)
k	=  7	18 =	display(1)
j	=  8	17 =	display(3)
d	=  9	16 =	(q)
clr	=   10	15 =	(sr)
not used	* 11	14 =	display(5)
not used	* 12	13 *	not used

## Simulación en Galaxy





Simulación en proteus

