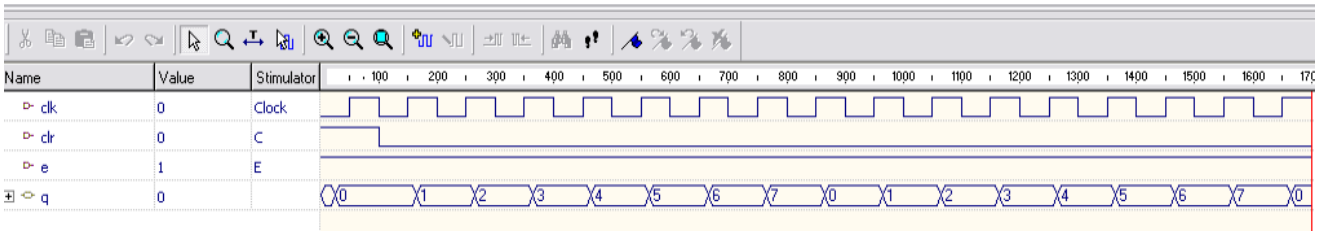
Córdova Pichardo Francisco Uziel

Practica 6

```
 1 library ieee;
 2 use ieee.std_logic_1164.all;
 3 use ieee.std_logic_arith.all;
 4 use ieee.std_logic_unsigned.all;
 5
 6 entity contador is port
 7 (
 8     clk, e, clr : in std_logic;
 9     q : out std_logic_vector (2 downto 0)
10 );
11 end contador;
12
13 architecture aContador of contador is
14 begin
15     process(clk,clr)
16     variable aux : std_logic;
17     variable d : std_logic_vector(2 downto 0);
18     begin
19         if(clr = '1')then
20             q <= "000";
21             d:=q;
22         elsif (clk'event and clk = '1')then
23             d:=q;
24             if(e='1')then
25                 for i in 0 to 2 loop
26                     aux := e;
27                     if(i=0)then
28                         q(i)<= d(i)xor e;
29                     else
30                         for j in 0 to i-1 loop
31                             aux := aux and d(j);
32                         end loop;
33                         q(i) <= d(i) xor aux;
34                     end if;
35                 end loop;
36             end if;
37         end if;
38     end process;
39 end aContador;
40
```

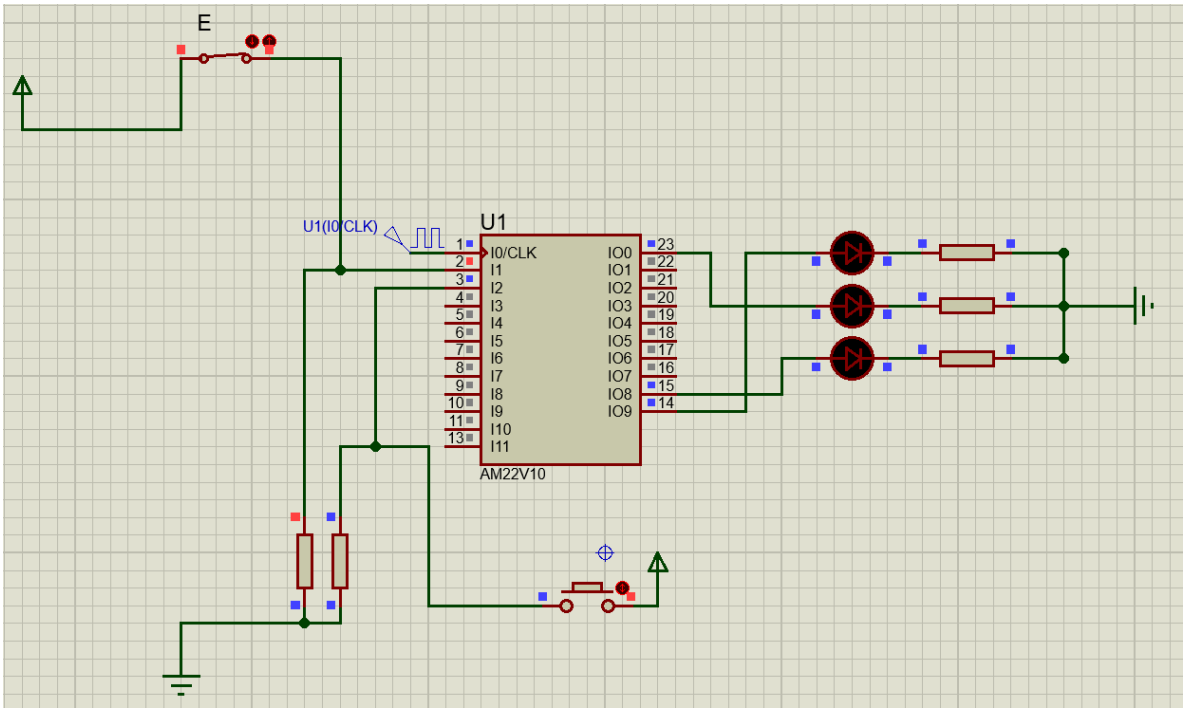
Simulación Galaxy

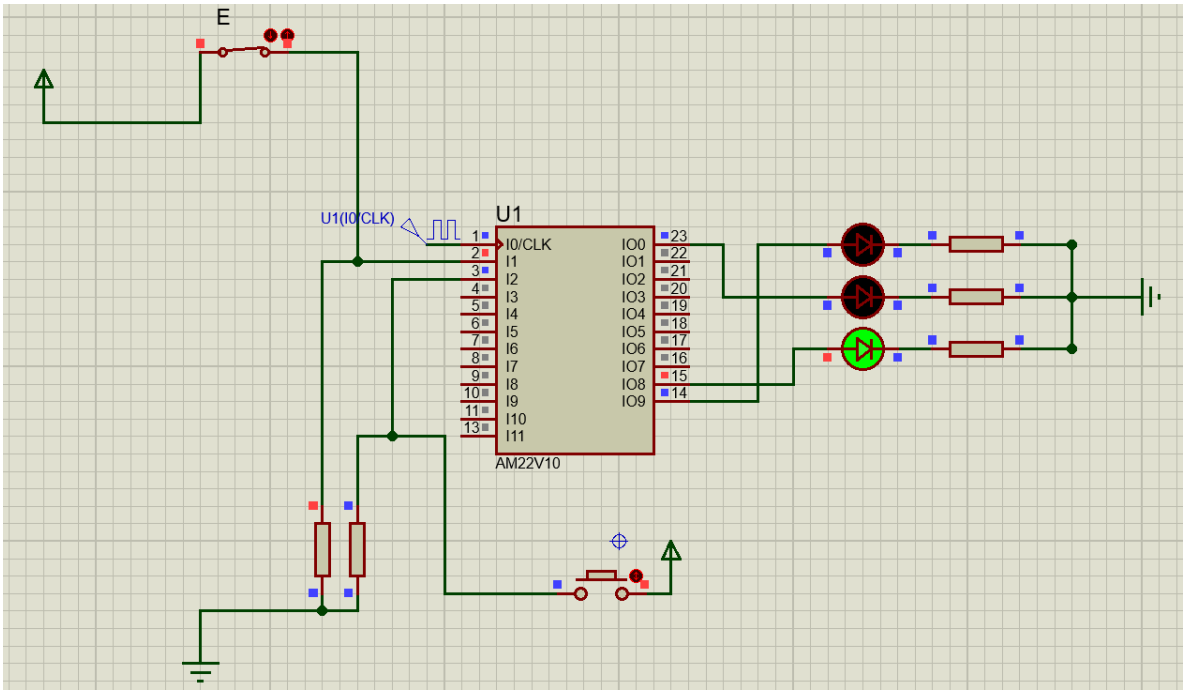


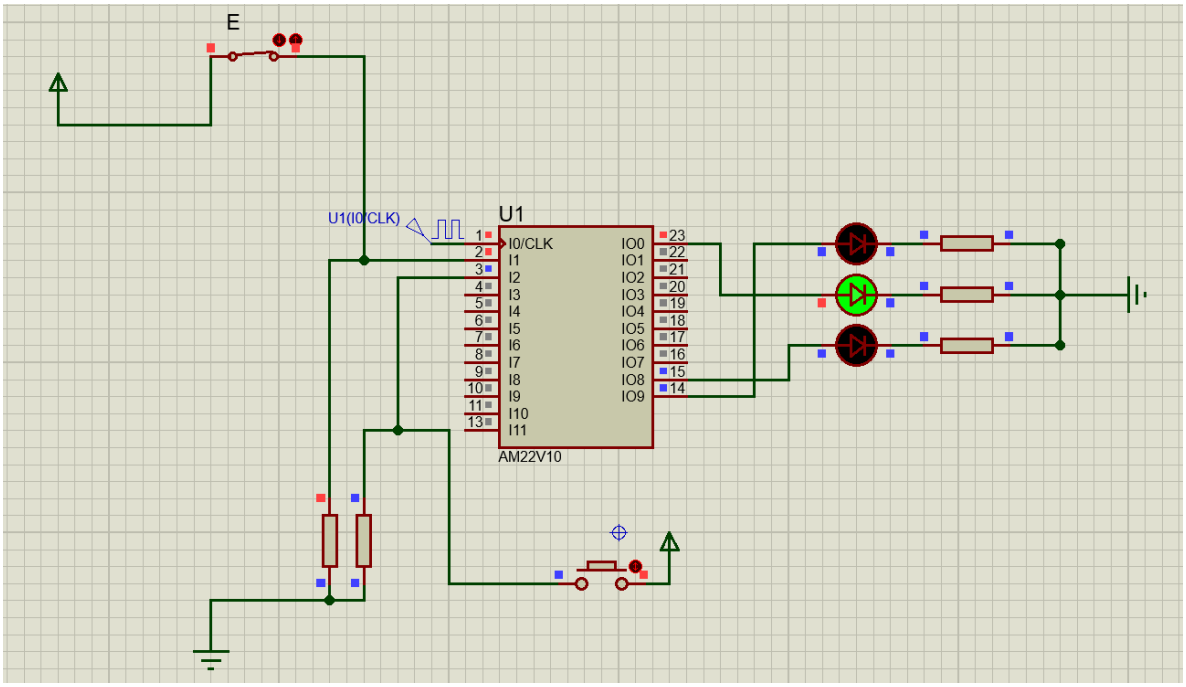
C22V10

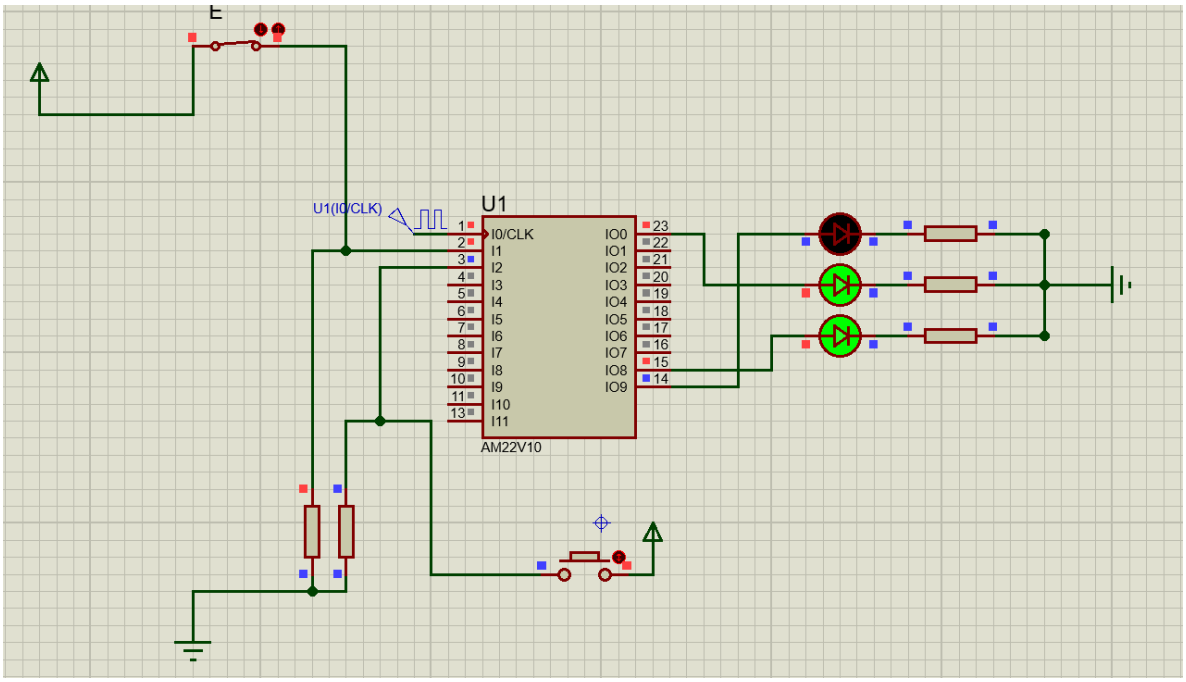
clk =	1	24	* not used
e =	2	23	= q(1)
clr =	3	22	* not used
not used *	4	21	* not used
not used *	5	20	* not used
not used *	6	19	* not used
not used *	7	18	* not used
not used *	8	17	* not used
not used *	9	16	* not used
not used *	10	15	= q(0)
not used *	11	14	= q(2)
not used *	12	13	* not used

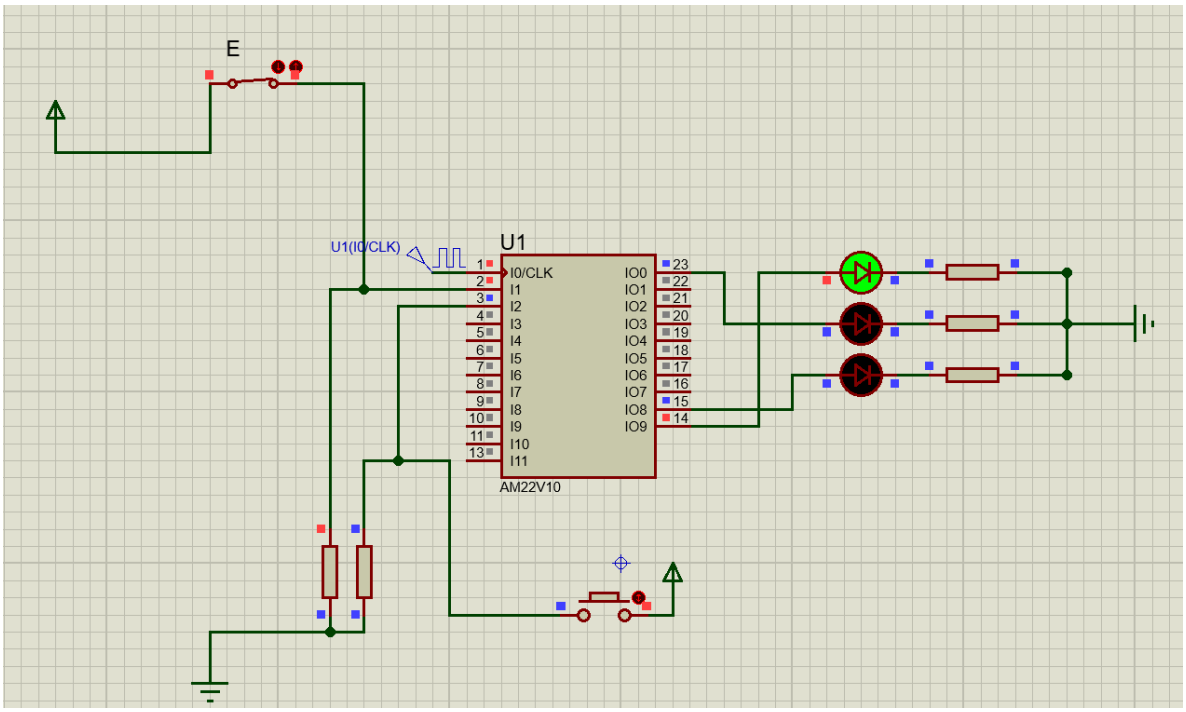
Simulación Proteus

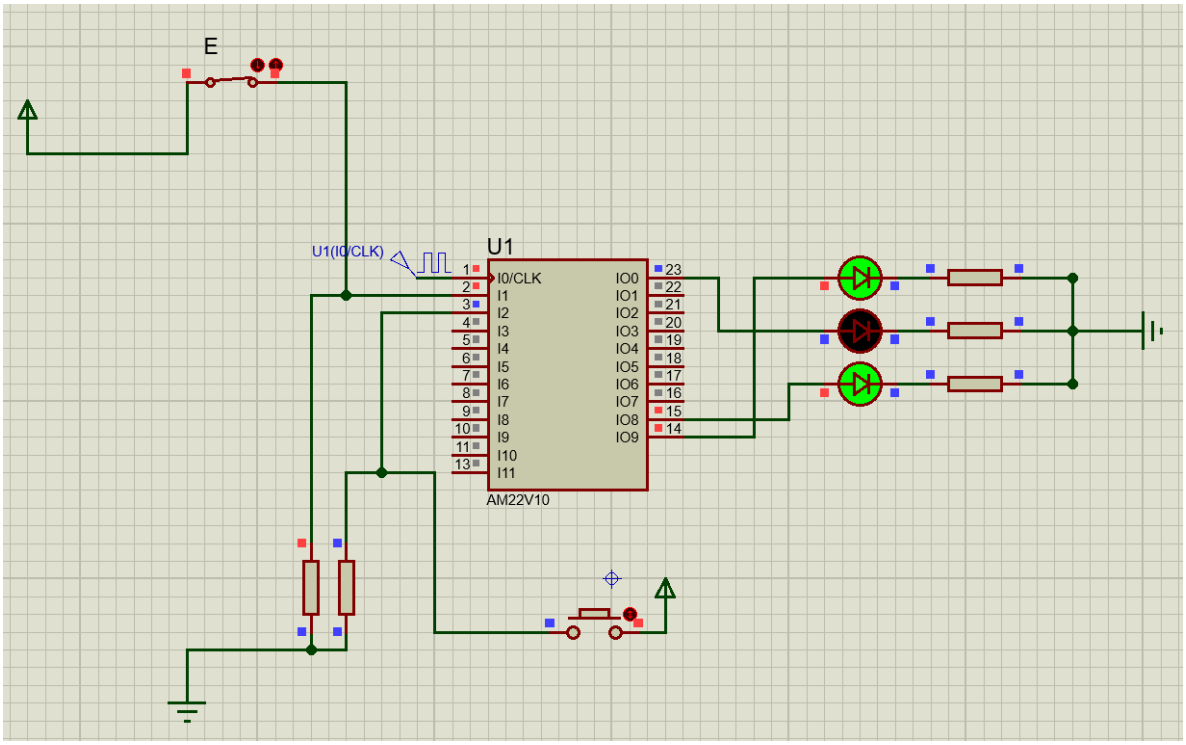


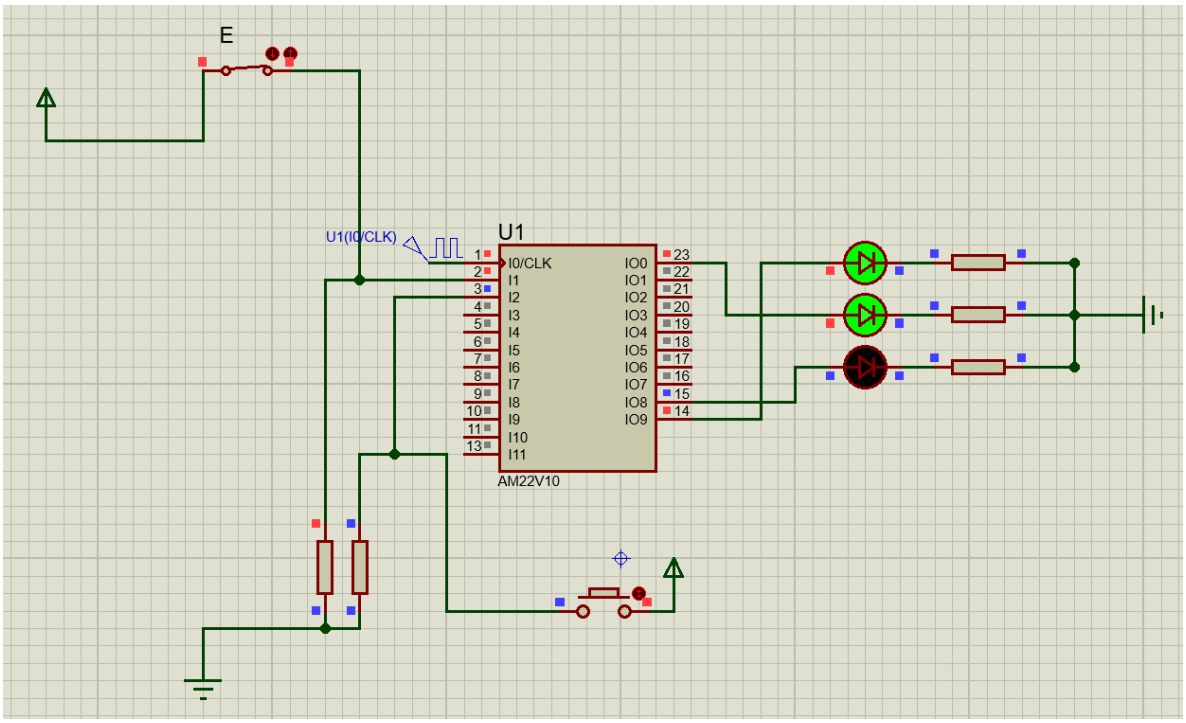

E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10

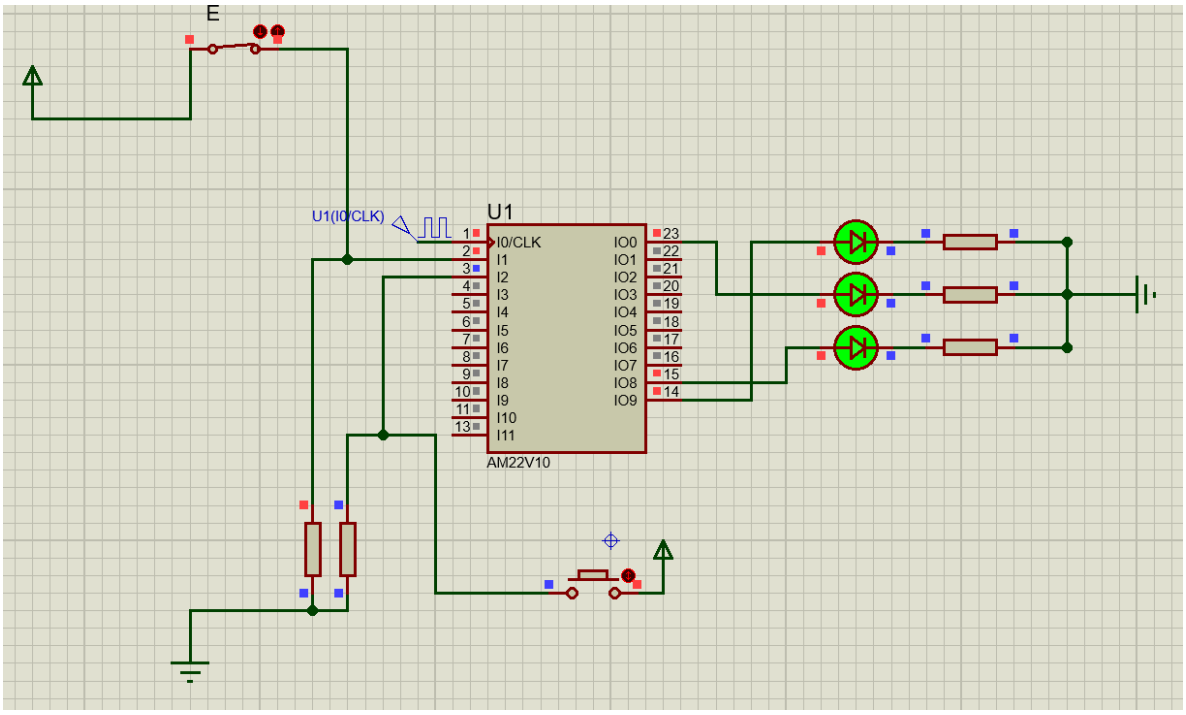

E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10

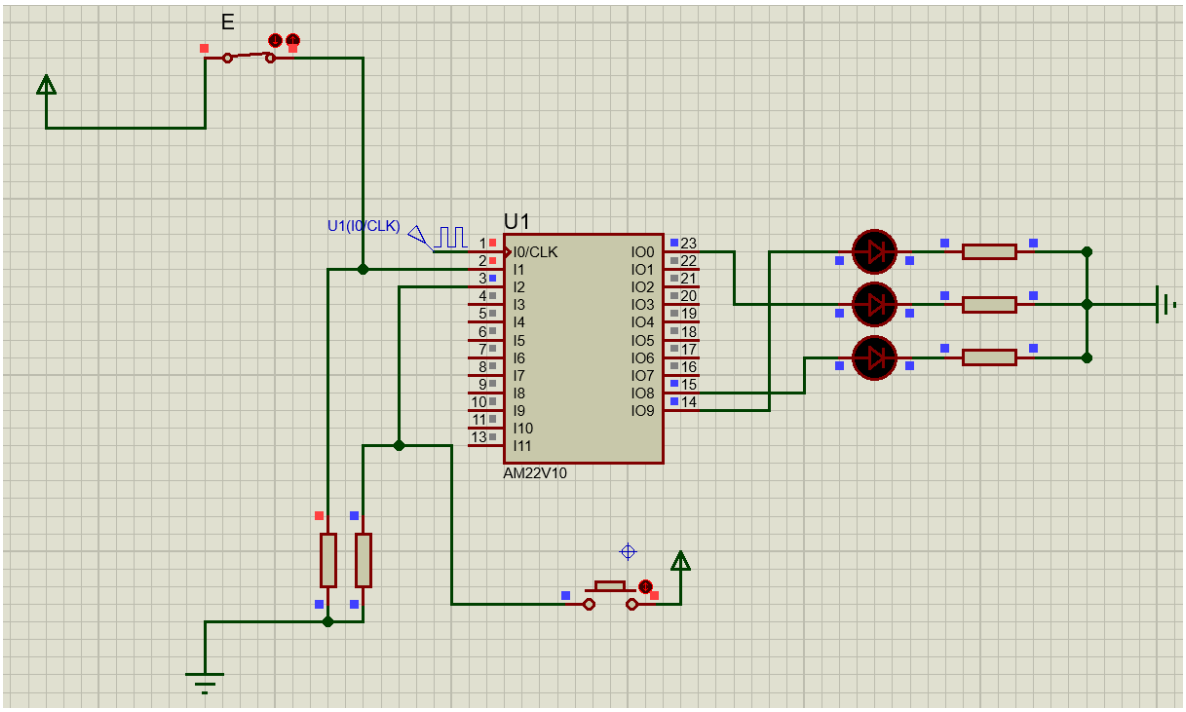

E
U1(IO/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10


E
U1(IO/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10


E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10

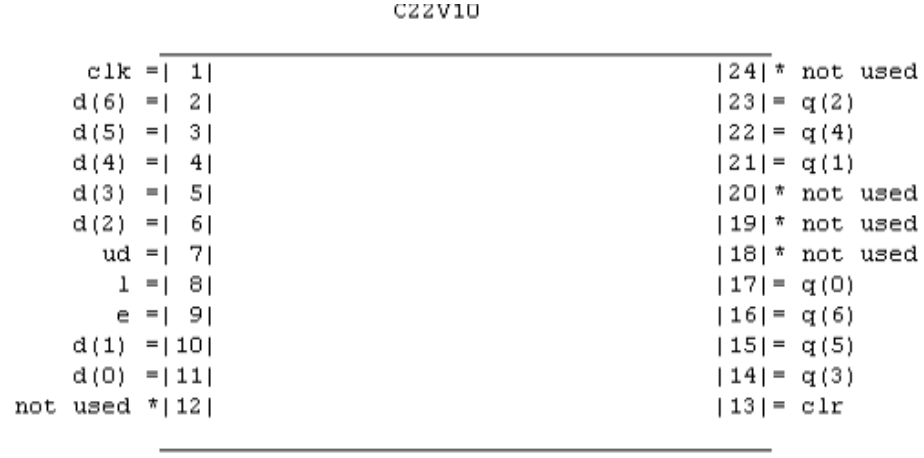

E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10

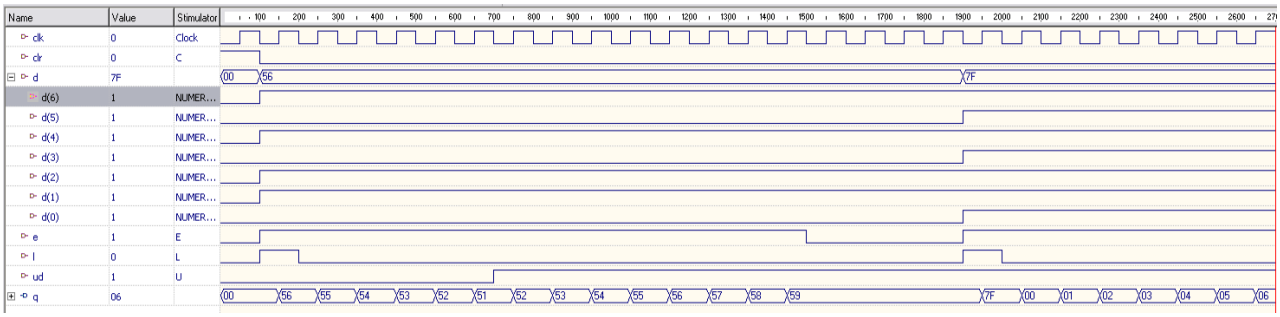

E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10

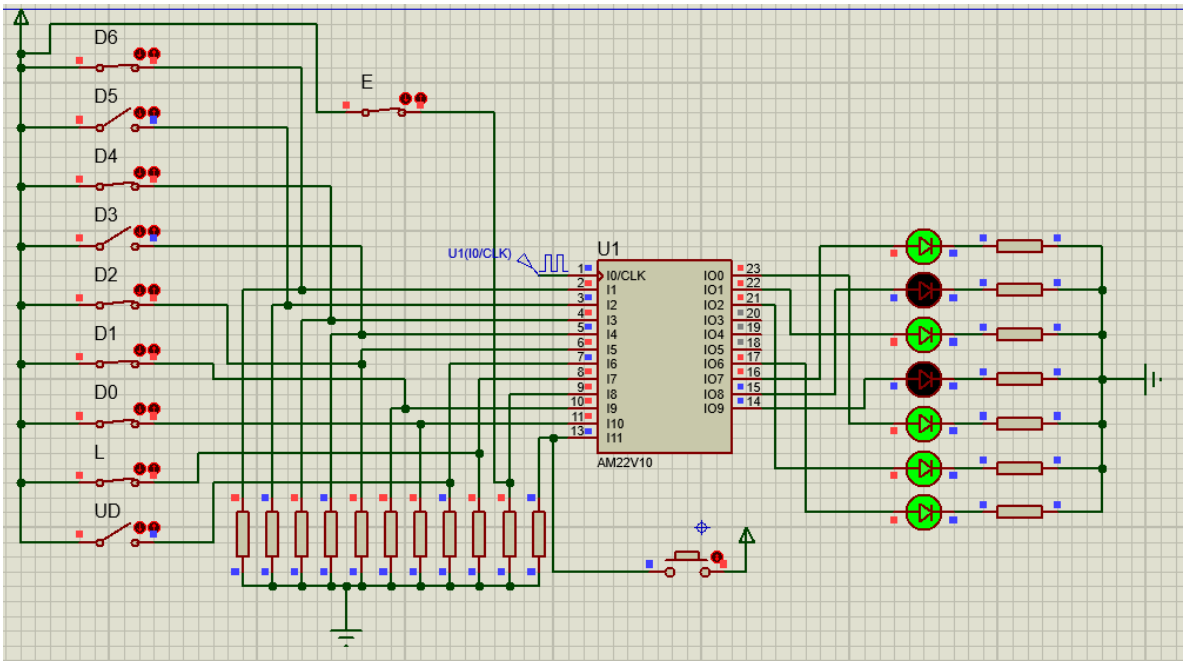

E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10

Parte 2

```
 1 library ieee;
 2 use ieee.std_logic_1164.all;
 3 use ieee.std_logic_arith.all;
 4 use ieee.std_logic_unsigned.all;
 5
 6 entity contador is port
 7 (
 8     clk, e, clr, l, ud : in std_logic;
 9     d: in std_logic_vector (6 downto 0);
10     q : out std_logic_vector (6 downto 0)
11 );
12 end contador;
13
14 architecture aContador of contador is
15 signal aux : std_logic_vector (6 downto 0);
16 begin
17
18     process(clk,clr)
19     begin
20         if(clr = '1')then
21             aux <= "0000000";
22         elsif (clk'event and clk = '1')then
23             if(e='0')then
24                 aux <= aux;
25             else
26                 if(l='1')then
27                     aux<=d;
28                 else
29                     if(ud='1')then
30                         aux <= aux+1;
31                     else
32                         aux <= aux-1;
33                     end if;
34                 end if;
35             end if;
36         end if;
37     end process;
38
39     q <= aux;
40 end aContador;
```




Name
Value
Stimulator
clk
0
Clock
clr
0
C
d
7F
d(6)
1
NUMER...
d(5)
1
NUMER...
d(4)
1
NUMER...
d(3)
1
NUMER...
d(2)
1
NUMER...
d(1)
1
NUMER...
d(0)
1
NUMER...
e
1
E
l
0
L
ud
1
U
q
06


D6
D5
D4
D3
D2
D1
D0
L
UD
E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
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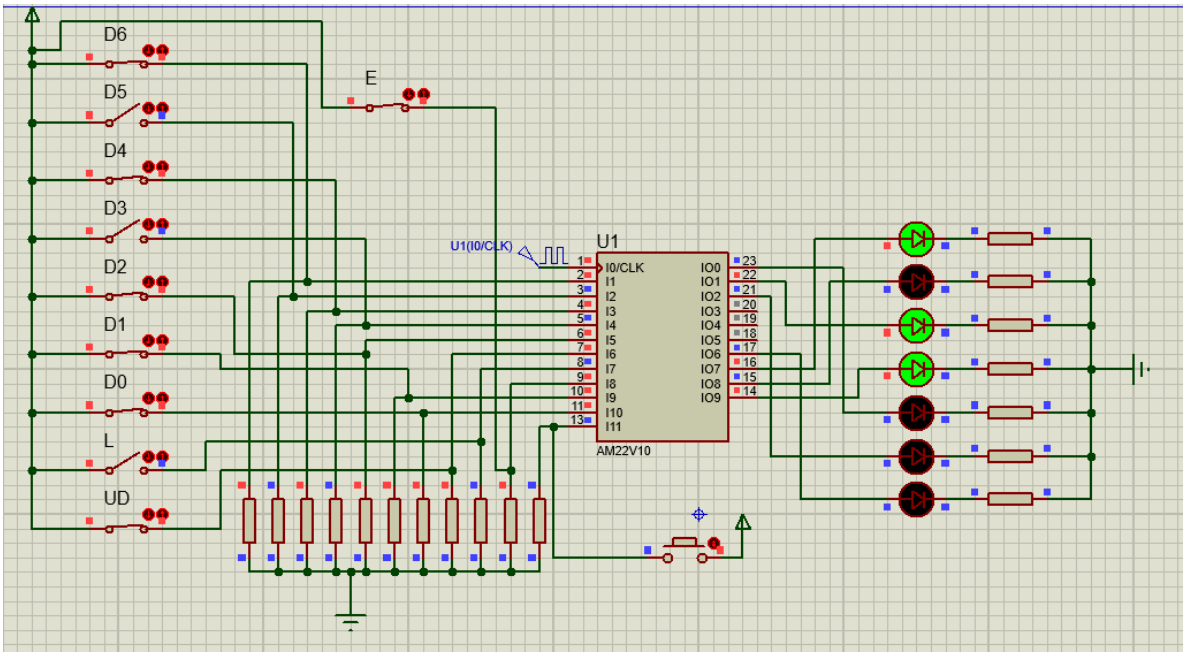
IO6
IO7
IO8
IO9
AM22V10


D6
D5
D4
D3
D2
D1
D0
L
UD
E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
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IO0
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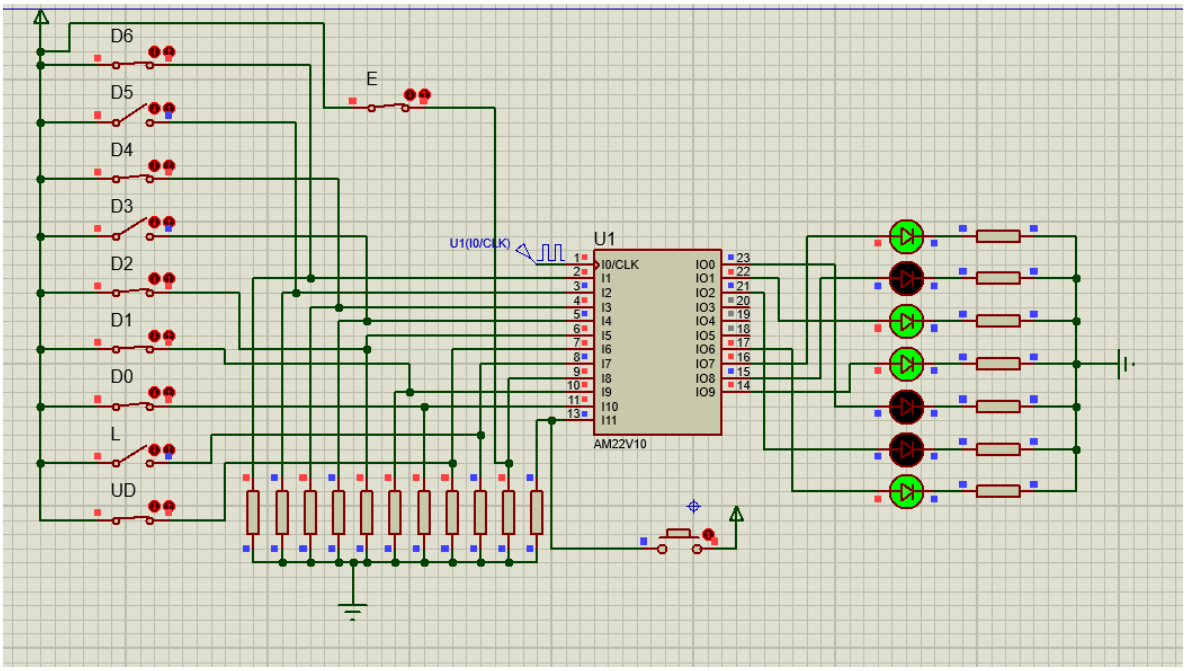
IO9
AM22V10


D6
D5
D4
D3
D2
D1
D0
L
UD
E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
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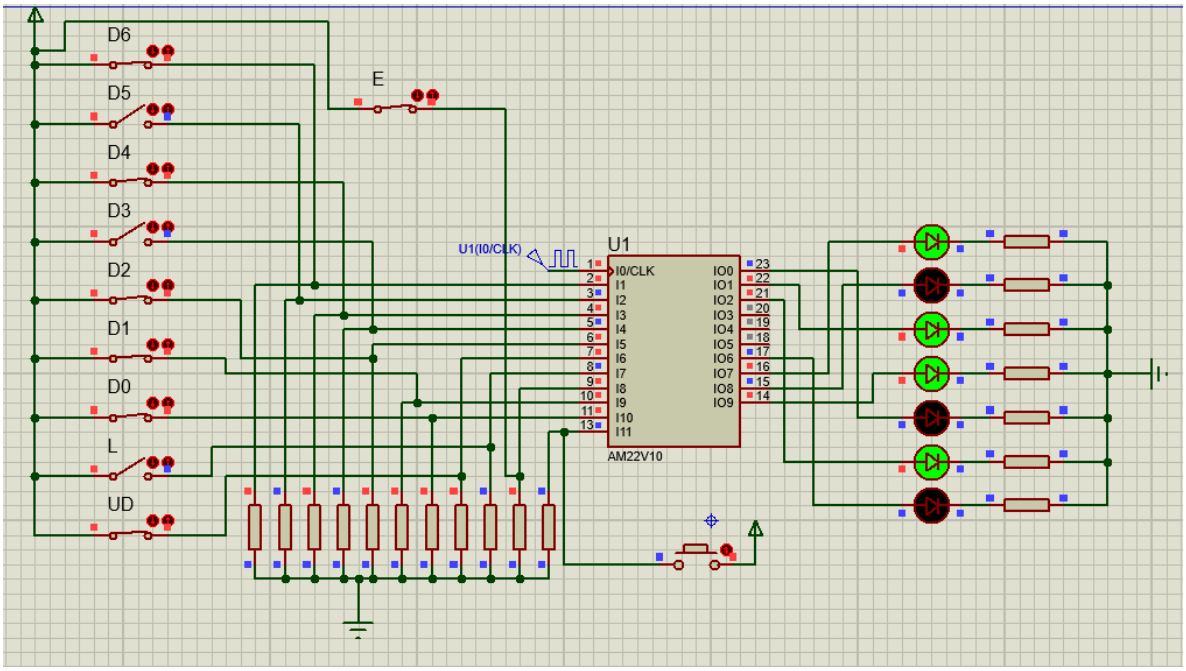
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10


D6
D5
D4
D3
D2
D1
D0
L
UD
E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
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I11
IO0
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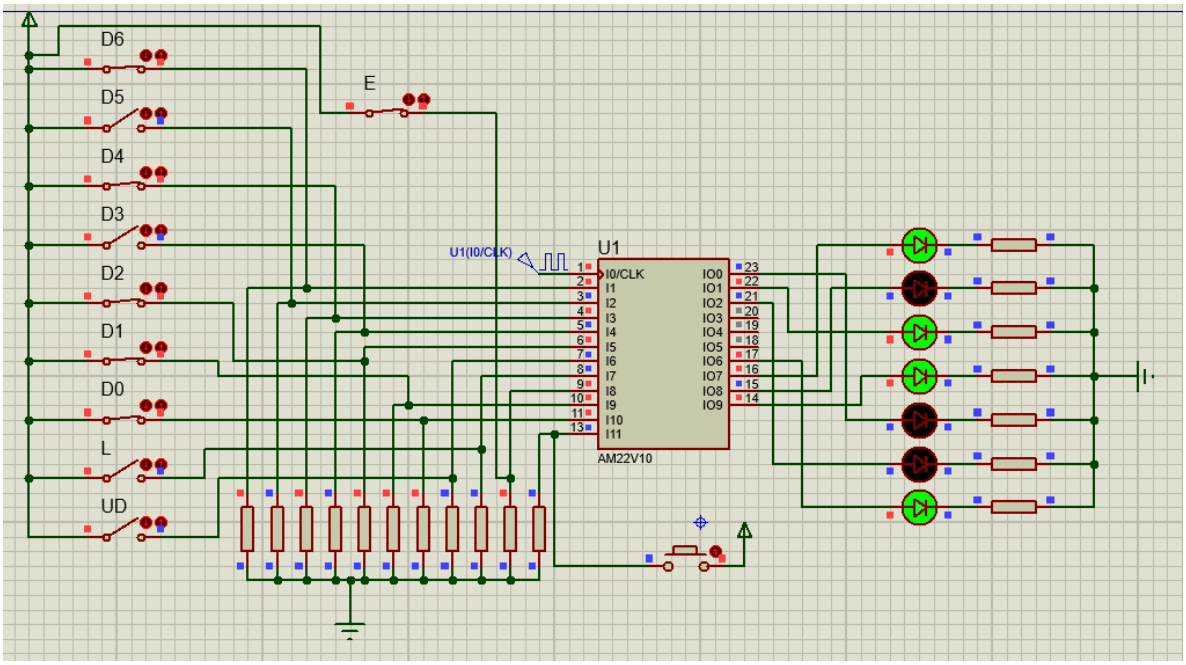
IO8
IO9
AM22V10


D6
D5
D4
D3
D2
D1
D0
L
UD
E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
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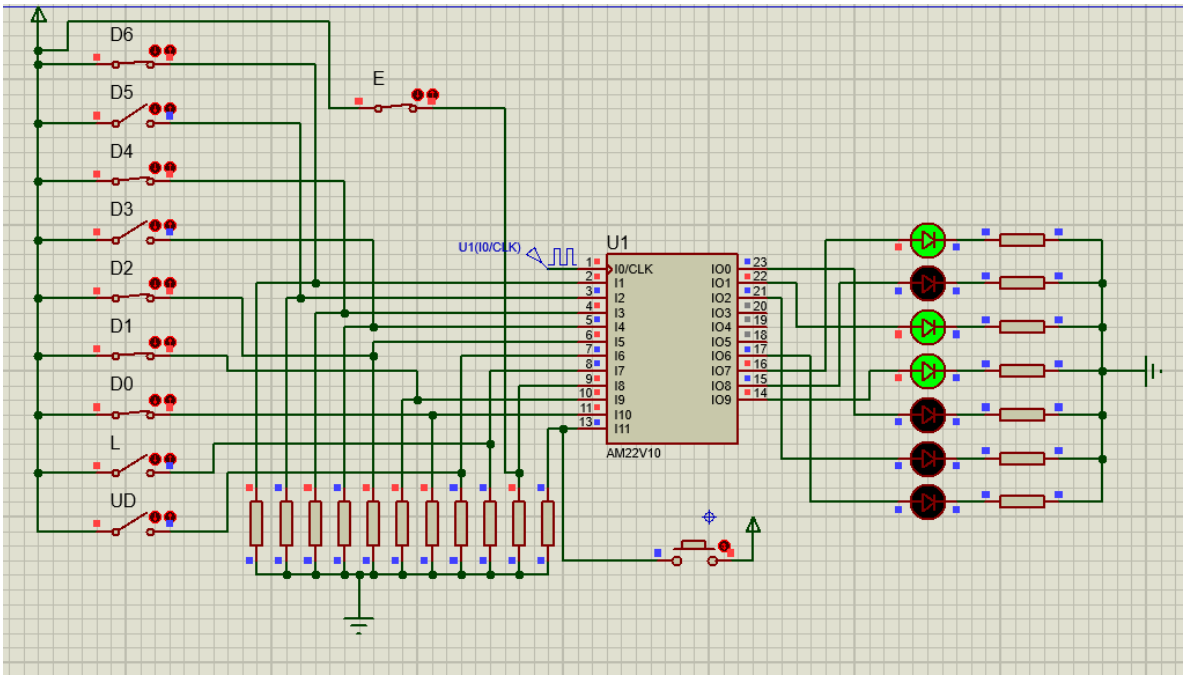
IO6
IO7
IO8
IO9
AM22V10


D6
D5
D4
D3
D2
D1
D0
L
UD
E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
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I6
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IO0
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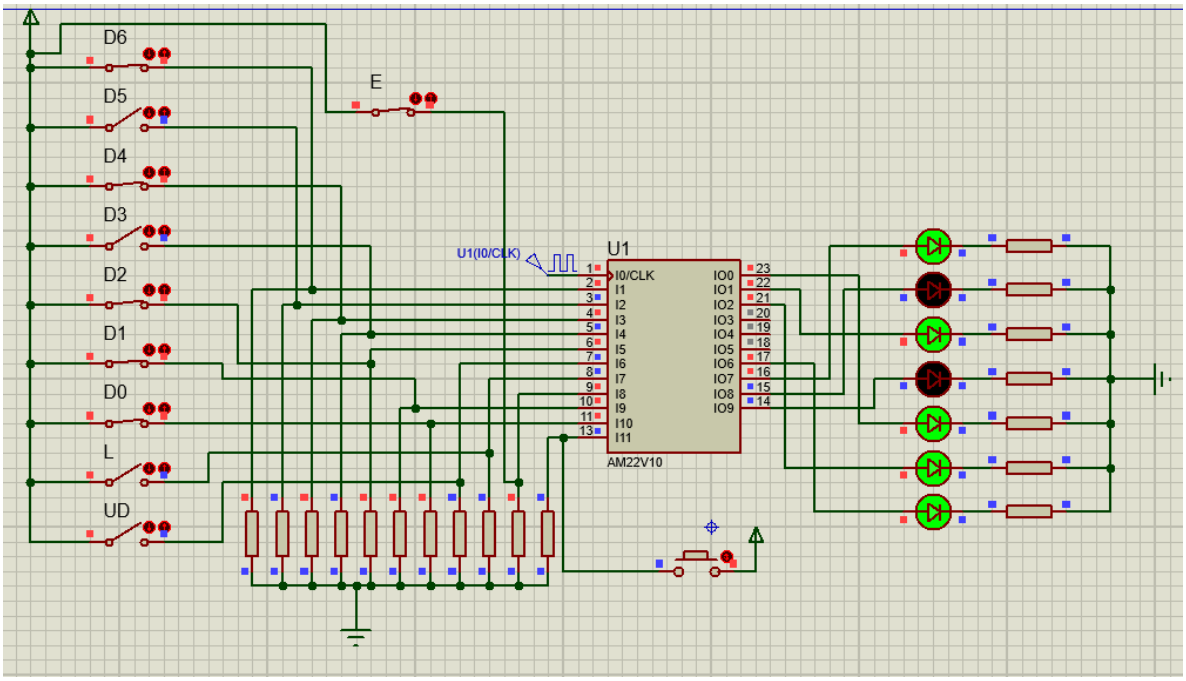
AM22V10


D6
D5
D4
D3
D2
D1
D0
L
UD
E
U1(I0/CLK)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10