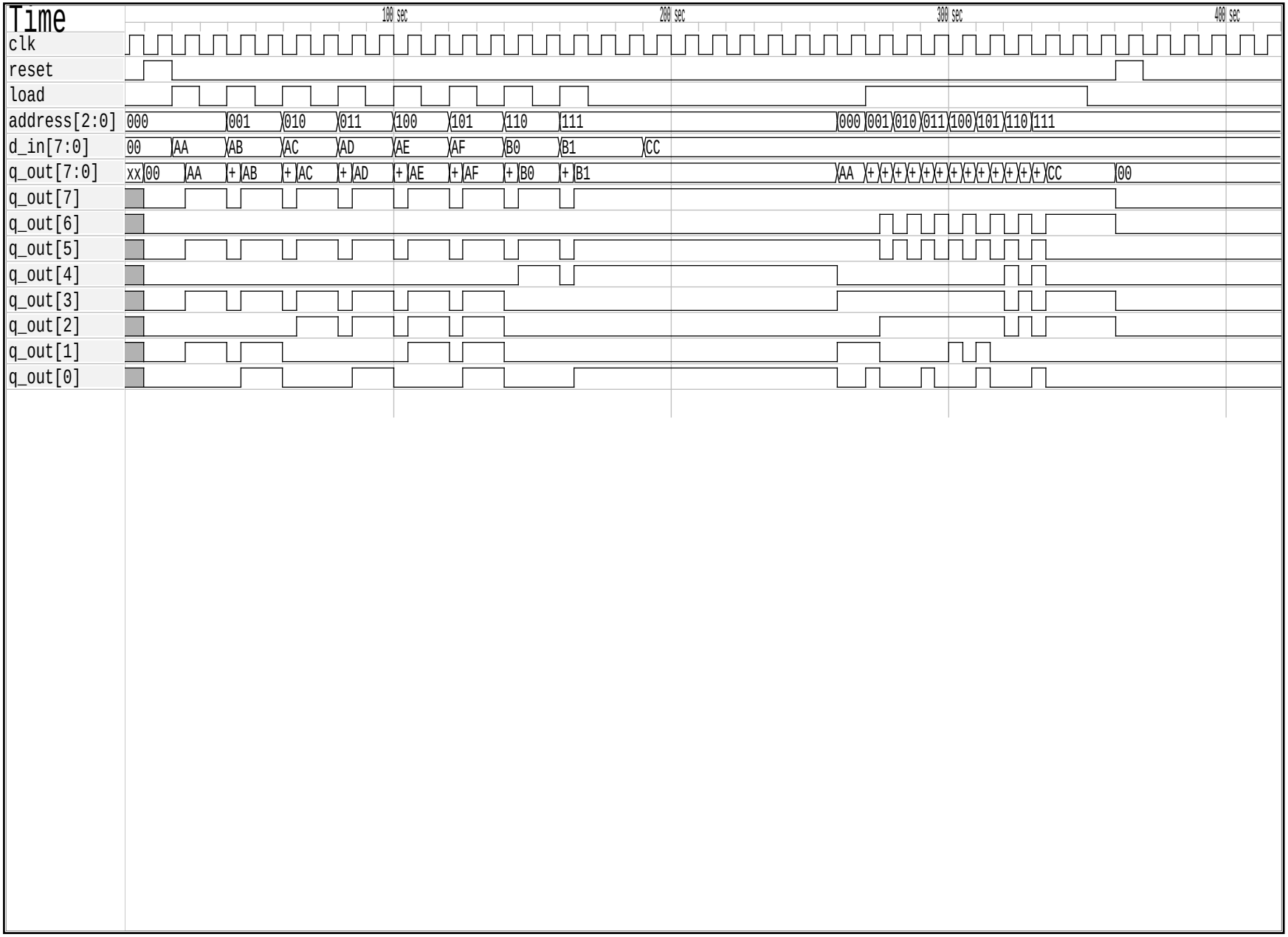
Time
100 sec
200 sec
300 sec
400 sec
clk
reset
load
address[2:0]
000 001 010 011 100 101 110 111 000 001 010 011 100 101 110 111
d_in[7:0]
00 AA AB AC AD AE AF B0 B1 CC
q_out[7:0]
xx 00 AA + AB + AC + AD + AE + AF + B0 + B1 AA + + + + + + + + + + + + CC 00
q_out[7]
q_out[6]
q_out[5]
q_out[4]
q_out[3]
q_out[2]
q_out[1]
q_out[0]