ECE 281 – Digital Design and Computer Architecture

POLICIES AND ADMINISTRATION

Instructors:

Capt Steve Beyer (CD) — Office: 2F46C
Phone: 333-6556 — Email: Steven.beyer@usafa.edu

Col Brian Neff — Office: 2F6A
Phone: 333-4213 — Email: brian.neff@usafa.edu

Lt Col Sam Stone — Office: 2E36C
Phone: 333-6957 — Email: samuel.stone@usafa.edu

1. **Course Goals:**

The goal of this course is for all cadets enrolled in the course to develop the ability to understand and design combinational and sequential circuits and construct, test, and debug these circuits using schematic diagrams and hardware description languages. Cadets shall demonstrate an understanding of basic computer architecture and how a computer executes simple programs.

2. **Course Objectives:**

Cadets shall be able to:

i) Demonstrate ability to design, analyze, and implement combinational and sequential circuits using schematic diagrams.
ii) Demonstrate ability to design, analyze, and implement combinational and sequential circuits using a hardware description language.
iii) Use contemporary software tools to debug a digital system design and verify that a digital system meets defined requirements.
iv) Demonstrate the ability to understand and analyze a microarchitecture (datapath and control unit) to implement a simple computer architecture.
v) Demonstrate the ability to properly record and report laboratory work.

3. **Course Prerequisites:** None

4. **Grade Distribution and Policy:**

Prog		**Final**	
GRs (1)	25%	GRs (2)	25%
Labs (2)	35%	Labs (4)	25%
Homework (3) & Quizzes	30%	Homework & Quizzes	15%
Readings & Exercises	10%	Readings & Exercises	10%
		Final Exam	25%
Total	100%	**Total**	100%

Electrical and Computer Engineering courses are contract graded using the following 100 point scale:

Grade	Grade	Grade	Grade
$93 \leq A \leq 100$	$87 \leq B+ < 90$	$77 \leq C+ < 80$	$60 \leq D < 70$
$90 \leq A- < 93$	$84 \leq B < 87$	$74 \leq C < 77$	$0 \leq F < 60$
	$80 \leq B- < 84$	$70 \leq C- < 74$	

You must complete all minimum functionalities on labs in order to complete the course. Even if an assignment is so late that no credit will be received, the assignment must be completed to the satisfaction of the instructor to prevent a grade of "Incomplete."

5. **Course Text:** Zybooks - learn.zybooks.com - USAFAECE281Spring2021

6. **Collaboration Policy:** For all assignments in this course, unless otherwise noted on the assignment, you may work with anyone. We expect all graded work, to include code, lab notebooks, and written reports, to be in your own work. Copying another person's work, with or without documentation, will result in **NO** academic credit. Furthermore, copying without attribution is dishonorable and will be dealt with as an honor code violation.

7. **EI Policy:** Schedule EI with an instructor if you are having difficulty with the course material. You must have read the assignment and attempted the homework *before* requesting EI. Note: You are responsible for material if you miss class, so get notes from someone in your section. For example, you miss the lesson where the instructor announces a quiz for the next lesson or the instructor assigns homework due next lesson. Even though you missed the lesson, you are still responsible for the quiz, homework, or any other assignments made. It is in your best interest to check with your classmates after an absence. After you've read the assignment, attempted the homework, and checked with your classmates, you may then schedule EI if you have difficulty with the material—not to make up a class you missed.

8. **CAS Policy:** You must notify your instructor of any class absence (with a descriptive reason—don't just send a CAS code or SCA number) as soon as possible, preferably before the absence occurs. E-mail is the preferred method to notify your instructor. Be sure to check your SCA to see if instructor "notification" or "permission" is required. There is a difference! If you need "permission," be sure to ask as soon as you know you need it.

9. **Late Work Policy:** All work is due as shown on the syllabus or in the assignment.

   If problems arise with graded assignments, see your instructor in advance. Assignments turned in later than the due date **without prior permission** from the instructor will be penalized (with instructor discretion) 25% per **calendar** day.

10. **Readings:** Reading assignments are provided in zybooks and must be done ***prior*** to class. There will not be a large amount of lecture and if you do not do the readings, you will fall behind.

11. **Assignments:** Assignments and due dates are included in the syllabus.

12. **Exams and Quizzes:** All exams and quizzes are closed textbook and notes. Quizzes will be given at instructor discretion. Testable material includes any concepts from the labs, lectures, exercises, homework, and assigned readings. **Not all testable concepts will necessarily be covered in class (e.g., readings).**

For missed GRs, the following policies are outlined in USAFA FOI 537-3:

- Scheduled Absence - If you know that you will be unable to take the GR during the scheduled GR period, you are required to inform your instructor as soon as possible before the GR and to schedule a make-up exam.

- Unscheduled Absence - If you miss the GR for reasons beyond your control (e.g. hospitalization, emergency leave, delayed field trip return, etc.), you must contact DFEC (x3190) within two working days to schedule a makeup. Exceptions can only be granted by the Department Head.

13. **Laboratories:** Labs are held in the department computer lab, but many of them include a prelab assignment that must be done before coming to class. The labs tend to be very hardware intensive and will probably require debugging to isolate and fix problems. In-class time is your primary chance to get active help for these problems so the more you prepare outside of class, the more successful you'll be. The 53 minutes go by extremely fast - don't waste them!

14. **In Class Exercises:** There will be a number of in class exercises designed to familiarize you with VHDL and to help you on your labs.

15. **Lab Reports:** The lab should allow you, or any knowledgeable engineer, to recreate your project. A template will be provided, but as applicable to the particular lab will contain the following:

a) Descriptive title
b) Objectives or purpose
c) Preliminary design and diagrams
d) Testing data and debug discussion
e) Answers to Lab Questions
f) Observations and Conclusions
g) Documentation

16. **Course Communication**: The primary site is **ECE281 - 2021** Team in **Teams**.

All syllabus information and handouts are distributed through Teams. Additionally, all correspondence will be primarily shared via the ECE281 - 2021 Team. The general channel will host information for the entire course. Communication specific to a certain section will be shared under that section's channel.

17. **Bitbucket:** A Bitbucket repository will be used to share your code with instructors. You will be provided directions to setup your repository during Lab 0.

18. **Gradescope:** All homework and lab reports will be submitted via Gradescope. You will be provided directions to use Graescope with HW1.

19. **Miscellaneous:** This course is designed to help in your development as an engineer or cyber scientist. Feel free to provide feedback on the lessons and labs at any time. If you have ideas to improve or enhance the course, please let me know. The class builds on concepts from the prerequisites so it is important for you to seek help as soon as you need it. Procrastination is truly the enemy in a hardware design course. A little foresight and planning and a lot of effort will result in an extremely rewarding experience serving as the basis for future microprocessor design work.

20. **Course Schedule as of 12/22/2020**

Lsn	Topic	Reading (before class)	Assigned	Assignment Due (Check Teams for Date/Time)
1	Course Introduction, Unsigned Binary and Base 2	Zybooks Lesson 1		
2	Numbering Systems, Signed Binary	Zybooks Lesson 2	HW 1	
3	Combinational Logic	Zybooks Lesson 3		HW1
4	Boolean Algebra Part 1	Zybooks Lesson 4	Lab 0	
5	Boolean Algebra Part 2 – ICE1 Breadboard	Zybooks Lesson 5		
6	Multilevel Combinational Logic	Zybooks Lesson 6	HW2	Lab 0 ICE1 Demo
7	VHDL Introduction Part 1 – ICE2 Half-Adder	Zybooks Lesson 7		HW2
8	K-Maps, Muxes, and Decoders	Zybooks Lesson 8		
9	Combinational Timing Analysis	Zybooks Lesson 9	Lab 1 Prelab	ICE2 Demo
10	Lab 1			Lab 1 Prelab
11	Lab 1			Lab 1 TTL Demo
12	VHDL Introduction Part 2 – ICE3 Full Adder			
13	Adders, Subtractors, and Comparators	Zybooks Lesson 13	Lab 2 Prelab	Lab 1 VHDL Demo/Turn In/ICE3 Demo
14	ALUs and Shifters	Zybooks Lesson 14		Lab 2 Prelab
15	Lab 2			
16	Lab 2			
17	Intro to Synchronous Circuits	Zybooks Lesson 17		Lab 2 Demo/Report
18	GR #1			
19	Finite State Machines, Design	Zybooks Lesson 19	HW3	
20	Finite State Machines, Analysis	Zybooks Lesson 20		

Lsn	Topic	Reading (before class)	Assigned	Assignment Due (Check Teams for Date/Time)
21	VHDL - Sequential Logic	Zybooks Lesson 21	Lab 3 prelab	HW3
22	VHDL – Sequential Logic 2	Zybooks Lesson 22		
23	ICE4 - Stoplight			Lab 3 prelab
24	Lab 3			ICE4 Demo
25	Lab 3			Lab 3 demo
26	Sequential building blocks and memory (RAM, ROM)	Zybooks Lesson 26	Lab 4 prelab	Lab 3
27	ICE5 – Basic Elevator Controller			Lab4 Prelab
28	ICE6 – TDM			ICE5 Demo
29	Lab 4			ICE6 Demo
30	Lab 4			Lab 4 MINIMUM funct demo
31	GR 2			
32	MIPS Architecture: Introduction	Zybooks Lesson 32		Lab 4 Moving Lights demo
33	Lab 4			Lab 4 More Floors demo
34	MIPS Architecture: Operations	Zybooks Lesson 34		Lab 4 Change Inputs & Passenger Pickup demo
35	MIPS Architecture: Instructions	Zybooks Lesson 35		Lab 4 Report
36	MIPS Architecture: Inst for Decisions & Procedures	Zybooks Lesson 36		
37	MIPS Architecture: Memory	Zybooks Lesson 37	HW4	
38	MIPS Microarchitecture: Datapath	Zybooks Lesson 38		
39	MIPS Microarchitecture: Control Unit	Zybooks Lesson 39		HW4
40	Review			