ECE 281 Lesson Objective Mappings

Course Goals:

The goal of this course is for all cadets enrolled in the course to develop the ability to **understand and design combinational and sequential circuits and construct, test, and debug these circuits** using schematic diagrams and hardware description languages. Cadets shall demonstrate an understanding of basic computer architecture and how a computer executes simple programs.

Course Objectives (COs):

Cadets shall be able to:

1. Demonstrate ability to design, analyze, and implement combinational and sequential circuits using **schematic diagrams**.
2. Demonstrate ability to design, analyze, and implement combinational and sequential circuits using a **hardware description language**.
3. Use contemporary software tools to debug a digital system design and verify that a digital system meets defined requirements.
4. Demonstrate the ability to understand, analyze, and test a microarchitecture (datapath and control unit) to implement a simple computer architecture.
5. Demonstrate the ability to properly record and report laboratory work.

Lesson Objectives:

Lessons 1-2 (Math/Numbering Systems) - CO 1

1. Be able to represent an unsigned (positive) number in any number base, 2 to N, but particularly in decimal, binary, and hexadecimal
2. Know the limitations of a number system (e.g., range)
3. Demonstrate the ability to add or subtract binary numbers and correctly identify if there is a carry or overflow

Lessons 3-6 (Logic) - CO 1

1. Understand the basic logic gates and their functions
2. Based on a problem description, design a solution using Boolean logic gates and/or equations to solve the problem
3. Utilize Boolean algebra to simplify Boolean equations or to derive a form that yields the most desirable hardware configuration
4. Demonstrate the ability to describe a combinational digital system by a truth table, Boolean equation, and schematic
5. Given any one form from above, produce the others

Lesson 7 – VHDL (CO 2)

1. Demonstrate the ability to use basic VHDL constructs such as entity, architecture, and signals to model combinational circuits using VHDL behavioral modelling

2. Given a VHDL behavioral entity model, draw a schematic that shows the complete entity and architecture

Lesson 8 – K-maps

1. Demonstrate how to use K-maps to represent and simplify combinational logic (CO 1)

Lesson 9 –Muxes, Decoders and Combinational Timing Analysis

1. Given a circuit with multiplexers or decoders, describe its logic using a truth table or Boolean equation(s) (CO 1)
2. Understand and recognize the VHDL idioms required to implement muxes and decoders (CO 2)
3. Understand the causes and impacts of delays in combinational circuitry (CO 1)
4. Understand how to read a basic timing diagram (CO 1)
5. Be able to identify the short path and critical path in a combinational circuit (CO 1)
6. Be able to correctly identify glitches in a circuit output (CO 1)

Lesson 10-11 – TTL vs VHDL Lab

1. Based on a problem description, design a solution using a truth to solve the problem
2. Design and implement the logic described in a truth table by creating combinational circuit schematics using various digital building blocks (Muxes, decoders) and logic gates (NANDs, ANDs, ORs, Inverters)
3. Build a physical digital circuit to gain experience using digital hardware tools and to gain an appreciation for the flexibility afforded by FPGA prototyping
4. Demonstrate ability to implement a simple combinational circuit using a HDL (CO 2)
5. Use Vivado simulation tools to verify that a combinational circuit meets defined requirements (CO 3)

Lesson 12 – VHDL (CO 2)

1. Understand how a “top-level” can be used to combine multiple VHDL components into a larger design

Lesson 13 – Adders, Subtractors, and Comparators (CO 1)

1. Understand how to create an adder, subtractor, or comparator
2. Know the tradeoffs of the three common carry propagate adders
3. Demonstrate ability to use digital building blocks (adders, subtractors, comparators, and muxes) to build more complex combinational circuits

Lesson 14 – ALUs and Shifters (CO 1)

1. Demonstrate ability to analyze and implement an ALU using a schematic diagram
2. Given a hardware schematic, correctly identify a particular shifter or rotator
3. Demonstrate how to multiply a number by 2^N using a LEFT bit shift of N bits
4. Demonstrate how to divide a number by 2^N using a RIGHT bit shift of N bits
5. Understand the difference between arithmetic and logical shifts

Lessons 15 – 16 (Lab 2 Seven-Segment Decoder)

1. Demonstrate ability to design, analyze, and implement a combinational circuit using a **hardware description language** (CO 2)
2. Use Vivado to debug a digital system design and verify that it meets defined requirements (CO 3)
3. Understand what the “top level” of a design is and why we use them.
4. Understand how to utilize existing components in a new design.