**ECE M216A Project, Fall 2024**

**Group-2 Team Members:**

Tianrun Gou, tgou@ucla.edu

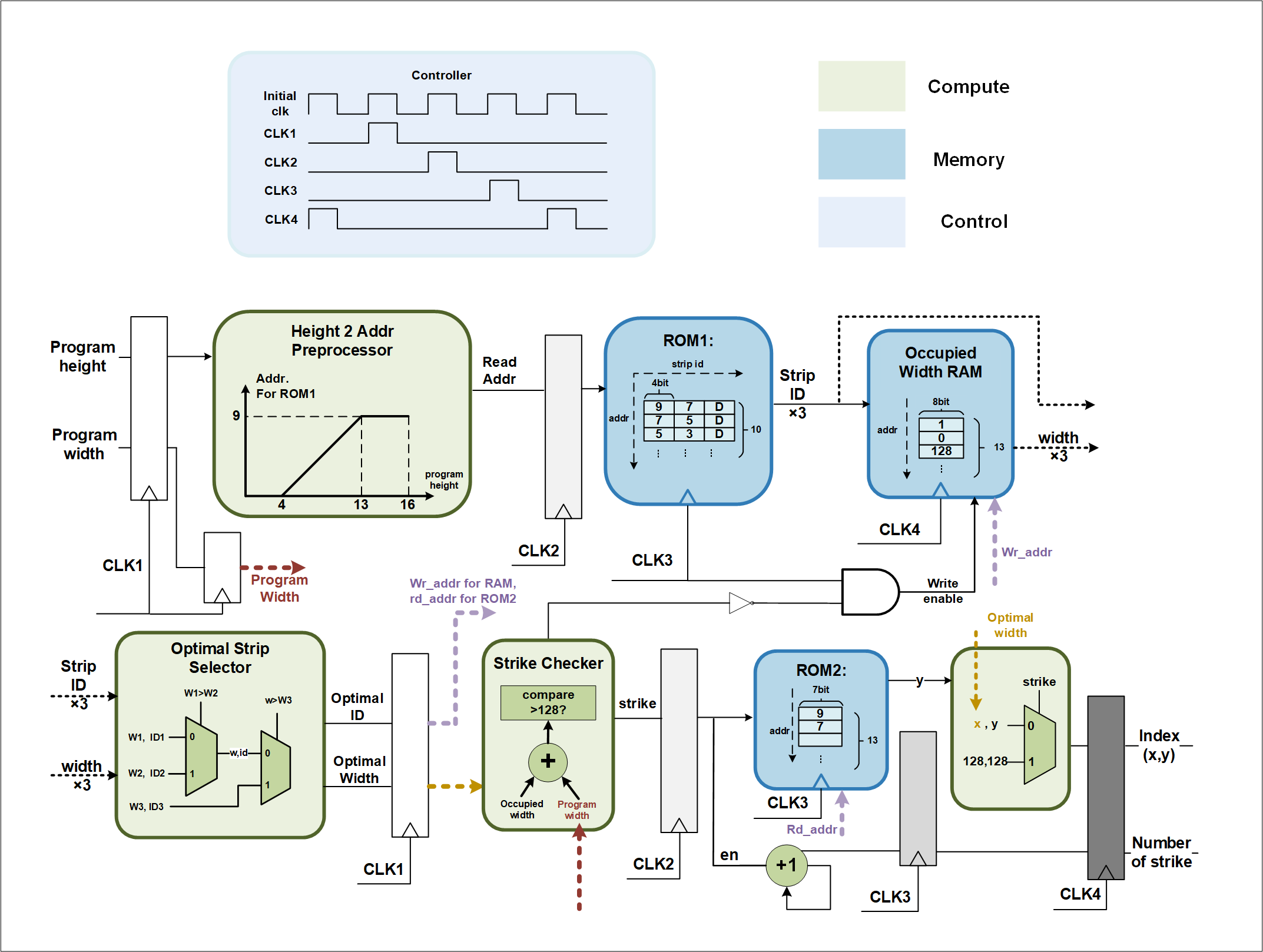
Tuo Yang, tyang08@ucla.edu

Fuyao Zhou, fuyaozhou@ucla.edu

**Group-2 Performance Summary**

|  |  |  |  |
| --- | --- | --- | --- |
| **Max fclk**  **[MHz]** | **Area**  **[]** | **Energy**  **[pJ]** | **Hold Time Slack**  **[ps]** |
| 694.44 | 3723.59 | 0.36 | 60 |

**Architecture:** Provide top-level architecture and indicate its key building blocks.



**Figure**. Architecture block diagram and its key building blocks.

**Design Highlights:**

* Achieved Max fclk**=**3571.43MHz at post synthesis simulation with TB unchanged, but 694.44MHz with corresponding clock period set in TB for an additional 1000-line input.txt
* Designed a HashMap to link program heights with strip ID ROM addresses, optimizing area usage
* Leveraged both RAM and ROM for value storage to reduce redundant computations
* Implemented clock gating for pipelining to disable unused stages when no new data is available