**ECE M216A Project, Fall 2024**

**Group-2 Team Members:**

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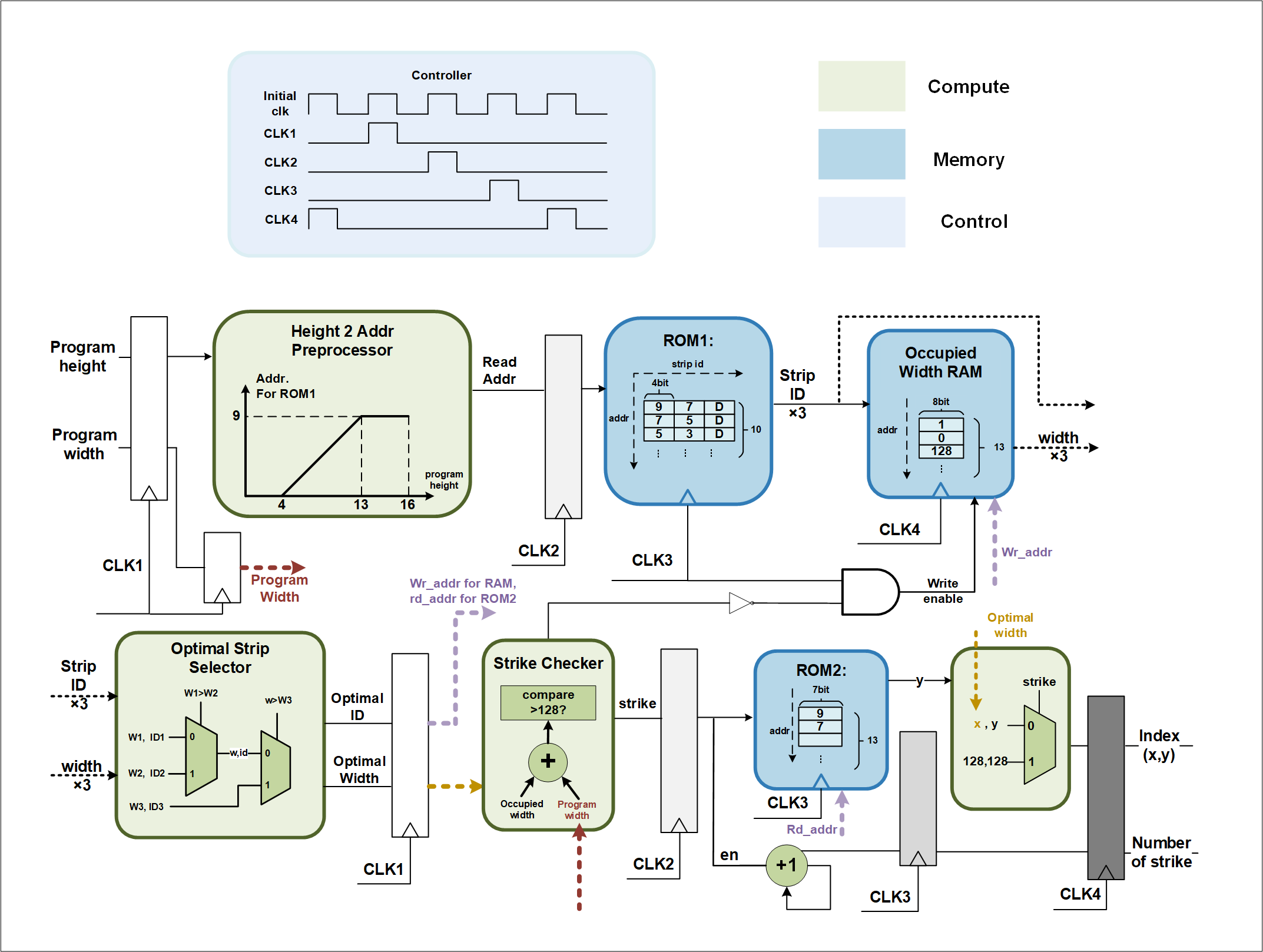
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**Group-2 Performance Summary**

|  |  |  |  |
| --- | --- | --- | --- |
| **Max fclk**  **[MHz]** | **Area**  **[]** | **Energy**  **[pJ]** | **Hold Time Slack**  **[ps]** |
| 1219.51 | 3723.59 | 0.36 | 60 |

**[Provide top-level architecture, and indicate its key building blocks]**



**Figure**. Architecture block diagram and its key building blocks.

**Design Highlights:**

* Designed a HashMap to link program heights with strip ID ROM addresses, optimizing area usage
* Leveraged both RAM and ROM for value storage to reduce redundant computations, enhancing power efficiency and performance
* Implemented pipelining to maximize parallelism and retiming to balance the logic between stages
* Integrated clock gating to disable unused stages when no new data is available