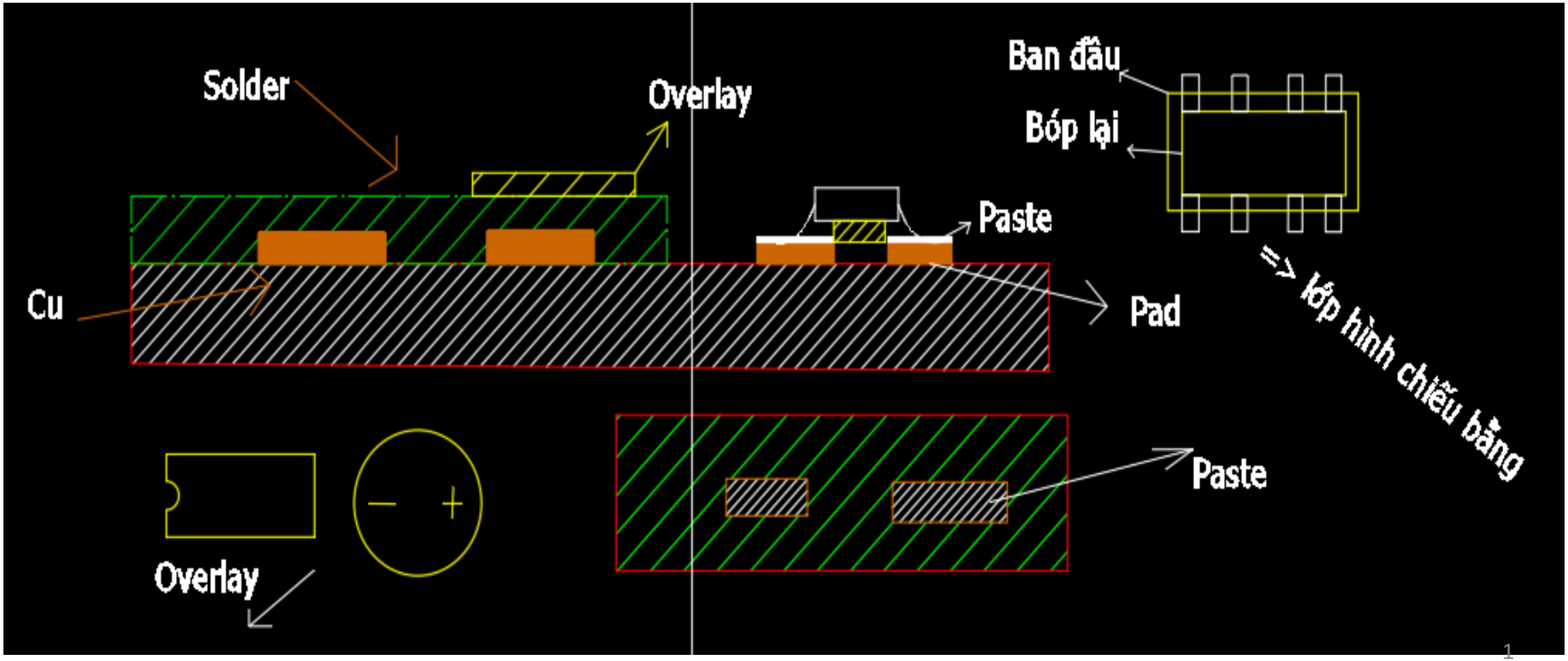
Giới thiệu các layer



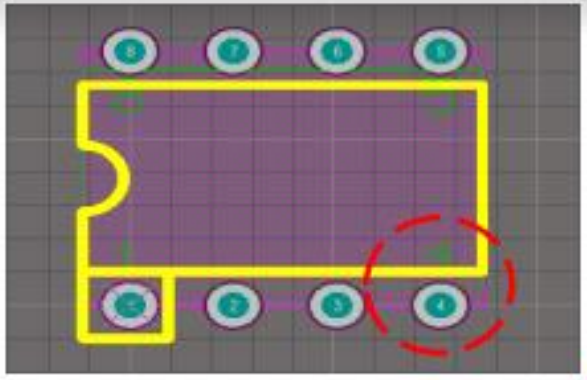
Giới thiệu các layer

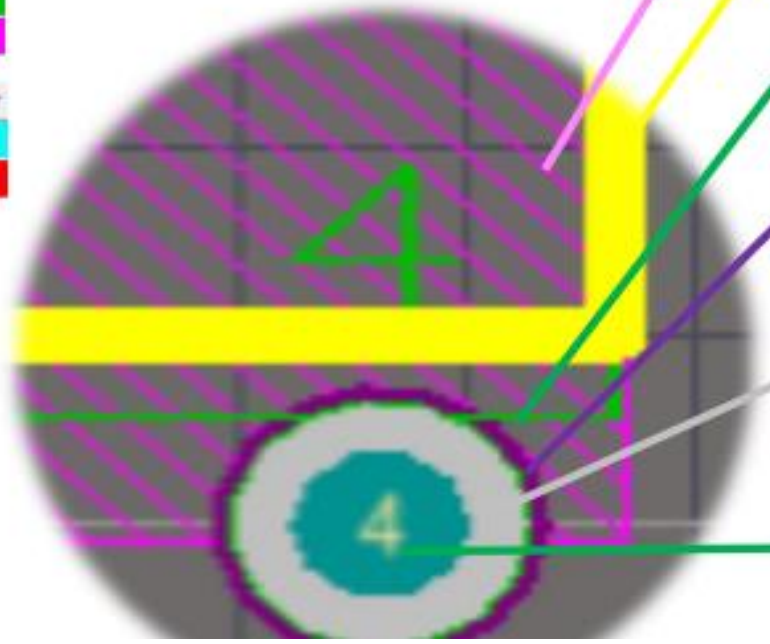
Mask Layers (A)	Color
Top Paste	
Bottom Paste	
Top Solder	
Bottom Solder	

Silkscreen Layers (K)	Color
Top Overlay (E)	
Bottom Overlay (R)	

Mechanical	Color
Mechanical 1	
Mechanical 13	

Signal Layers (S)	Color
Top Layer (T)	
Bottom Layer (B)	





Mechanical 13: Mô hình 3D của linh kiện

Silkscreen/overlay: Thể hiện đường bao và chỉ thị của linh kiện

Mechanical 2,3: Hình chiếu bằng của linh kiện

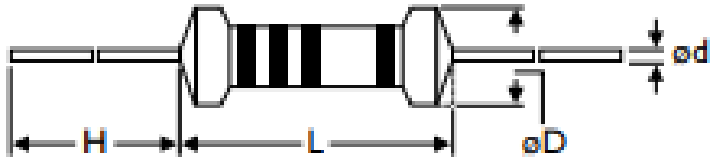
Solder (Rezist): Vùng quy định lớp sơn resit không được tràng vào

Patten (Pad): Vùng vành khuyên kết nối mối hàn giữa chân linh kiện và bo mạch

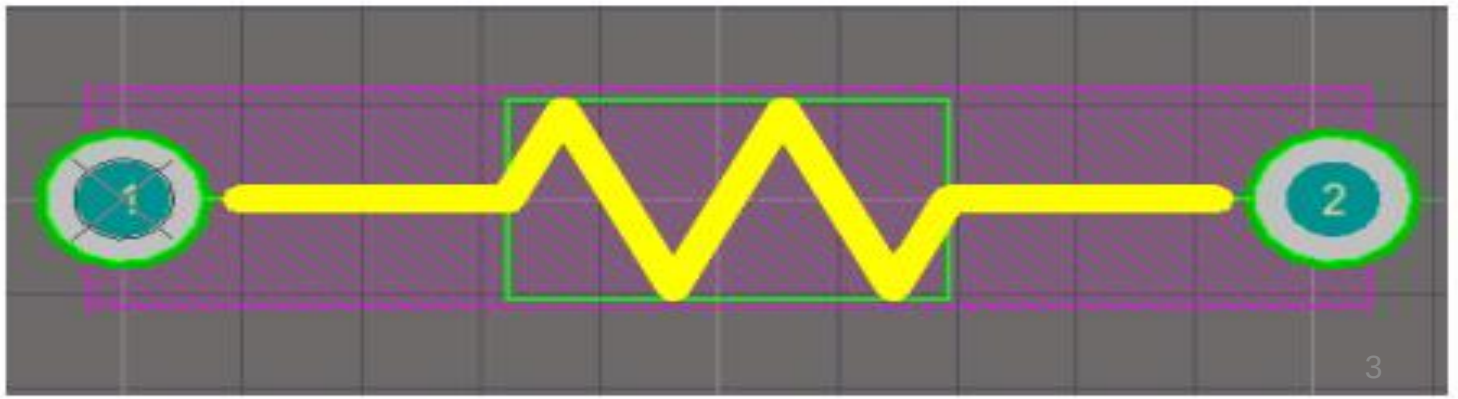
Through Hole: Lỗ xuyên thủng, để xỏ chân linh kiện vào

Thư viện chân xuyên

TRỞ CFR25S (1/4W)



STYLE		DIMENSION			
Normal	Miniature	L	øD	H	ød
CFR-12	CFR25S	3.4±0.3	1.9±0.2	28±2.0	0.45±0.05
CFR-25	CFR50S	6.3±0.5	2.4±0.2	28±2.0	0.55±0.05
CFR-50	CFR1WS	9.0±0.5	3.3±0.3	26±2.0	0.55±0.05
CFR100	CFR2WS	11.5±1.0	4.5±0.5	35±2.0	0.8±0.05
CFR200	CFR3WS	15.5±1.0	5.0±0.5	33±2.0	0.8±0.05



TRỞ CFR25S (1/4W)

Tiêu chuẩn chọn VIA cho lỗ chân xuyên

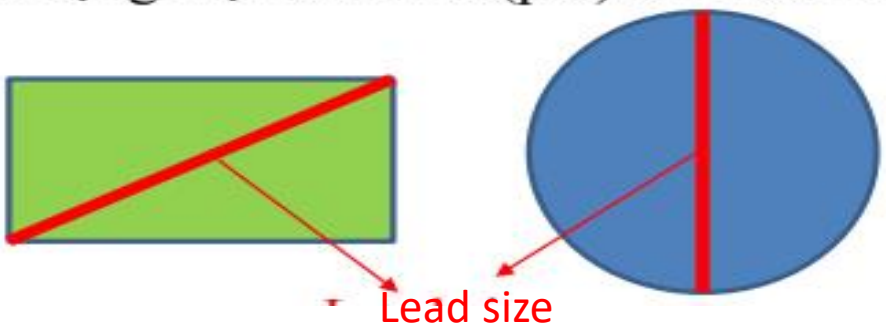
BẢNG 1: TIÊU CHUẨN CHỌN TBL(VIA)

Lead size	Hole	Type
Under 0.59Φ	0.8	TBL8
06~0.79	1	TBL10
0.8~1.09	1.3	TBL13
1.1~1.29	1.6	TBL16
1.3~1.59	2	TBL20

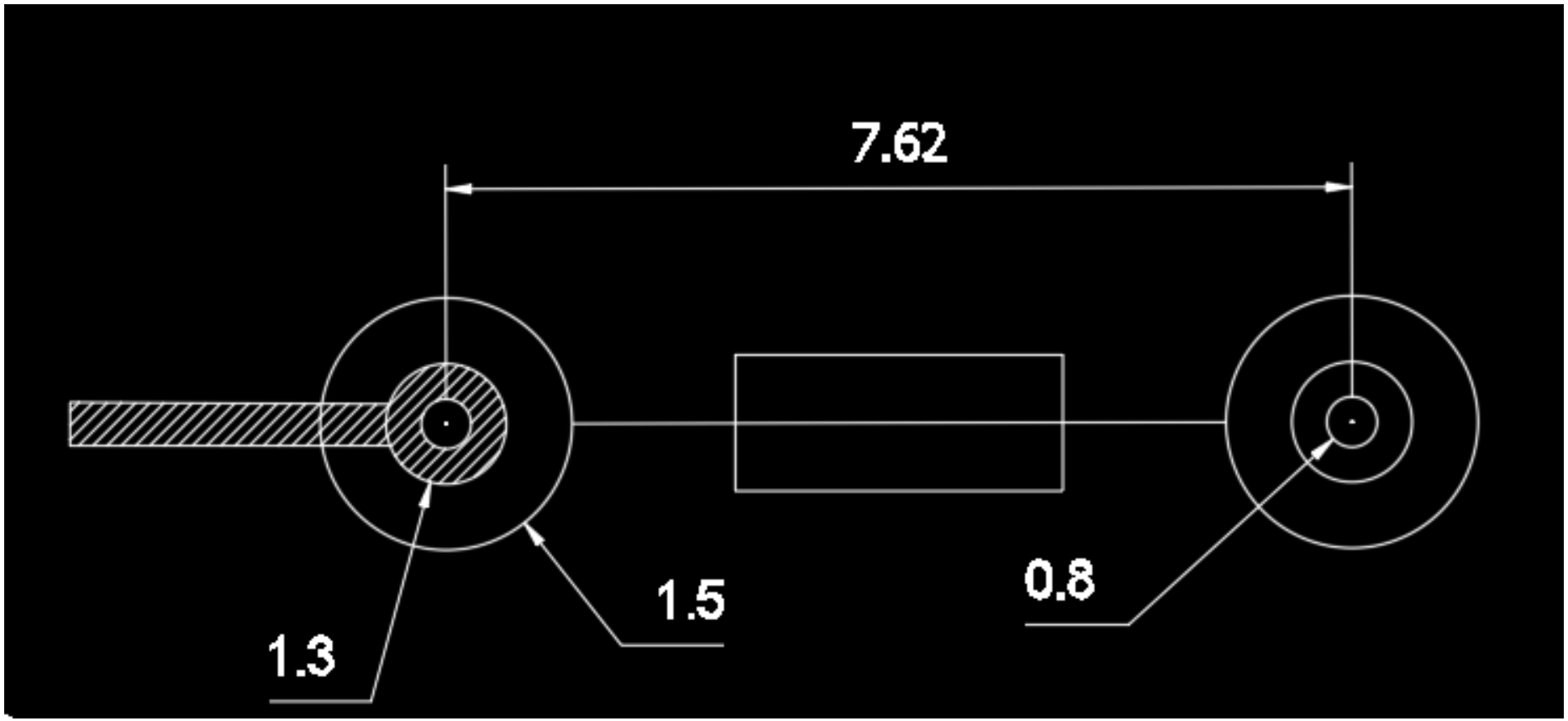
BẢNG 2: TIÊU CHUẨN CHO 1 VIA

Type	Hole	Patten	Rezist
TBL8	0.8	1.3	1.5
TBL9	0.9	1.3	1.5
TBL10	1	1.6	1.8
TBL11	1.1	1.7	1.9
TBL12	1.2	2	2.2
TBL13	1.3	2	2.2
TBL14	1.4	2.2	2.4
TBL15	1.5	2.5	2.7
TBL16	1.6	2.5	2.7
TBL17	1.7	3	3.2
TBL18	1.8	3	3.2
TBL19	1.9	3	3.2
TBL20	2	3	3.2

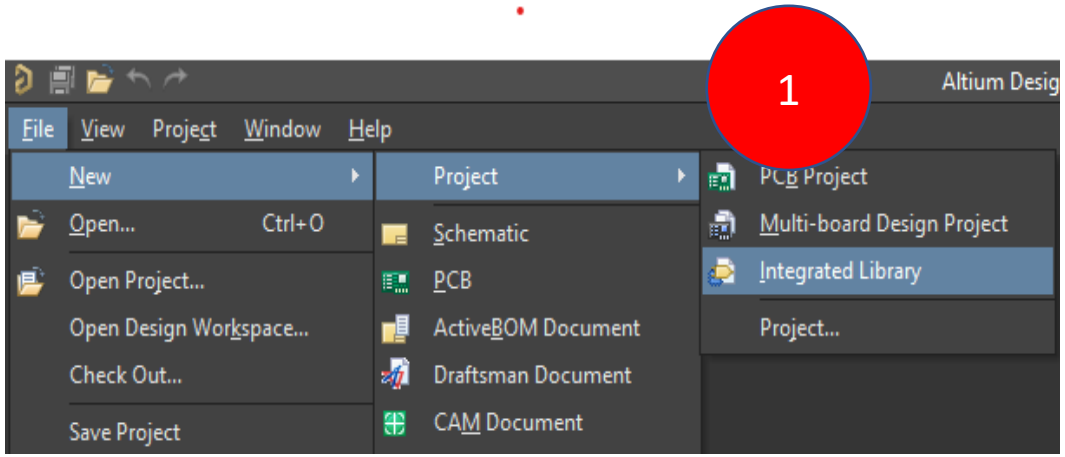
Hai dạng mặt cắt chân (pin) của linh kiện

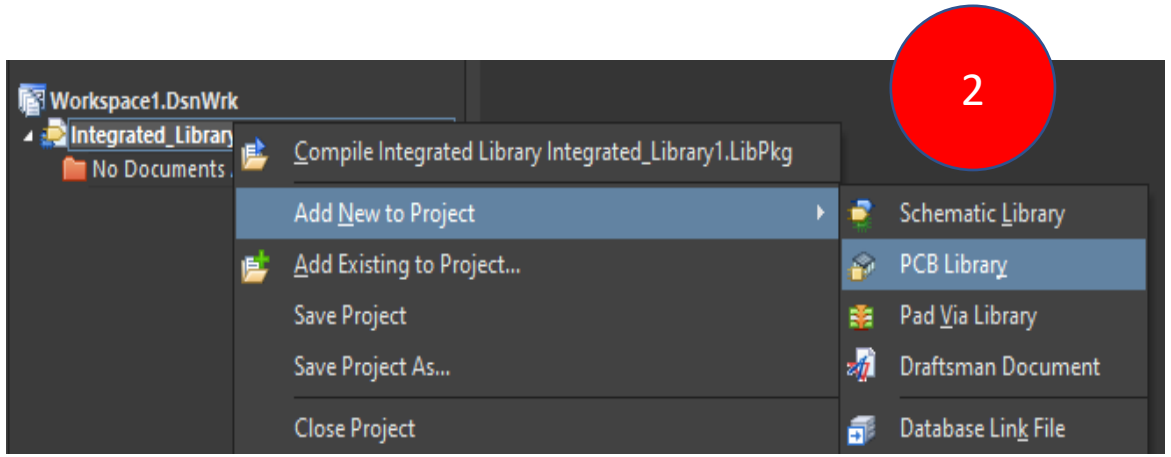


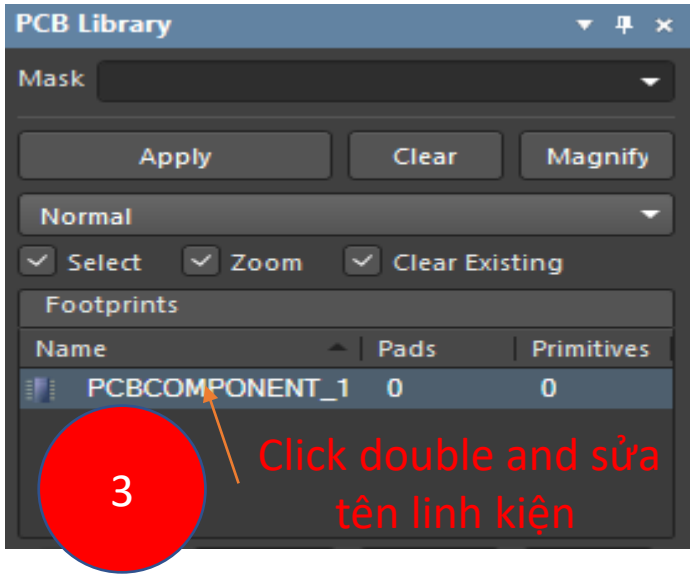
TRỞ CFR25S (1/4W)

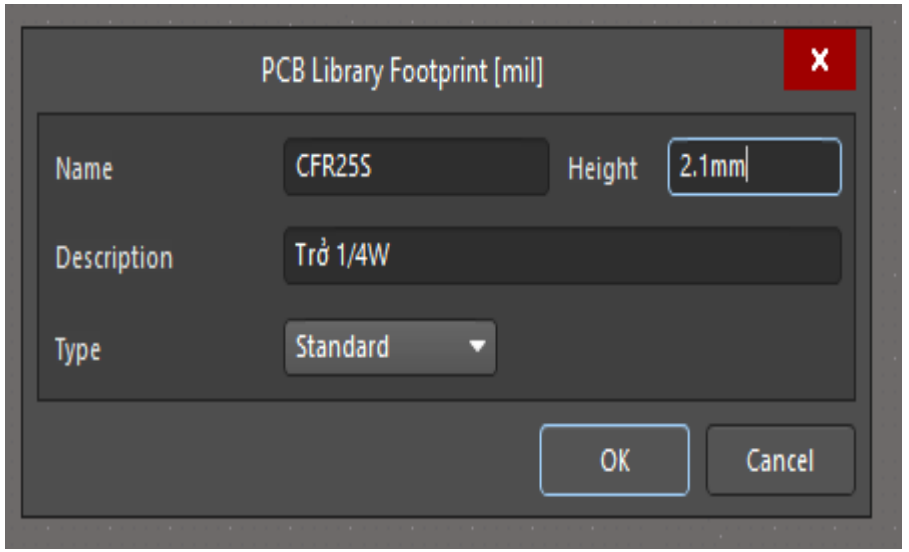


TRỞ CFR25S (1/4W)

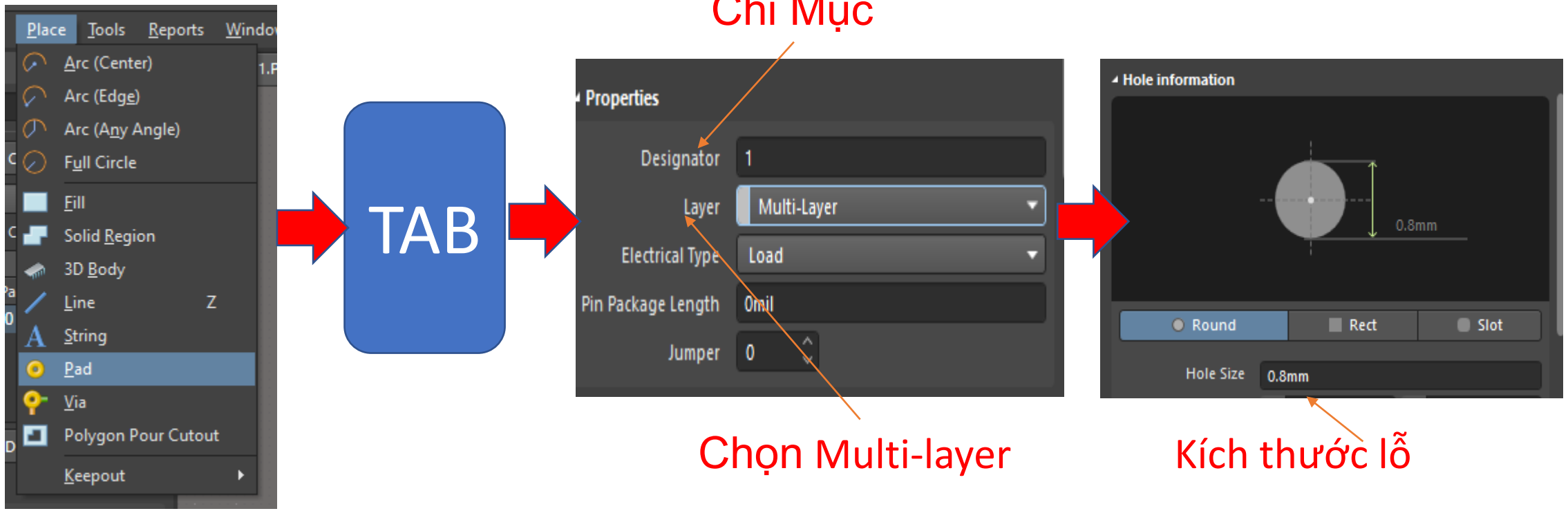




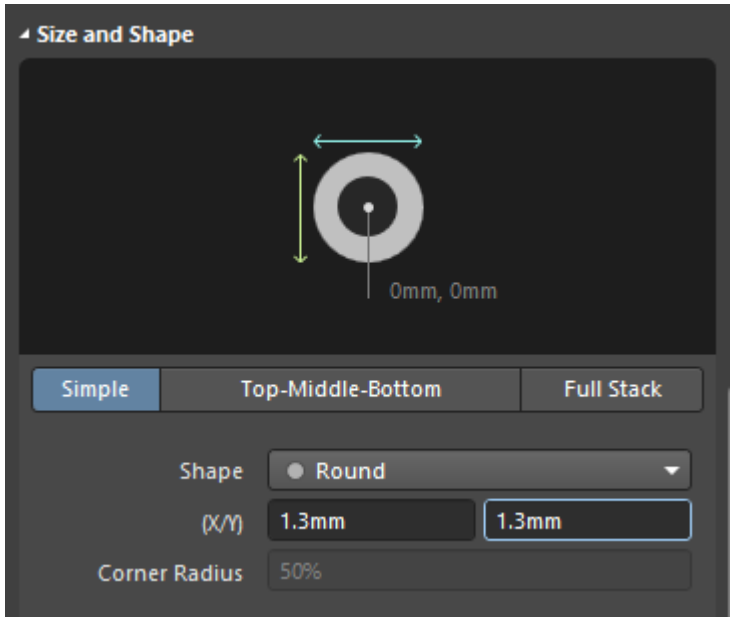


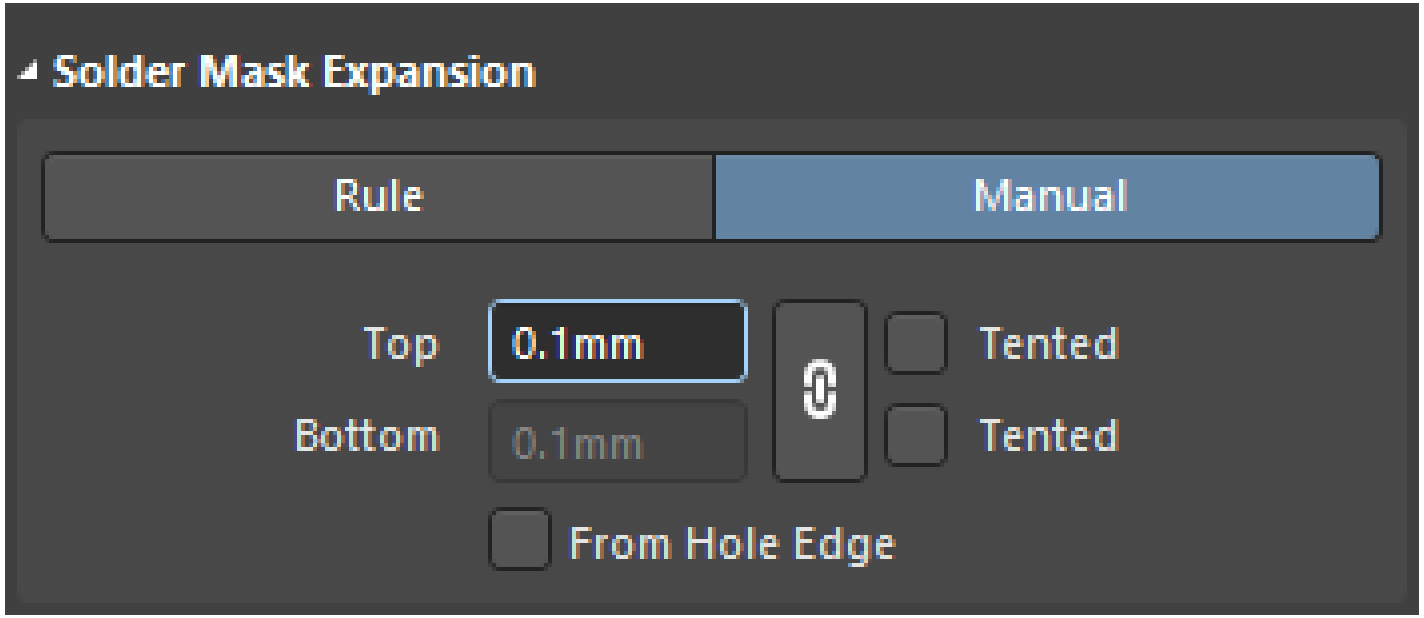


TRỞ CFR25S (1/4W)



TRỞ CFR25S (1/4W)

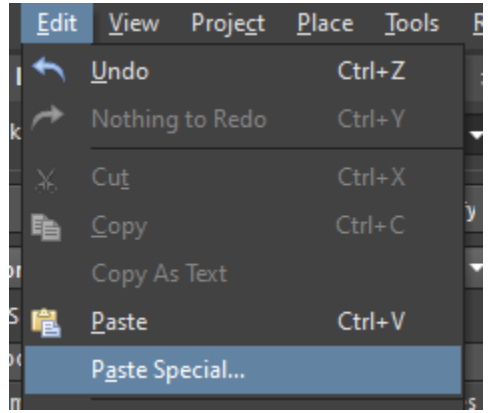


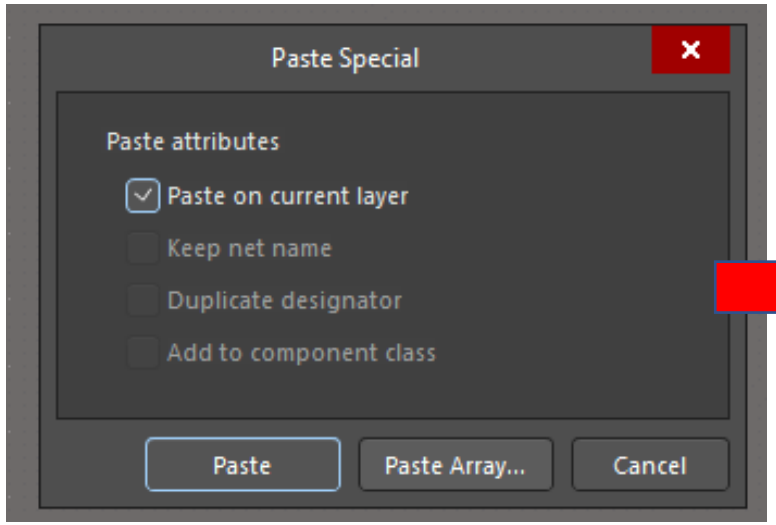


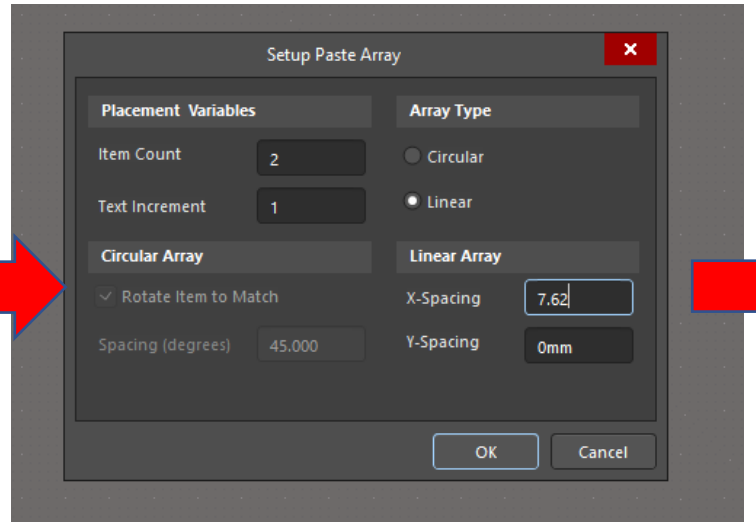
Lớp sơn cách điện cách lớp pad (1.5-1.3)/2

TRỞ CFR25S (1/4W)

Ctrl C → Chọn tâm →

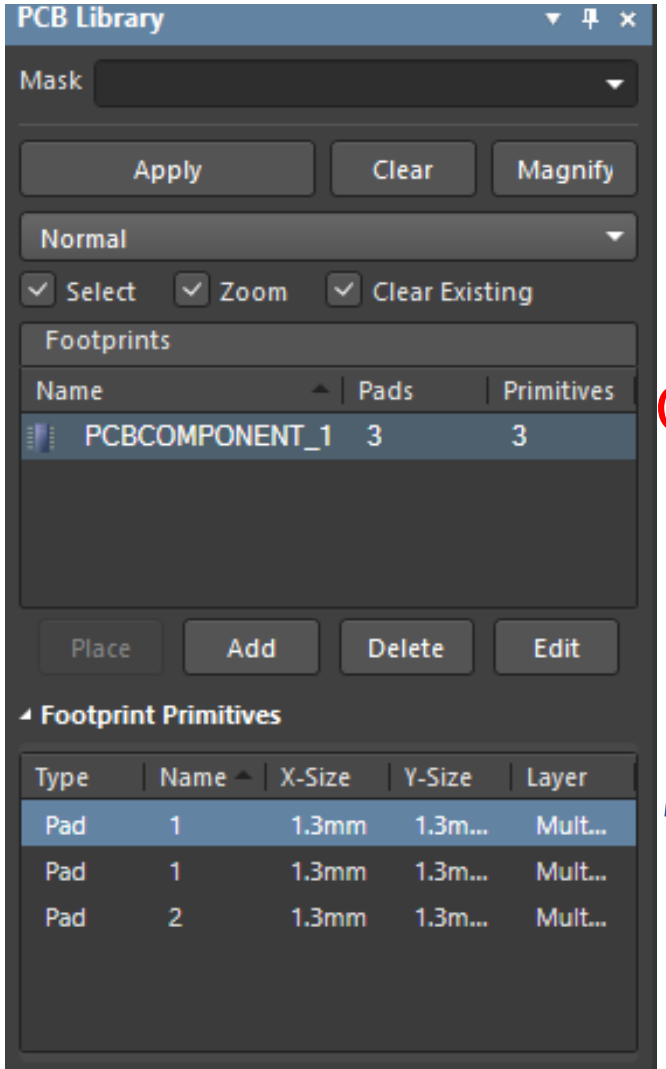




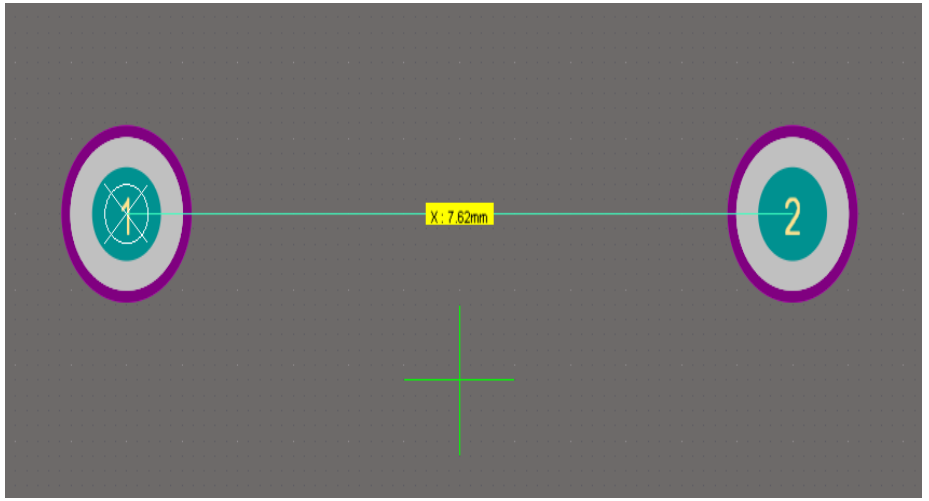


→ Ta sẽ chọn gốc dán và gốc copy trùng nhau

TRỞ CFR25S (1/4W)

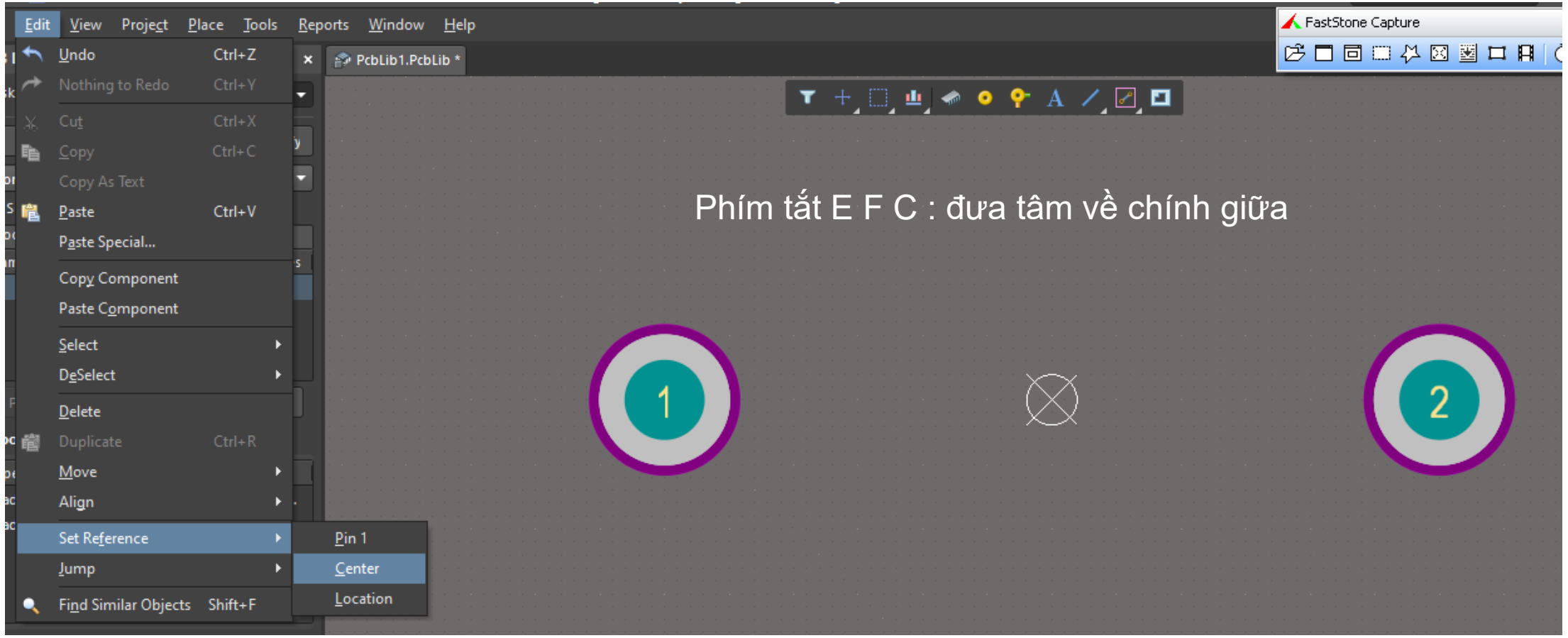


Có 2 cái 1 liền nên XÓA 1 cái đi



1. Ctrl m : Đo khoảng cách
2. Ship C : Để xóa

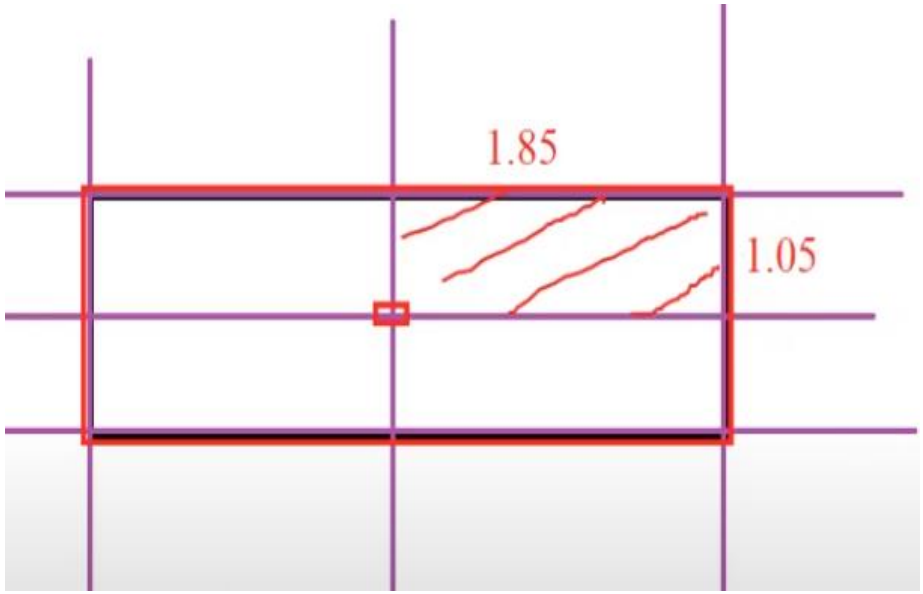
TRỞ CFR25S (1/4W)

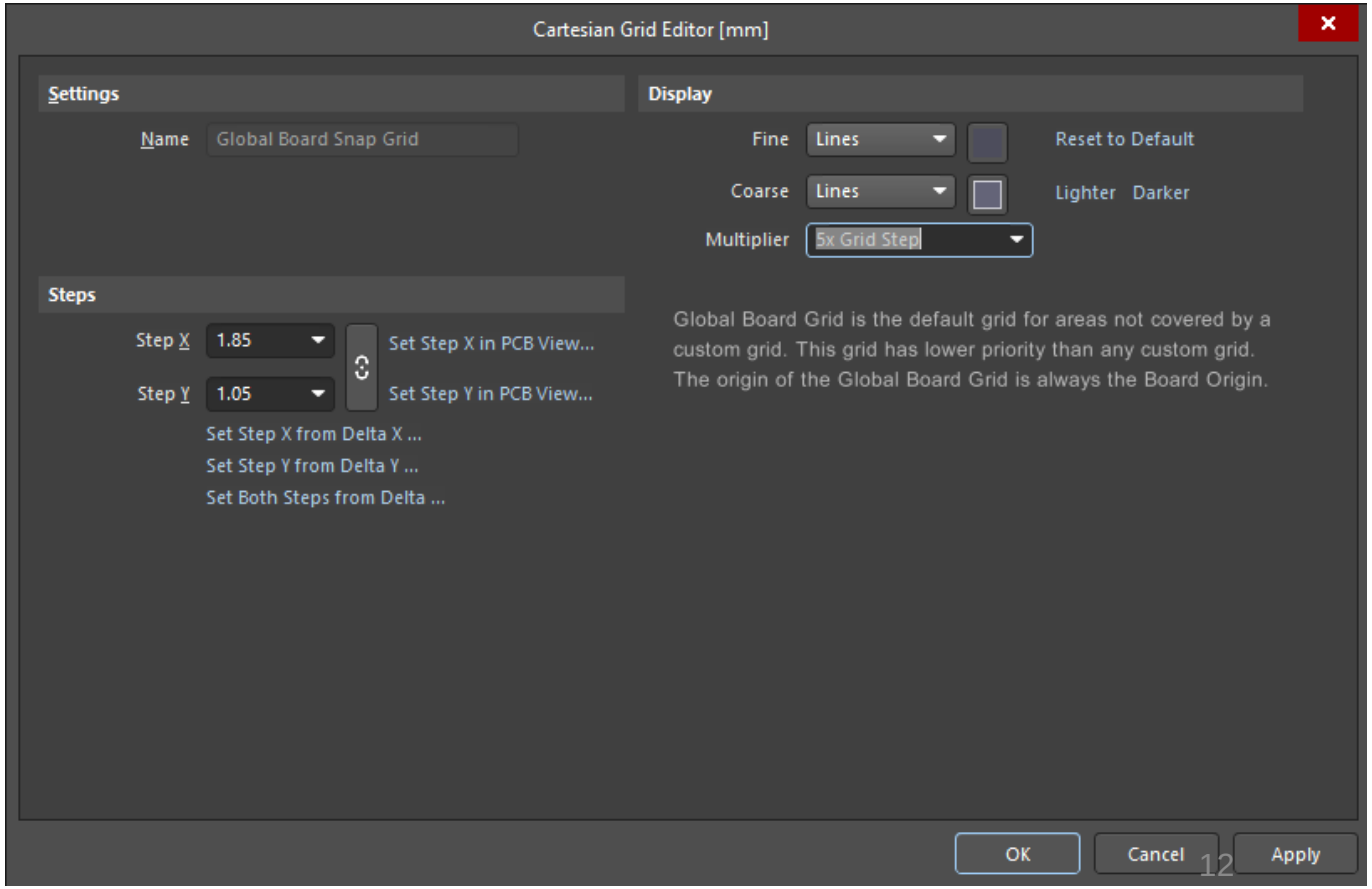


Cách 1

+ Tạo lưới có dạng như hình mong muốn

Ctrl G

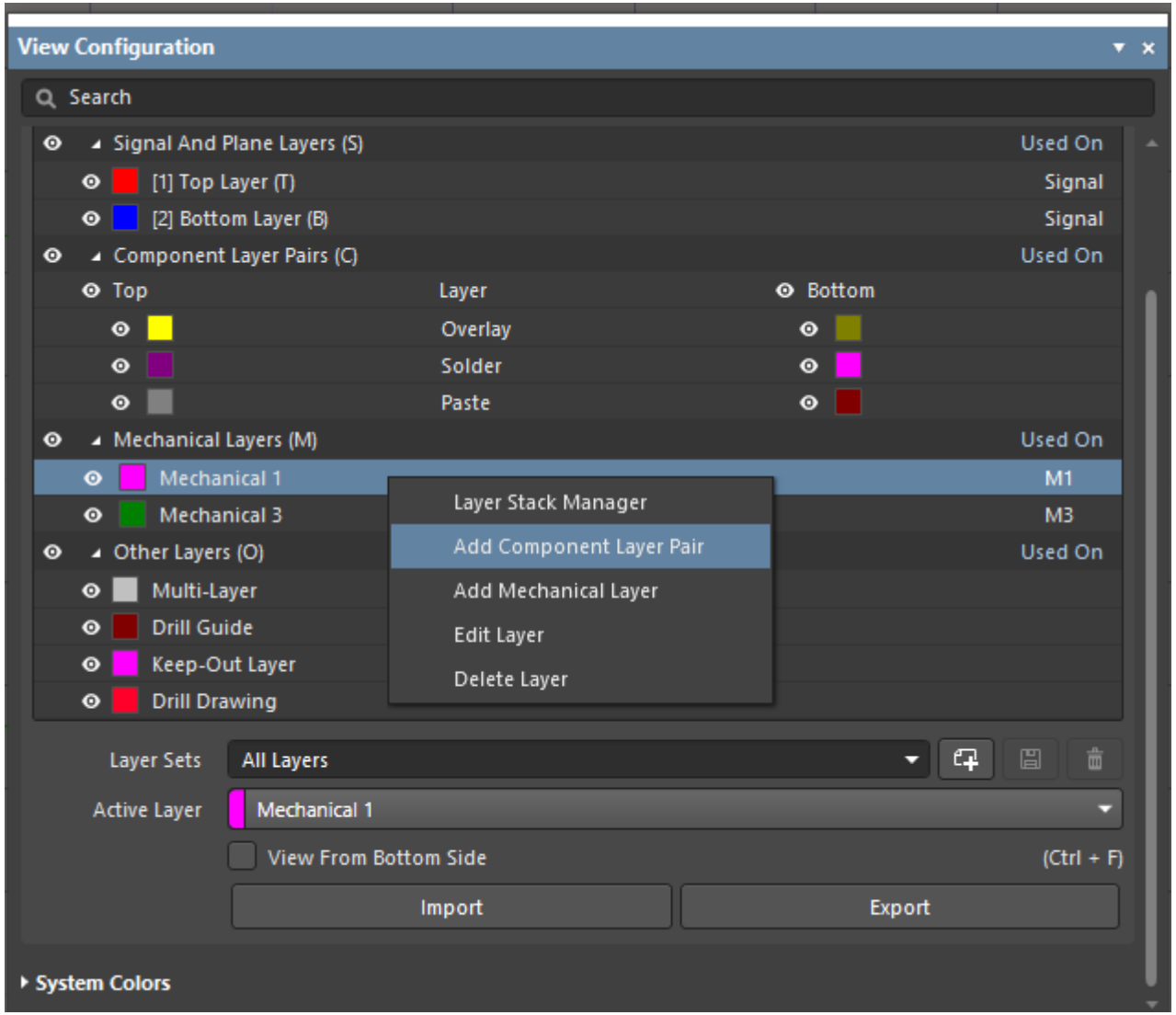




Cách 1

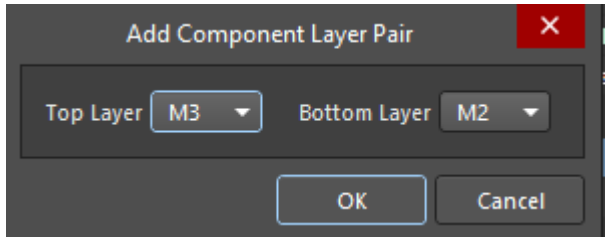
+ Bấm lệnh L

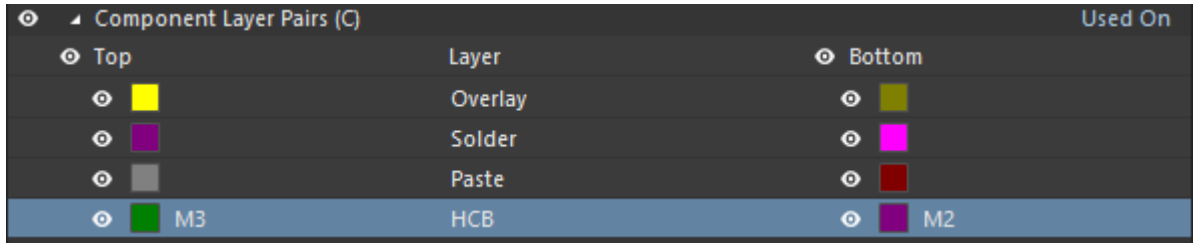
+ Vẽ HCB trước



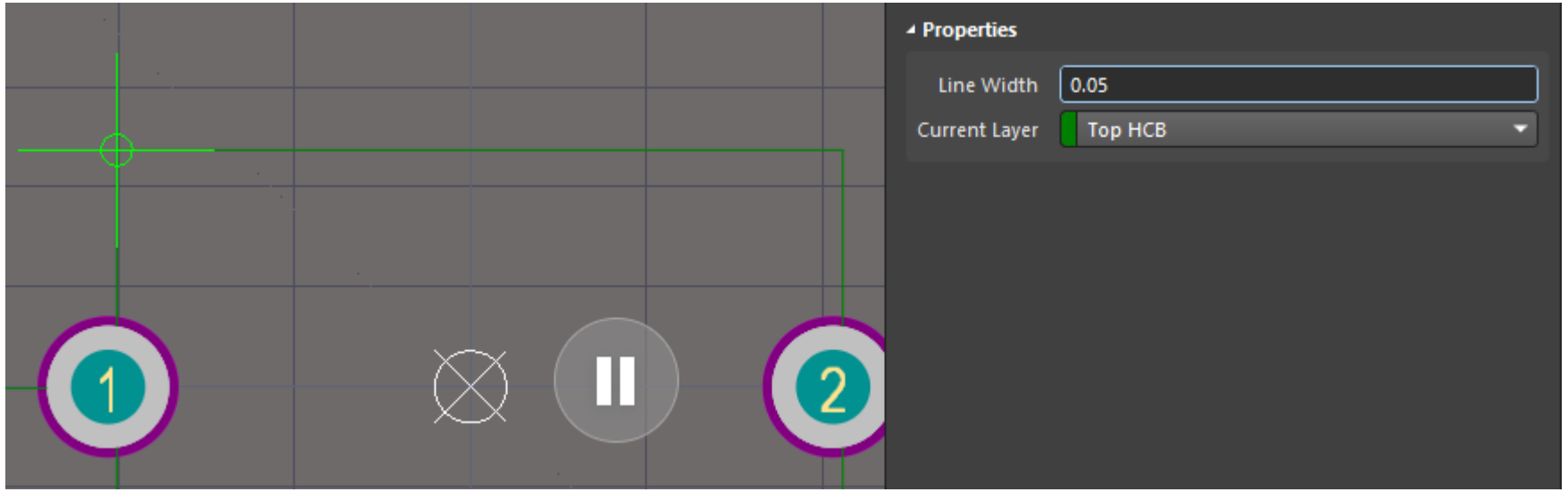
Thiết kế thư viện

Sửa tên thành HCB



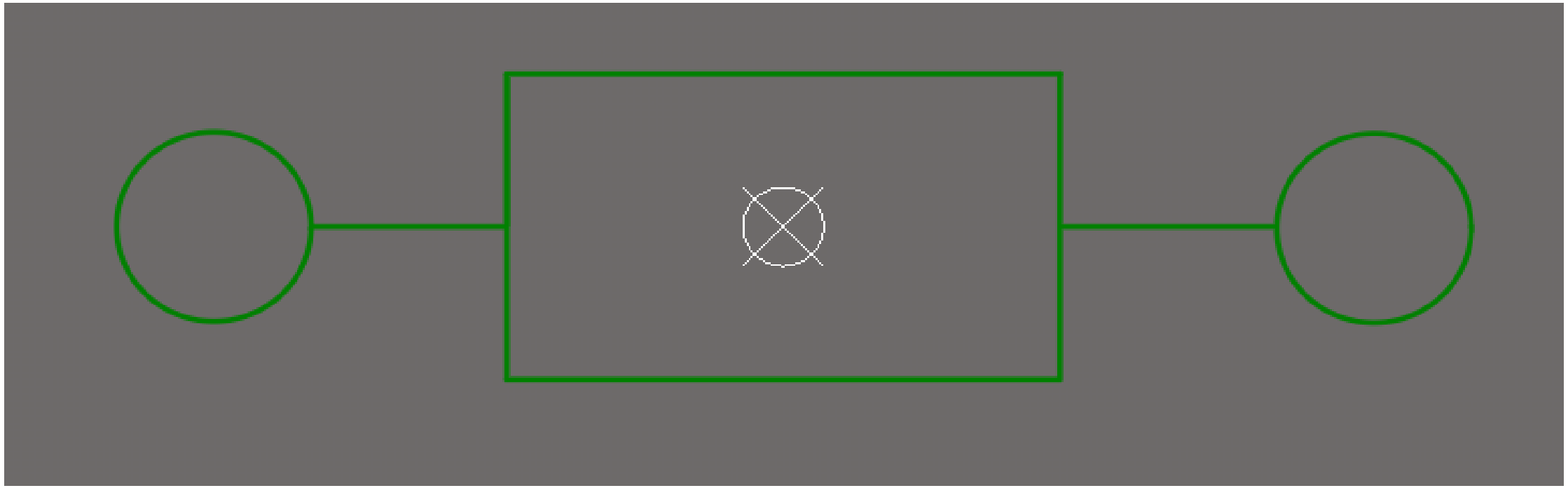


Chọn Line bấm Tab, độ dày luôn là 0.05



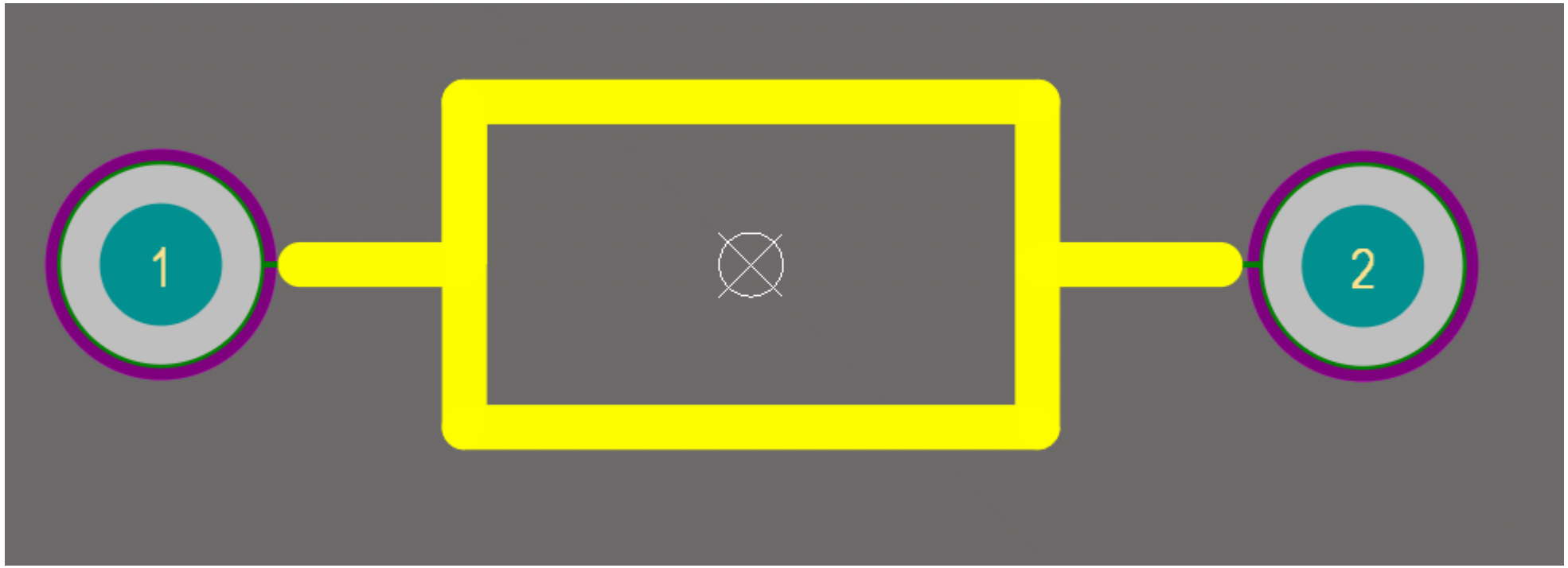
Thiết kế thư viện

Ctrl ship G : Thay đổi nhanh kích thước lưới
Ship S : Thay đổi kiểu nhìn



Thiết kế thư viện

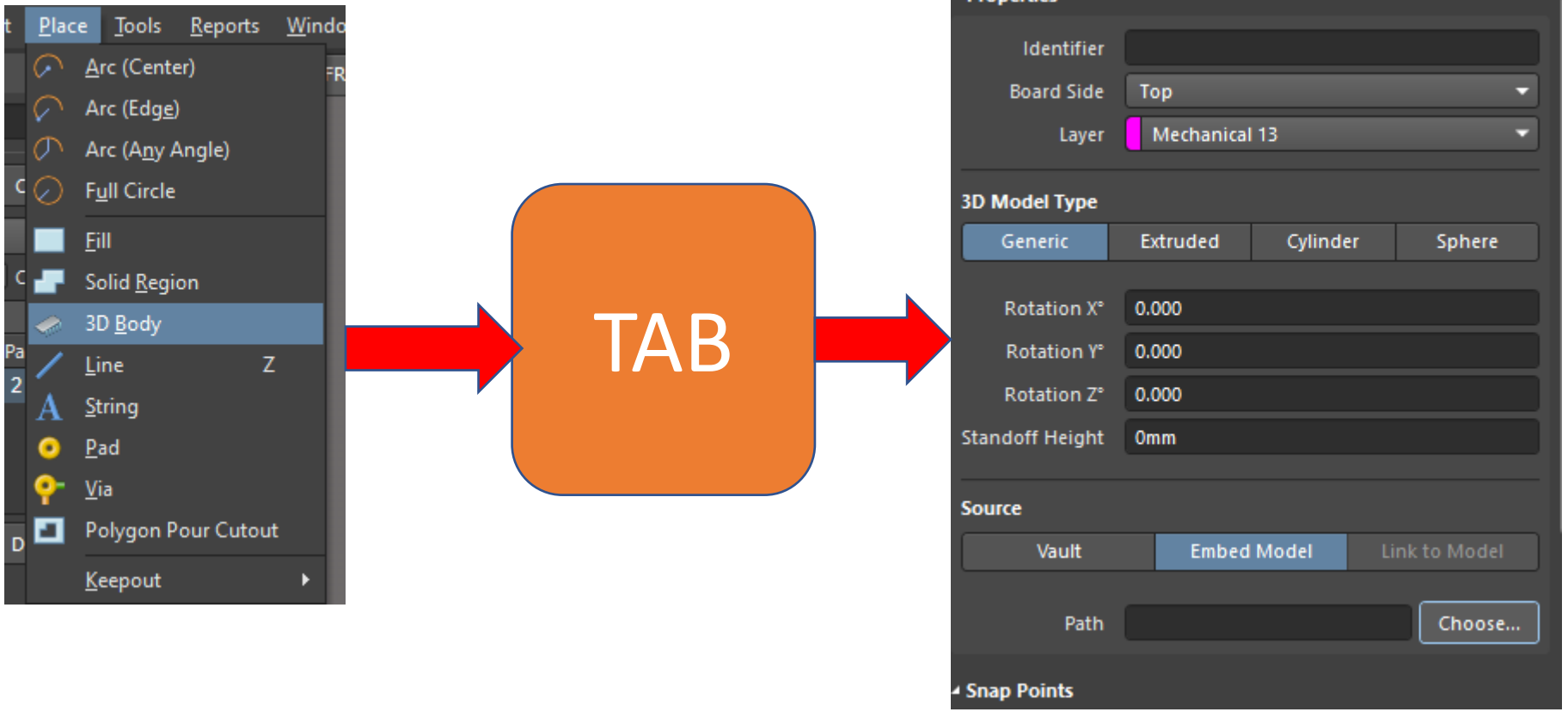
Copy nó 1 lần nữa và chuyển về layer TopOverlay với độ dày 0.3



OK

Thiết kế thư viện

+ Lên trang 3dcontent tải 3d về và add vào
+ Tạo them layer M13 để add 3D vào

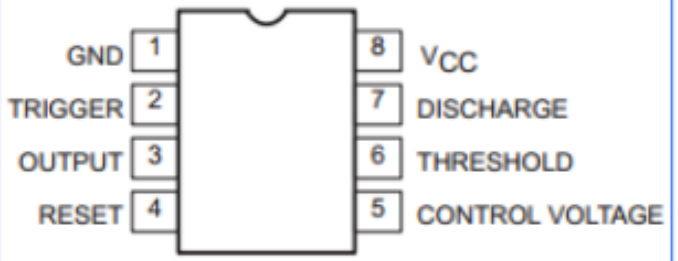


Hiệu chỉnh và OK

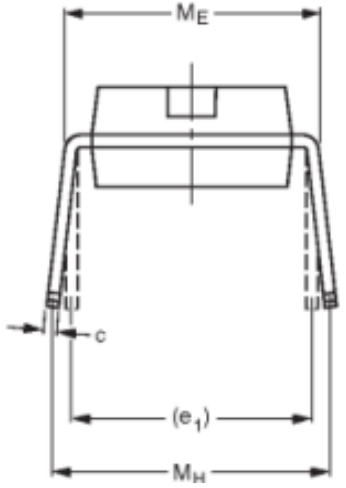
IC555

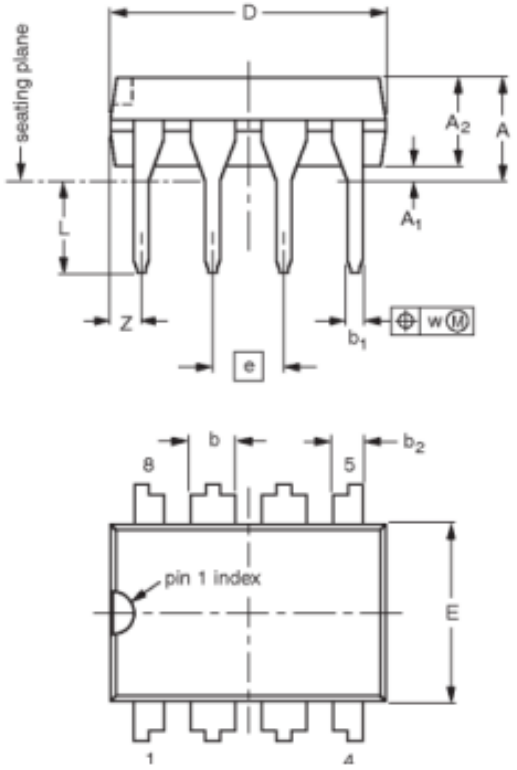
Ví dụ 4: LM555 DIP8

D and N Packages



SL00349



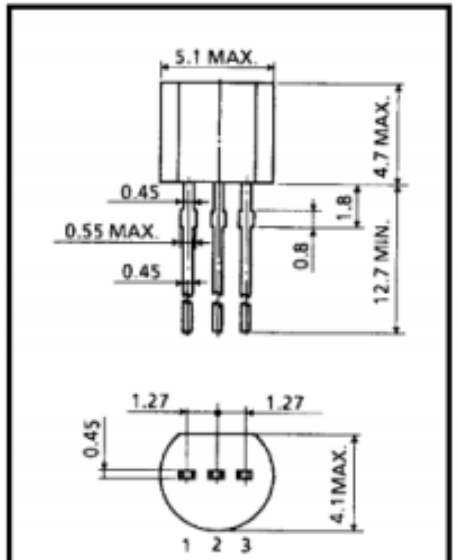


UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Thiết kế thư viện

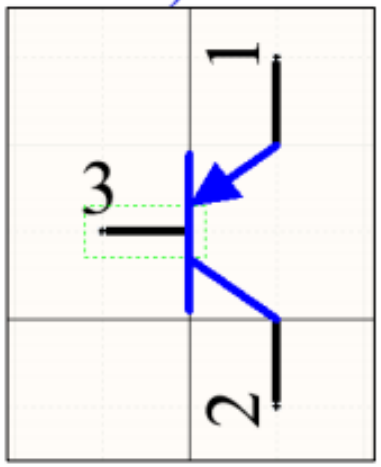
Ví dụ 2: 2SA1015 (TO-92)

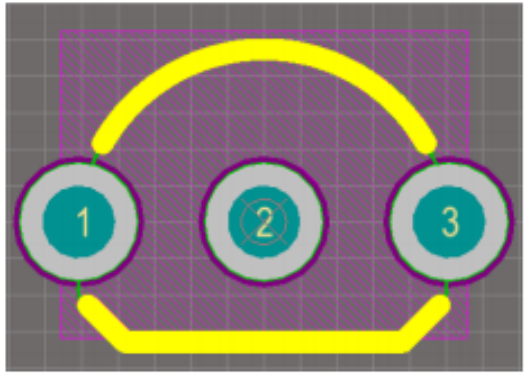
Unit: mm

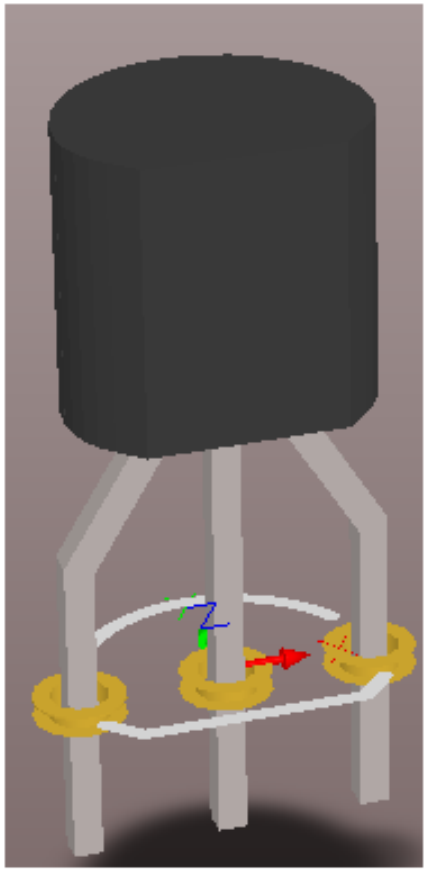


1. EMITTER
2. COLLECTOR
3. BASE

JEDEC	TO-92
JEITA	SC-43
TOSHIBA	2-5F1B

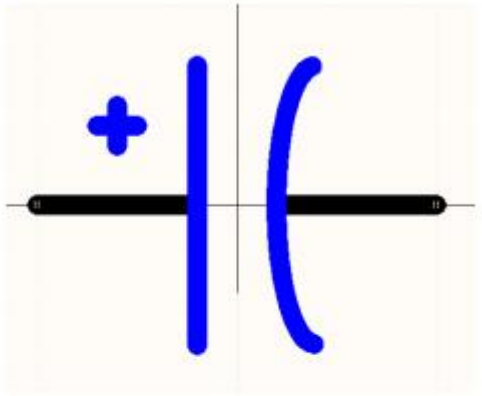


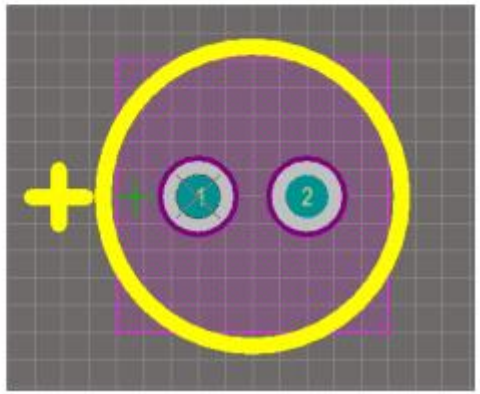




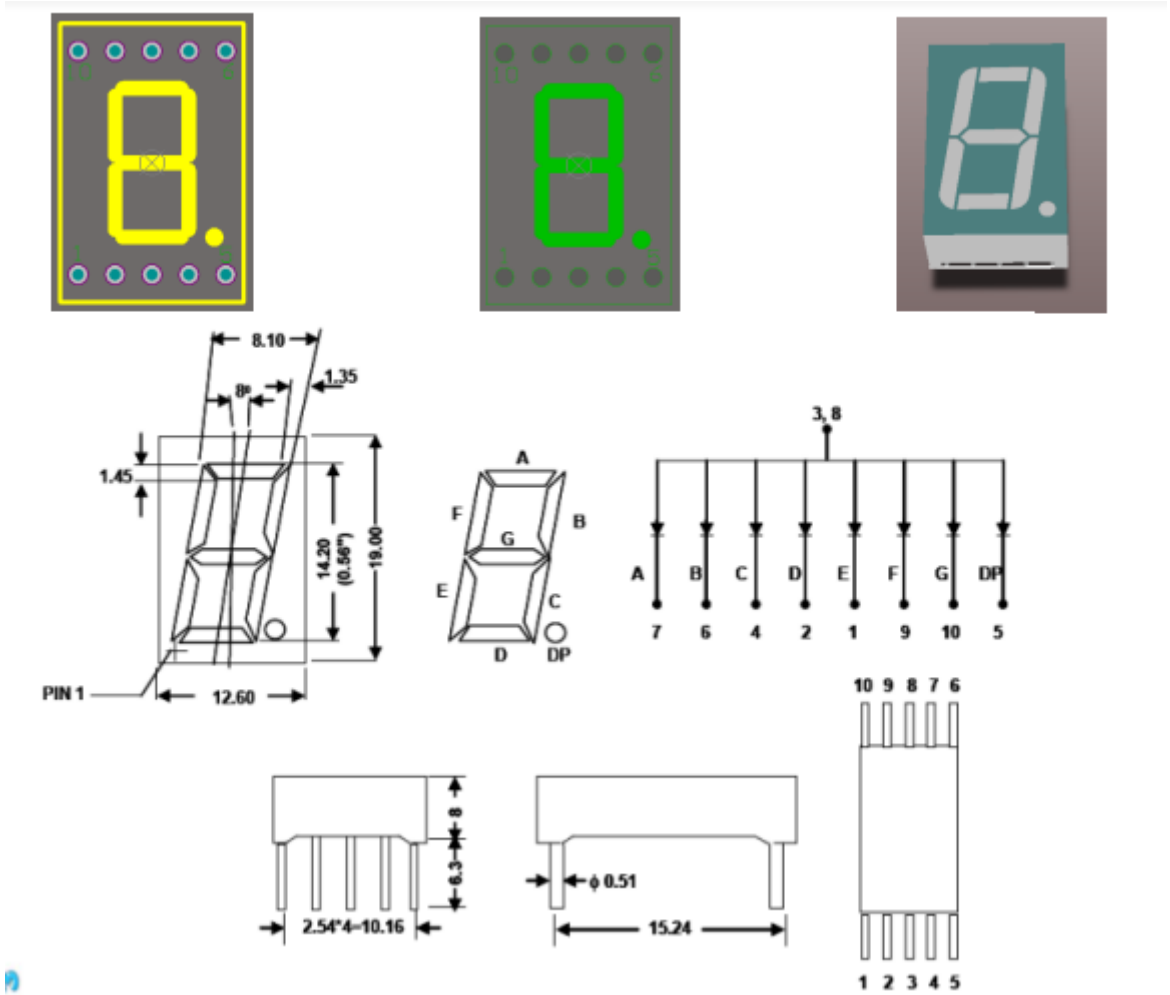
Thiết kế thư viện

Ví dụ 3: Aluminum 10uF 50V

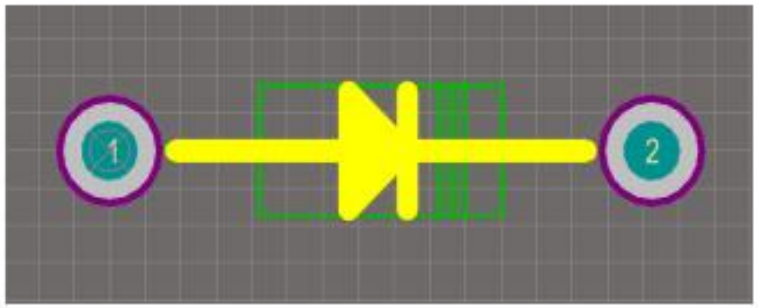


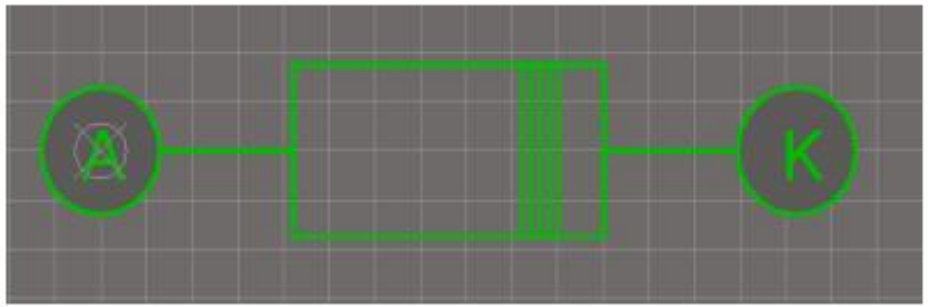


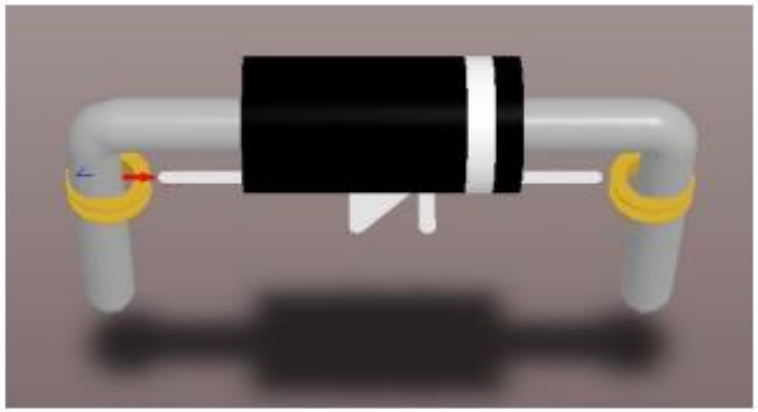
Thiết kế thư viện

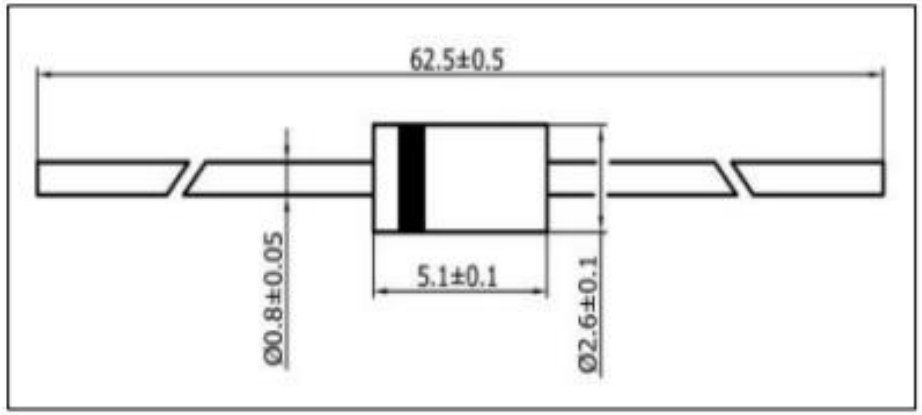


Thiết kế thư viện

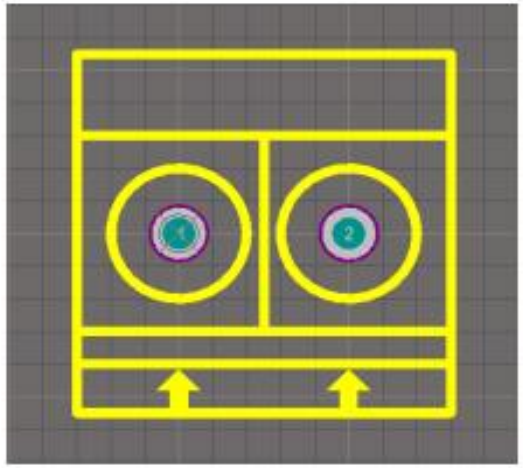


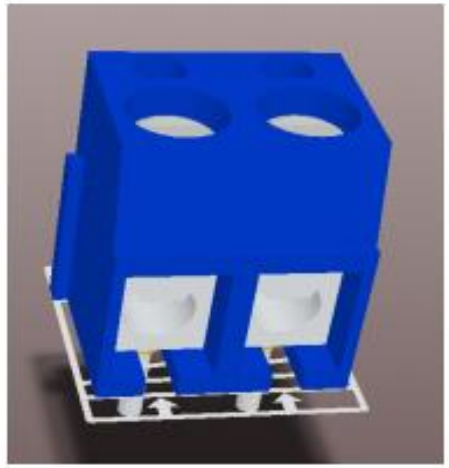


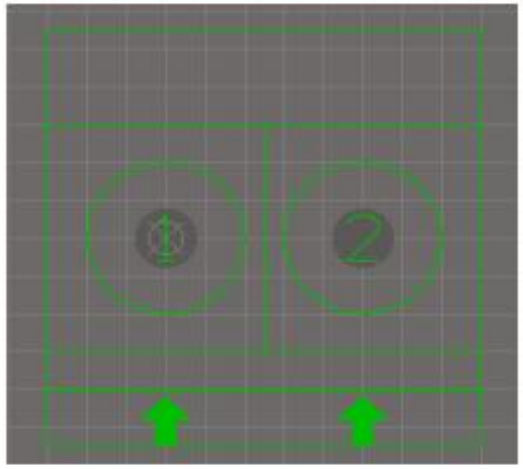




Thiết kế thư viện



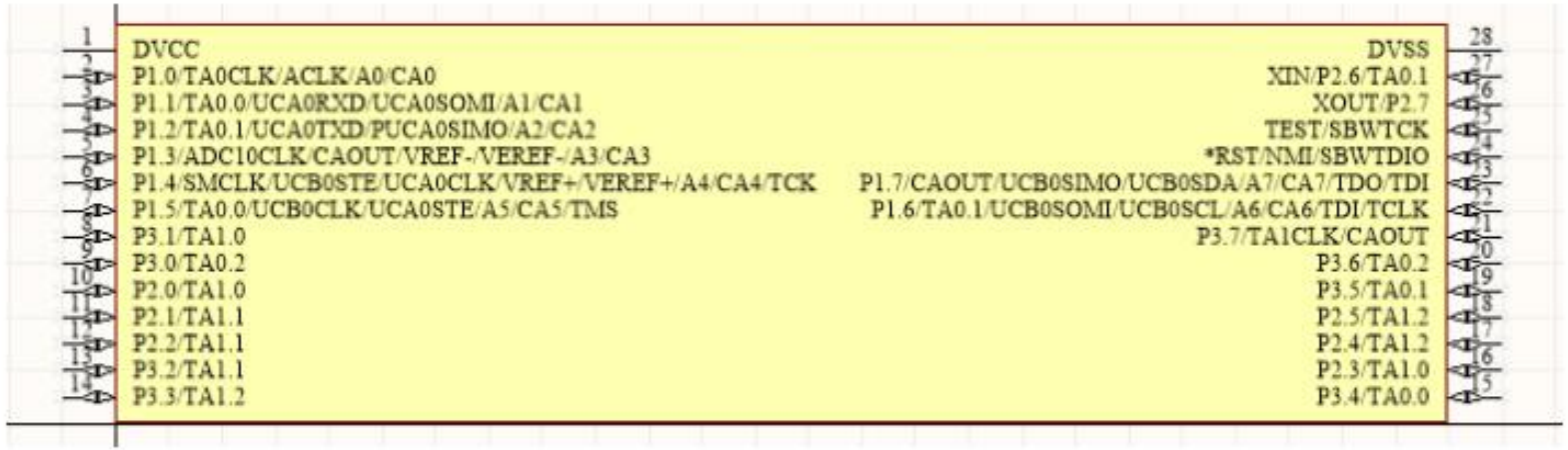


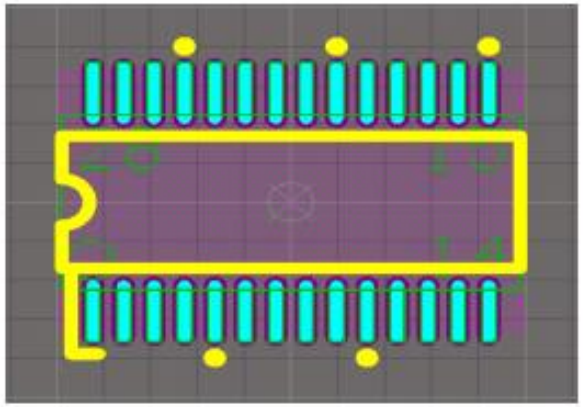


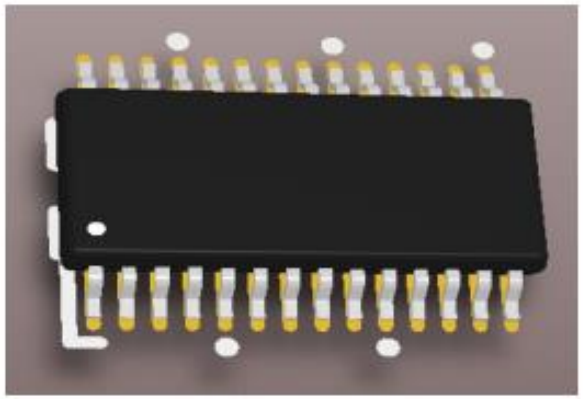
Chân dán

Loại 1 : Datasheet cho hết các thông số

Ví dụ 5: MSP430G2553 (PW-G28) (tt)

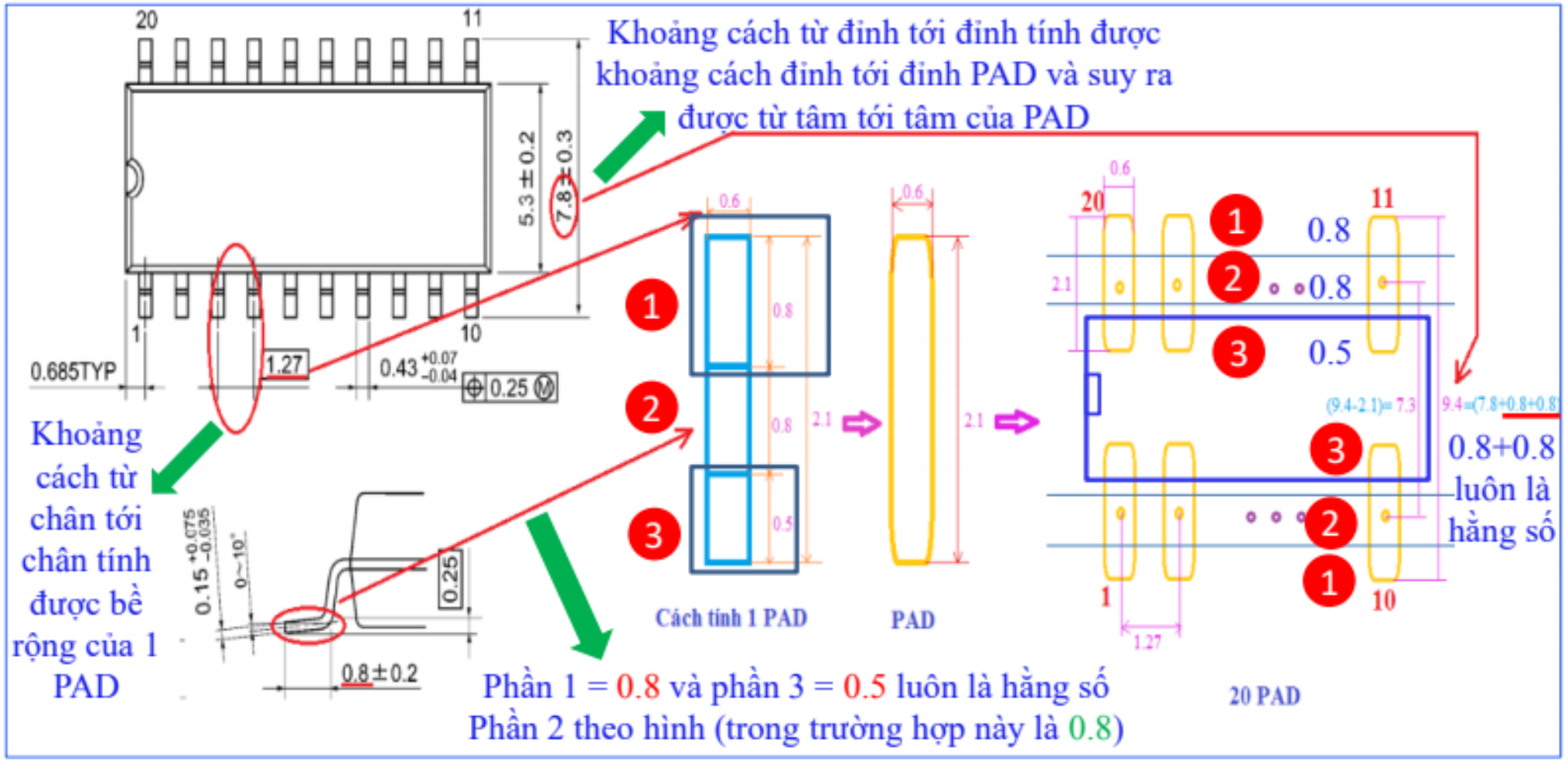






Chân dán

Loại 2 : Datasheet chưa cho



Chân dán

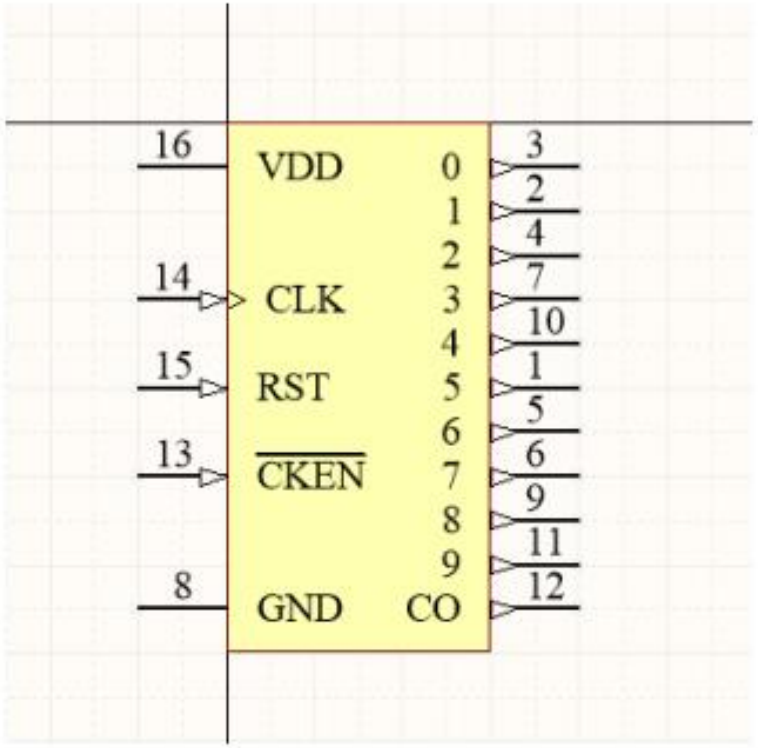
Loại 2 : Datasheet chưa cho

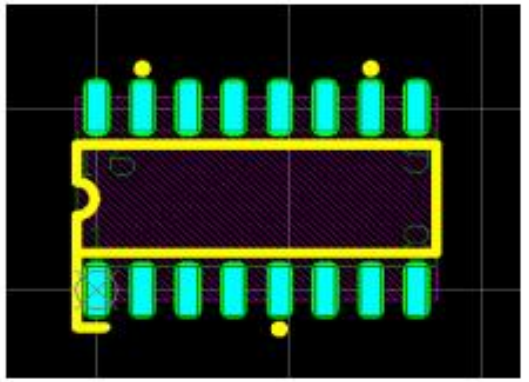
CÁCH TÍNH PAD CHO LINH KIỆN SMD

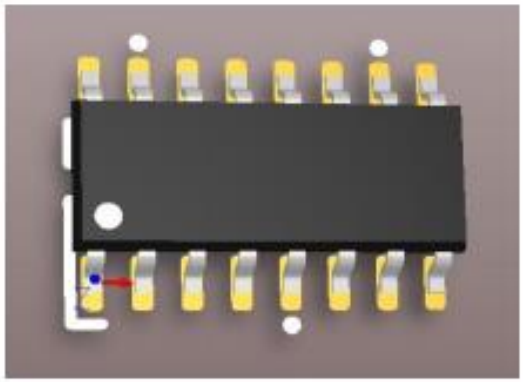
PIN PITCH(pin to pin) Khoảng cách từ chân tới chân	*PATTERN(PAD)* Top/Bot Layer	*RESIST* Top/Bot Solder	*MASK* Top/Bot Paste
0.4mm	0.2	0.3	0.2
0.5mm	0.3	0.4	0.3
0.55mm	0.35	0.45	0.35
0.6mm	0.4	0.5	0.4
0.635mm	0.4	0.5	0.4
0.8mm	0.5	0.7	0.5
1.0mm	0.6	0.8	0.6
Ví dụ 1.27mm	0.6	0.8	0.6

Thiết kế thư viện

Ví dụ 6: 74HC4017 (SO16-SOT109-1) (tt)

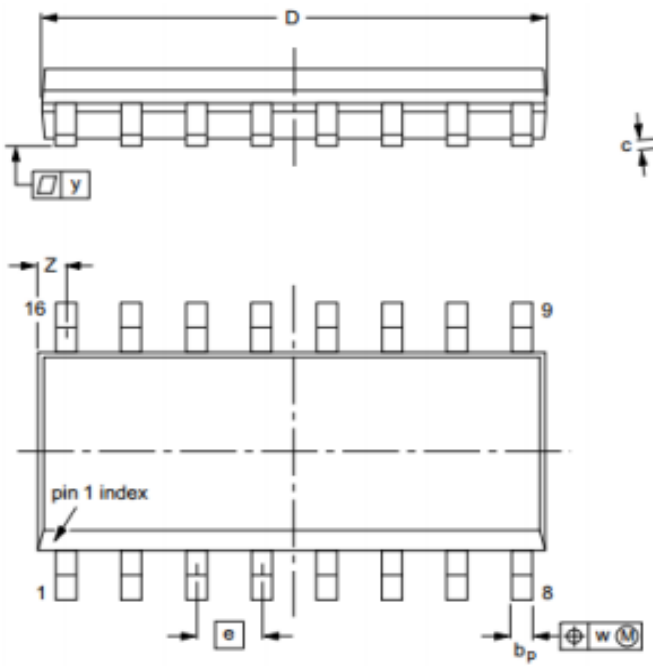






Thiết kế thư viện

Ví dụ 6: 74HC4017 (SO16-SOT109-1)



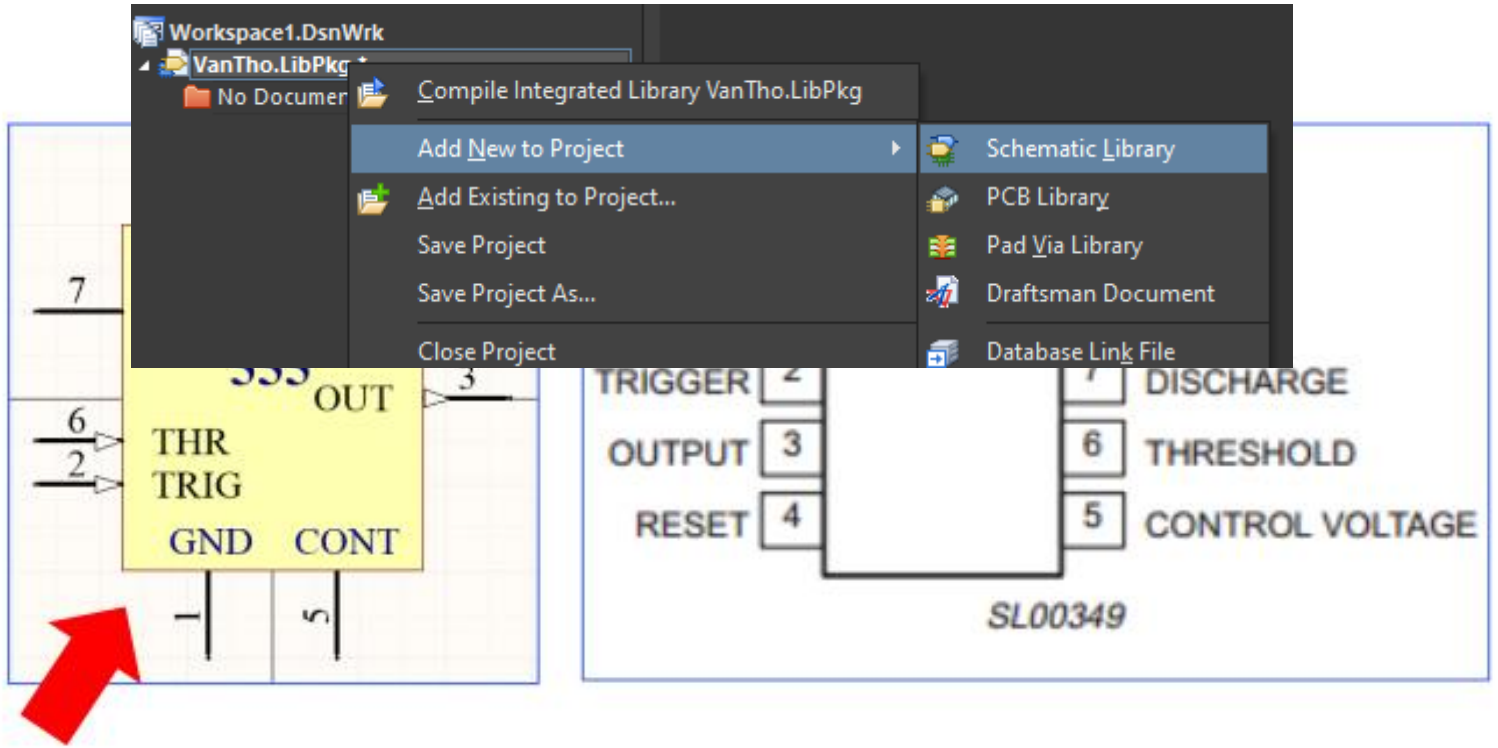
Chú ý: Đường bao của linh kiện như chiều dài, chiều rộng, chiều cao lấy MAX, các thông số còn lại lấy trung bình.

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

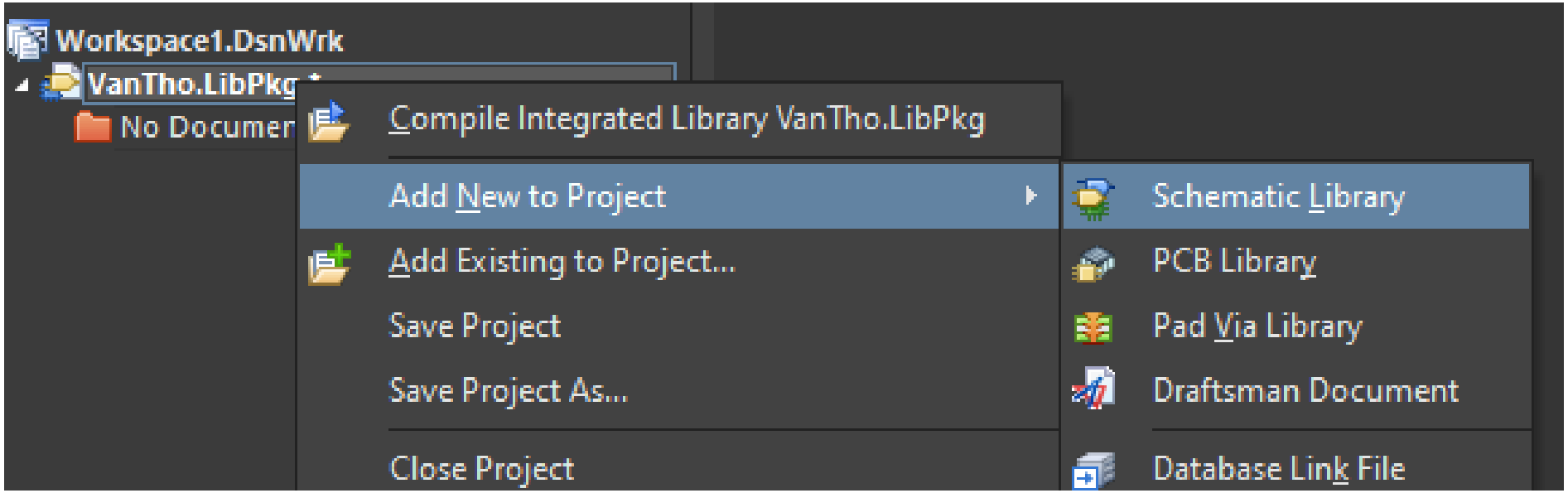
Thiết kế thư viện nguyên lý

Ví dụ 3: NE555 DIP8 (tt)

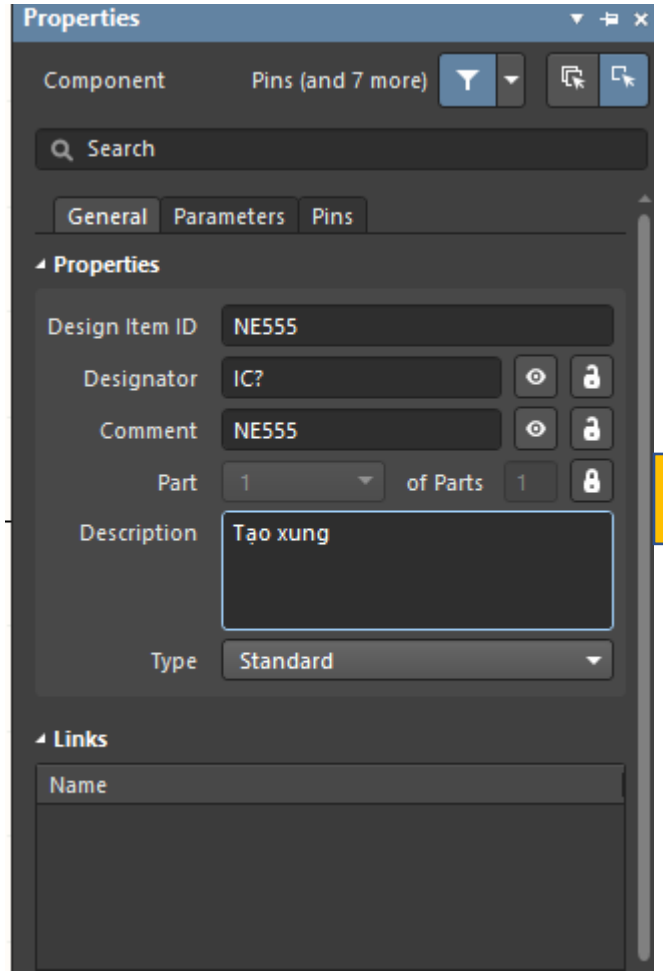


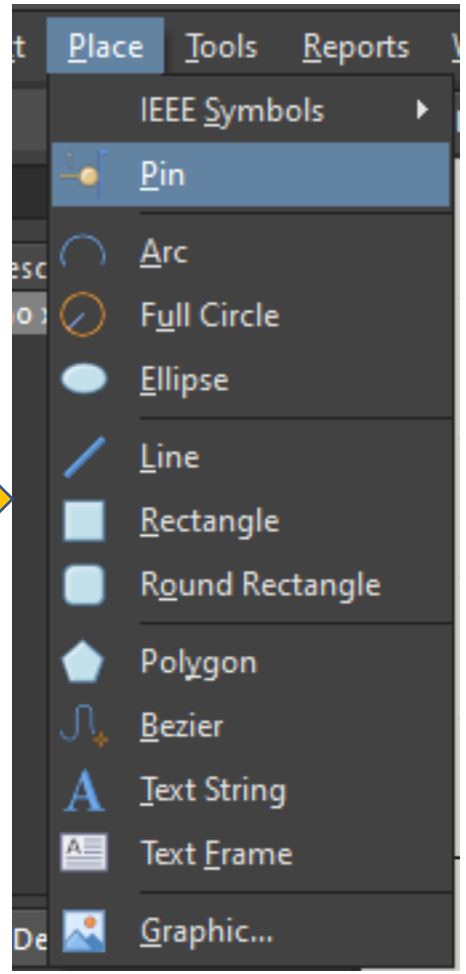
Thiết kế thư viện nguyên lý

- Kiểu thiết kế thư viện nguyên lý theo chân linh kiện
- Kiểu thiết kế thư viện nguyên lý theo chức năng

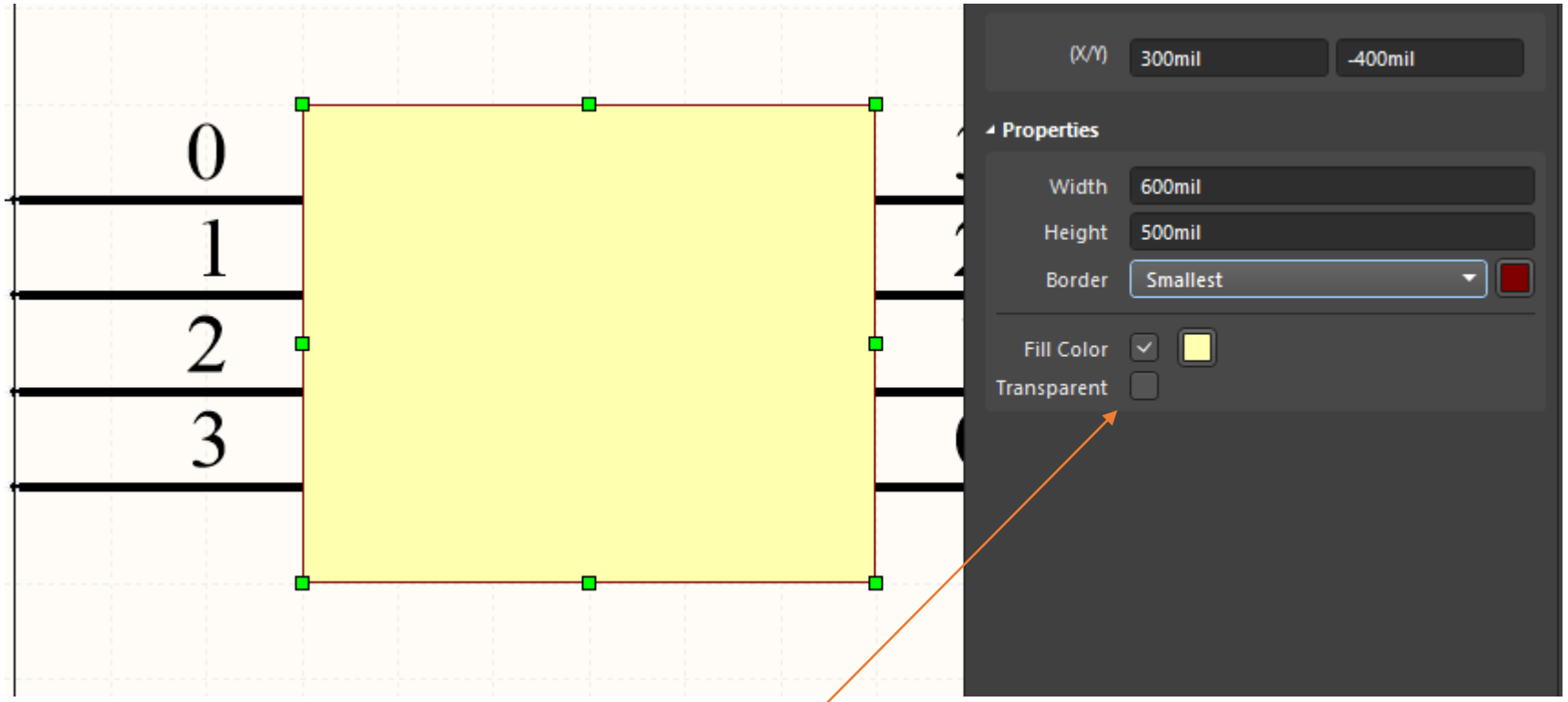


Thiết kế thư viện nguyên lý



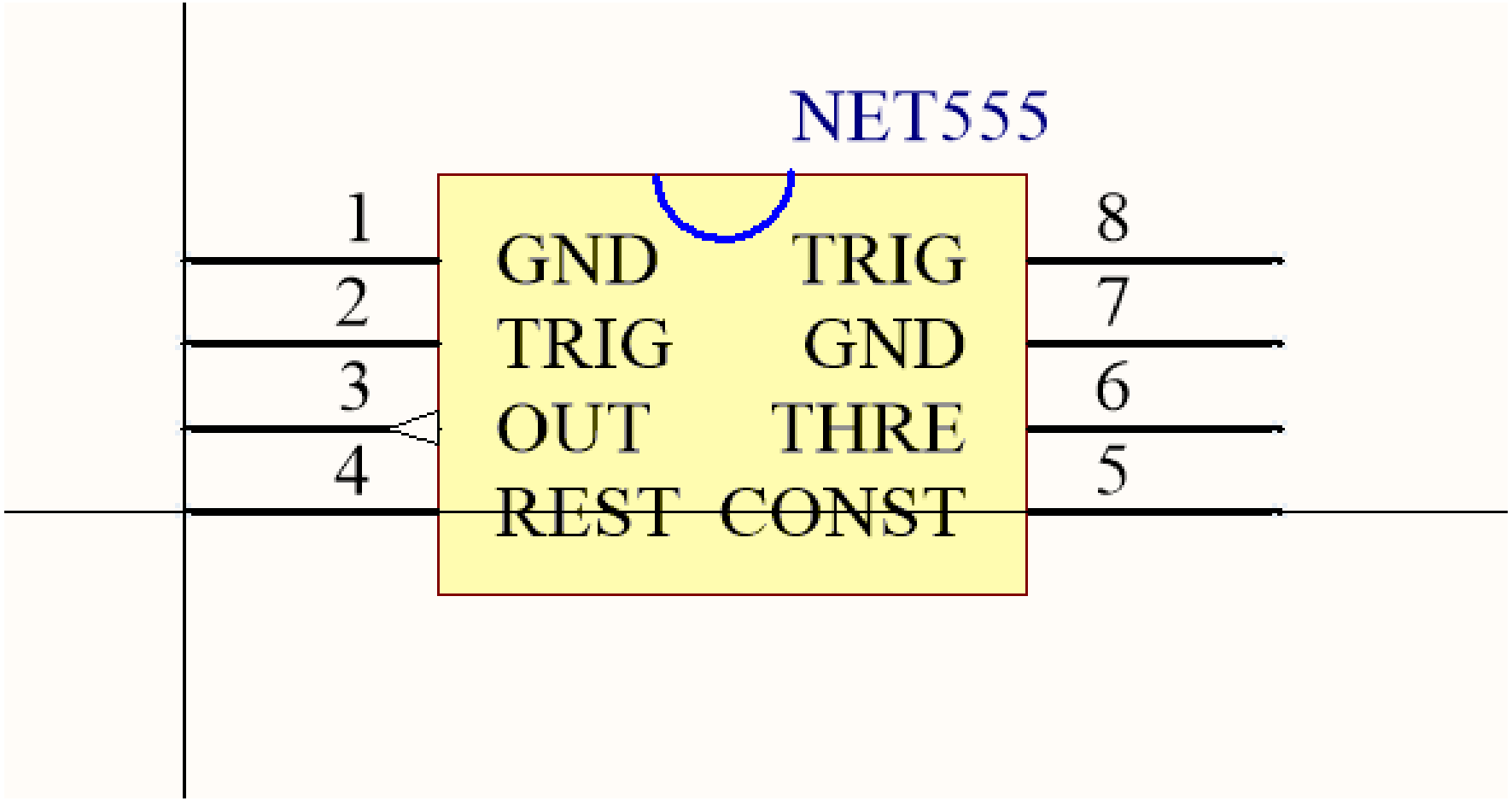


Thiết kế thư viện nguyên lý



Click vào Transparent

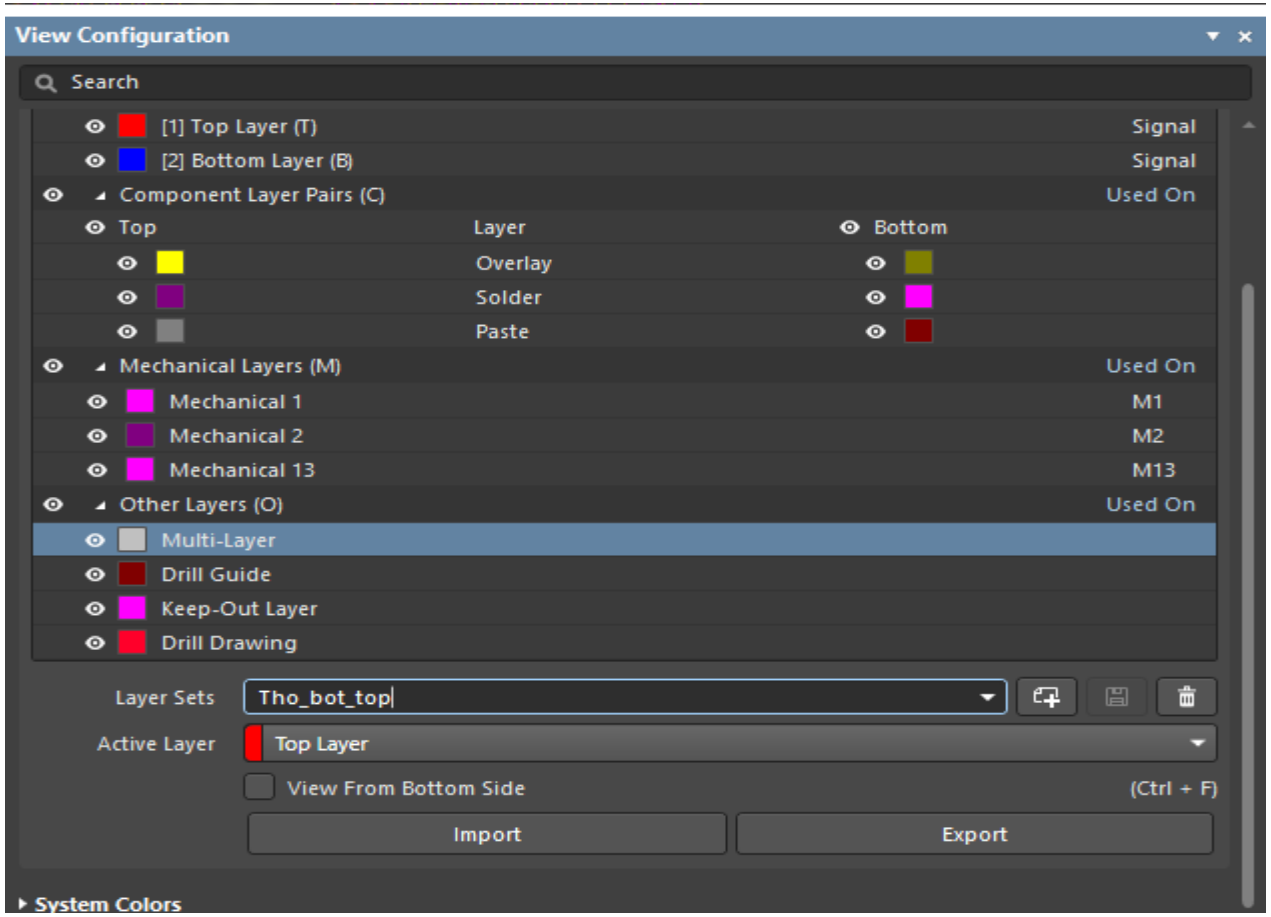
Thiết kế thư viện nguyên lý



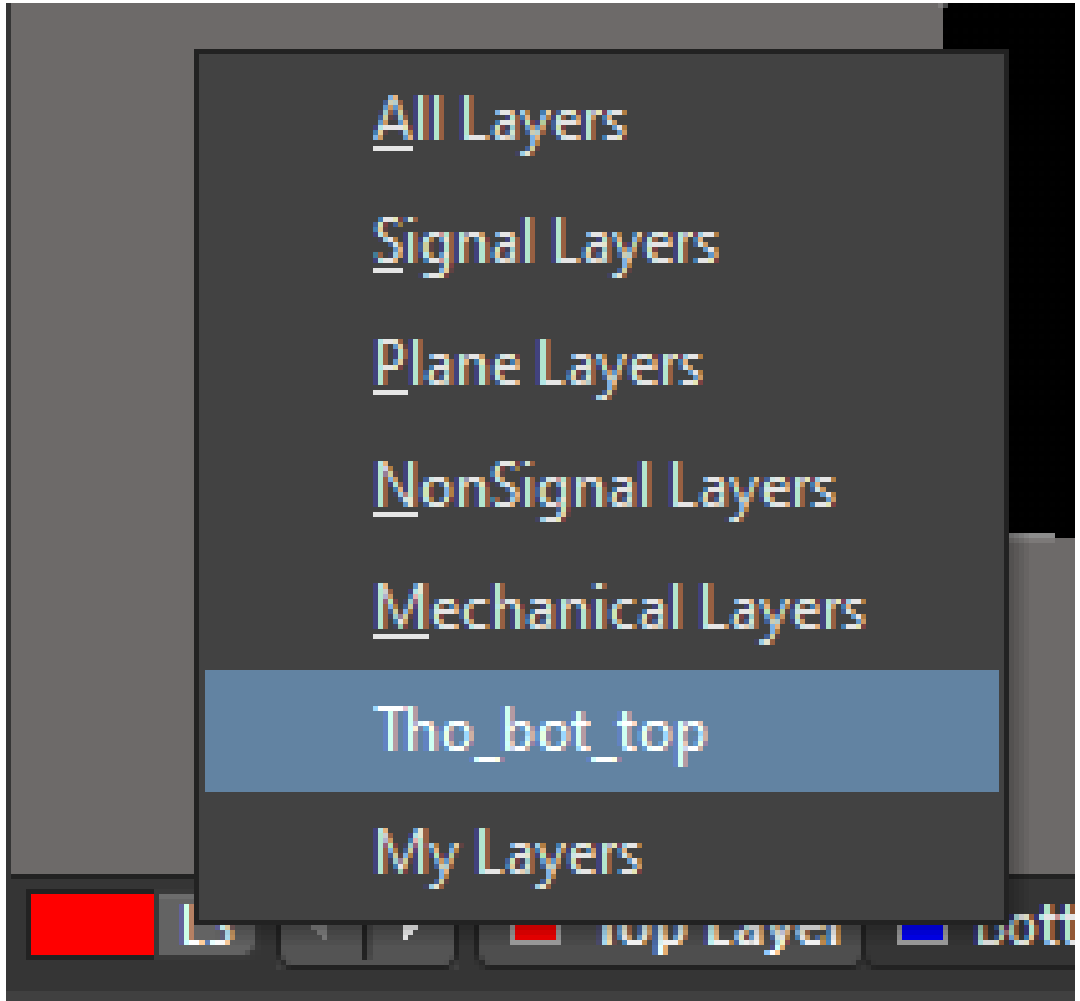
Tạo layer-set

- Giúp nhìn nhanh linh kiện, đỡ rối mắt
- Tăng tốc độ đi dây

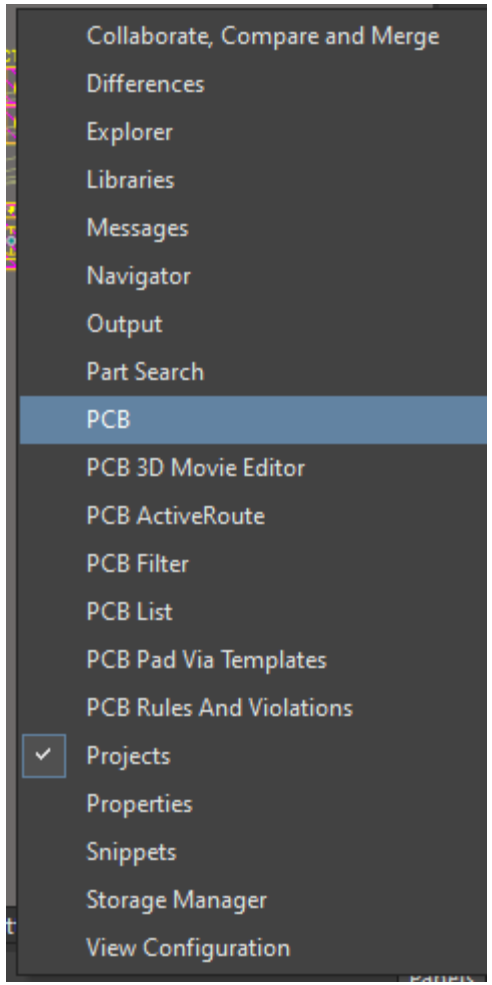
1. Bấm L
2. Tạo new layer-set
3. Đặt tên và ẩn hiện các layer theo mong muốn

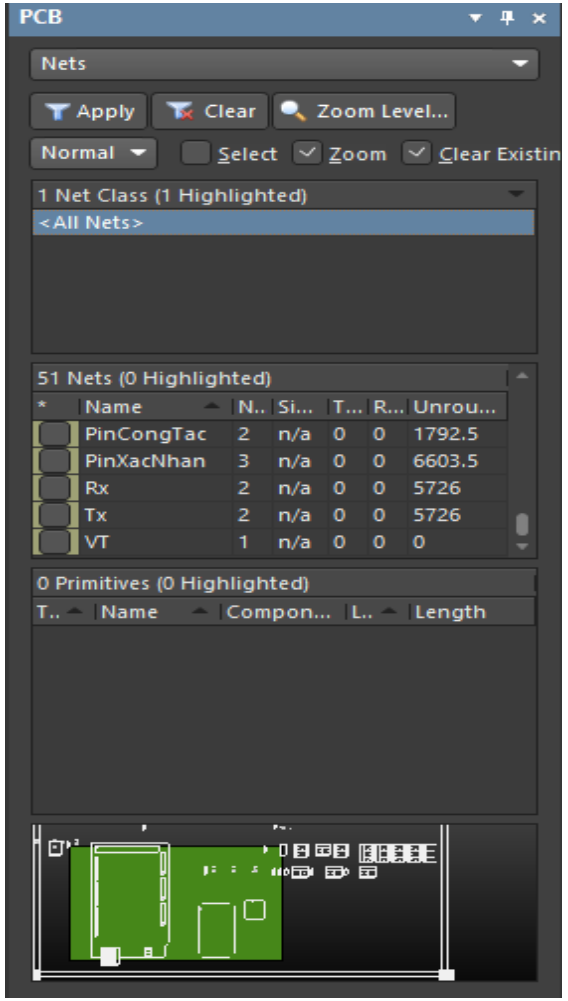


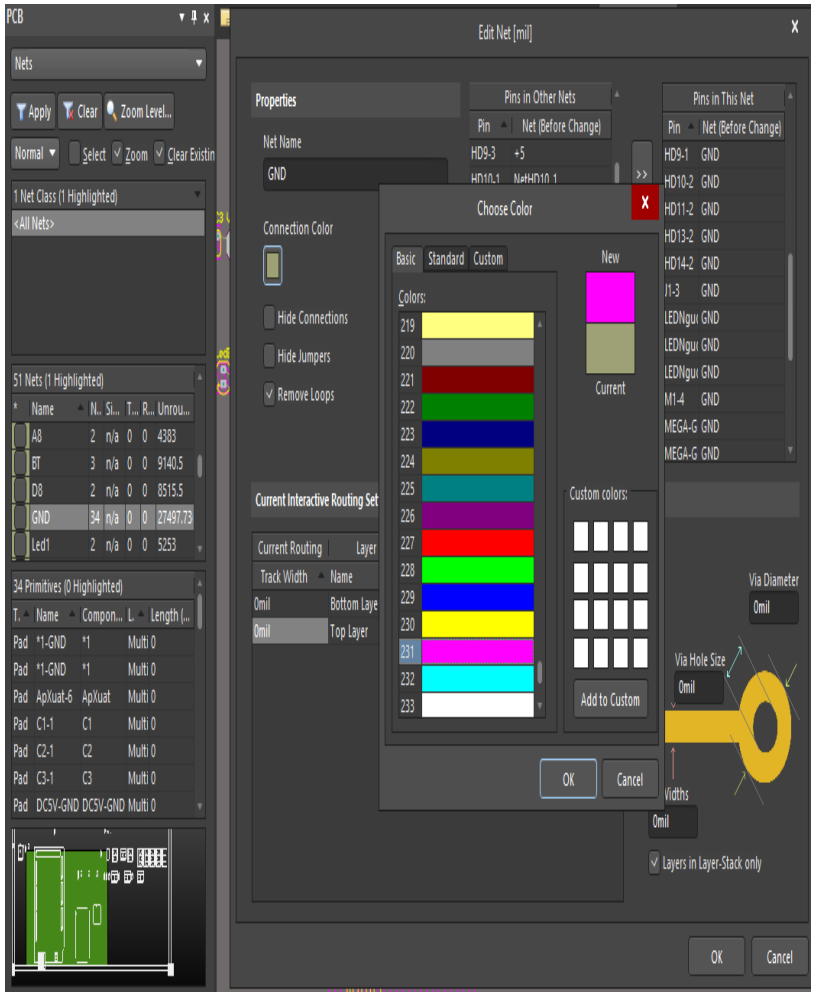
Tạo layer-set



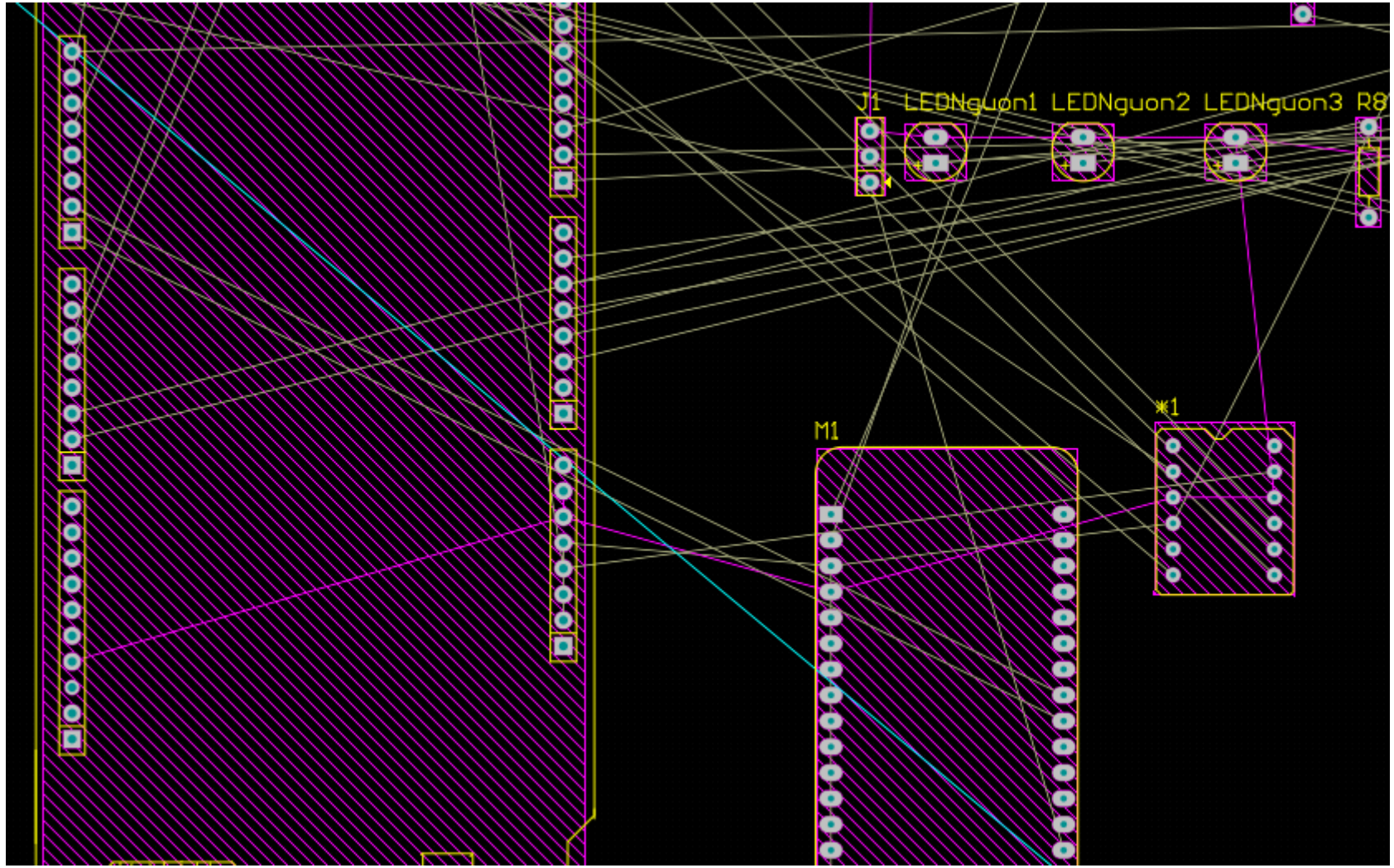
Đổi màu đường dây





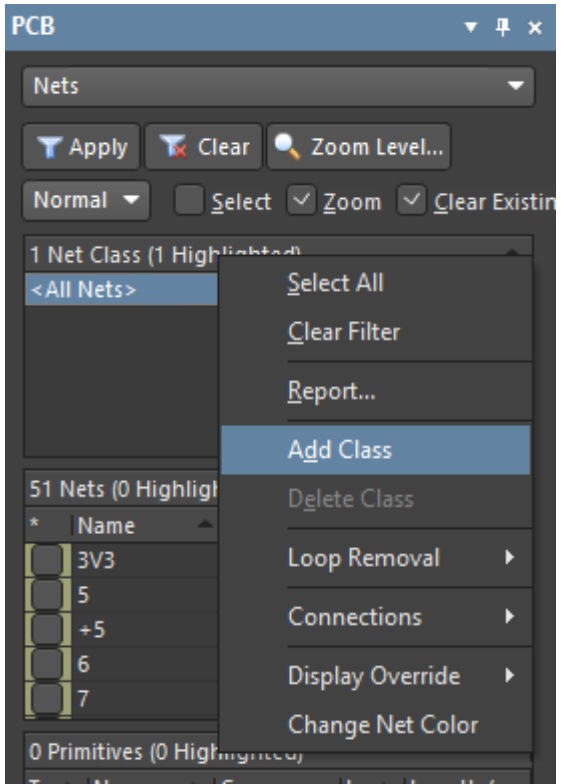


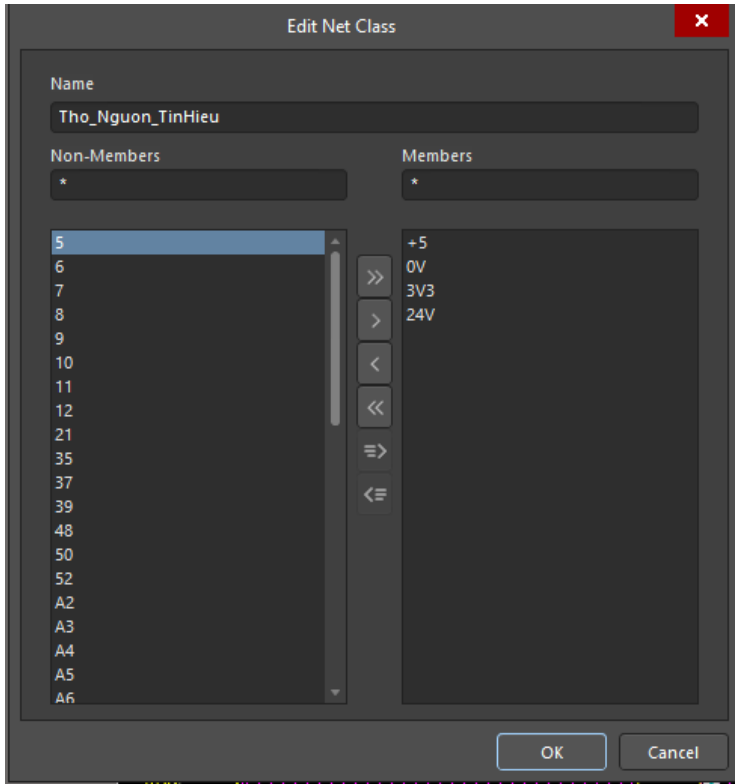
Đổi màu đường dây

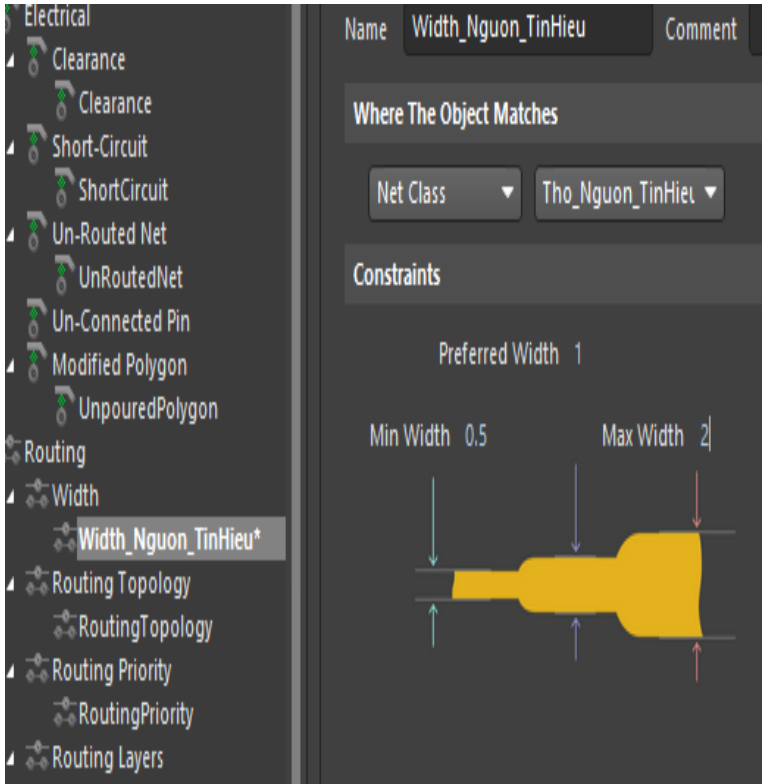


Tạo Net_Class

- Quản lý các nét rõ ràng hơn
- Tập hợp các nét cần to hơn
- Không phải vào chọn lại độ dày của nét

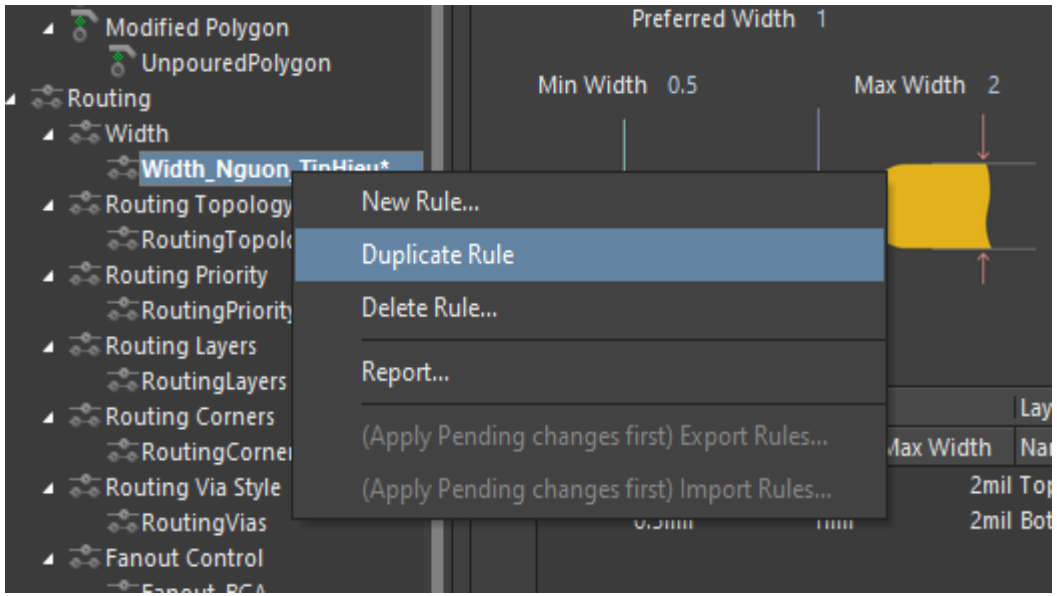


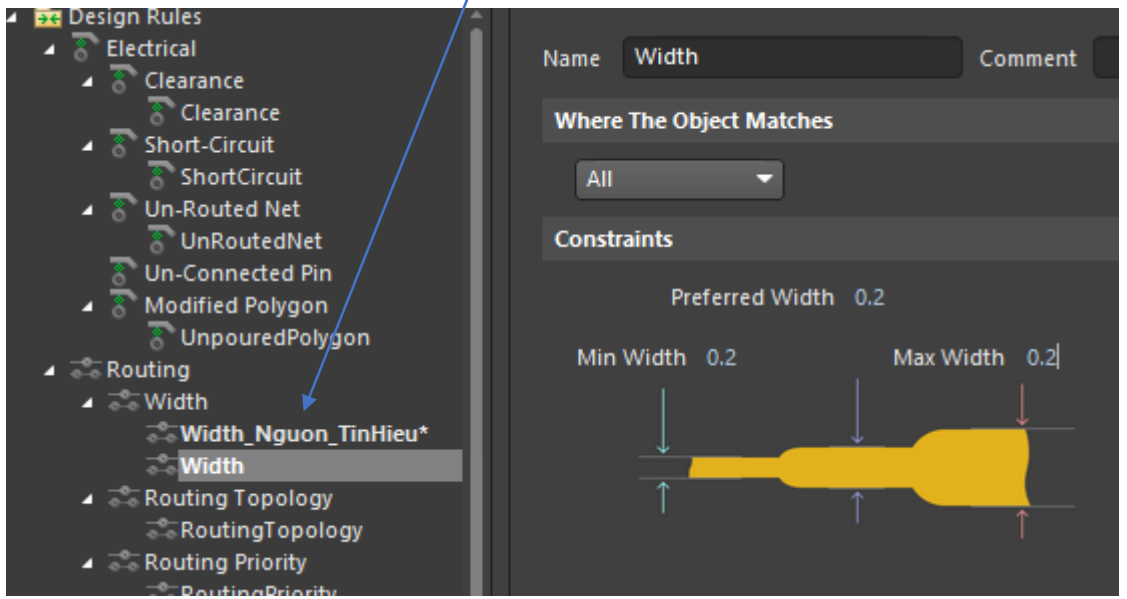




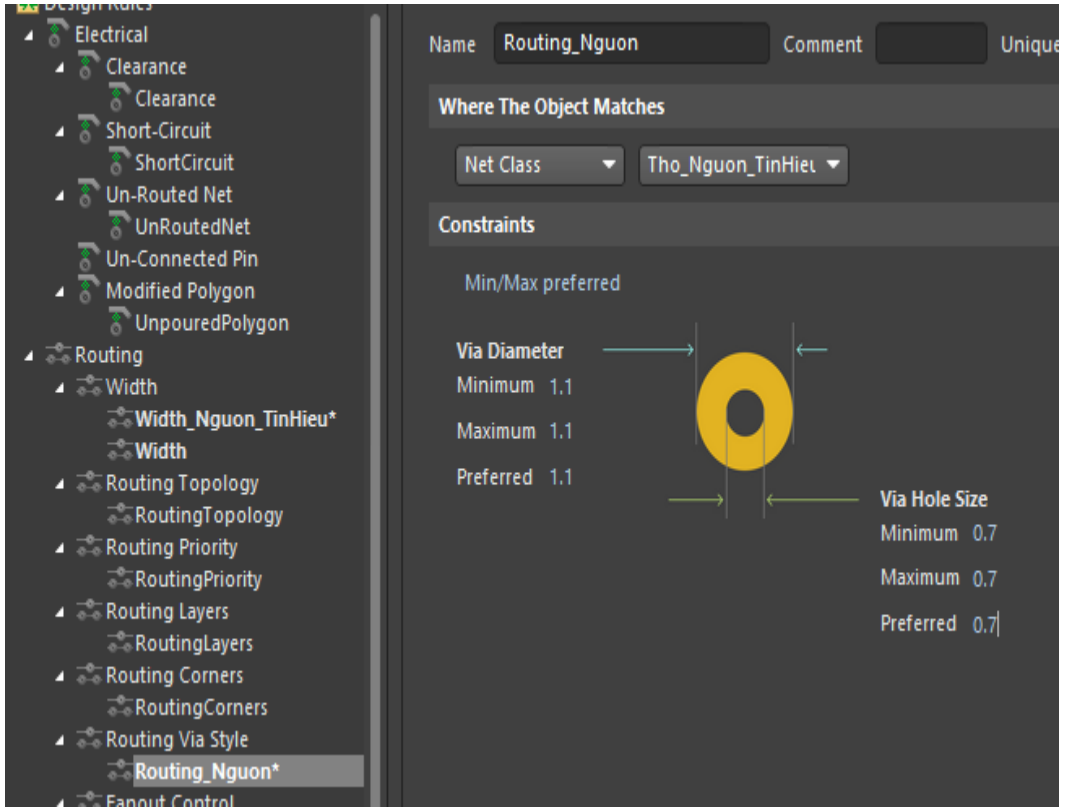
Tạo Net_Class

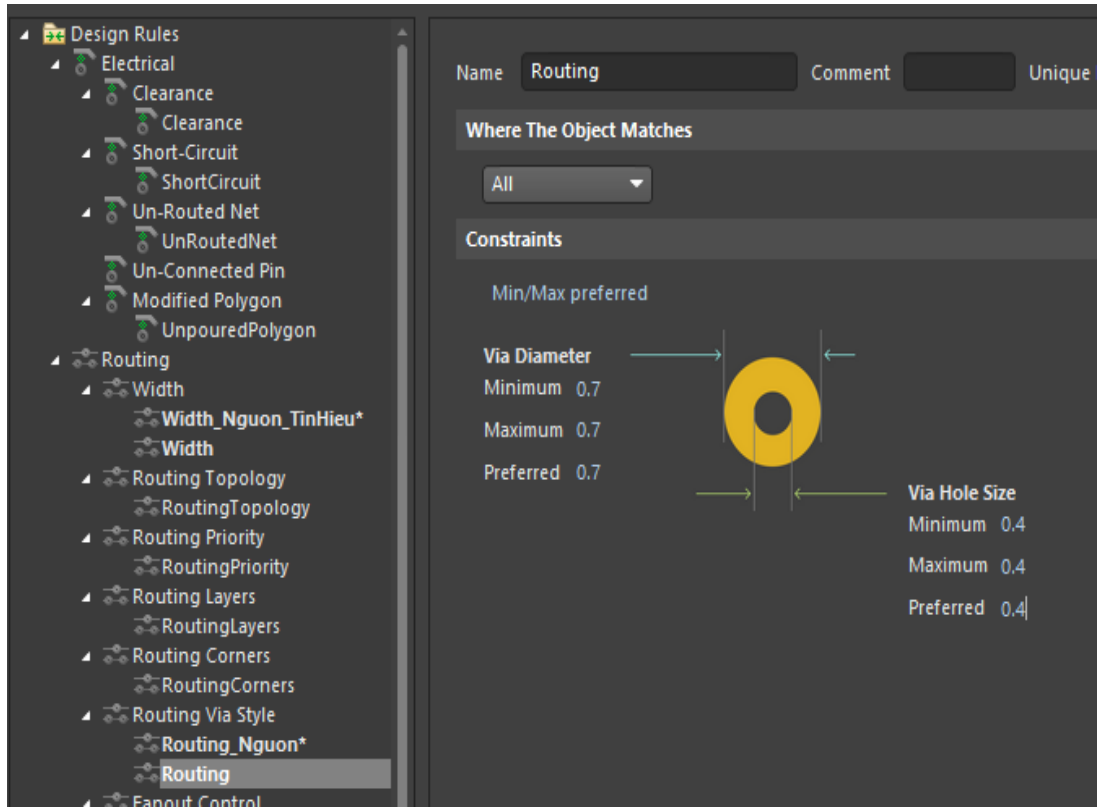
Độ ưu tiên ?





Tạo Net_Class





XONG

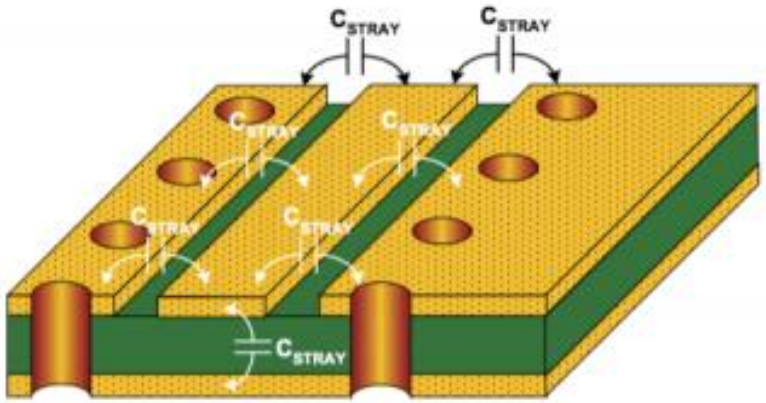
Hight Speck

NOTE

Stray Capacitance

Stray Capacitance is Good and Bad

- Good because it helps form a characteristic impedance (Z0) when desired.
- Bad because it causes capacitance when a characteristic impedance is NOT desired. This can slow down a signal or cause an amplifier to ring or oscillate.
- Dominated by Layer-to-Layer Capacitance due to Surface Area. Trace Height (thickness) is very small (0.001" typ.), thus small area and capacitance.



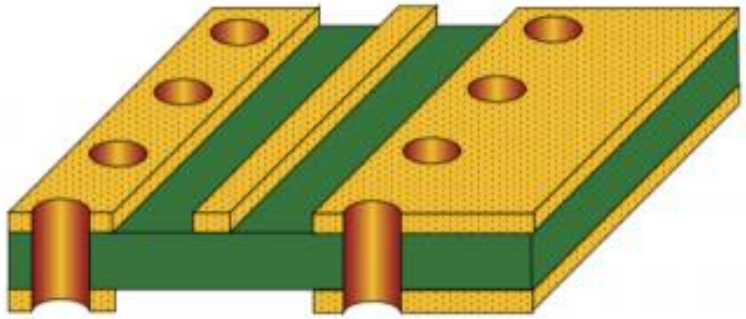
Hight Speck

NOTE

Stray Capacitance - Reducing

Possible Solutions

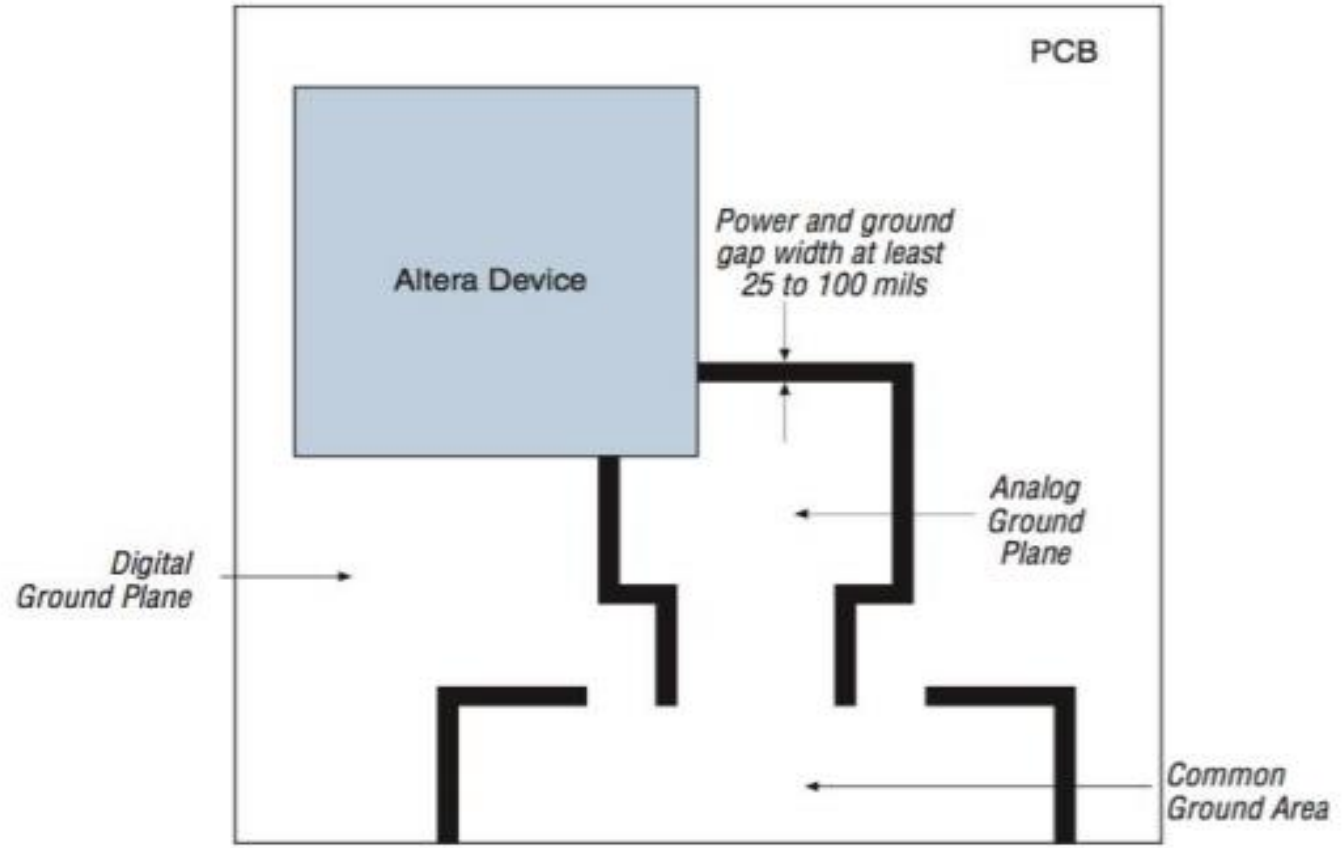
- If trace is NOT a characteristic impedance, reduce it's width. Not too much or else inductance can increase too much.
- Remove the GND plane under the trace. Connect the planes elsewhere.
- Increase distance between trace and same-Layer GND plane.



Hight Speck

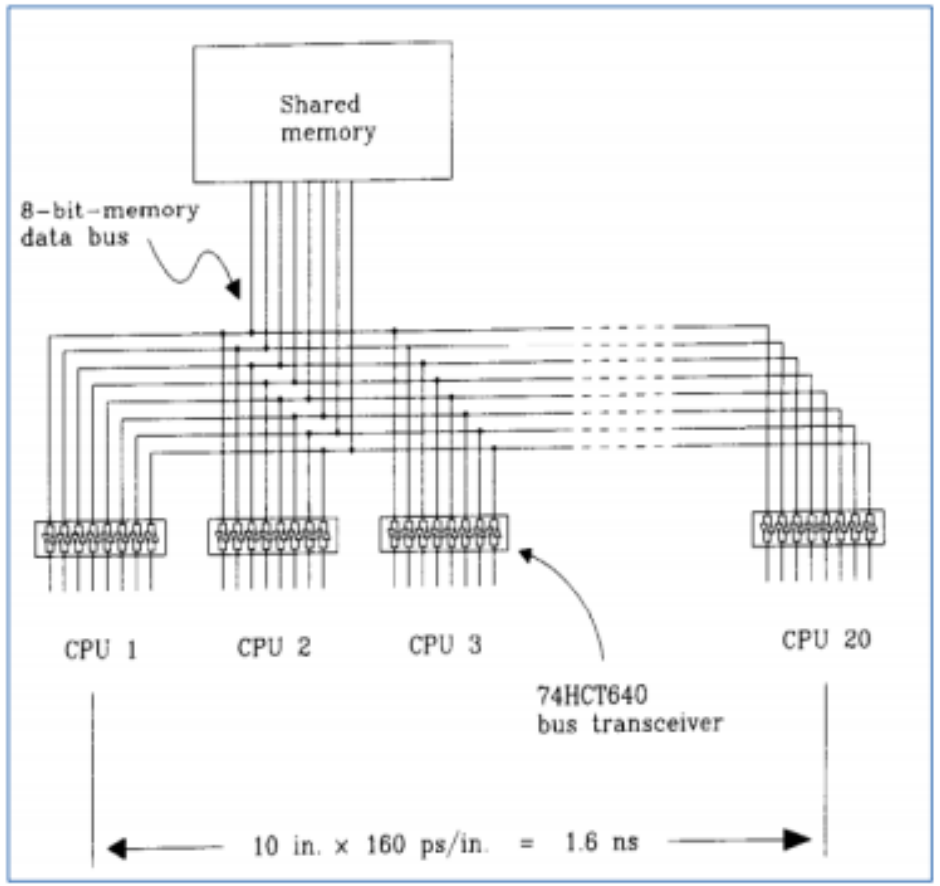
NOTE

Figure 11–35. Board Layout for General-Purpose PLL Ground Islands



Hight Speck

+ Việc truyền tín hiệu để CPU nhận cùng 1 lúc



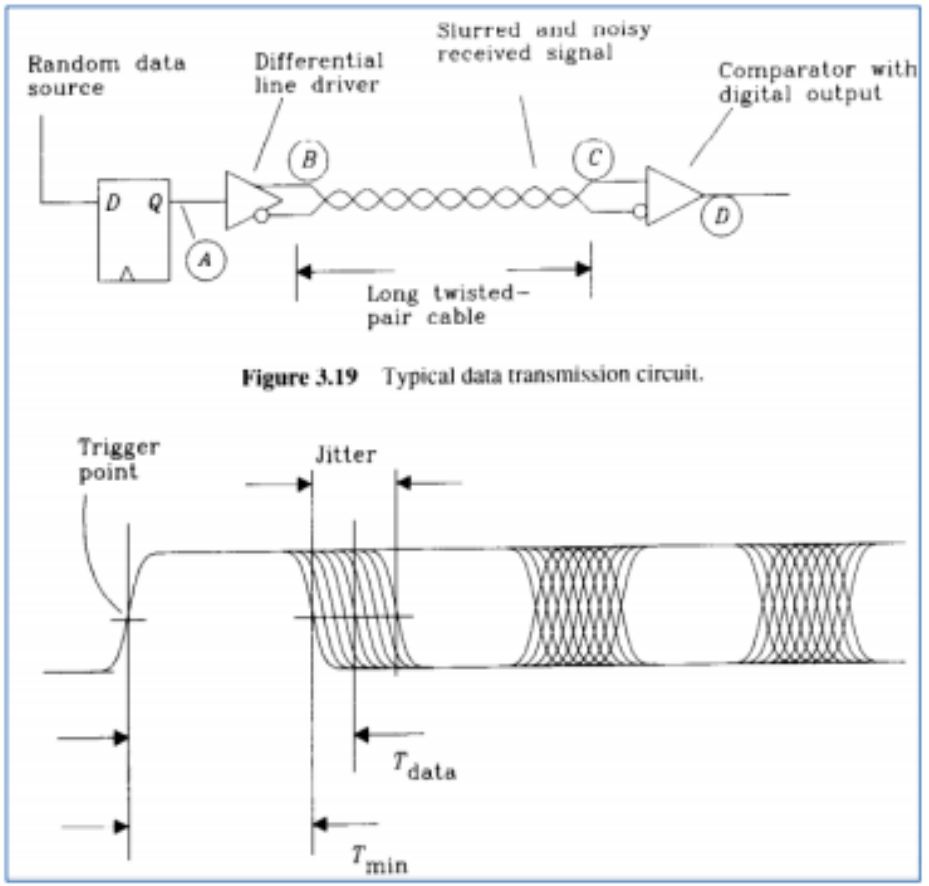


Figure 3.19 Typical data transmission circuit.

Hight Speck

+ Việc truyền tín hiệu để CPU nhận cùng 1 lúc

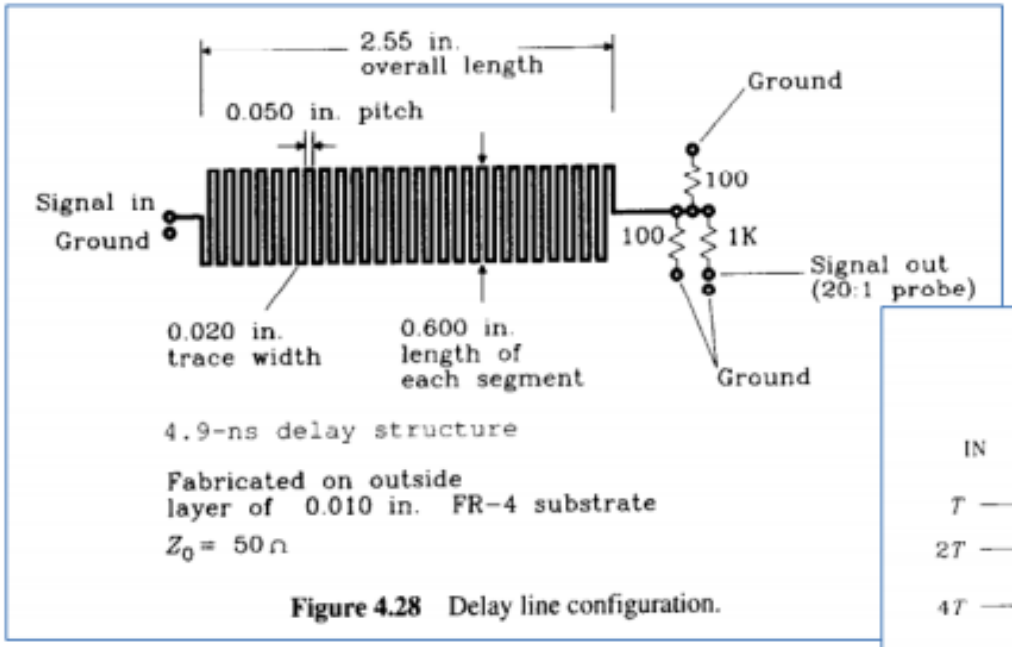


Figure 4.28 Delay line configuration.

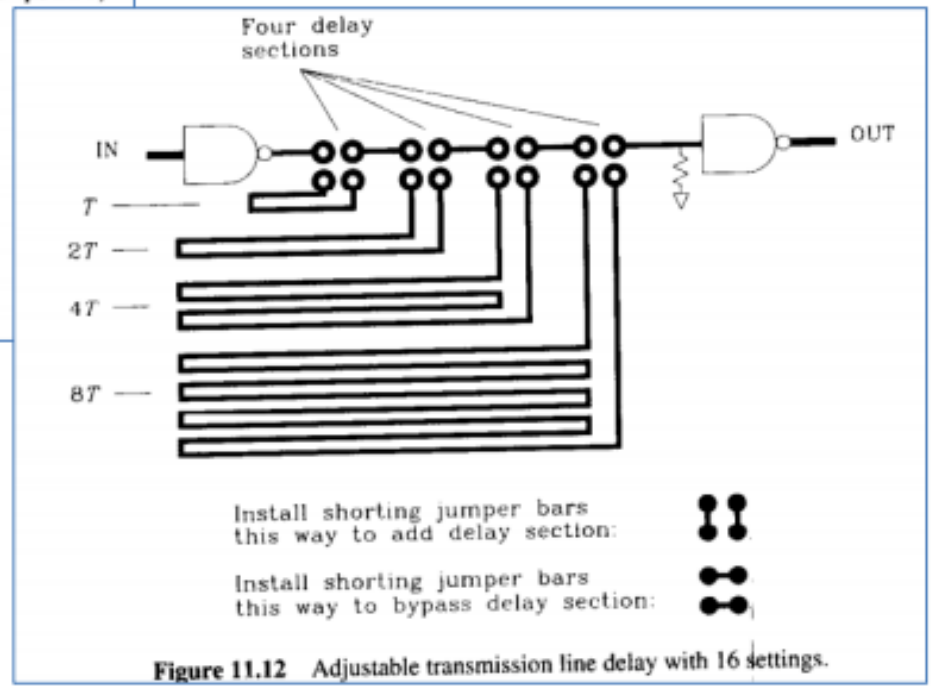
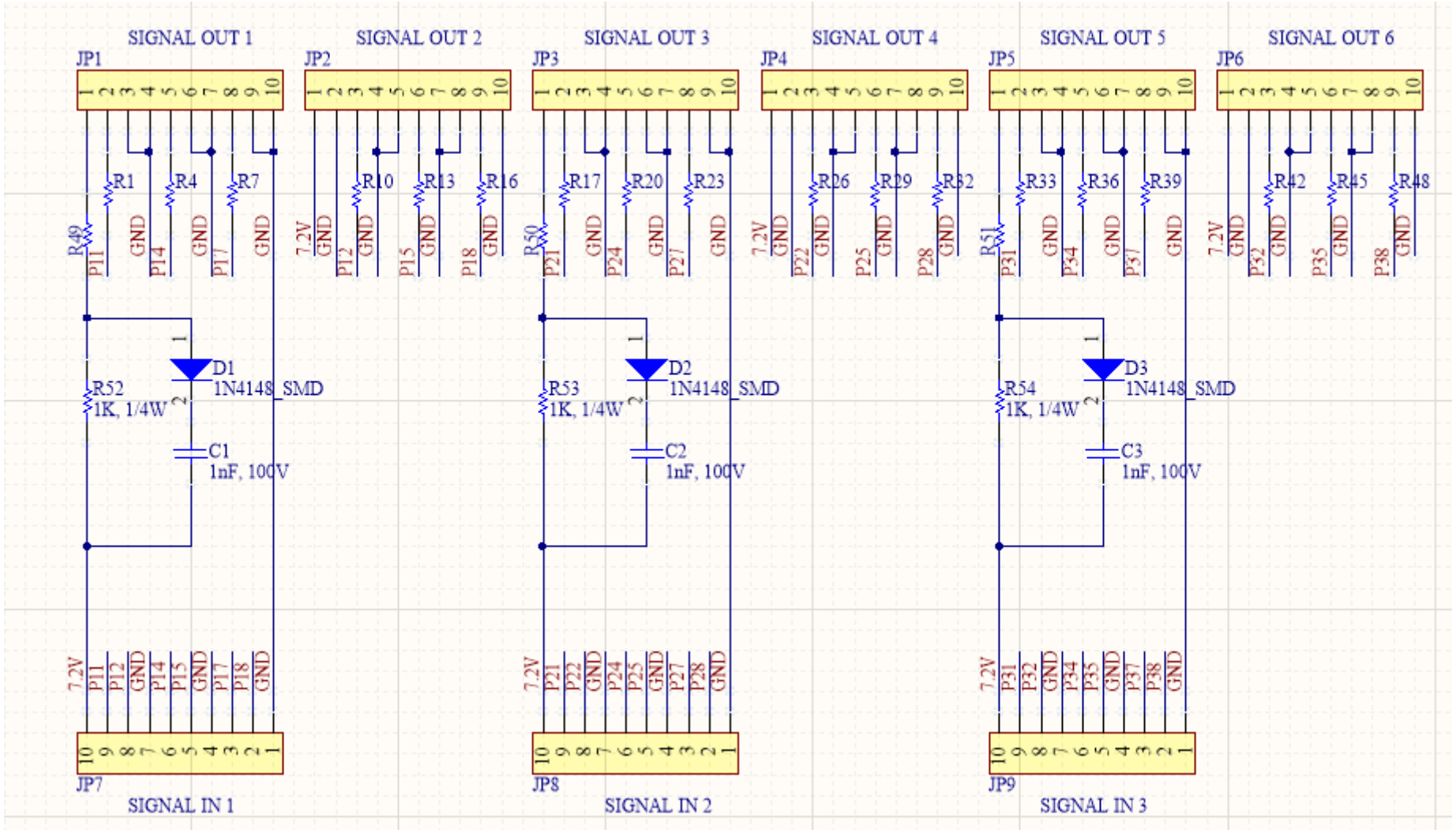


Figure 11.12 Adjustable transmission line delay with 16 settings.

Hight Speck

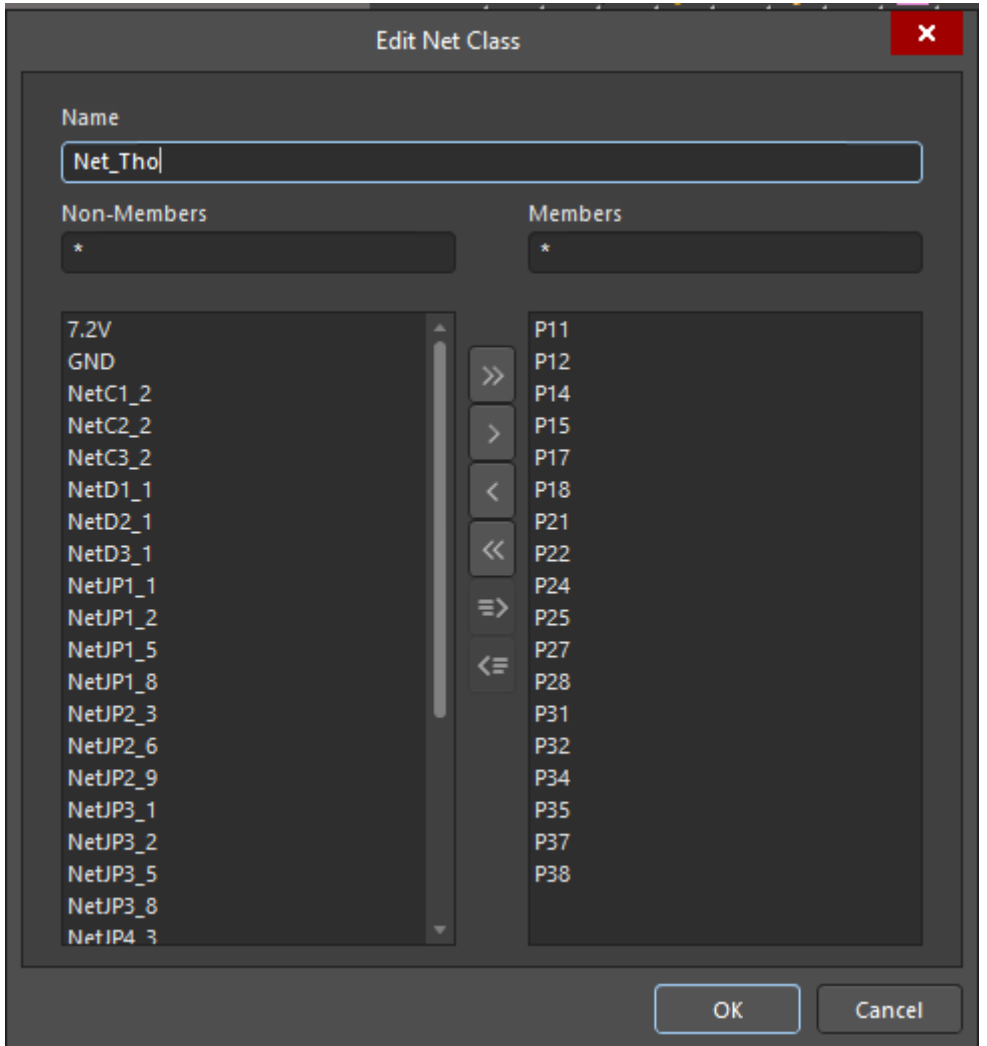
+ Việc truyền tín hiệu để CPU nhận cùng 1 lúc



Length Matching, Length Turing

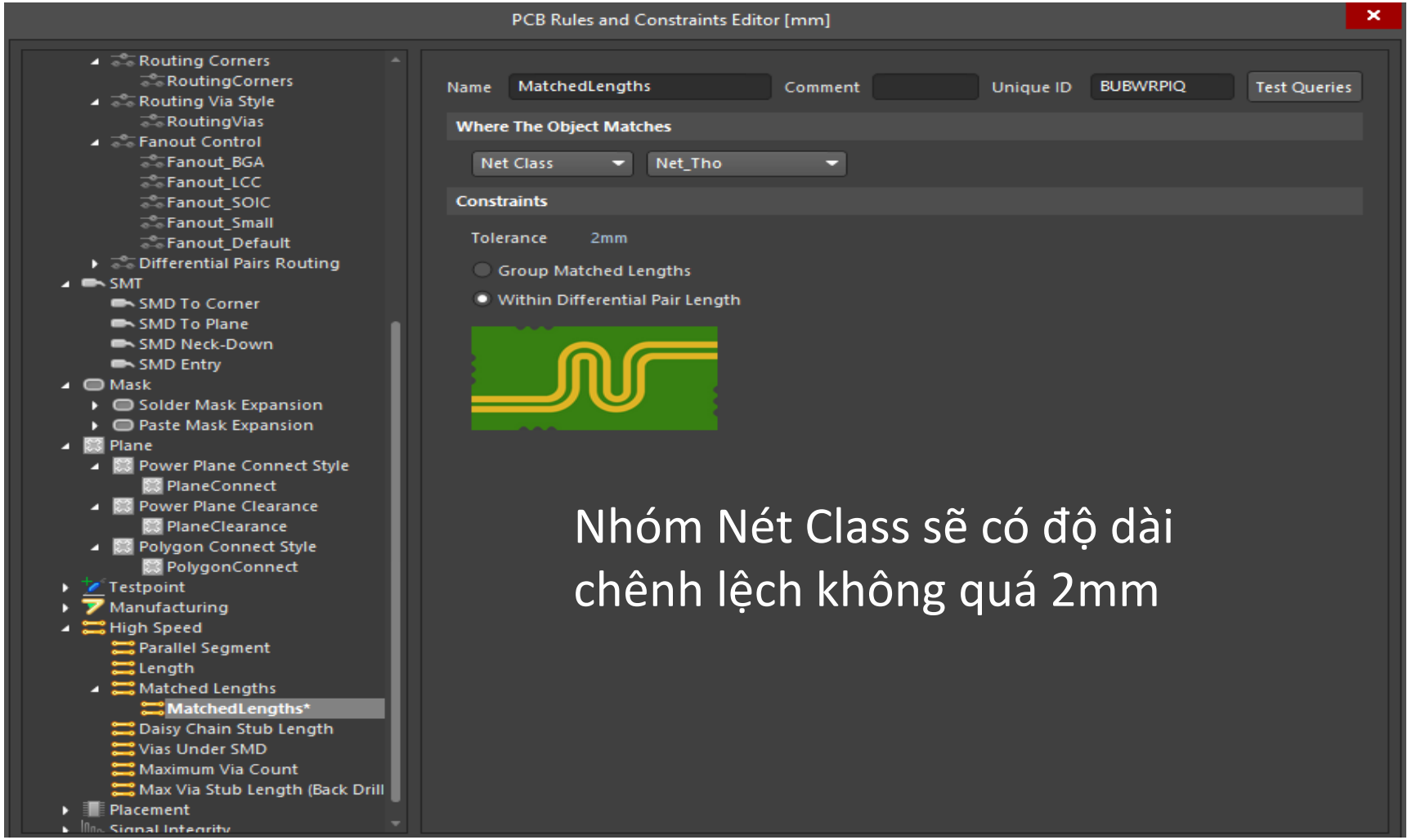
➢Bước 1: Thiết lập Nét Class

+ Các nét mà ta muốn tạo

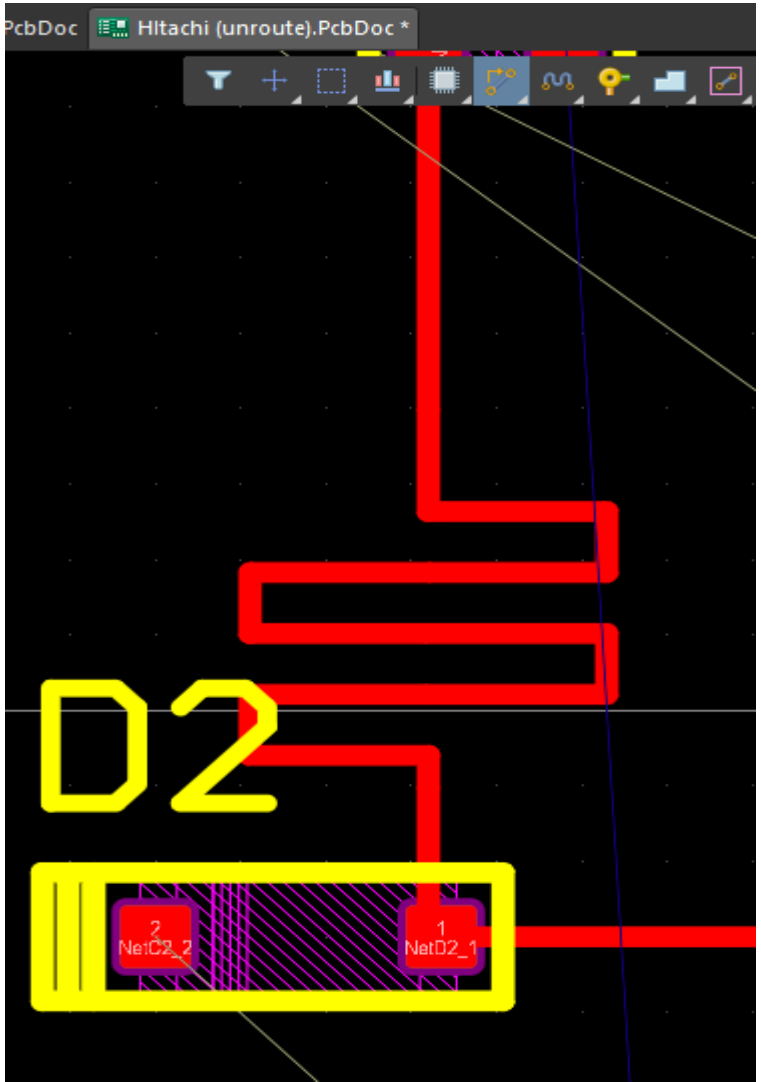


Hight Speck

D R



Hight Speck




Thank You