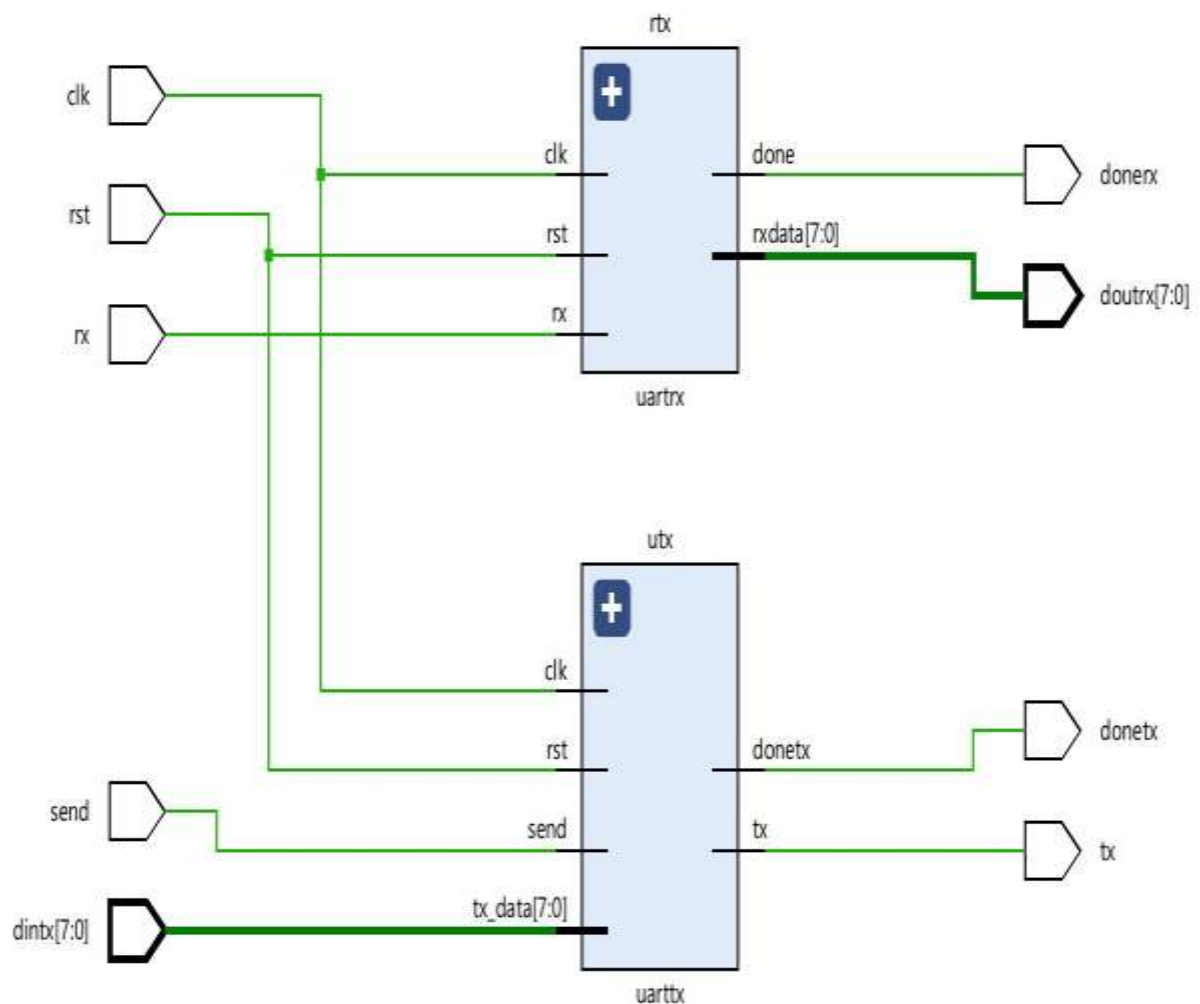


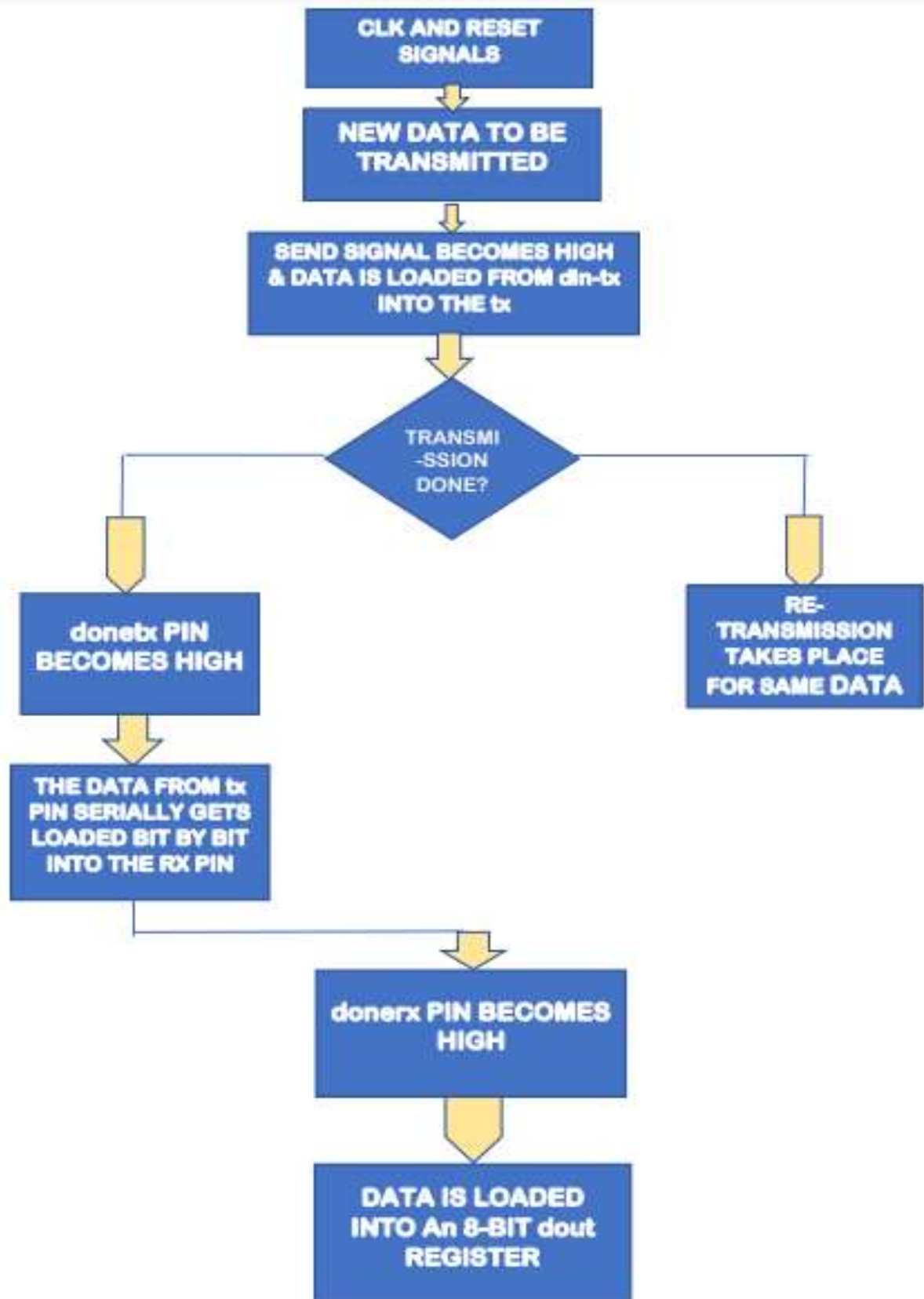
# DESIGN AND VERIFICATION RESULTS

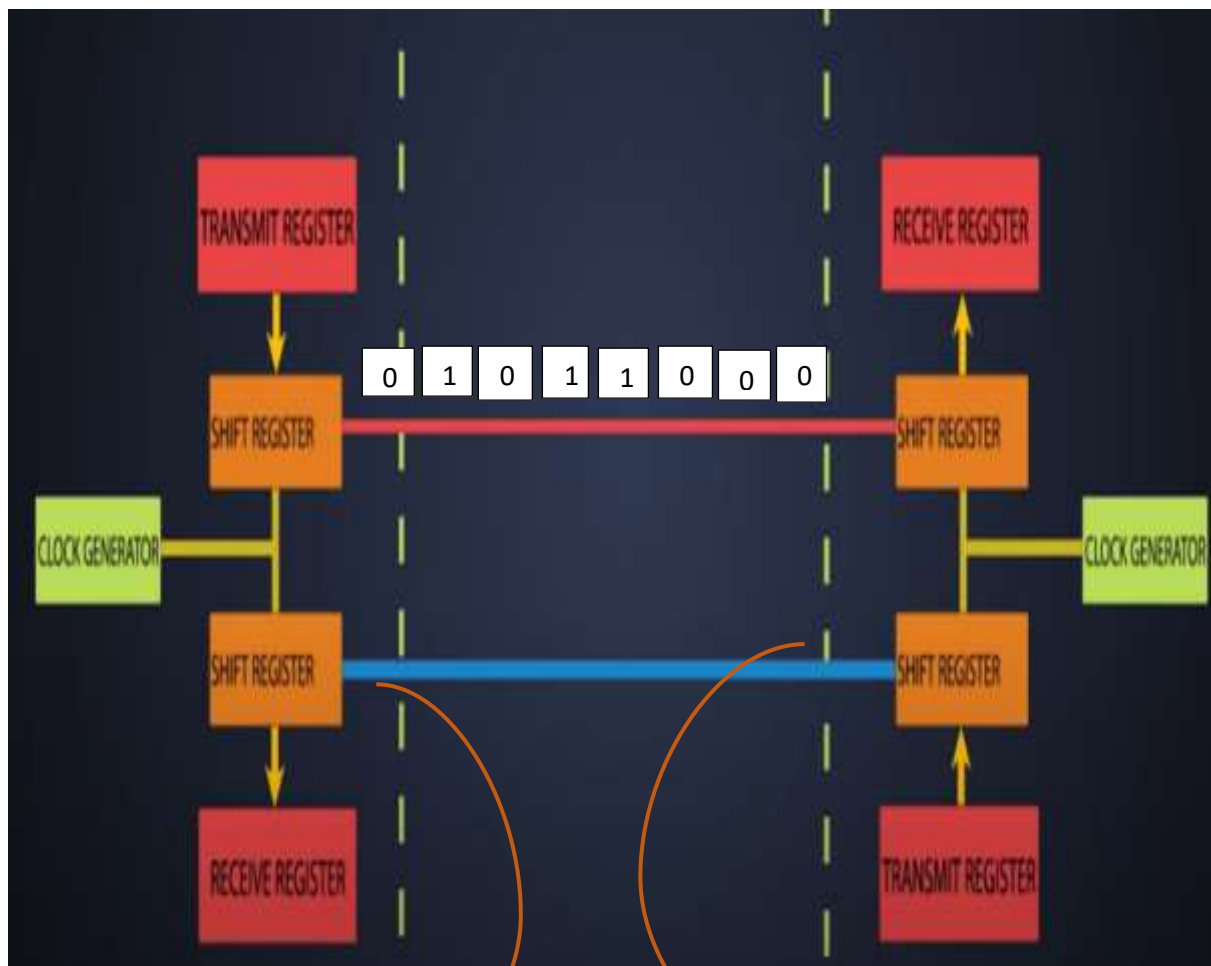
This is the schematic design result from Vivado.



The below flow-chart explains the data flow in the UART protocol.

# FLOWCHART

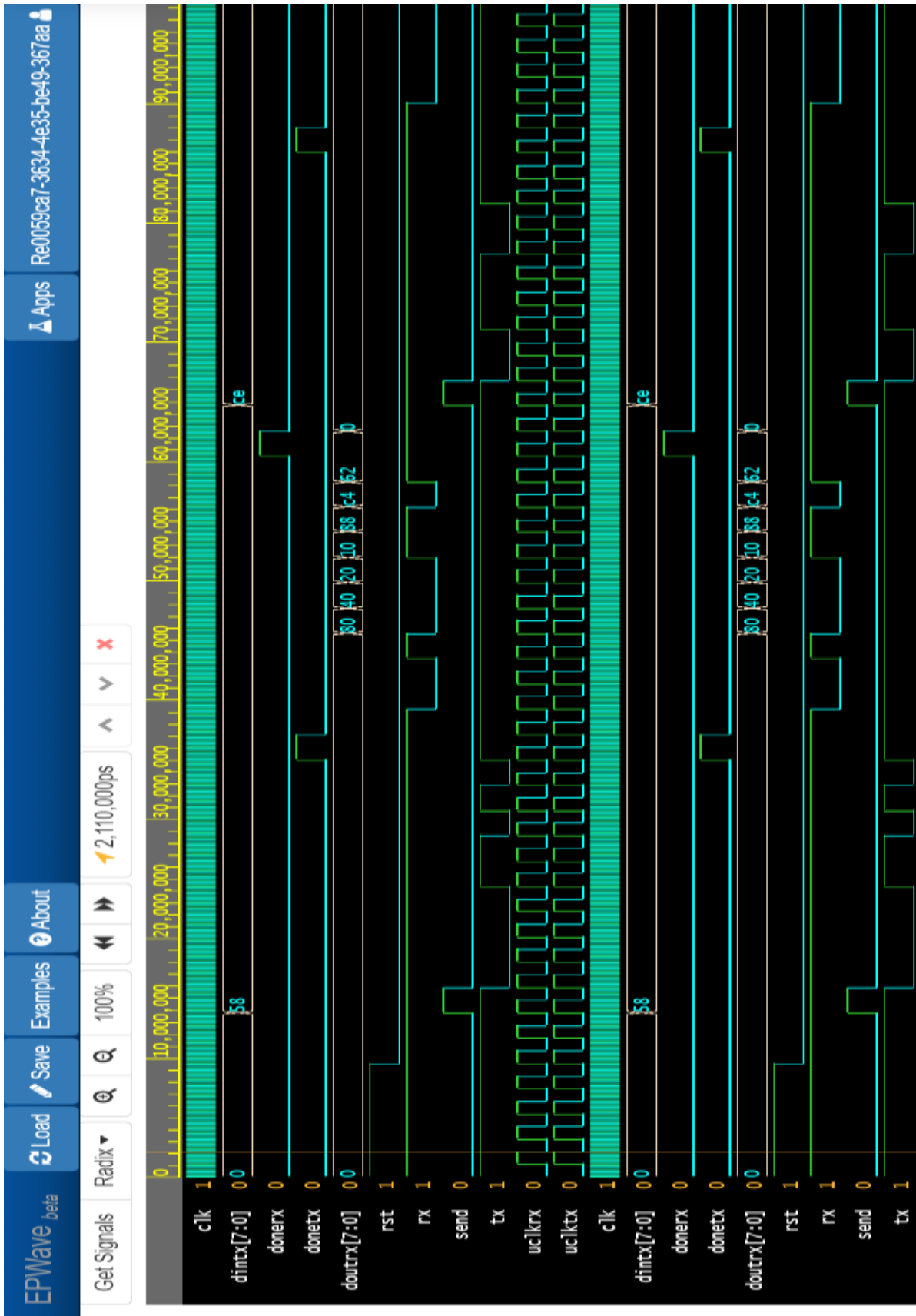




**TRANSMITTER  
MODEL**

**RECIEVER  
MODEL**

# EDA PLAYGROUND WAVEFORM RESULTS



In the above waveform we can see that random 8-bit data has been generated and it is loaded into the **dintx[7:0]**.

Whenever the new data is available then the **send** signal becomes high and then the data gets loaded from the **dintx** register into the **tx** pin.

Then **tx** signal becomes high and when the transmission is completed the **donetx** signal becomes high and immediately the **rx** pin becomes high . after the whole 8-bit data reception is completed the **donerx** signal becomes high and then the data gets stored into the **doutrx** register.

## LOG WINDOW RESULTS

---

```
# KERNEL: Kernel process initialization done.
# Allocation: simulator allocated 5599 kB (elbread=459 elab2=4975 kernel=164 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: [DRV] : RESET DONE
# KERNEL: [GEN] : oper : write send : 0 TX_DATA : 01011000 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX : 0 DONE_RX : 0
# KERNEL: [DRV]: Data Sent : 88
# KERNEL: [MON] : DATA SEND on UART TX 88
# KERNEL: [SCO] : DRV : 88 MON : 88
# KERNEL: DATA MATCHED
# KERNEL: [GEN] : oper : read send : 0 TX_DATA : 00001010 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX : 0 DONE_RX : 0
# KERNEL: [DRV]: Data RCVD : 98
# KERNEL: [MON] : DATA RCVD RX 98
# KERNEL: [SCO] : DRV : 98 MON : 98
# KERNEL: DATA MATCHED
# KERNEL: [GEN] : oper : write send : 0 TX_DATA : 11001110 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX : 0 DONE_RX : 0
# KERNEL: [DRV]: Data Sent : 206
# KERNEL: [MON] : DATA SEND on UART TX 206
# KERNEL: [SCO] : DRV : 206 MON : 206
# KERNEL: DATA MATCHED
```

**The above image explains the log window results where every test bench component results are shown clearly.**