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## School of Electronics Engineering (SENSE)

### Certificate of Completion

This is to certify that **G.R.Varshitha** bearing Regd. No. **22BEC7004** has successfully completed the value added course of **Advanced Digital Design Through System Verilog Verification**. This course is organized by School of Electronics Engineering (SENSE), VIT-AP University, Amaravati, India during 27<sup>th</sup> January- 26<sup>th</sup> April, 2025.

**Dr. Deepak Ch**  
Course Coordinator  
VIT-AP University

**Dr. M Girish Kumar**  
Course Coordinator  
VIT-AP University

**Dr. Umakanta Nanda**  
Dean, SENSE  
VIT-AP University