LC86F8208A

On-chip 8K-byte ROM, 136K-byte Flash EPROM and On-chip 256-byte RAM 8-bit Single Chip Microcomputer

Overview

The LC86F8208A microcomputers is 8-bit single chip microcomputer with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.75µs (microseconds)
- On-chip ROM capacity : 8K bytes for OS program (user not programmable)
- On-chip Flash EPROM : 8K bytes for program
  : 128K bytes for data
- On-chip RAM capacity : 256 bytes
- 16-bit timer/counter (or two 8-bit timers)
- 8-bit synchronous serial-interface circuits
- 9-source 8-level vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

(1) Flash Erasable and programmable Read Only Memory (Flash EPROM)
: 8192 × 8 bits for program
: 131072 × 8 bits for data

(2) Read Only Memory (ROM) : 8192 × 8 bits for OS program (user not programmable)

(3) Random Access Memory (RAM) : 256 × 8 bits (calculation area)

This product incorporates technology licensed from Silicon Storage Technology Inc.

This catalog provides information as of June, 1997. Specifications and information herein are subject to change without notice.

(4) Bus cycle time / Instruction cycle time :

Bus cycle time	Instruction cycle time	System clock oscillation	Oscillation frequency	Voltage
0.5µs	1.0µs	Ceramic (CF)	6MHz	3.3V – 4.0V
7.5µs	15µs	Internal RC	800kHz	3.3V – 4.0V

*Bus cycle time means ROM read period.

(5) Ports :
- Input/output ports : 3 ports (20 terminals)
  - Input/output port programmable in a nibble : 1 port (4 terminals)
  - Input/output port programmable in a bit : 2 ports (16 terminals)
- Input port : 1 port (4 terminals)

(6) Serial-interface
- 8-bit serial-interface circuit
  LSB first/MSB first function available
- Internal 8-bit baud-rate generator

(7) Timer
- Timer 0 (T0L, T0H)
  16-bit timer/counter
  2-bit prescaler + 8-bit programmable prescaler
  - Mode 0 : Two 8-bit timers with programmable prescaler
  - Mode 1 : 8-bit timer with programmable prescaler + 8-bit counter
  - Mode 2 : 16-bit timer with programmable prescaler
  - Mode 3 : 16-bit counter

(8) Remote-control receiver (using P73/INT3/T0IN terminal)
- Noise rejection available
- The interrupt polarity selectable

(9) Watchdog timer
- The watchdog timer is taken on RC outside (using P70/INT0 terminal)
- Watchdog timer operation selectable : interrupt system, system reset

(10) Interrupt system
- 9-source 8-level vectored interrupts :
  1. External interrupt INT 0 (includes watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2, timer/counter T0L (timer 0 lower 8-bit)
  4. External interrupt INT3,
  5. Timer/counter T0H (timer 0 upper 8-bit)
  6. Serial-interface SIO 0
  7. Port 3
- Interrupt Priority control available
  Microcomputer allows 3 levels of interrupt ; low level, high level, and highest level of multiplex interrupt. It can specify a low level or a high level interrupt priority from INT2/T0L through port 3 (the above interrupt number from three through seven). It can also specify a low level or the highest level interrupt priority to INT0 and INT1.

(11) Flash EPROM
- Page-erase/page-write operation
- 128 bytes per page
- Program and read operation for data area
  Parallel program/read
  (PROM writer or software by using built-in OS-ROM)
- Program and read operation for program area
  Parallel program/read
  (PROM writer)
- Single +3.3 to +4.0 Volt programming and read operations
- High reliable CMOS technology
  Page erase/program cycles : 10^4 program cycles per page
  10-year data retention

(12) Sub-routine stack levels
- 128 levels (Max.) : Stack area included in the RAM area

(13) Multiplication and division
16-bit ´ 8-bit (7 instruction cycle times)
16-bit / 8-bit (7 instruction cycle times)

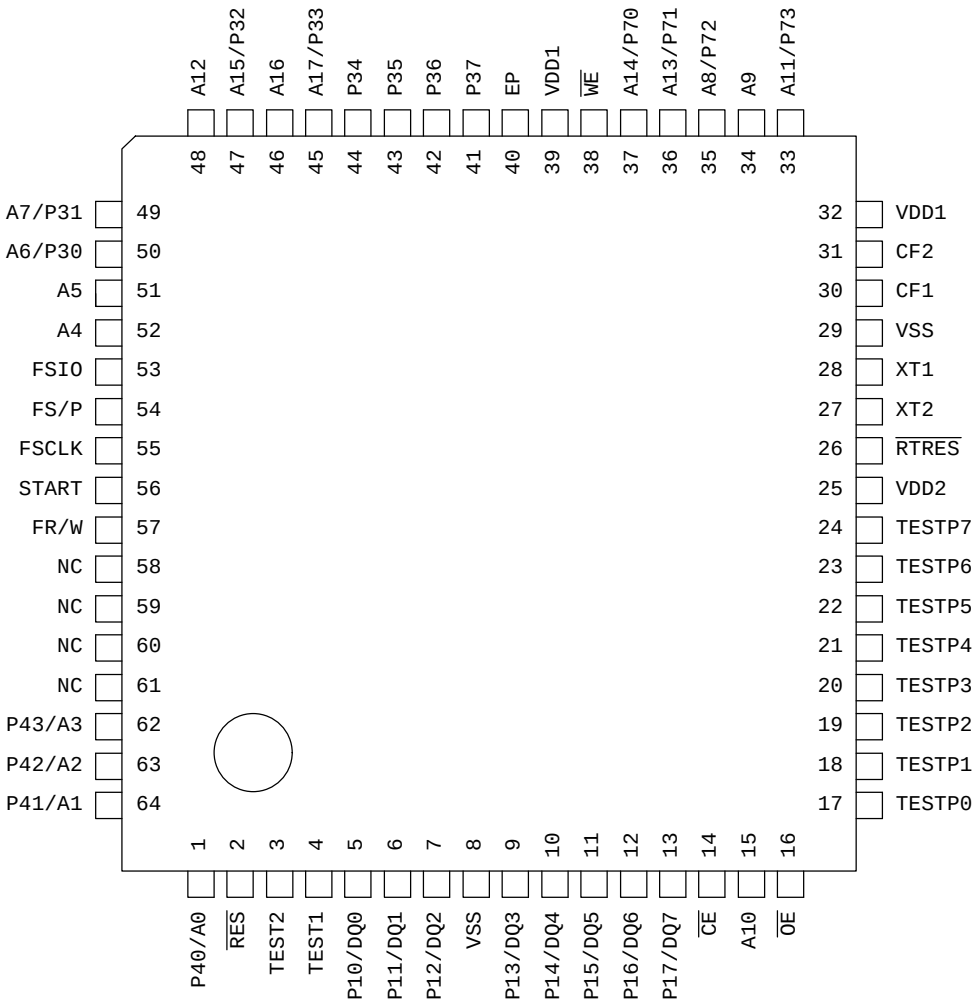
(14) 2 oscillation circuits
- On-chip RC oscillation circuit using for the system clock
- On-chip CF oscillation circuit using for the system clock

(15) Standby function
- HALT mode function
  The HALT mode is used to reduce power dissipation. In this operation mode, program execution is stopped. This operation mode can be released by the interrupt request signals or setting to low level for the reset terminal ($\overline{\text{RES}}$).
- HOLD mode function
  The HOLD mode is used to freeze all the oscillations ; RC (internal) and CF oscillations.
  This mode can be released by the following operations :
  - Reset terminal ($\overline{\text{RES}}$) set to Low level
  - Set to assigned level to INT0/1 terminals
  - Set to assigned level to Port 3

(16) Factory shipment
- QFP64

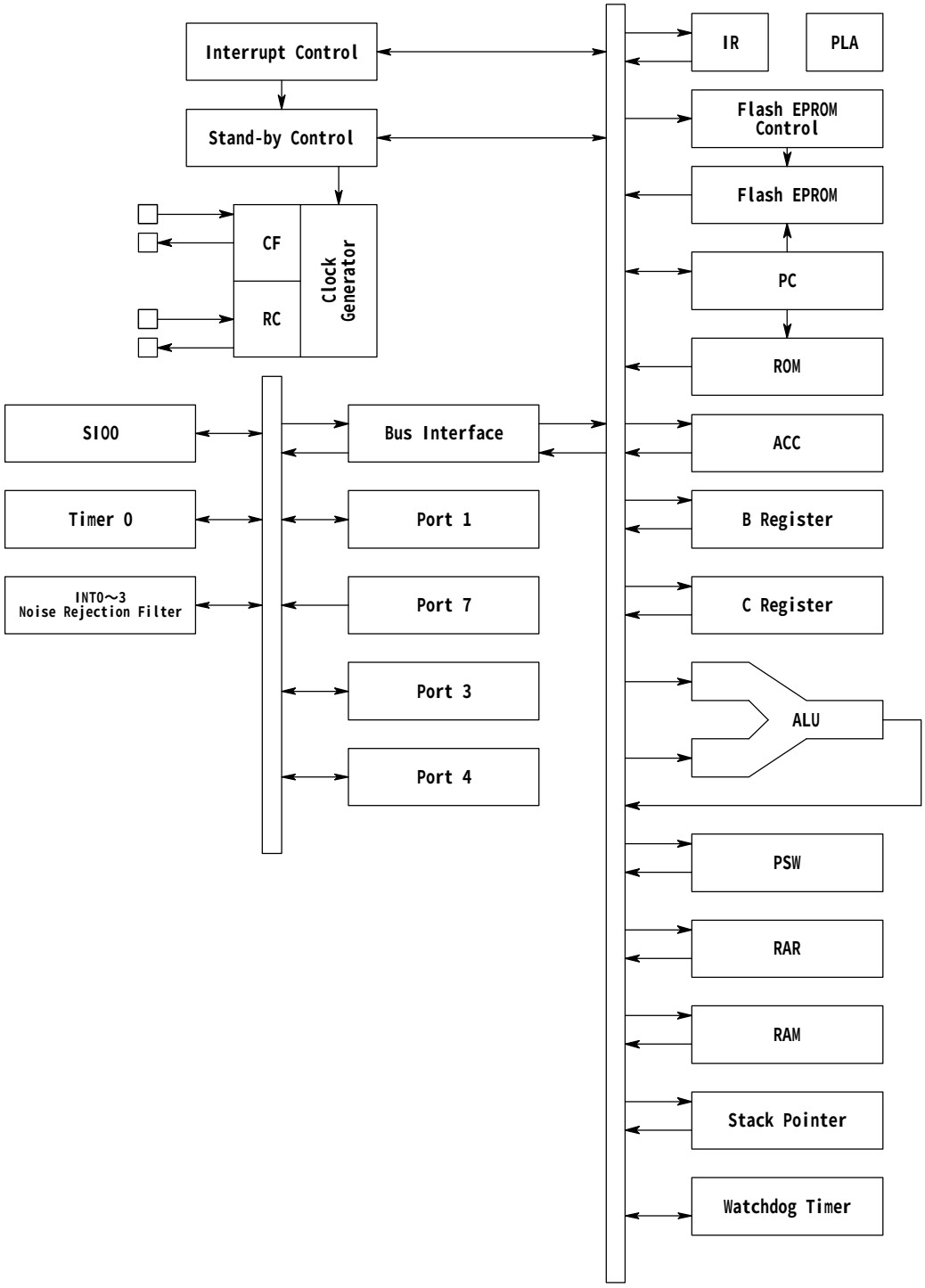
(17) Development support tools
- Evaluation (EVA) chip : LC868099
- Emulator : EVA-86000 + ECB868200 (Evaluation chip board)

Pin Assignment



NC : No connect.

System Block Diagram



LC86F8208A Terminal description

<table>
<tr><th>Name</th><th>No.</th><th>I/O</th><th>Function description</th><th>Input/Output specification</th></tr>
<tr><td>VSS</td><td>8,29</td><td></td><td>Power terminal (-)</td><td></td></tr>
<tr><td>VDD1</td><td>32,39</td><td></td><td>Power terminal (+) for CPU</td><td></td></tr>
<tr><td>VDD2</td><td>25</td><td></td><td>Power terminal (+)</td><td></td></tr>
<tr><td>PORT1
P10 to P17</td><td>5-7
9-13</td><td>I/O</td><td>•8-bit input/output port
•Input/output can be specified in a bit
•Another functions
P10 SIO0 data output
P11 SIO0 data input, bus input/output
P12 SIO0 clock input/output</td><td>•Output form :
P10, P14 : N-ch open drain
P11 to P14, P15 to P17 : CMOS
•Programmable pull-up resistor provided.
•Input form : Schmitt</td></tr>
<tr><td>PORT3
P30 to P37</td><td>50,49
47
45-41</td><td>I/O</td><td>•8-bit input/output port
•Input/output in a bit
•Input for key interrupt</td><td>•Pull-up resistor : Provided
•Output form : CMOS
•Input form : Schmitt</td></tr>
<tr><td>PORT4
P40 to P43</td><td>1
64-62</td><td>I/O</td><td>•4-bit input/output port
•Input/output can be specified in 4 bits</td><td>•Pull-up resistor : Provided
•Output form : CMOS
•Input form : Schmitt</td></tr>
<tr><td>PORT7
P70 to P73</td><td>37-35
33</td><td>I</td><td>•4-bit input port
•Another functions
P70 INT0 input/HOLD release/N-ch Tr. output for watchdog timer
P71 INT1 input/HOLD release
P72 INT2 input/timer 0 event input
P73 INT3 input with noise filter/timer 0 event input
•Interrupt received form, vector address
<table>
<tr><th></th><th>leading</th><th>trailing</th><th>Leading & trailing</th><th>High level</th><th>Low Level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>•Pull-up resistor : Provided
•Input form : Schmitt</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>2</td><td>I</td><td>Reset for CPU</td><td>Input form : Schmitt</td></tr>
<tr><td>XT1</td><td>28</td><td>I</td><td>Connect to VSS</td><td></td></tr>
<tr><td>XT2</td><td>27</td><td>O</td><td>This terminal should be left unconnected</td><td></td></tr>
<tr><td>CF1</td><td>30</td><td>I</td><td>Input for ceramic resonator oscillation</td><td></td></tr>
<tr><td>CF2</td><td>31</td><td>O</td><td>Output for ceramic resonator oscillation</td><td></td></tr>
<tr><td>$\overline{\text{RTRES}}$</td><td>26</td><td>I</td><td>This terminal should be left unconnected</td><td></td></tr>
<tr><td>A4
A5
A9
A10
A12
A16</td><td>52
51
34
15
48
46</td><td>I</td><td>Address terminal at Flash EPROM operating mode</td><td></td></tr>
<tr><td>$\overline{\text{WE}}$
$\overline{\text{OE}}$
$\overline{\text{CE}}$
EP</td><td>38
16
14
40</td><td>I</td><td>Control input terminal at Flash EPROM operating mode</td><td></td></tr>
</table>

*All of port options can be specified in abit.

*A state of port at initial

Name	I/O mode	A state of pull-up resistor specified at pull-up option
Port 7	Input	Fixed pull-up resistor exist
Port 1 Port 3	Input	Programmable pull-up resistor OFF
Port 4	Input	Programmable pull-up resistor ON

*Pin configurations at Flash EPROM operating mode

	Name	Function
Address Inputs	P40	A0
	P41	A1
	P42	A2
	P43	A3
	A4	A4
	A5	A5
	P30	A6
	P31	A7
	P72	A8
	A9	A9
	A10	A10
	P73	A11
	A12	A12
	P71	A13
	P70	A14
	P32	A15
	A16	A16
	P33	A17

	Name	Function
Data Inputs/Output	P10	DQ0
	P11	DQ1
	P12	DQ2
	P13	DQ3
	P14	DQ4
	P15	DQ5
	P16	DQ6
	P17	DQ7
Control inputs	$\overline{WE}$	$\overline{WE}$
	$\overline{OE}$	$\overline{OE}$
	$\overline{CE}$	$\overline{CE}$
	EP	*1

*1) Setting to Flash EPROM operating mode

1. Absolute maximum ratings / Ta=25°C, VSS =0V

Parameter		Symbol	Pins	Conditions	Limits				
					VDD[V]	min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD1			-0.3		+7.0	V
			VDD2			-0.3		+7.0	
Input voltage		VI(1)	•Ports 71, 72, 73 • $\overline{\text{RES}}$,FS/P,FSCLK •START,FR/W,A4 •A5,A9,A10,A12 •A16,EP, $\overline{\text{CE}}$, $\overline{\text{OE}}$ • $\overline{\text{WE}}$			-0.3		VDD1+0.3	
		VI(2)	$\overline{\text{RTRES}}$			-0.3		VDD2+0.3	
Output voltage		VO(1)	•TEST1,TEST2			-0.3		VDD1+0.3	
Input/output voltage		VIO(1)	•Ports 1, 3, 4 •Port 70 •TESTP0,FSI0			-0.3		VDD1+0.3	
High level output current	Peak output current	IOPH(1)	•Ports 1, 3, 4 •TESTP0,TEST1 •TEST2,FSI0	•CMOS output •At each pins		-4			mA
	Total output current	∑IOAH(1)	•Ports 1, 3, 4 •TESTP0,TEST1 •TEST2,FSI0	Total all pins		-25			
Low level output current	Peak output current	IOPL(1)	•Ports 1, 3, 4 •TESTP0,TEST1 •TEST2,FSI0	At each pins				20	
		IOPL(2)	Port 70	At each pins				15	
	Total output current	∑IOAL(1)	TESTP0	Total all pins				40	
		∑IOAL(2)	•Port 4 •TEST1,TEST2	Total all pins				40	
		∑IOAL(3)	Port 1	Total all pins				40	
		∑IOAL(4)	Port 3, FSI0	Total all pins				40	
		∑IOAL(5)	Port 70	Total all pins				15	
Maximum power dissipation		Pdmax	QFP64	Ta=+5 to +50°C				420	mW
Operating temperature range		Topr				+5		+50	°C
Storage temperature range		Tstg				-55		+125	

2. Recommended operating range / Ta=+5°C to +50°C, VSS =0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Operating supply voltage range	VDD(1)	VDD1	0.98µs ≤ tCYC ≤ 400µs		3.3		4.0	V
	VDD(2)	VDD2			3.3		4.0	
Hold voltage	VHD	VDD1	RAMs and the registers hold voltage at HOLD mode.		2.0		4.0	
Input high voltage	VIH(1)	TESTP0 (Schmitt)	Output disable	3.3-4.0	0.4VDD +0.9		VDD	
	VIH(2)	•Ports 1, 4 •Ports 72, 73 (Schmitt)	Output disable	3.3-4.0	0.75VDD		VDD	
	VIH(3)	•Port 70 Port input/interrupt •Port 71 • $\overline{\text{RES}}$ (Schmitt)	Output N-channel Tr. OFF	3.3-4.0	0.75VDD		VDD	
	VIH(4)	Port 70 Watchdog timer	Output N-channel Tr. OFF	3.3-4.0	0.9VDD		VDD	
	VIH(5)	Port 3	Output disable	3.3-4.0	0.75VDD		VDD	
	VIH(6)	$\overline{\text{RTRES}}$ (Schmitt)		VDD2= 3.3-4.0	0.75VDD		VDD	
	VIH(7)	•FS/P,FSCLK •START,FR/W •FSI0		3.3-4.0	0.9VDD		VDD	
	VIH(8)	•A4,A5,A9,A10 •A12,A16,EP • $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$		3.3-4.0	2.0		VDD	
Input low voltage	VIL(1)	TESTP0 (Schmitt)	Output disable	33-4.0	VSS		0.2VDD	
	VIL(2)	•Ports 1, 4 •Ports 72, 73 (Schmitt)	Output disable	3.3-4.0	VSS		0.25VDD	
	VIL(3)	•Port 70 Port input/interrupt •Port 71 • $\overline{\text{RES}}$ (Schmitt)	Output N-channel Tr. OFF	3.3-4.0	VSS		0.25VDD	
	VIL(4)	Port 70 Watchdog timer	Output N-channel Tr. OFF	3.3-4.0	VSS		0.8VDD -1.0	
	VIL(5)	Port 3	Output disable	3.3-4.0	VSS		0.25VDD	
	VIL(6)	$\overline{\text{RTRES}}$ (Schmitt)		VDD2= 3.3-4.0	VSS		0.25VDD	
	VIL(7)	•FS/P,FSCLK •START,FR/W •FSI0		3.3-4.0	VSS		0.1VDD	
	VIL(8)	•A4,A5,A9,A10 •A12,A16,EP • $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$		3.3-4.0	VSS		0.8	
Operation cycle time	tCYC			3.3-4.0	0.98		400	µs
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	3.3-4.0	5.88	6	6.12	MHz
	FmRC		RC oscillation	3.3-4.0	0.4	0.8	2.0	
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 2	3.3-4.0		0.1	3.0	ms

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical characteristics / Ta=+5°C to +50°C, VSS =0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Input high current	IIH(1)	•Ports 1, 3, 4 •TESTP0	•Output disable •Pull-up MOS Tr. OFF. VIN=VDD1 (including the off-leak current of the output Tr.)	3.3-4.0			1	µA
	IIH(2)	Port 7 without pull-up MOS Tr.	Output Nch Tr.OFF. VIN=VDD1 (including the off-leak current of the output Tr.)	3.3-4.0			1	
	IIH(3)	$\overline{\text{RES}}$	VIN=VDD1	3.3-4.0			1	
	IIH(4)	•A4,A5,A9,A10 •A12,A16 • CE , OE , WE	VIN=VDD1	3.3-4.0			1	
Input low current	IIL(1)	•Ports 1, 3, 4 •TESTP0	•Output disable •Pull-up MOS Tr. OFF. VIN=VSS (including the off-leak current of the output Tr.)	3.3-4.0	-1			
	IIL(2)	Port 7 without pull-up MOS Tr.	Output Nch Tr.OFF. VIN=VSS (including the off-leak current of the output Tr.)	3.3-4.0	-1			
	IIL(3)	$\overline{\text{RES}}$	VIN=VSS	3.3-4.0	-1			
	IIL(4)	•A4,A5,A9,A10 •A12,A16 • CE , OE , WE	VIN=VSS	3.3-4.0	-1			
Output high voltage	VOH(1)	TESTP0	IOH=-1.0mA	3.3-4.0	VDD-0.4			V
	VOH(2)	•CMOS output of ports 1, 3, 4 •TEST1,TEST2	IOH=-0.1mA	3.3-4.0	VDD-0.5			
	VOH(3)	FSI0	IOH=-0.1mA	3.3-4.0	VDD-0.5			
Output low voltage	VOL(1)	•Ports 1,3,4,TEST1 •TEST2,TESTP0	•IOL=1mA •The current of any measurement pin is not over 1mA	3.3-4.0			0.4	
	VOL(2)	Port 70	IOL=0.5mA	3.3-4.0			0.4	
	VOL(3)	FSI0	IOL=0.5mA	3.3-4.0			0.4	
Pull-up MOS Tr. resistor	Rpu(1)	•Ports 1, 3, 4 •Port 7,TESTP0	VOH=0.9VDD	3.3-4.0	25	60	120	kΩ
	Rpu(2)	FSCLK	VOH=0.9VDD	3.3-4.0	250	500	1000	
	Rpu(3)	$\overline{\text{RTRES}}$	VOH=0.9VDD VDD2=3.3 to 4.0V	3.3-4.0	100	200	400	
Pull-down MOS Tr. resistor	Rpd	•FSI0,FS/P •START •FR/W,EP	VOL=0.1VDD	3.3-4.0	250	500	1000	

Continue.

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Hysteresis voltage	VHIS(1)	•Ports 1,3,4 •Port 7,TESTP0 • $\overline{\text{RES}}$	Output disable	3.3-4.0		0.1VDD		V
	VHIS(2)	$\overline{\text{RTRES}}$	VDD2=3.3 to 4.0V	3.3-4.0		0.1VDD		
Pin capacitance	CP	All pins	•f=1MHz •Unmeasurement terminals for the input are set to VSS level. •Ta=25°C	3.3-4.0		10		pF

4. Serial input/output characteristics / Ta=+5°C to +50°C, VSS =0V

Parameter			Symbol	Pins	Conditions	Limits				
						VDD[V]	min.	typ.	max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0	Refer to figure 4.	3.3-4.0	2			tCYC
		Low Level pulse width	tCKL(1)			3.3-4.0	1			
		High Level pulse width	tCKH(1)			3.3-4.0	1			
	Output clock	Cycle	tCKCY(2)	SCK0	•Use pull-up resistor (1kΩ) when N-ch open drain output. •Refer to figure 4.	3.3-4.0	2			
		Low Level pulse width	tCKL(2)			3.3-4.0		1/2 tCKCY		
		High Level pulse width	tCKH(2)			3.3-4.0		1/2 tCKCY		
Serial input	Data set up time		tICK	•SI0 •SB0	•Data set-up to SCK0 •Data hold from SCK0 •Refer to figure 4.	3.3-4.0	0.4			µs
	Data hold time		tCKI			3.3-4.0	0.4			
Serial output	Output delay time (Using external clock)		tCKO(1)	•SO0 •SB0	•Data set up to SCK0 •Use pull-up resistor (1kΩ) when N-ch open drain output. •Refer to figure 4.	3.3-4.0			7/12tCYC +1	
	Output delay time (Using internal clock)		tCKO(2)		•Data hold from SCK0 •Use pull-up resistor (1kΩ) when N-ch open drain output. •Refer to figure 4.	3.3-4.0			1/3tCYC +1	

5. Pulse input conditions / Ta=+5°C to +50°C, VSS =0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN •Refer to figure 5	•Interrupt acceptable •Timer 0 countable	3.3-4.0	1			tCYC
	tPIH(2) tPIL(2)	•INT3/T0IN (The noise rejection clock is selected to 1/1.) •Refer to figure 5	•Interrupt acceptable •Timer 0 countable	3.3-4.0	2			
	tPIH(3) tPIL(3)	•INT3/T0IN (The noise rejection clock is selected to 1/16.) •Refer to figure 5	•Interrupt acceptable •Timer 0 countable	3.3-4.0	32			
	tPIH(4) tPIL(4)	•INT3/T0IN (The noise rejection clock is selected to 1/64.) •Refer to figure 5	•Interrupt acceptable •Timer 0 countable	3.3-4.0	128			
	tPIL(5)	• $\overline{\text{RES}}$ •Refer to figure 5	Reset acceptable	33-4.0	200			µs
	tPIL(6)	• $\overline{\text{RTRES}}$ •Refer to figure 5	•Reset acceptable •VDD2=3.3 to 4V	3.3-4.0	200			

6. Current dissipation characteristics / Ta=+5°C to +50°C, VSS =0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD1	•FmCF=6MHz Ceramic resonator oscillation •OCR7=1 •System clock : 6MHz •Internal RC oscillation stops •Refer to figure 6	3.3-4.0		10	25	mA
	IDDOP(2)		•FmCF=0Hz (oscillation stops) resonator oscillation •System clock : internal RC oscillation •Refer to figure 6	3.3-4.0		2	5	
Current dissipation in HALT mode (Note 4)	IDDHALT(1)	VDD1	•HALT mode •FmCF=6MHz Ceramic resonator oscillation •OCR7=1 •System clock : 6MHz •Internal RC oscillation stops •Refer to figure 6	3.3-4.0		3	7	mA
	IDDHALT(2)		•HALT mode •FmCF=0Hz (oscillation stops) resonator oscillation •System clock : internal RC oscillation •Refer to figure 6	3.3-4.0		250	650	µA
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)	VDD1	•HOLD mode •Refer to figure 6	3.3-4.0		5	20	µA

(Note 4) The currents of the output transistors, pull-up transistors and pull-down transistors are ignored.
*OCR7 : Bit 7 of the oscillation control register.

7. Power-up Timings

Parameter	Symbol	Typical	Units
Power-up to Read operation	tPU_READ	100	µs
Power-up to Write operation	tPU_WRITE	5	ms

Table 1. Ceramic resonator oscillation recommended constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2
6MHz ceramic resonator oscillation	Murata	CSA6.00MG	33pF	33pF
		CST6.00MGW	-	
	Kyocera	KBR-6.0MSA	33pF	33pF

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
•If you use other oscillators herein, we provide no guarantee for the characteristics.

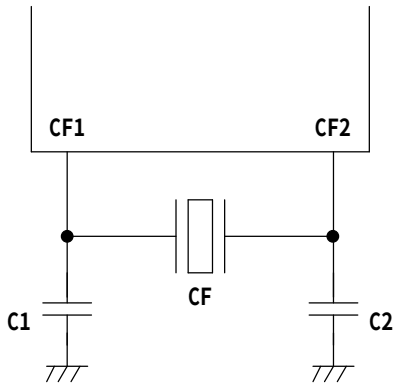


Figure 1 Ceramic oscillation circuit

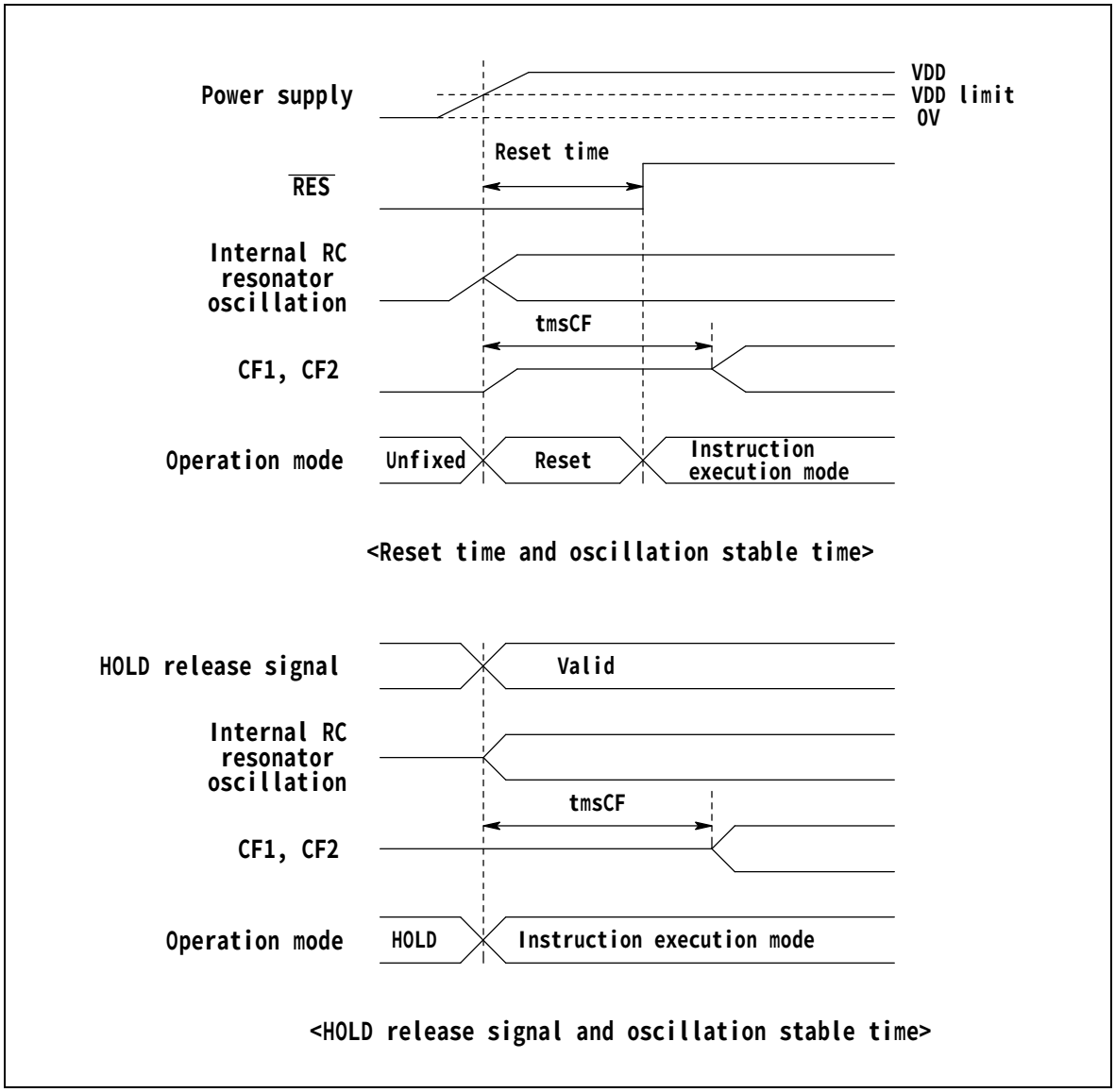
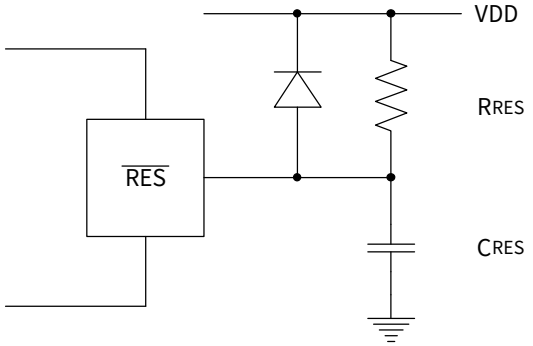


Figure 2 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 3 Reset circuit

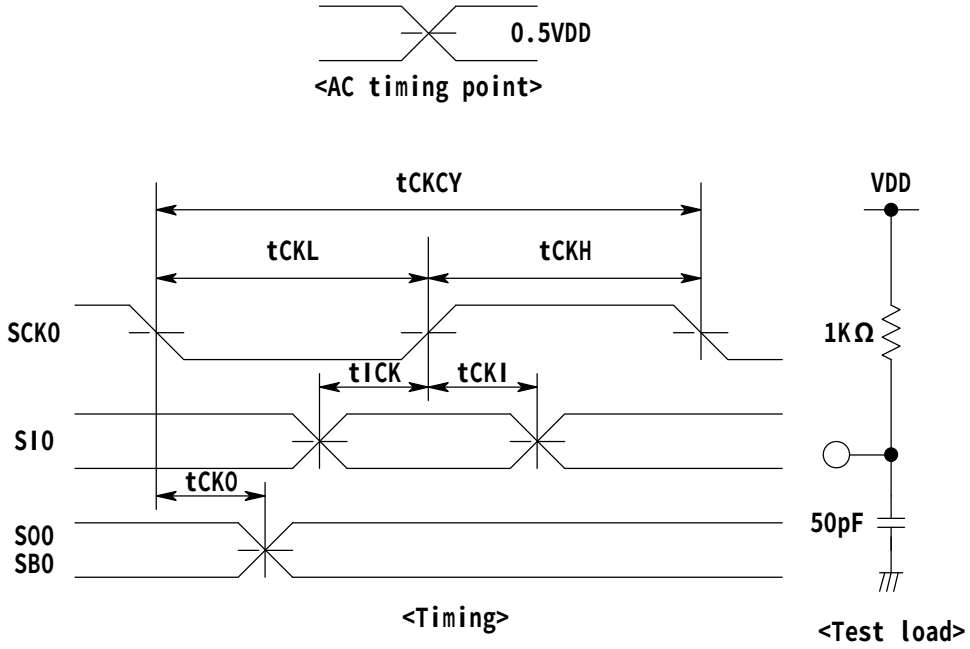


Figure 4 Serial input / output test condition

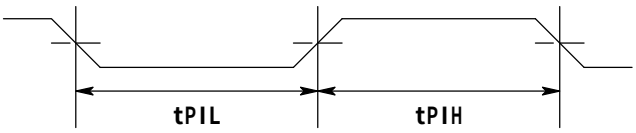


Figure 5 Pulse input timing condition

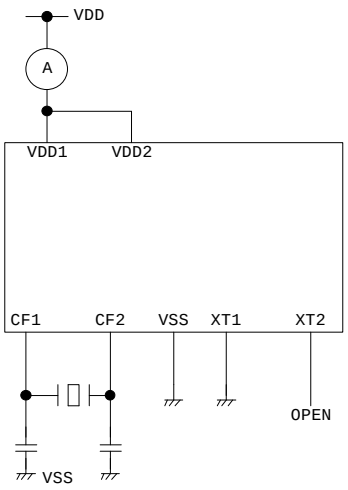


Figure 6 Current dissipation measurement