SONY

CXK5V8257BTM/BYM/BM -70LL/10LL

32768-word × 8-bit High Speed CMOS Static RAM

For the availability of this product, please contact the sales office.

Description

The CXK5V8257BTM/BYM/BM is 262,144 bits high speed CMOS static RAM organized as 32768-words by 8 bits.

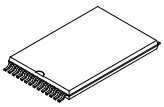
A polysilicon TFT cell technology realized extermely low stand-by current and higher data retention stability.

Operating on a single 3.3V supply, directly LVTTL compatible (All inputs and outputs).

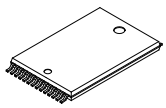
And special feature are, low power consumption, high speed and broad package line-up.

The CXK5V8257BTM/BYM/BM is a suitable RAM for portable equipment with battery back up.

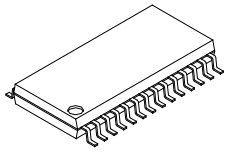
CXK5V8257BTM
28 pin TSOP (Plastic)



CXK5V8257BYM
28 pin TSOP (Plastic)



CXK5V8257BM
28 pin SOP (Plastic)



Features

- Single +3.3V supply: 3.3V ±0.3V
- Directly LVTTL compatible: All inputs and outputs
- Fast access time: (Access time)

  CXK5V8257BTM/BYM/BM

  -70LL 70ns (Max.)

  -10LL 100ns (Max.)
- Low standby current:

  CXK5V8257BTM/BYM/BM

  -70LL/10LL 3.5µA (Max.)
- Low power data retention: 2.0V (Min.)
- Available in many packages

  CXK5V8257BTM/BYM 8mm × 13.4mm 28 pin TSOP Package

  CXK5V8257BM 450mil 28 pin SOP Package

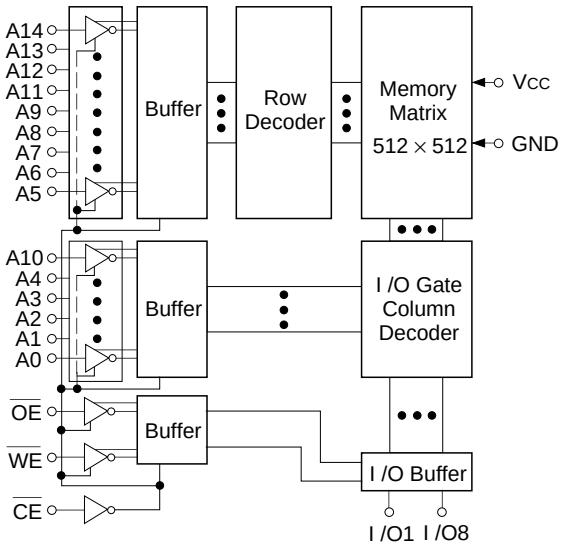
Function

32768-word × 8 bit static RAM

Structure

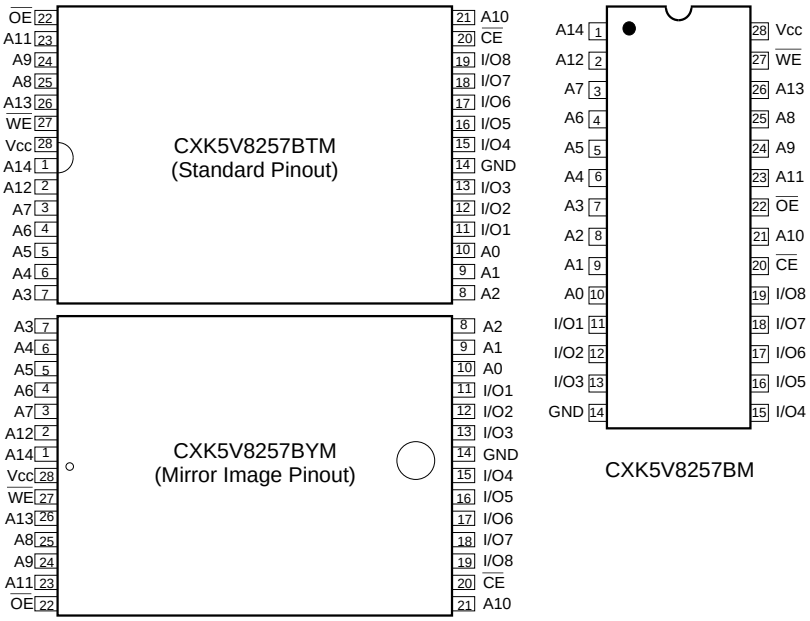
Silicon gate CMOS IC

Block Diagram



E93836A5Z-ST

Pin Configuration (Top View)



CXK5V8257BM

Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{CC}	+3.3V power supply
GND	Ground

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +4.6	V
Input voltage	V_{IN}	–0.5*1 to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	–0.5*1 to V_{CC} + 0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +150	°C
Soldering temperature · time	Tsolder	235 · 10	°C · s

*1 V_{IN}, $V_{I/O}$ = –3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}

×: "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	
Input low voltage	V_{IL}	–0.3*2	—	0.8	

*2 V_{IL} = –3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics (V_{CC} = 3.3V ± 0.3V, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test Conditions		Min.	Typ.*1	Max.	Unit
Input leakage current	I_{LI}	VIN = GND to VCC		–0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = GND to V_{CC}		–0.5	—	0.5	µA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		—	0.9	2	mA
Average operating current	I_{CC2}	Min. cycle, Duty = 100%, I_{OUT} = 0mA	70LL	—	21	40	mA
			10LL	—	18	35	
Standby current	I_{SB1}	$\overline{CE}$ ≥ V_{CC} – 0.2V	0 to +70°C	—	—	3.5	µA
			0 to +40°C	—	—	0.7	
			+25°C	—	0.12	0.35	
	I_{SB2}	$\overline{CE}$ = V_{IH}		—	0.06	0.7	mA
Output high voltage	V_{OH}	I_{OH} = –2mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.0mA		—	—	0.4	V

*1 V_{CC} = 3.3V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

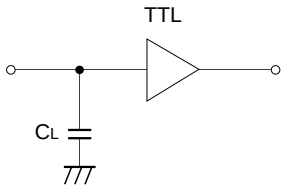
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	8	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions (V_{CC} = 3.3V ± 0.3V, Ta = 0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH} = 2.0V
Input pulse low level		V_{IL} = 0.8V
Input rise time		tr = 5ns
Input fall time		tf = 5ns
Input and output reference level		1.4V
Output load conditions	-70LL	C_L*2 = 30pF, 1TTL
	-10LL	C_L*2 = 100pF, 1TTL



*2 C_L includes scope and jig capacitances.

• **Read cycle** ($\overline{WE}$ = "H")

Item	Symbol	-70LL		-10LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	100	—	ns
Address access time	t_{AA}	—	70	—	100	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	70	—	100	ns
Output enable to output valid	t_{OE}	—	35	—	50	ns
Output hold from address change	t_{OH}	20	—	20	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	10	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*1	—	30	—	35	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*1	—	30	—	35	ns

*1 t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

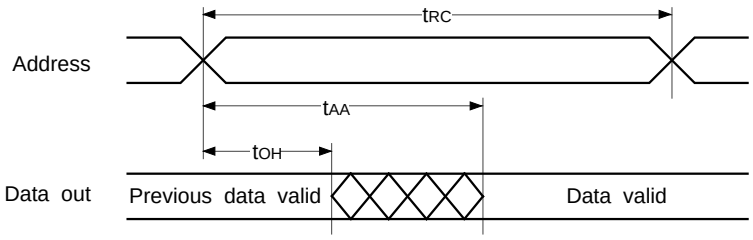
• **Write cycle**

Item	Symbol	-70LL		-10LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	100	—	ns
Address valid to end of write	t_{AW}	60	—	80	—	ns
Chip enable to end of write	t_{CW}	60	—	80	—	ns
Data to write time overlap	t_{DW}	30	—	35	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	55	—	60	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*2	—	30	—	35	ns

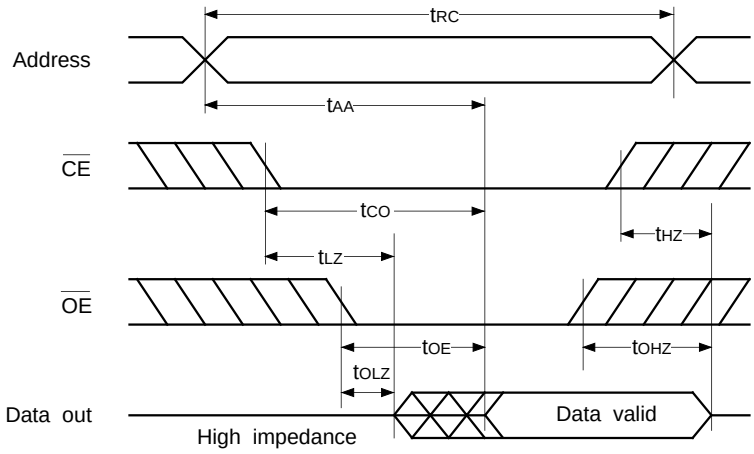
*2 t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

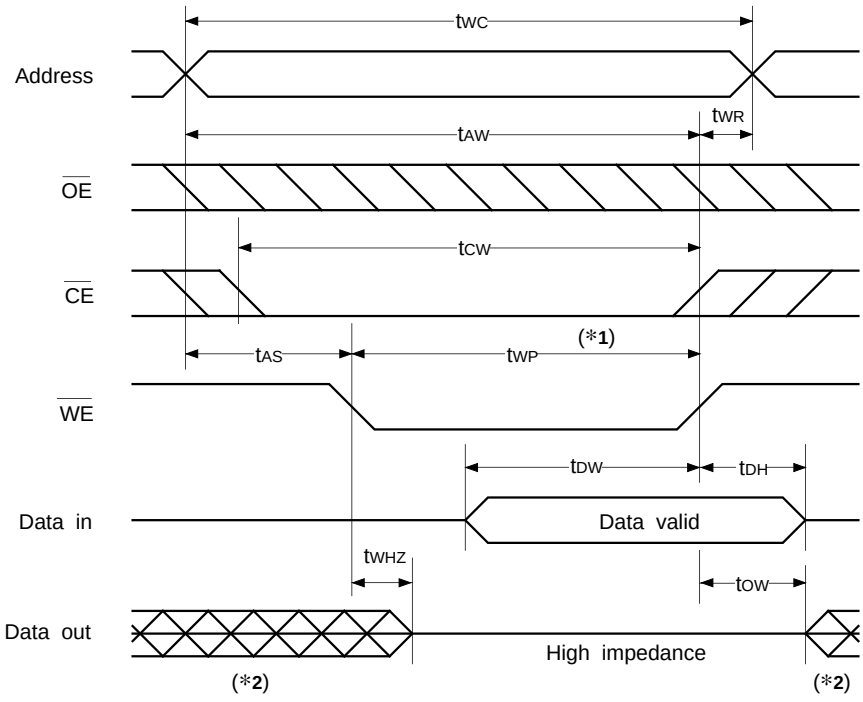
• **Read cycle (1):** $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}



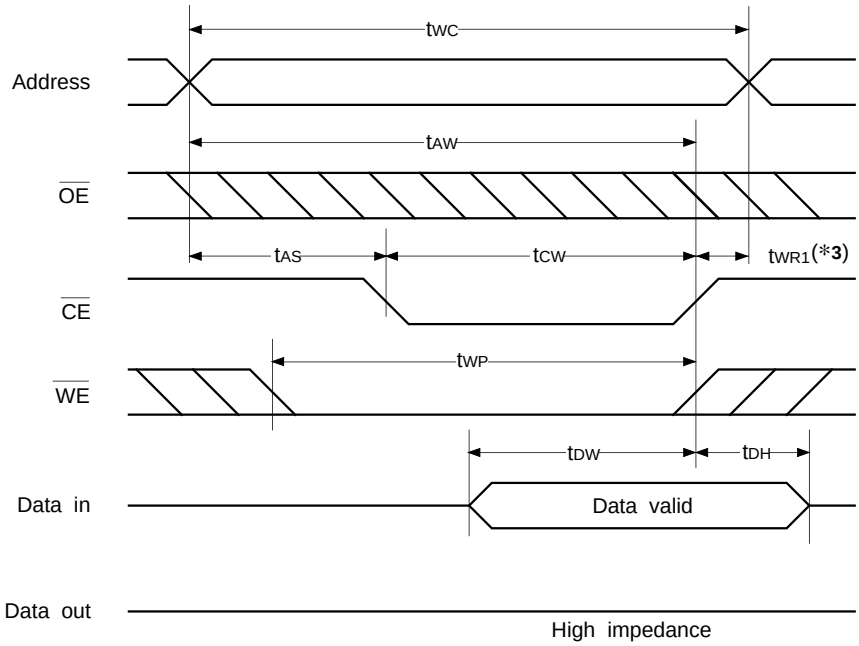
• **Read cycle (2):** $\overline{WE}$ = V_{IH}



• **Write cycle (1):** $\overline{WE}$ control



• **Write cycle (2):** $\overline{CE}$ control



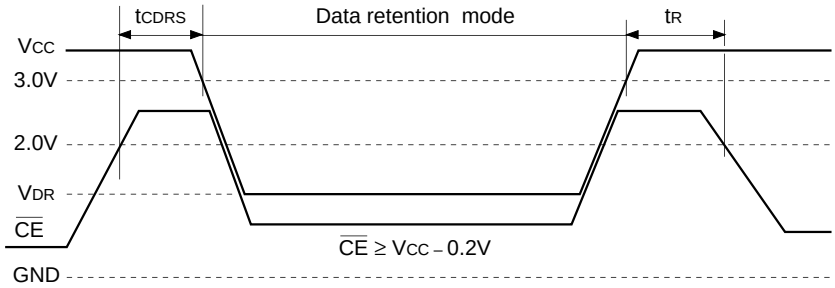
*1 Write is executed when both $\overline{CE}$ and $\overline{WE}$ are at low simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

*3 t_{WR1} is measured at the period from the rising edge of $\overline{CE}$ to the end of write cycle.

Data retention waveform

• Low supply voltage data retention waveform



Data Retention Characteristics (Ta = 0 to +70°C)

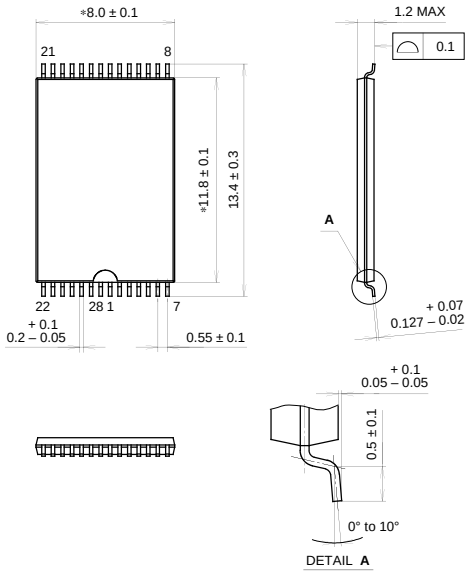
Item	Symbol	Test condiitions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$		2.0	—	3.6	V
Data retention current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CE} \geq 2.8V$	0 to +70°C	—	—	3	µA
			0 to +40°C	—	—	0.6	
			+25°C	—	0.1	0.3	
	I_{CCDR2}	V_{CC} = 2.0 to 3.6V, $\overline{CE} \geq V_{CC} - 0.2V$		—	0.12*1	3.5	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t_R			5	—	—	ms

*1 V_{CC} = 3.3V, Ta = 25°C

Package Outline Unit: mm

CXK5V8257BTM

28PIN TSOP (Plastic)



NOTE: Dimension "∗" does not include mold protrusion.

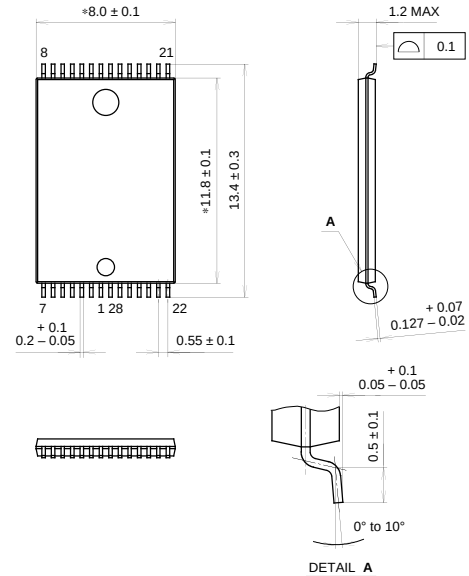
SONY CODE	TSOP-28P-L01
EIAJ CODE	TSOP028-P-0000-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

CXK5V8257BYM

28PIN TSOP (Plastic)



NOTE: Dimension "∗" does not include mold protrusion.

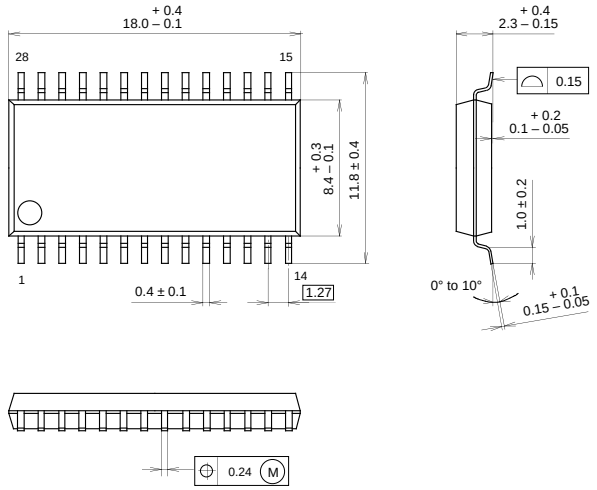
SONY CODE	TSOP-28P-L01R
EIAJ CODE	TSOP028-P-0000-B
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

CXK5V8257BM

28PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-28P-L05
EIAJ CODE	∗SOP028-P-0450
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.7g