Alternate *ACM* SIG Proceedings Paper in LaTeX Format*

[Extended Abstract] †

Po-Cheng Pan‡
Institute of Electronics and SoC Center
National Chiao Tung University
Hsinchu, Taiwan
pocheng.pan@g2.nctu.edu.tw

Prof. Hung-Ming Chen§
Institute of Electronics and SoC Center
National Chiao Tung University
Hsinchu, Taiwan
hmchen@mail.nctu.edu.tw

ABSTRACT

This is the abastract section

1. THE FIRST SECTION

Content in first section [1]

2. FLOW OF OUR FRAMEWORK

In order to provide fast prototyping for layout migration, this software extracted the reference layout with placement and routing respectively. The migrated layout is generated according to the extracted information. and then it dumps into real design after physical verification for performance simulation. Fig. 1 shows the overall flow diagram of our methodology. The flow is mainly separated into three stages:

1. **Extraction and Preservation**: A layout extraction and preservation technique [1] can not only be applied to generalized layout, but also hierarchical design.

2. **Prototyping**: The preserved topology of original layout can be generated into multiple layout candidates with placement and routing.

3. **Wire optimization**: A detailed routing refinement is applied automatically to route the unrouted nets for final verification and simulation.

In the end, a set of layouts with refinement is obtained, which provides designers a quick look of possible solutions that can be used. The layout results are automatically dumped into industrial layouts for demonstration and simulation.

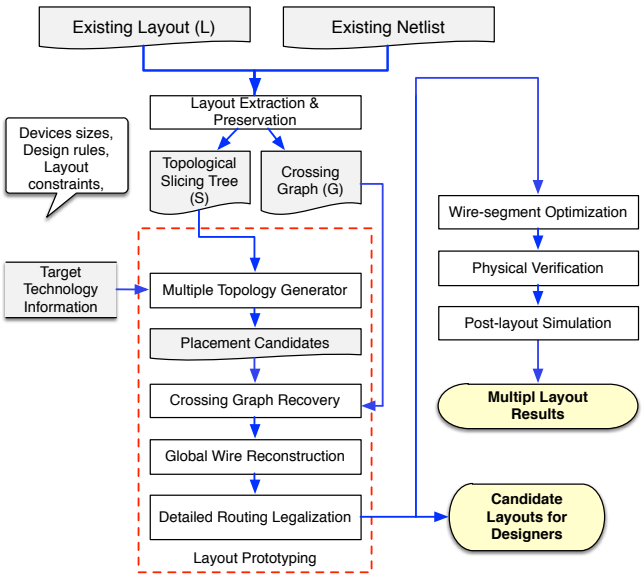

Figure 1: Overall flow of the proposed layout migration framework.

3. PROGRAM SETTING AND RESULTS

Our Software is developed with g++ 4.1.2 for methodology, Synopsys PyCell Studio™ 4.7.1 for layout realization and Qt 4.8.4 for GUI demonstration. We also display the layout with the reference one and the generated layout via Cadence® Virtuoso® 6.1.5. The migration of a variable-gain amplifier (VGA), a folded-cascode operational amplifier (OpAmp) and low dropout regulator (LDO) will be demonstrated step-by-step as applications to show the feasibility of our Software.

4. REFERENCES

[1] C.-Y. Chin, P.-C. Pan, H.-M. Cheng, T.-C. Chen, and J.-C. Lin. Efficient analog layout prototyping by layout reuse with routing preservation. In *International Conference on Computer-Aided Design*, pages 40–47, Nov 2013.

*(Produces the permission block, and copyright information). For use with SIG-ALTERNATE.CLS. Supported by ACM.

†A full version of this paper is available as *Author's Guide to Preparing ACM SIG Proceedings Using LaTeX2ε and BibTeX* at `www.acm.org/eaddress.htm`

‡note

§Professor

DAC '16 June 5–9, 2016, Auxtin, TX, USA

DOI: 10.1145/1235

Table 1: Specification of experimental circuits: OpAmp and VGA

Circuit	OpAmp	VGA
technology	umc90nm	umc90nm
V_{dd}	1V	1.1V
Load Capacitance	200pF	1.5pF
Gain	$\geq 48.653dB$	$\geq 18.48dB$
Gain Bandwidth	$\geq 100MHz$	$\geq 5MHz$
Phase Margin	$\geq 45deg$	$\geq 45deg$
Area	832.66 μm^2	10889.88 μm^2