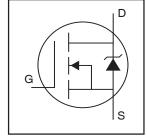
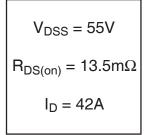
International Rectifier

IRLR2905ZPbF IRLU2905ZPbF

Features HEXFET® Power MOSFET

- Logic Level
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free





Description

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low onresistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	60	
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	43	Α
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Package Limited)	42	
I _{DM}	Pulsed Drain Current ①	240	
P _D @T _C = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.72	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E _{AS (Thermally limited)}	Single Pulse Avalanche Energy ^②	57	mJ
E _{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ®	85	
I _{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	Α
E _{AR}	Repetitive Avalanche Energy (9		mJ
T _J	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ®		1.38	
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) ♡		40	°C/W
$R_{\theta JA}$	Junction-to-Ambient		110	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Тур.	Max.	Units	Conditions	
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	55			V	$V_{GS} = 0V, I_D = 250\mu A$	
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.053		V/°C	Reference to 25°C, I _D = 1mA	
R _{DS(on)}	Static Drain-to-Source On-Resistance		11	13.5	mΩ	V _{GS} = 10V, I _D = 36A ③	
				20	mΩ	V _{GS} = 5.0V, I _D = 30A ③	
				22.5	mΩ	V _{GS} = 4.5V, I _D = 15A ③	
V _{GS(th)}	Gate Threshold Voltage	1.0		3.0	٧	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
gfs	Forward Transconductance	25		_	S	$V_{DS} = 25V, I_D = 36A$	
I _{DSS}	Drain-to-Source Leakage Current	_		20	μA	$V_{DS} = 55V, V_{GS} = 0V$	
				250		$V_{DS} = 55V, V_{GS} = 0V, T_{J} = 125^{\circ}C$	
I _{GSS}	Gate-to-Source Forward Leakage	_		200	nA	V _{GS} = 16V	
	Gate-to-Source Reverse Leakage		_	-200		V _{GS} = -16V	
Q_g	Total Gate Charge		23	35		$I_D = 36A$	
Q_{gs}	Gate-to-Source Charge		8.5		nC	$V_{DS} = 44V$	
Q_{gd}	Gate-to-Drain ("Miller") Charge		12			V _{GS} = 5.0V ③	
t _{d(on)}	Turn-On Delay Time		14			$V_{DD} = 28V$	
t _r	Rise Time		130			$I_D = 36A$	
t _{d(off)}	Turn-Off Delay Time		24		ns	$R_G = 15 \Omega$	
t _f	Fall Time		33			V _{GS} = 5.0V ③	
L _D	Internal Drain Inductance		4.5			Between lead,	
					nΗ	6mm (0.25in.)	
Ls	Internal Source Inductance		7.5			from package	
						and center of die contact	
C _{iss}	Input Capacitance		1570			$V_{GS} = 0V$	
Coss	Output Capacitance		230			$V_{DS} = 25V$	
C _{rss}	Reverse Transfer Capacitance		130		pF	f = 1.0MHz	
C _{oss}	Output Capacitance		840			$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$	
C _{oss}	Output Capacitance		180	_		$V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz$	
C _{oss} eff.	Effective Output Capacitance		290			$V_{GS} = 0V$, $V_{DS} = 0V$ to 44V $\textcircled{4}$	

Source-Drain Ratings and Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions	
IS	Continuous Source Current			42		MOSFET symbol	
	(Body Diode)				Α	showing the	
I _{SM}	Pulsed Source Current			240		integral reverse	
	(Body Diode) ①					p-n junction diode.	
V_{SD}	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C, I_S = 36A, V_{GS} = 0V$ ③	
t _{rr}	Reverse Recovery Time		22	33	ns	$T_J = 25^{\circ}C$, $I_F = 36A$, $V_{DD} = 28V$	
Q _{rr}	Reverse Recovery Charge		14	21	nC	di/dt = 100A/μs ③	
t _{on}	Forward Turn-On Time	Intrinsi	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

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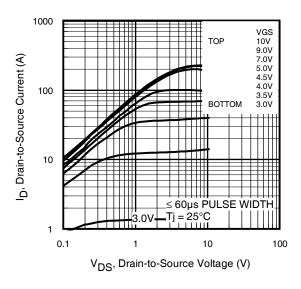


Fig 1. Typical Output Characteristics

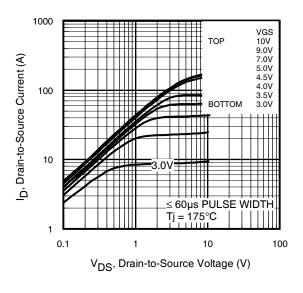


Fig 2. Typical Output Characteristics

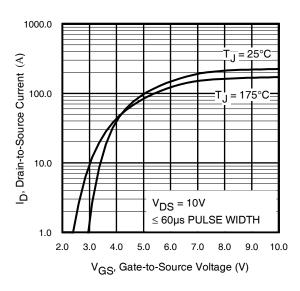


Fig 3. Typical Transfer Characteristics

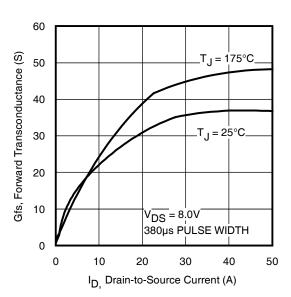


Fig 4. Typical Forward Transconductance Vs. Drain Current

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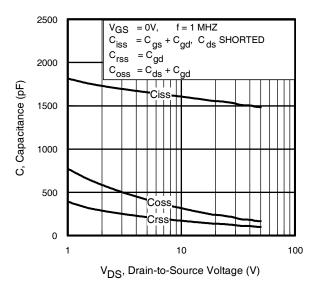


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

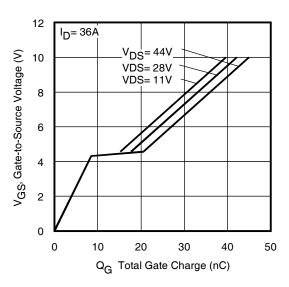


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

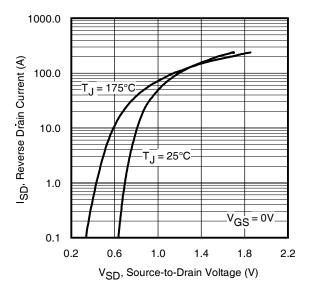


Fig 7. Typical Source-Drain Diode Forward Voltage

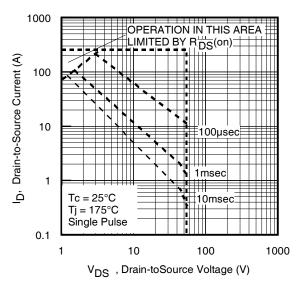


Fig 8. Maximum Safe Operating Area

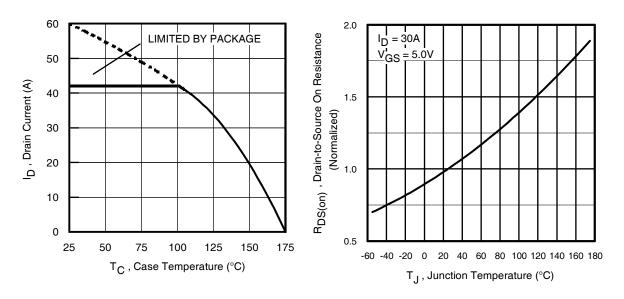


Fig 9. Maximum Drain Current Vs. Case Temperature

Fig 10. Normalized On-Resistance Vs. Temperature

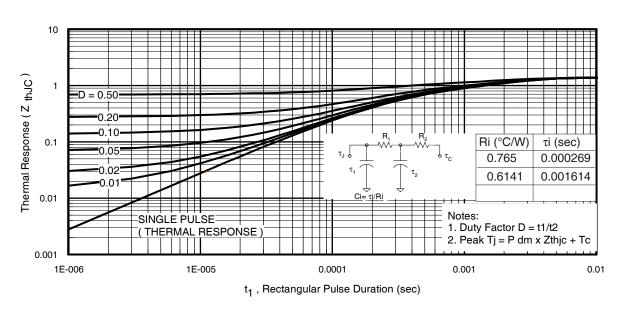


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

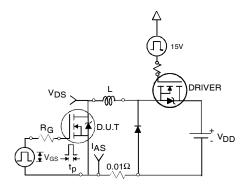


Fig 12a. Unclamped Inductive Test Circuit

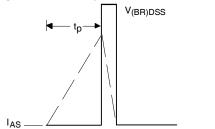


Fig 12b. | Unclamped Inductive Waveforms

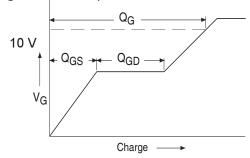


Fig 13a. Basic Gate Charge Waveform

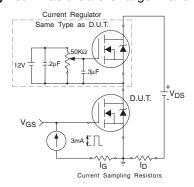


Fig 13b. Gate Charge Test Circuit 6

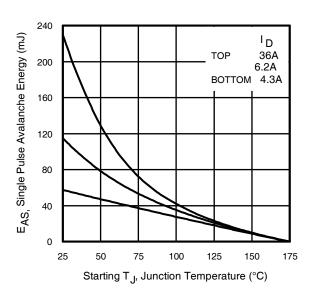


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

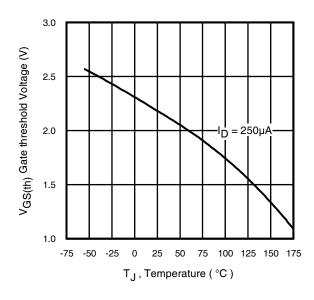


Fig 14. Threshold Voltage Vs. Temperature www.irf.com

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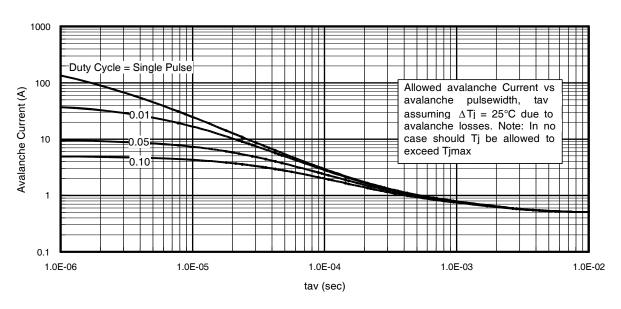


Fig 15. Typical Avalanche Current Vs. Pulsewidth

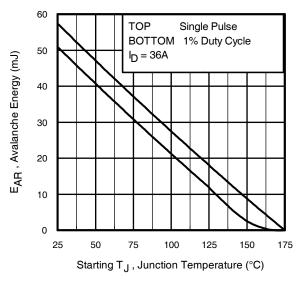


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

- Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
- 2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
- P_{D (ave)} = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. I_{av} = Allowable avalanche current.
- 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).

 t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = $t_{av} \cdot f$

 $Z_{th,JC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$\begin{split} P_{D \text{ (ave)}} &= 1/2 \text{ (} 1.3 \cdot \text{BV} \cdot I_{av} \text{)} = \triangle \text{T/ } Z_{thJC} \\ I_{av} &= 2\triangle \text{T/ } [1.3 \cdot \text{BV} \cdot Z_{th}] \\ E_{AS \text{ (AR)}} &= P_{D \text{ (ave)}} \cdot t_{av} \end{split}$$

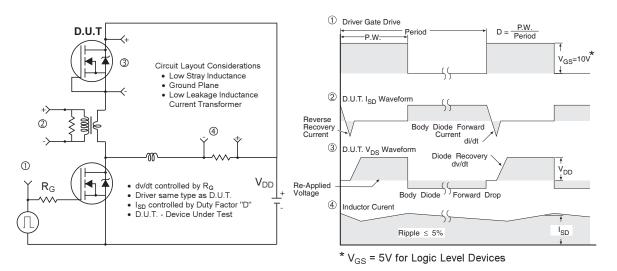


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

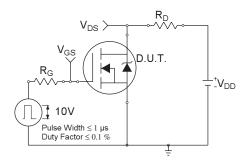


Fig 18a. Switching Time Test Circuit

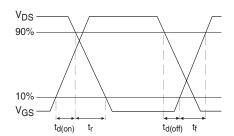


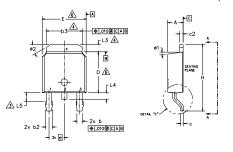
Fig 18b. Switching Time Waveforms

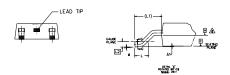
International IOR Rectifier

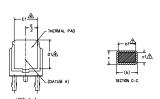
IRLR/U2905ZPbF

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)







- NOTES: 1.— DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

- DIMENSION DI, ET, L3 & 63 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.

 5.— SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. WOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE, THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY,
- A- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- A- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

S		Ŋ				
M B O	MILLIM	ETERS	INC	O T E S		
0	MIN.	MAX.	MIN.	MAX.	E S	
Α	2,18	2.39	.086	.094		
A1	-	0.13	-	.005		
ь	0.64	0.89	.025	.035		
ь1	0.65	0.79	.025	.031	7	
b2	0.76	1,14	.030	.045		
ь3	4.95	5.46	.195	.215	4	
С	0.46	0.61	.018	.024		
c1	0.41	0.56	.016	.022	7	
c2	0.46	0.89	.018	.035		
D	5.97	6.22	.235	.245	6	
D1	5.21	-	.205	-	4	
Ε	6.35	6.73	.250	.265	6	
E1	4,32	-	.170	-	4	
e	2,29	BSC	.090 BSC			
н	9.40	10,41	.370	.410		
L	1,40	1,78	.055	.070		
L1	2,74	BSC	.108	REF.		
L2	0,51	BSC	.020 BSC			
L3	0.89	1.27	.035	.050	4	
L4	-	1.02	-	.040		
L5	1,14	1,52	.045	.060	3	
ø	0.	10*	0,	10*		
ø1	0,	15*	0,	15*		
ø2	25*	35*	25*	35.		

LEAD ASSIGNMENTS

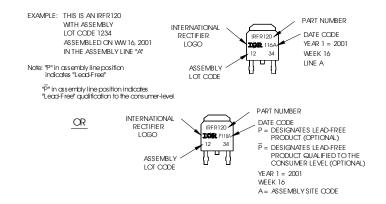
<u>HEXFET</u>

- 1.- GATE 2.- DRAIN 3.- SOURCE 4.- DRAIN

1 - GATE

- 2.- COLLECTOR
 3.- EMITTER
 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

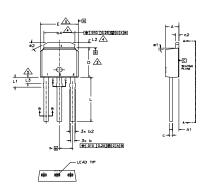


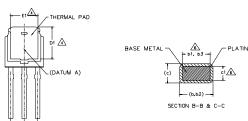
- 1. For an Automotive Qualified version of this part please seehttp://www.irf.com/product-info/auto/
- 2. For the most current drawing please refer to IR website at http://www.irf.com/package/



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)





- NOTES:
 1.— DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- △ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0,13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- A- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION 64, L2, E1 & D1.
- ▲- LEAD DIMENSION UNCONTROLLED IN L3.
- A- DIMENSION 61, 63 & c1 APPLY TO BASE METAL ONLY.
- 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
- 8.- CONTROLLING DIMENSION; INCHES.

S	DIMENSIONS				
M B O	MILLIMETERS INCHES		O T E S		
0	MIN.	MAX.	MIN.	MAX.	E
Α	2.18	2,39	.086	.094	
A1	0.89	1.14	.035	.045	
ь	0.64	0.89	.025	.035	
b1	0.65	0,79	.025	.031	6
b2	0.76	1,14	.030	.045	
ь3	0,76	1.04	.030	.041	6
b4	4,95	5,46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0,41	0,56	,016	,022	6
c2	0,46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29	BSC	.090 BSC		
L	8.89	9.65	.350	.380	
L1	1,91	2,29	.045	.090	
L2	0.89	1,27	.035	.050	4
L3	1,14	1,52	.045	.060	5
ø1	0*	15*	0,	15*	
ø2	25*	35*	25*	35*	

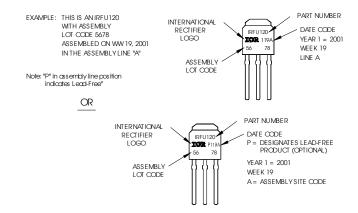
LEAD ASSIGNMENTS

HEXFET

1.- GATE 2.- DRAIN

3.- SOURCE 4.- DRAIN

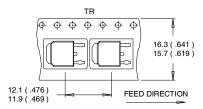
I-Pak (TO-251AA) Part Marking Information

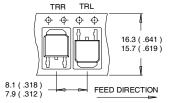


- 1. For an Automotive Qualified version of this part please seehttp://www.irf.com/product-info/auto/
- 2. For the most current drawing please refer to IR website at http://www.irf.com/package/

D-Pak (TO-252AA) Tape & Reel Information

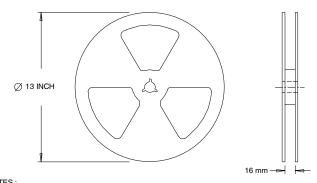
Dimensions are shown in millimeters (inches)





NOTES

- 1. CONTROLLING DIMENSION : MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25$ °C, L = 0.089mH③ $R_G = 25\Omega$, $I_{AS} = 36A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ③ Pulse width \leq 1.0ms; duty cycle \leq 2%.
- 4 Coss eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
 - Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- This value determined from sample failure population. 100% tested to this value in production.
- When mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994
- R_θ is measured at T_J approximately 90°C

Data and specifications subject to change without notice. This product has been designed for the Industrial market. Qualification Standards can be found on IR's Web site.



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