Isolated Error Amplifier for DCDC Feedback
IZL-200-140-150

FEATURES

- **Extreme Temperature Range**
  - **Continuous Operation: -55°C to 175°C**
  - **Intermittent Operation: 200°C (1000h)**
- **Bandwidth = 400 KHz**
- **Total current consumpton (I_{DD1} + I_{DD2}) = <6.5 mA total**
- **Stability In Isolated Feedback applications**
  - **0.5 % accuracy**
- **Reference voltages: 1.2 V (1.217 mean)**
- **Voltage supply range**
  - **VDD1 & VDD2 : 5 V ± 10%**
  - **XX V UVLO (4.3 V up, 4.1 V down)**
- **3000 V Peak Isolation (60 s)**
  - **Double Capacitive Isolation**
  - **High Radiated Electromagnetic Immunity**
- **< 0.5 pF Isolation capacitance**
- **CMTI > 200 kV/µs**
- **2kV ESD Protection**
- **Standard SOIC-16 Package (300mils wide body)**

APPLICATIONS

- **Applications with high thermal constrints**
- **High Voltage Motor Control**
- **DC-DC Switched Power Supplies**
- **High Voltage Inverters**
- **Compatible with type II or type III compensation networks**

DESCRIPTION

The IZL-200-140-150 is an isolated error amplifier based on VDDTECH's capacitive isolation technology. The IZL-200-140-150 is ideal for linear feedback power supplies. The primary side controllers of the IZL-200-140-150 enable improvements in transient response, precision, power density, and stability as compared to commonly used optocoupler and shunt regulator solutions. Unlike optocoupler-based solutions, which have an uncertain current transfer ratio over lifetime and at high temperatures, the IZL-200-140-150 transfer function does not change over its lifetime, and it is stable over a wide temperature range of -40°C to +175°C. Included in the IZL-200-140-150 is a wideband operational amplifier for a variety of commonly used power supply loop compensation techniques. The IZL-200-140-150 allows a feedback loop to react to fast transient conditions and overcurrent conditions. Also included is a 1.25 V reference to compare with the supply output setpoint. The IZL-200-140-150 is packaged in a 16-lead wide SOIC package for a 2.5 kV rms isolation voltage rating.

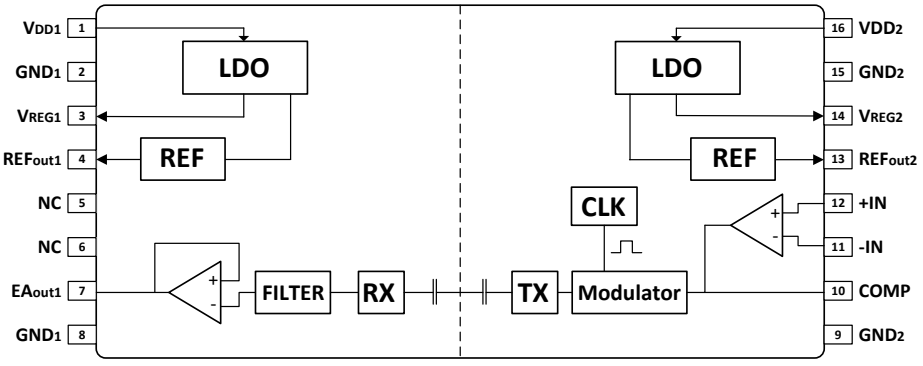

Figure 1: IZL-200-140-150 Functional block schematic illustration.

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PIN CONFIGURATION AND DESCRIPTION

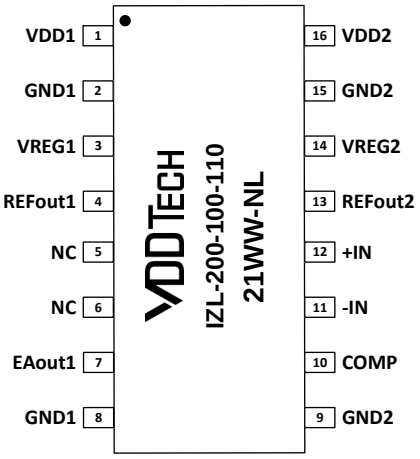

Figure 2: IZL-200-140-150 Pin Definition.

Table 1: Revisions

PIN NUMBER	PIN NAME	FUNCTION	DESCRIPTION
1	VDD1	Positive Supply	5 V Power Supply for left side. Connect a $1\mu F$ capacitor between VDD1 and GND1
2,8	GND1	Ground	Ground connection for VDD1
3	VREG1	Analog Output	3.3 V Internal Power Supply for left side. Connect a $1\mu F$ capacitor between VREG1 and GND1
4	REFout1	Analog Output	Reference output Voltage for left side. Max cap
5,6	NC	Not Connected	No connection. Connect pin 5,6 to GND; do not leave floating
7	EAout1	Analog Output	Isolated Output Voltage
9,15	GND2	Ground	Ground connection for VDD2
10	COMP	Analog Output	Op Amp Output. Compensation network can be connected between COMP pin and -IN pin
11	-IN	Analog Input	Inverting Op Amp Input. Pin 11 is the connection of the power supply setpoint and compensation network
12	+IN	Analog Input	Noninverting Op Amp Input. Pin 12 can be used as reference input.
13	REFout2	Analog Output	Reference output Voltage for right side. Max cap
14	VREG2	Analog Output	3.3 V Internal Power Supply for right side. Connect a $1\mu F$ capacitor between VREG1 and GND1
16	VDD2	Positive Supply	5V Power Supply for right side

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SPECIFICATIONS

V_{DD1} = V_{DD1} = 5V for T_A = T_{MIN} to T_{MAX}. All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD1} = 5V, unless otherwise noted

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
ACCURACY	(1.2V-EA_{out})/1.2 x 100%; see figure XXX					
Initial Error		T_A = 25°C		0.4898		%
Total Error		T_A = T_{MIN} to T_{MAX}				%
OP AMP						
Offset Error						mV
Open-Loop Gain						dB
Input Common-Mode Range						V
Gain Bandwidth Product						MHz
Common-Mode Rejection						dB
Input Capacitance						pF
Output Voltage Range	COMP pin					V
Input Bias Current						μ
Reference						
Output Voltage	0 mA to 1mA load, Crefout	T_A = 25 °C	1.2015	1.2035	1.2045	V
	0 mA to 1mA load, Crefout	T_A =T_{MIN} to T_{MAX}				V
Output Current	Crefout}					mA
UVLO						
Positive Going Threshold				4.3		V
Negative Going Threshold				4.1		V
EA_{out} Impedance	V_{DD1} < UVLO threshold					mA
OUTPUT CHARACTERISTICS	See figure XXX					
Output Gain	From COMP to EA_{out}, 0.4 V to 1.8 V, ±3 mA			0.99		V/V
Output Offseet Voltage	From COMP to EA_{out}, 0.4 V to 1.8 V, ±3 mA		-0.115	-0.85	-0.065	V
Output Linearity	From COMP to EA_{out}, 0.4 V to 1.8 V, ±3 mA					%
Output -3 dB Bandwidth	From COMP to EA_{out}, 0.4 V to 1.8 V, ±3 mA			498		kHz
Output Voltage, EA_{out}	±3 mA output					
Low Voltage						V
High Voltage						V
Noise, EA_{out}						mV rms
POWER SUPPLY						
Operating Range, Side 1	V_{DD1}					
Operating Range, Side 2	V_{DD2}					
Power Supply Rejection	DC, V_{DD1} = V_{DD1} 3V to 20V					dB
Supply Current						
I_{DD1}				2.4		mA
I_{DD2}				4.1		mA

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Absolute Maximum Ratings

PADS used: VDDALLPADF5(5v vdd), APR00DEF, VDDALLPADEF(vreg), GNDALLPADEF

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
VDD1 vs. GND1	Left side DC Supply	-0.5	7	V
VDD2 vs. GND2	Right side DC Supply	-0.5	7	V
GND1 vs. GND2	DC Isolation	-500	500	V
I/O vs. GNDx	Input/Output voltage on +IN, -IN, REFoutx, COMP, EAout pins versus GNDx	-0.5	VDDx+0.5	V
IOUT 5V	Output current per Output pin for VDDx = 5V	-10	10	mA
Tj	Junction temperature	-55	185	°C

ESD Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V_{HBM}	Human Body Model Robustness	-4000	4000	V
V_{MM}	Machine Model Robustness	-100	100	V
V_{CDM}	Charged Device Model robustness	-500	500	V
$I_{LATCHUP}$	Latch-up immunity	-200	200	mA

Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
VDD1 vs. GND1	Left side DC Supply vs. GND1	4.5	5.5	V
VDD2 vs. GND2	Right side DC Supply vs. GND2	4.5	5.5	V
I/O vs. GNDx	Input/Output voltage on +IN, -IN, REFoutx, COMP, EAout pins versus GNDx	-0.5	3.6	V
T_R/T_F	Input signal Riseand Fall times		1	ms
T_A	Ambient temperature	-55	175	°C

Insulation Characteristics

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CLR	External clearance: Shortest primary-to-secondary distance through air	8		mm
CRP	External creepage: Shortest primary-to-secondary distance along the package	8		mm
DTI	Isolation distance: Minimum internal isolation gap	6		μm
C_{IB}	Total isolation barrier capacitance	0.5		pF
V_{IOTM}	Maximum transient isolation voltage	4		kV
V_{IORM}	Maximum repetitive peak isolation voltage	1		kV

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TEST CIRCUITS

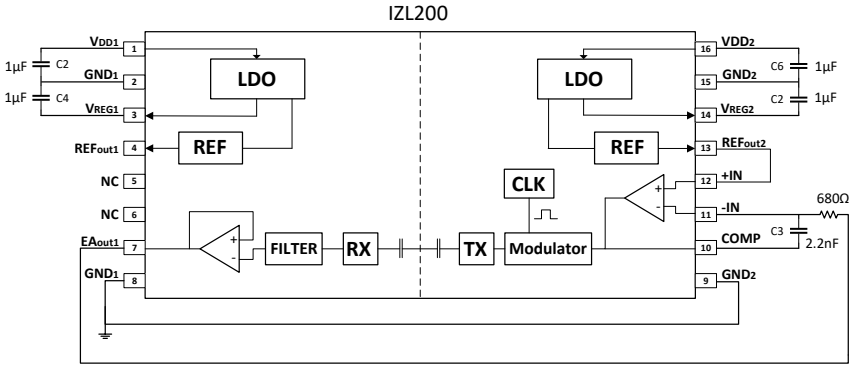


Figure 3: Test circuit 1: Accuracy Circuit using EAout.

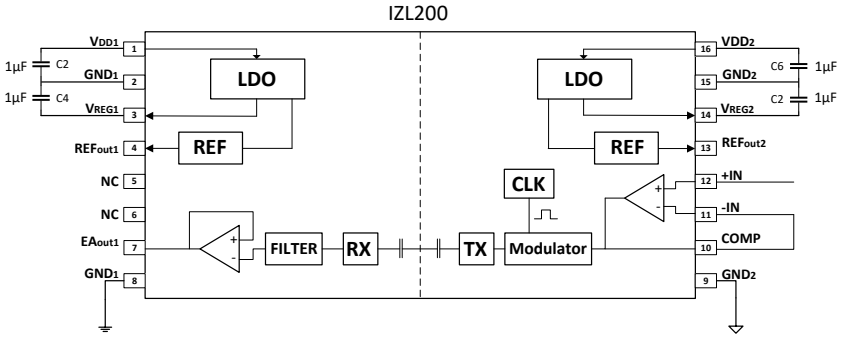


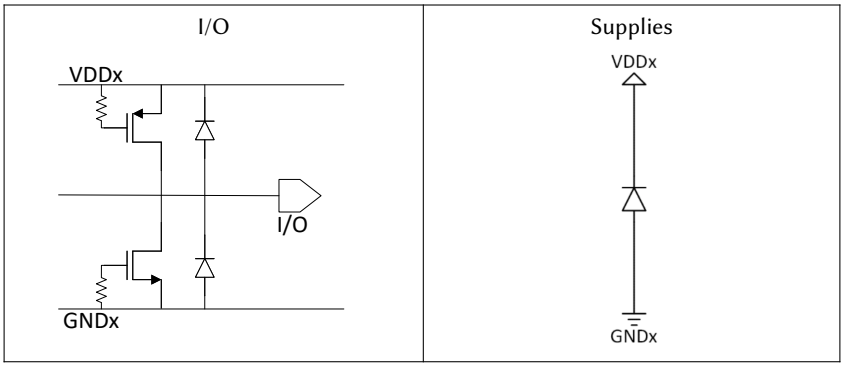
Figure 4: Test circuit 2: Isolated Amplifier Circuit.

DEVICE INFORMATION

Power up/down description

During the power-up sequence of VDDx, the UVLO block puts in power down mode the corresponding EAout output until VDDx is higher than UVLO threshold $V_{TH\_UVLO\_UP}$. During the power-down sequence of VDDx, the UVLO block puts in power down mode the corresponding EAout output until VDDx is lower than UVLO threshold $V_{TH\_UVLO\_DN}$.

ESD I/O Schematics



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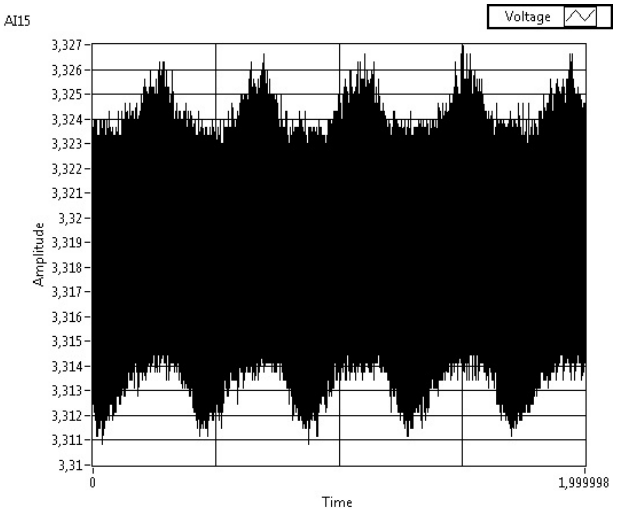
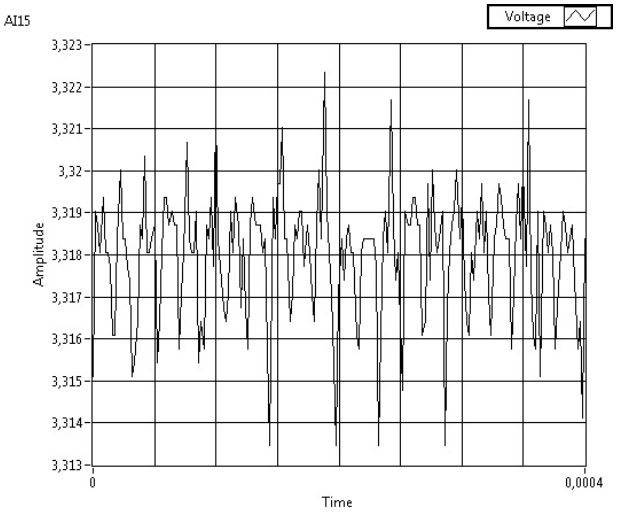
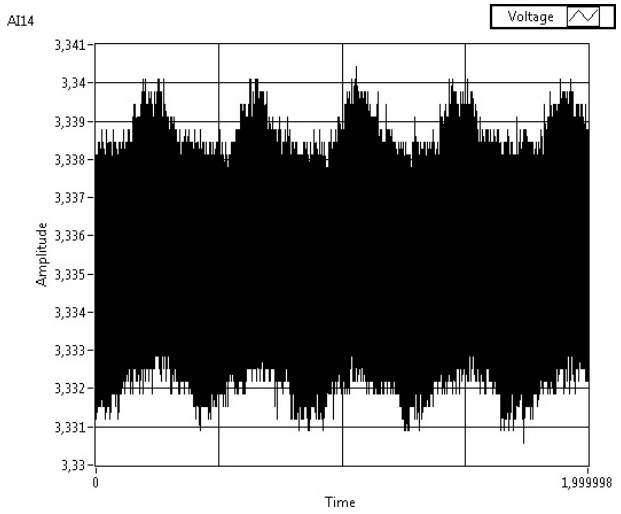
TYPICAL PERFORMANCE CHARACTERISTICS



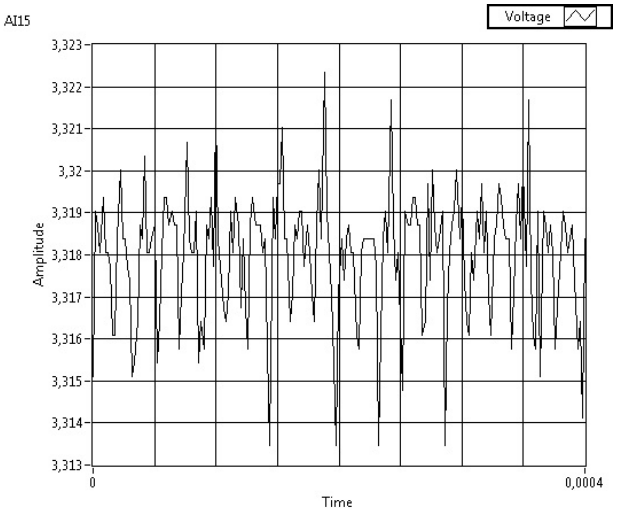
(a) VREG1 at T = 25 °C, Vrms = 3.318081



(b) VREG1 at T = 25 °C



(c) VREG2 at T = 25 °C, Vrms = 3.324125



(d) VREG2 at T = 25 °C

Figure 5: VREGx 3.3 V output at T = 25 °C

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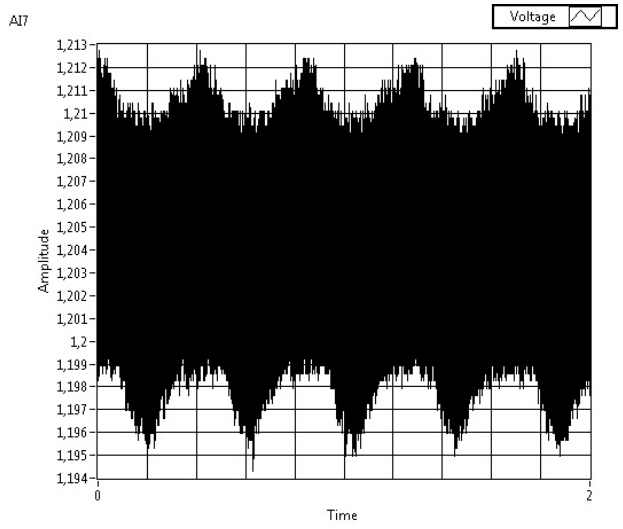
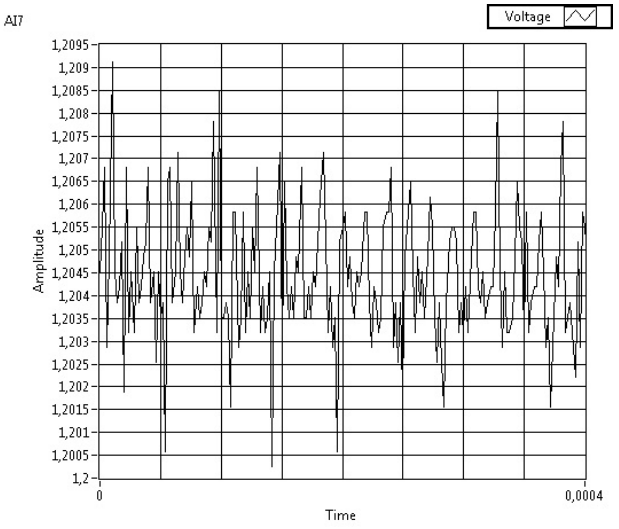
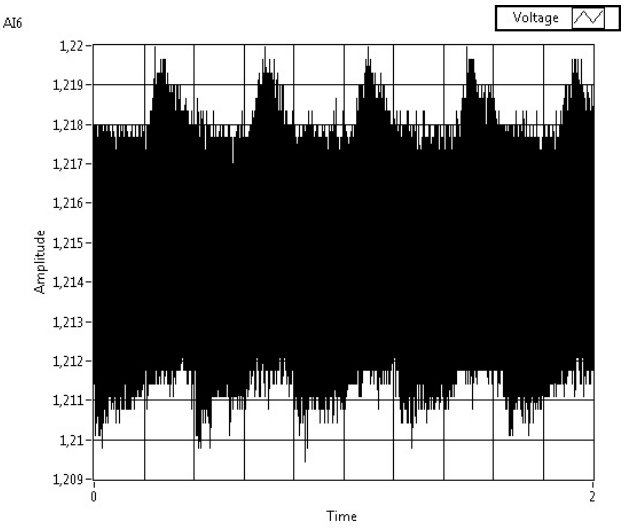


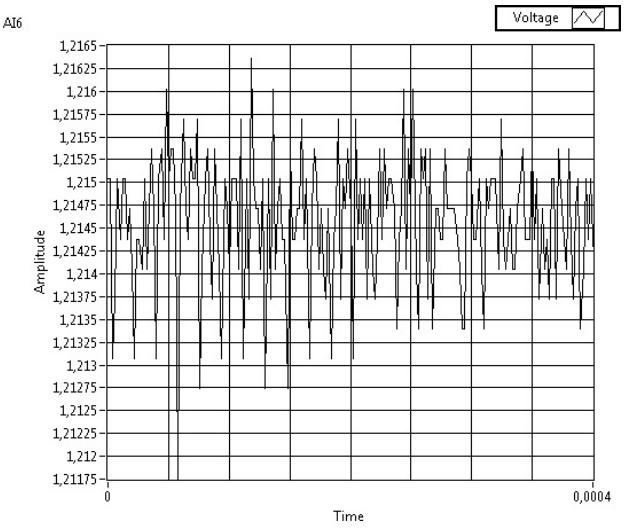
(a) REFout1 at T = 25 °C, Vrms = 3.318081



(b) REFout1 at T = 25 °C



(c) REFout2 at T = 25 °C, Vrms = 3.324125



(d) REFout2 at T = 25 °C

Figure 6: REFoutx 1.2 V output at T = 25 °C

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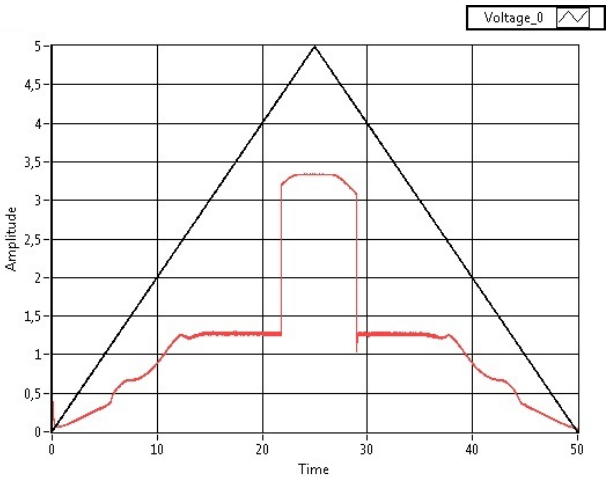
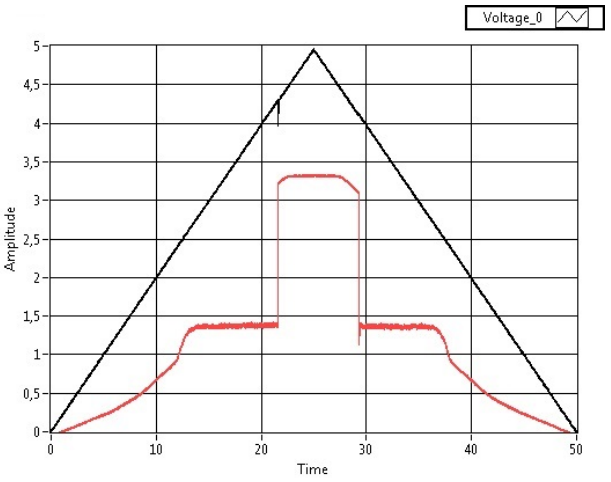
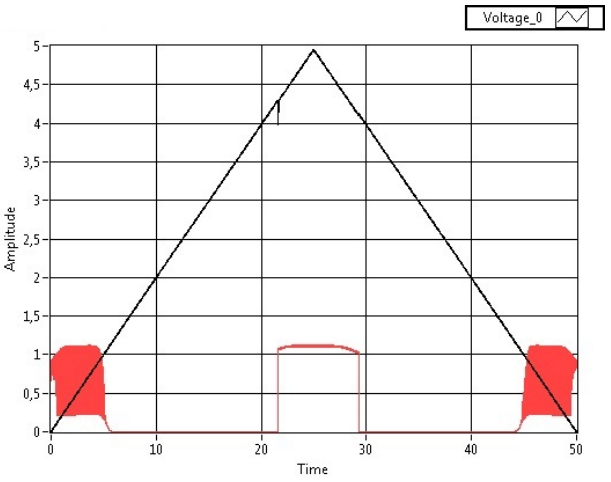


(a) Right side UVLO vs VREG at T = 25 °C



(b) Left side UVLO vs VREG at T = 25 °C



(c) Left side UVLO vs EAout at T = 25 °C

Figure 7: VDDx sweep vs VREGx and EAout

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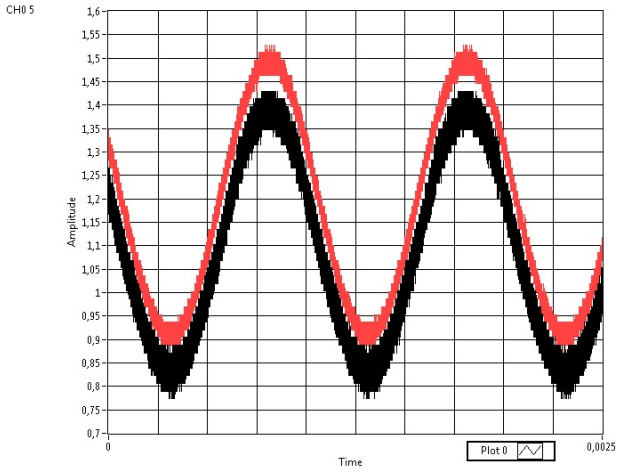
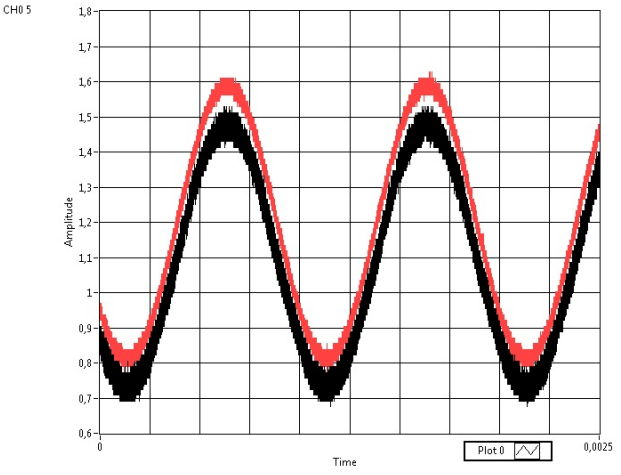
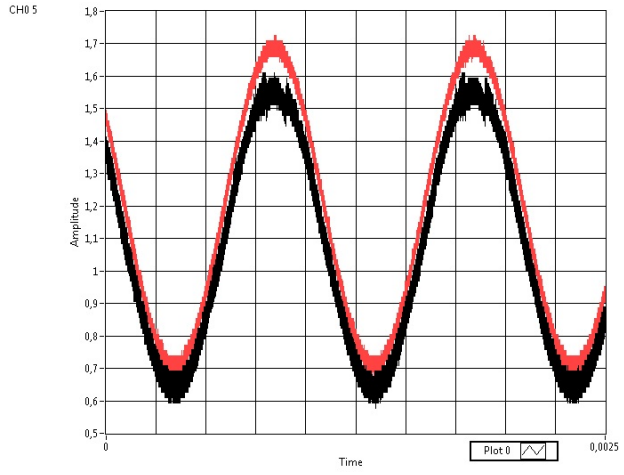


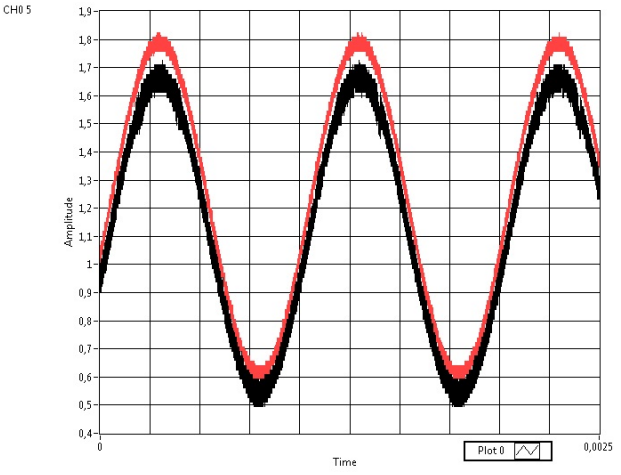
(a) Frequency 1 kHz, Offset 1.2 V, Amplitude 0.3 Vp



(b) Frequency 1 kHz, Offset 1.2 V, Amplitude 0.4 Vp



(c) Frequency 1 kHz, Offset 1.2 V, Amplitude 0.5 Vp



(d) Frequency 1 kHz, Offset 1.2 V, Amplitude 0.6 Vp

Figure 8: Input signal vs Eaout at T = 25 °C

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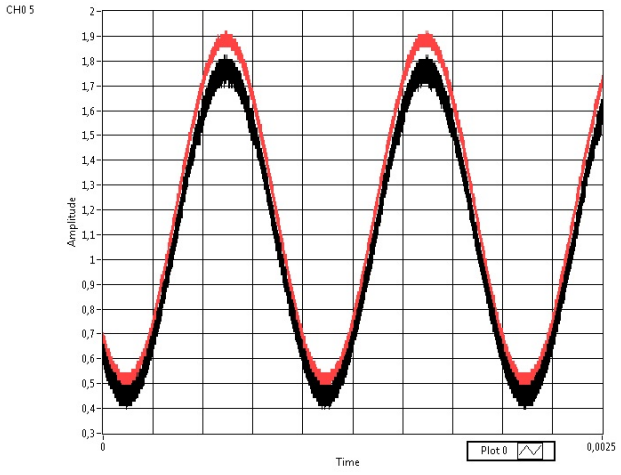
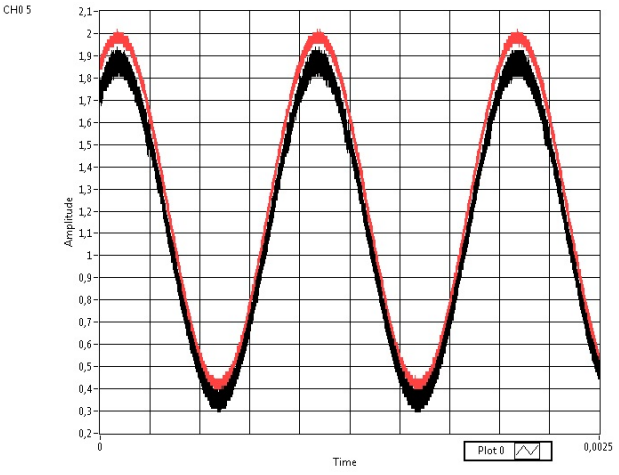
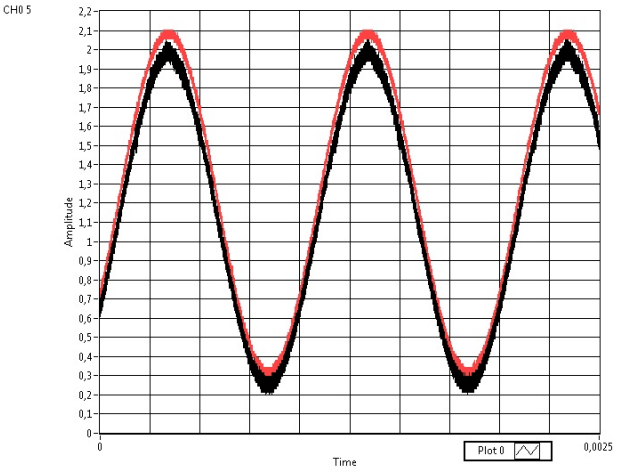


(a) Frequency 1 kHz, Offset 1.2 V, Amplitude 0.7 Vp



(b) Frequency 1 kHz, Offset 1.2 V, Amplitude 0.8 Vp



(c) Frequency 1 kHz, Offset 1.2 V, Amplitude 0.9 Vp

Figure 9: Input signal vs Eaout at T = 25 °C

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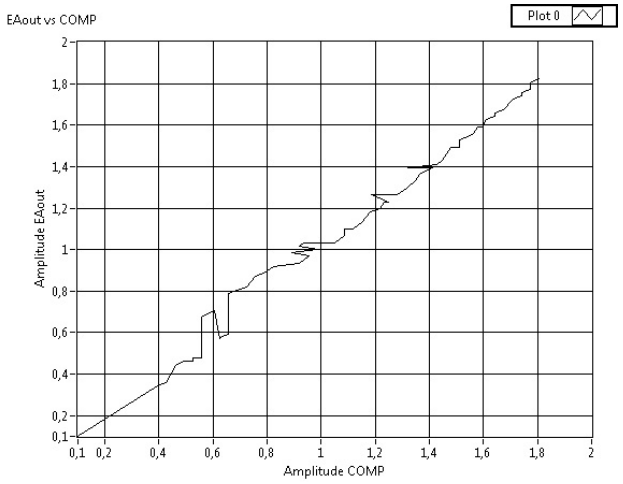
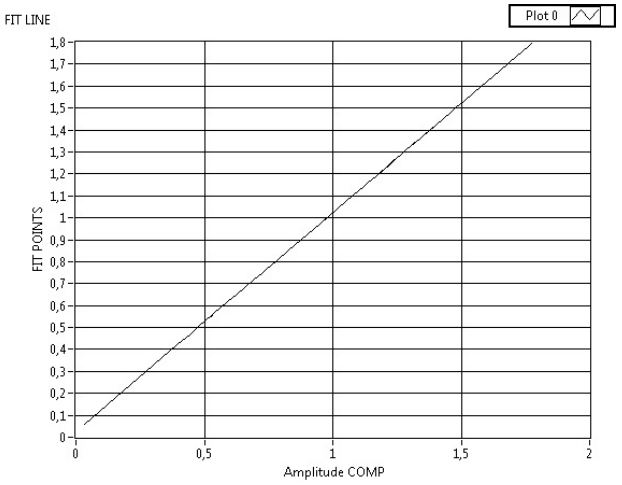
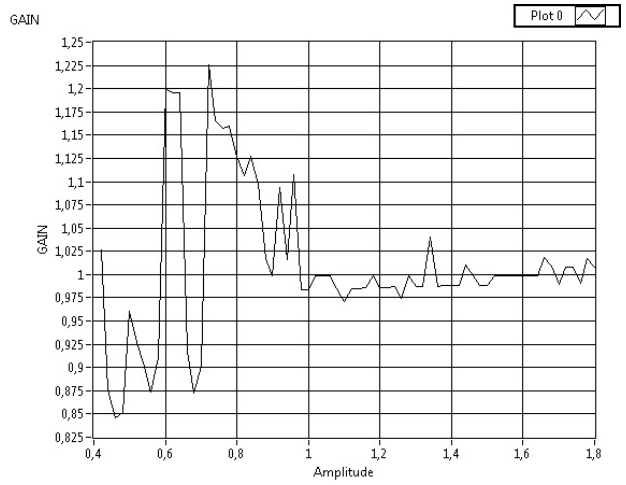


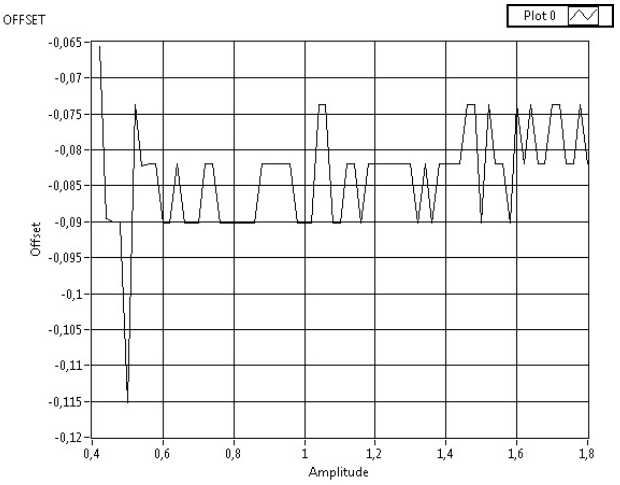
(a) EAout amplitude vs COMP amplitude for a 1kHz sine input at T = 25 °C



(b) EAout amplitude vs COMP amplitude best fit line



(c) Gain vs amplitude for a 1kHz sine input at T = 25 °C



(d) Offset vs amplitude for a 1kHz sine input at T = 25 °C

Figure 10: Gain, Offset and Linearity measurements at T = 25 °C

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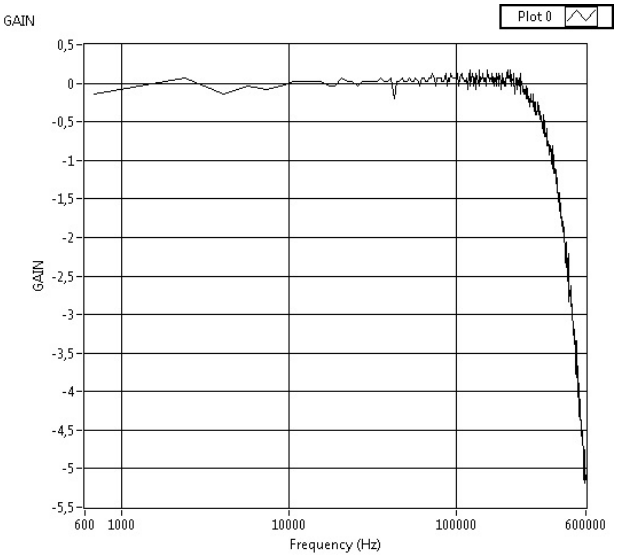
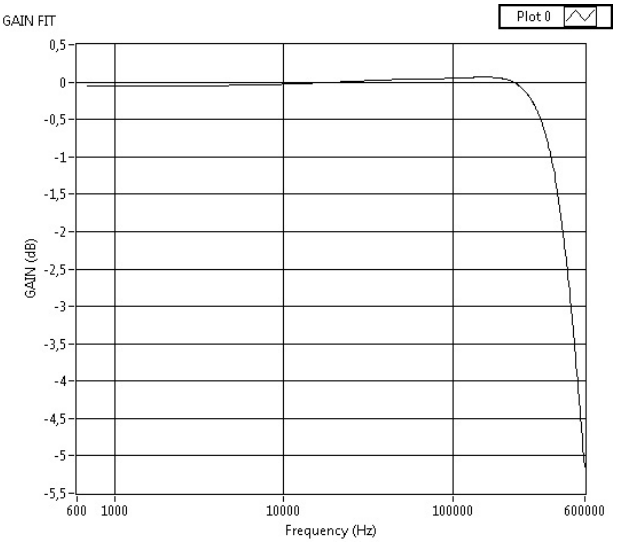
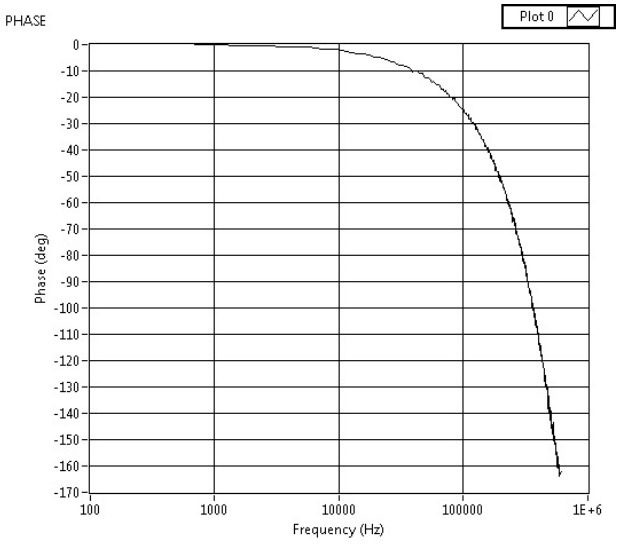


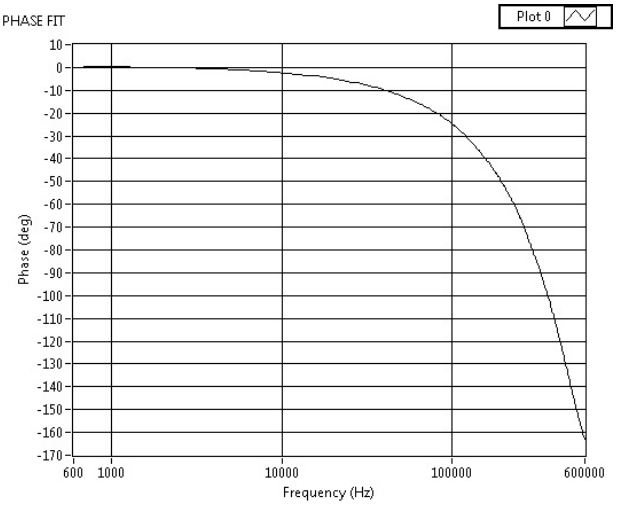
(a) Gain frequency response



(b) Gain frequency response best fit line



(c) Phase frequency response



(d) Phase frequency response best fit line

Figure 11: Frequency response at T = 25 °C

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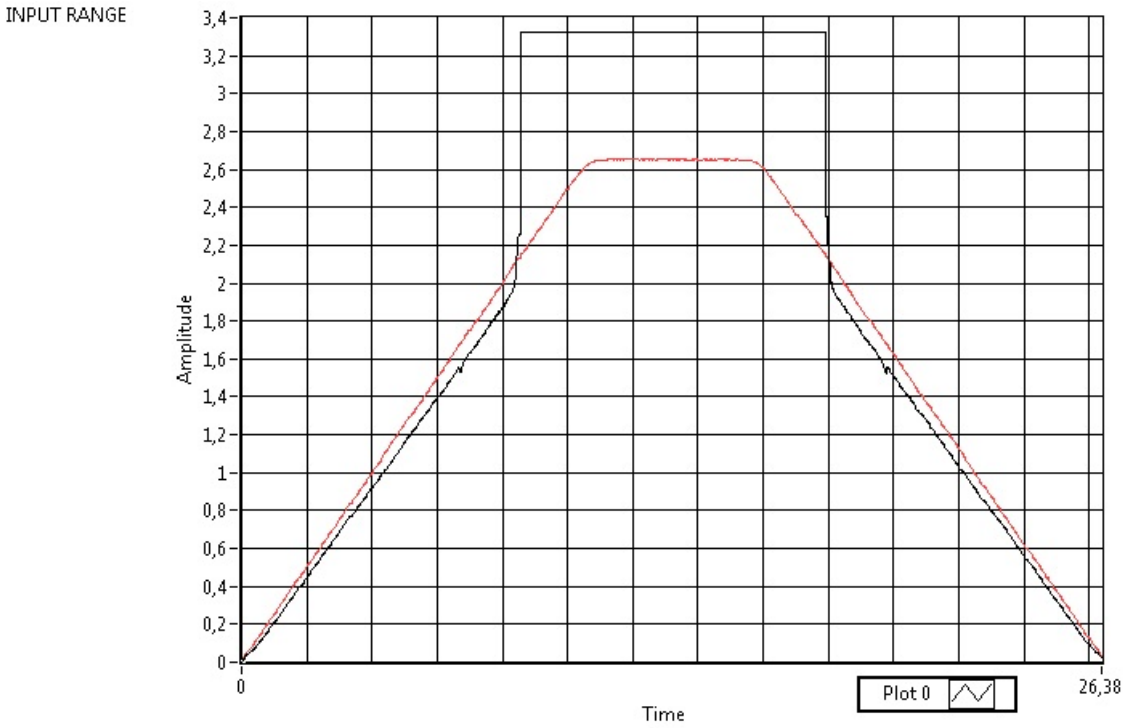

Figure 12: +IN sweep vs EAout, see fig 4.

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PACKAGING INFORMATION

AVAILABLE SOON: SOIC16

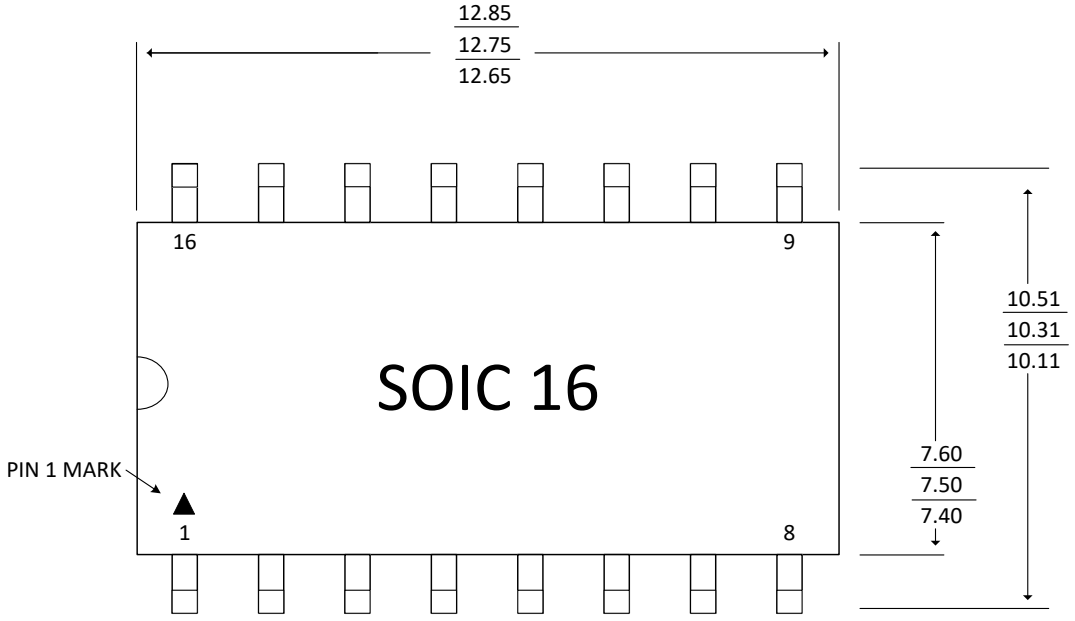

Figure 13: SOIC 16 Package Drawing.

Prototype samples package (die on PCB)

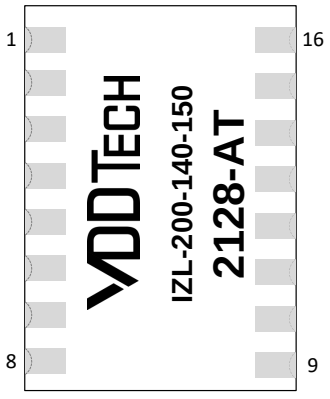

Figure 14: Prototype sample package (top view) pinout and marking indication. Note that pins are located on the bottom and thus not visible from the top. Pin 1 is located at the end of VDDTECH marking.

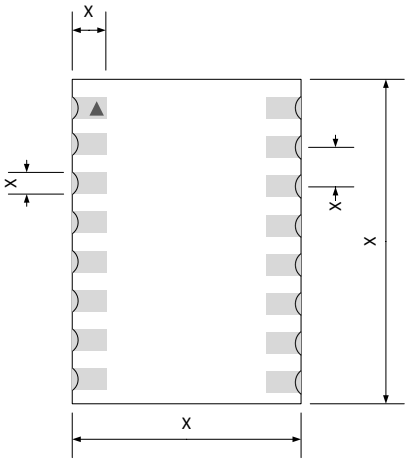

Figure 15: Prototype sample package (Bottom view). Shaded areas are metal leads on bottom of PCB . Note that Pin 1 lead is rounded.

9.2.1 Note on samples soldering

During manual soldering process, care should be taken with residues of flux or cleaning substances since they could cause leakage currents between pins at high temperature. For this reason reflow soldering is recommended.

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