UCC12050 500-mW, High-Efficiency, Low-Emissions, 5-kV_{RMS} Isolated DC-DC Converter

1 Features

- Fully integrated high-efficiency isolated DC-DC converter
- Low electromagnetic emissions
- Input voltage: 4.5 V to 5.5 V
- 500-mW typical output power
- Regulated 5.0-V or 3.3-V output with selectable 400-mV headroom voltage to power an LDO
- Short circuit tolerant
- Thermal shutdown
- 16-pin wide SOIC package
- Extended ambient temperature range: –40ºC to +125ºC
- 100-V/ns typical common mode transient immunity
- Planned safety-related certifications:
  - 7071-V_{PK} reinforced isolation per DIN V VDE V 0884-11:2017-01
  - 5000-V_{RMS} isolation for 1 minute per UL 1577
  - CSA certification per IEC 60950-1, IEC 62368-1 and IEC 60601-1 end equipment standards
  - CQC approval per GB4943.1-2011

2 Applications

- Isolated instrumentation supply
- Industrial control and instrumentation
- 4-mA to 20-mA loop supply
- Precision sensors
- Automated test equipment
- Motor drive monitor and control

3 Description

UCC12050 is a high isolation voltage DC/DC converter designed to provide efficient isolated power to isolated circuits that require well-regulated supply voltages. The UCC12050 integrates a transformer and DC/DC controller with a proprietary architecture to achieve high efficiency with very low emissions. UCC12050 provides 500 mW (typical) of isolated output power at high efficiency.

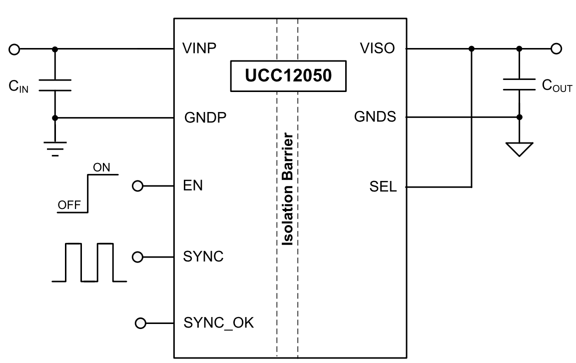
Requiring a minimum of external components and including on-chip device protection, UCC12050 provides extra features such as an enable pin, synchronization of switching frequency among multiple devices, and selection of isolated output voltages.

Device Information(1)

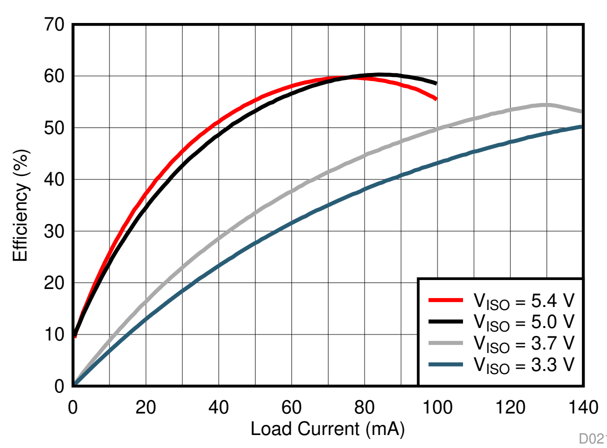
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC12050	DVE SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Typical Efficiency vs. Load



V_{INP} = 5.0 V T_A = 25ºC

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4 Revision History

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• Updated I_{VINO} Typical Values in *Electrical Characteristics* Table	7

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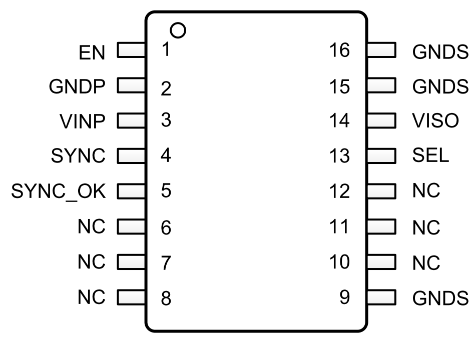
5 Pin Configuration and Functions

DVE Package
16-Pin SOIC
Top View



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Forcing EN low will disable the device. Pull high to enable normal device functionality.
GNDP	2	P	Power ground return connection for VINP
VINP	3	P	Primary side input supply voltage pin. A 10-µF ceramic capacitor to GNDP on pin 2, placed close to the device pins, is required.
SYNC	4	I	Synchronous clock input pin. Provide a clock signal to synchronize multiple UCC12050 devices or connect to GNDP for standalone operation using the internal oscillator. If the SYNC pin is left open it should be separated from any switching noise to avoid false clock coupling.
SYNC_OK	5	O	Active-low, open-drain diagnostic output. Pin is asserted LOW if an no external SYNC clock or one that is outside of the operating range of the UCC12050 is detected. In this state, the external clock is ignored and the DC-DC converter is clocked by the device's internal oscillator. The pin is in high-impedance if a good clock is applied on SYNC.
NC	6, 7, 8	—	No internal connection. Pin belongs to primary-side voltage domain. Connect to GNDP on printed circuit board.
GNDS	9	P	Connect to GNDS plane on printed circuit board.
NC	10, 11, 12	—	No internal connection. Pin belongs to isolated voltage domain. Connect to GNDS on printed circuit board.
SEL	13	I	V_{ISO} selection pin. V_{ISO} setpoint is 5.0 V when SEL is shorted to V_{ISO}. V_{ISO} setpoint is 5.4 V when SEL is shorted to V_{ISO}through a 100-kΩ resistor. For more information see the Device Functional Modes.
VISO	14	P	Isolated supply voltage pin. A 10-µF ceramic capacitor to GNDS on pin 15, placed close to the device pins, is required.
GNDS	15	P	Secondary side ground return connection for VISO. Connect bypass cap from VISO to this pin.
GNDS	16	P	Connect to GNDS plane on printed circuit board.

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
VINP to GNDP	–0.3	6.0	V
EN, SYNC, SYNC_OK, to GNDP	–0.3	VINP + 0.3, ≤ 6.0	V
VISO to GNDS	–0.3	6.0	V
SEL to GNDS	–0.3	VISO + 0.3, ≤ 6.0	V
Operating junction temperature range, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VINP	Primary side supply voltage	4.5	5.0	5.5	V
EN, SYNC	Input voltage	0		5.5	V
f_{SYNC}	External DC-DC converter synchronization signal frequency	14.4	16.0	17.6	MHz
T_a	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC		UCC12050	UNIT
		DVE (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

6.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 120	µm

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

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Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage Category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01 (Planned Certification Targets)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} = 10000 V_{PK} (qualification)	6250	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 1696 V_{PK}, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM} = 2262 V_{PK}, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM} = 2651 V_{PK}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	~3.5	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5000 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} = 6000 V_{RMS}, t = 1 s (100% production)	5000	V_{RMS}
UL 1577 (Planned Certification Target)				

(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

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6.6 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN V VDE V 0884-11:2017-01	Plan to certify according to IEC 60950-1, IEC 62368-1, and IEC 60601-1	Plan to certify under UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/ A12:2011/A2:2013
Reinforced insulation Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1414 V_{PK}; Maximum surge isolation voltage, 6250 VPK	Reinforced insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1-14 and IEC 62368-1 2nd Ed., 800 V_{RMS} maximum working voltage (pollution degree 2, material group I) ; 2 MOPP (Means of Patient Protection) per CSA 60601- 1:14 and IEC 60601-1 Ed.3+A1, 250 V_{RMS} maximum working voltage	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage	5000 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} 5000 V_{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/ A12:2011/A2:2013 up to working voltage of 800 V_{RMS}
Certificate number: (planned)	Master contract number: (planned)	File number: (planned)	Certificate number: (planned)	Client ID number: (planned)

6.7 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MAX	UNIT
I_S	Safety input current (1)	$R_{\theta JA}$ = 63.8°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C	356	mA
		$R_{\theta JA}$ = 63.8°C/W, V_I = 4.5 V, T_J = 150°C, T_A = 25°C	435	
P_S	Safety input power	$R_{\theta JA}$ = 63.8°C/W, T_J = 150°C, T_A = 25°C	1960	mW
T_S	Safety temperature (1)		150	ºC

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.8 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 150°C), V_{INP} = 4.5V to 5.5V, C_{INP} = C_{OUT} = 10 µF, SEL connected to V_{ISO}, unless otherwise noted. All typical values at T_J = 25°C and V_{INP} = 5.0V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
I_{VINQ}	VINP quiescent current,disabled	EN=LOW			100	uA
I_{VINO}	VINP operating current, no load	EN=HI; SEL shorted to VISO (5.0V output)		50		mA
		EN=HI; SEL 100kΩ to VISO (5.4V output)		45		
		EN=HI; SEL shorted to GNDS (3.3V output)		90		
		EN=HI; SEL 100kΩ to GNDS (3.7V output)		80		
I_{VIN_SC}	DC current from VINP supplyunder short circuit on VISO	VISO short to GNDS		245		mA
V_{UVPR}	VINP under-voltage lockout rising threshold			4.2		V
V_{UVPF}	VINP under-voltage lockout falling threshold			3.7		V
V_{UVPH}	VINP under-voltage lockout hysteresis			0.5		V
EN, SYNC INPUT PINS						
V_{IR}	Input voltage threshold, logic HIGH	Rising edge			2.2	V
V_{IF}	Input voltage threshold, logic LOW	Falling edge	0.8			V
I_{EN}	Enable Pin Input Current	V_{EN} = 5.0 V		5	10	uA
I_{SYNC}	SYNC Pin Input Current	V_{SYNC} = 5.0 V		0.02	1	uA
SYNC_OK PIN						
V_{OL}	SYNC_OK output low voltage	I_{SYNC_OK} = - 2 mA		0.15		V
$I_{LKG\_SYNC\_OK}$	SYNC_OK pin leakage current	V_{SYNC_OK} = 5.0 V			1	uA
DC-DC CONVERTER						
V_{ISO}	Isolated supply output voltage	SEL shorted to VISO (5.0V output); T_J = 25℃, I_{ISO} load = 0 – 100 mA, V_{INP} ≥ 5.0V	4.7	5	5.3	V
		SEL 100kΩ to VISO (5.4 V output); T_J = 25℃, I_{ISO} load = 0 – 90 mA, V_{INP} ≥ 5.0V	5.1	5.4	5.7	V
		SEL shorted to GNDS (3.3V output); T_J = 25℃, I_{ISO} load = 0 – 150 mA, V_{INP} ≥ 5.0V	3.1	3.3	3.5	V
		SEL 100kΩ to GNDS (3.7 V output); T_J = 25℃, I_{ISO} load = 0 – 130mA, V_{INP} ≥ 5.0V	3.5	3.7	3.9	V

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Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 150°C), V_{INP} = 4.5V to 5.5V, C_{INP} = C_{OUT} = 10 µF, SEL connected to V_{ISO}, unless otherwise noted. All typical values at T_J = 25°C and V_{INP} = 5.0V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ISO(RIP)}$	Voltage ripple on isolated supply output (pk-pk)	20-MHz bandwidth, CLOAD = 10 uF || 0.1 uF, SEL 100kΩ to VISO (5.4V output); I_{ISO} = 90 mA		50		mV
		20-MHz bandwidth, CLOAD = 10 uF || 0.1 uF, SEL shorted to VISO (5.0V output); I_{ISO} = 100 mA		50		mV
		20-MHz bandwidth, CLOAD = 10 uF || 0.1 uF, SEL shorted to GNDS (3.7V output); I_{ISO} = 130 mA		50		mV
		20-MHz bandwidth, CLOAD = 10 uF || 0.1 uF, SEL shorted to GNDS (3.3V output); I_{ISO} = 150 mA		50		mV
$V_{ISO(LINE)}$	V_{ISO} DC line regulation	SEL shorted to VISO (5.0 V output); I_{ISO} = 50 mA, VINP = 4.5 V to 5.5 V		1%		
		SEL shorted to GNDS (3.3 V output); I_{ISO} = 75 mA, VINP = 4.5 V to 5.5 V		1%		
$V_{ISO(LOAD)}$	V_{ISO} DC load regulation	SEL shorted to VISO (5.0 V output); I_{ISO} = 0 to 100 mA		1.5%		
	V_{ISO} DC load regulation	SEL shorted to GNDS (3.3 V output); I_{ISO} = 0 to 150 mA		1.5%		
EFF_{pk}	Peak Efficiency (1)	SEL 100kΩ to VISO (5.4V output)		60%		
		SEL shorted to VISO (5.0 V output)		60%		
		SEL 100kΩ to GNDS (3.7V output)		53%		
		SEL shorted to GNDS (3.3V output)		50%		
t_{RISE}	VISO rise time, 10% - 90%	EN = change from LO to HI, SEL shorted to VISO (5.0V output); I_{ISO} = 1 mA		750		µs
		EN = change from LO to HI, SEL 100kΩ to GNDS (3.3V output); I_{ISO} = 1 mA		300		µs
THERMAL SHUTDOWN						
TSD_{THR}	Thermal shutdown threshold	Junction Temperature, Rising		165		ºC
TSD_{HYST}	Thermal shutdown hysteresis	Junction Temperature, Falling		27		ºC

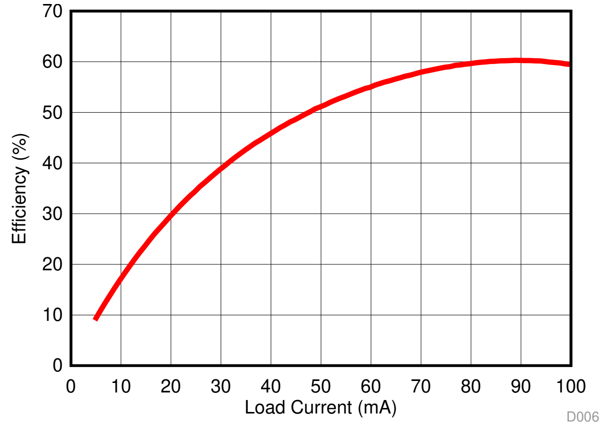
(1) Efficiency calculation: EFF = (V_{ISO} x I_{ISO}) / (V_{INP} x I_{INP})

6.9 Switching Characteristics

Over operating temperature range (T_J = –40°C to 150°C), V_{INP} = 4.5V to 5.5V, C_{INP} = C_{OUT} = 10 µF, SEL connected to V_{ISO}, unless otherwise noted. All typical values at T_J = 25°C and V_{INP} = 5.0V.

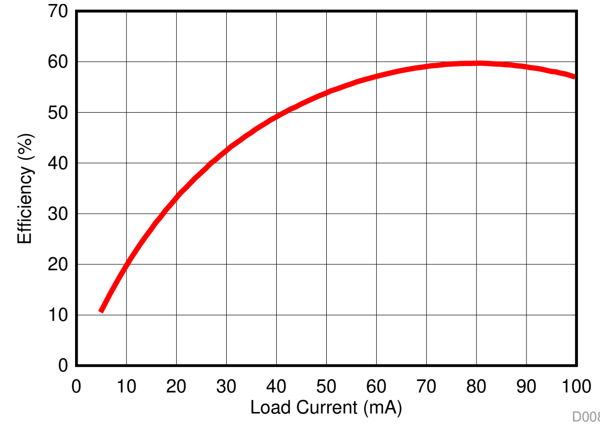
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYNC}	DC-DC Converter Clock	Internal clock mode	7.2	8	8.8	MHz
CMTI	Static common-mode transient immunity	Slew Rate of GNDP versus GNDS, V_{CM} = 1000 V		100		V/ns

6.10 Typical Characteristics



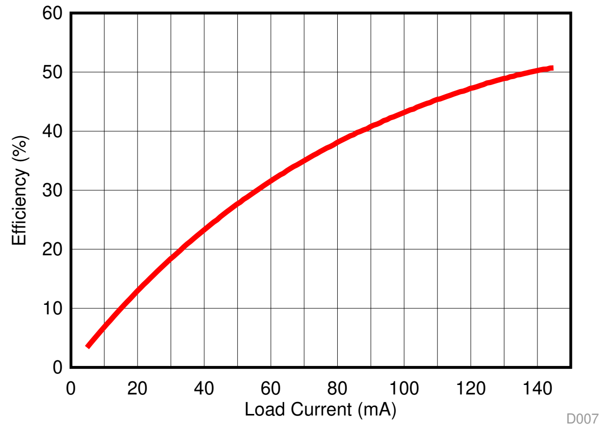
V_{INP} = 5.0 V V_{ISO} = 5.0 V T_A = 25ºC

Figure 1. Power Supply Efficiency vs Load Current (I_{ISO})



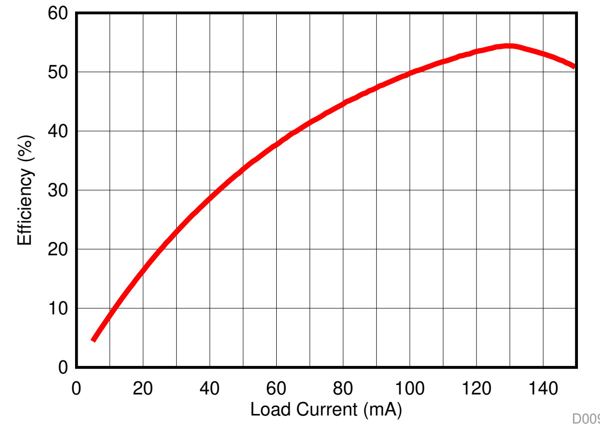
V_{INP} = 5.0 V V_{ISO} = 5.4 V T_A = 25ºC

Figure 2. Power Supply Efficiency vs Load Current (I_{ISO})



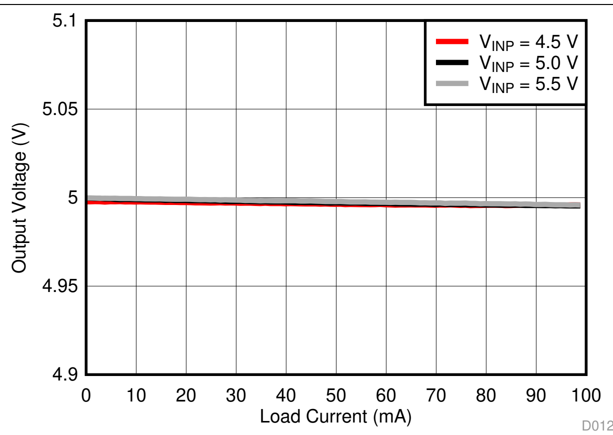
V_{INP} = 5.0 V V_{ISO} = 3.3 V T_A = 25ºC

Figure 3. Power Supply Efficiency vs Load Current (I_{ISO})



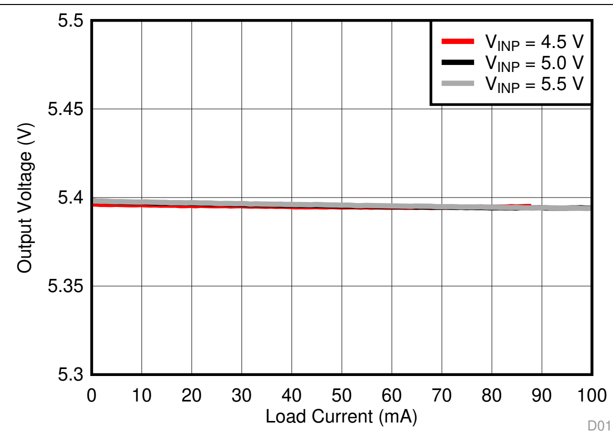
V_{INP} = 5.0 V V_{ISO} = 3.7 V T_A = 25ºC

Figure 4. Power Supply Efficiency vs Load Current (I_{ISO})



V_{ISO} = 5.0 V T_A = 25ºC

Figure 5. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})



V_{ISO} = 5.4 V T_A = 25ºC

Figure 6. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})

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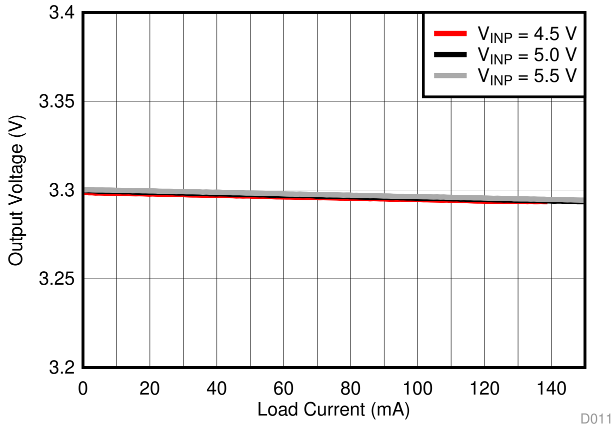
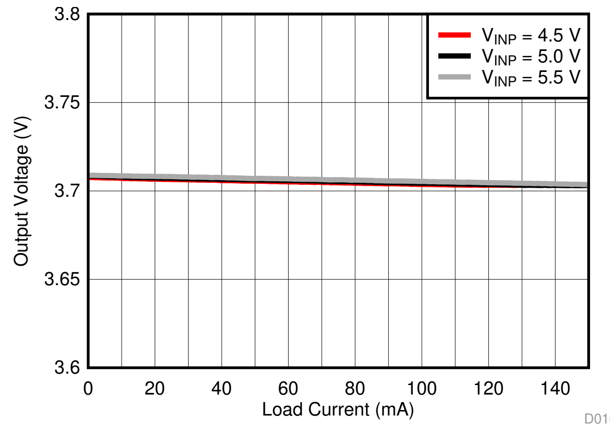
Typical Characteristics (continued)



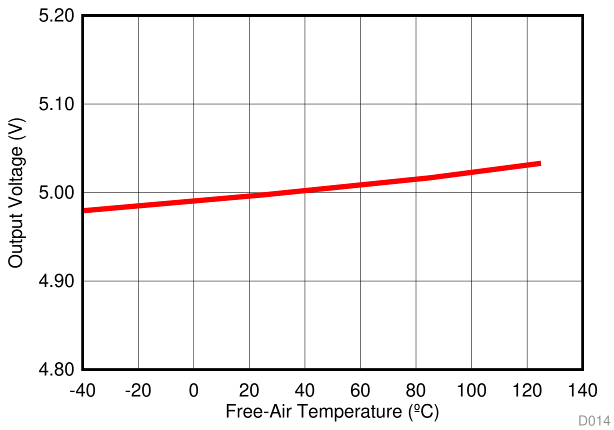
V_{ISO} = 3.3 V T_A = 25ºC

Figure 7. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})



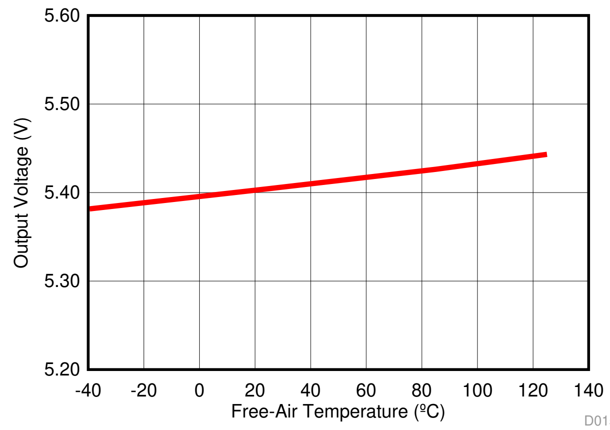
V_{ISO} = 3.7 V T_A = 25ºC

Figure 8. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})



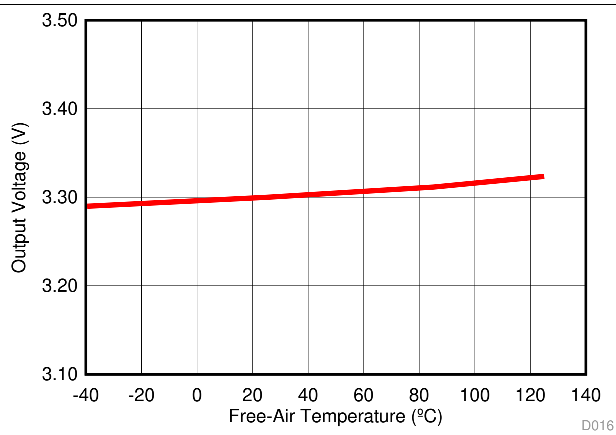
V_{INP} = 5.0 V V_{ISO} = 5.0 V I_{ISO} = 50 mA

Figure 9. Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature



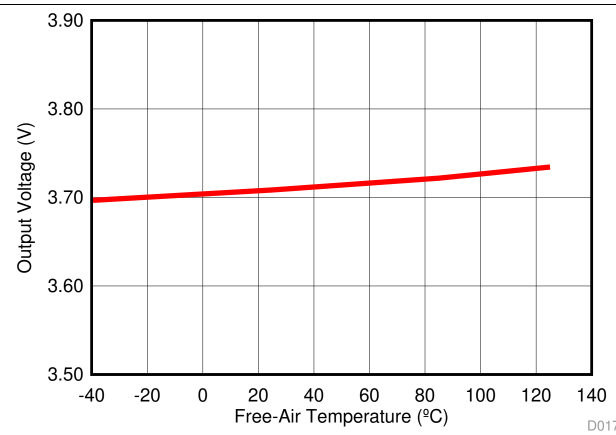
V_{INP} = 5.0 V V_{ISO} = 5.4 V I_{ISO} = 50 mA

Figure 10. Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature



V_{INP} = 5.0 V V_{ISO} = 3.3 V I_{ISO} = 75 mA

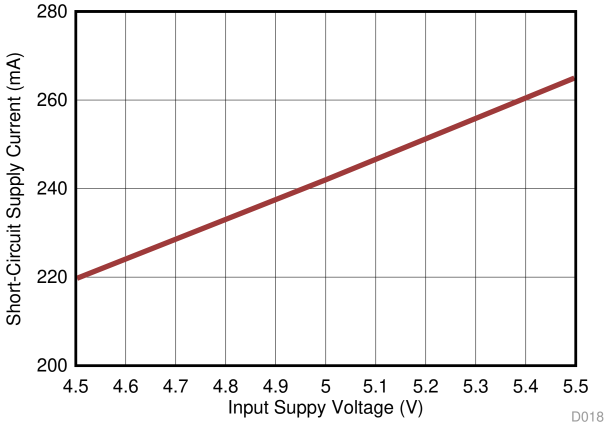
Figure 11. Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature



V_{INP} = 5.0 V V_{ISO} = 3.7 V I_{ISO} = 75 mA

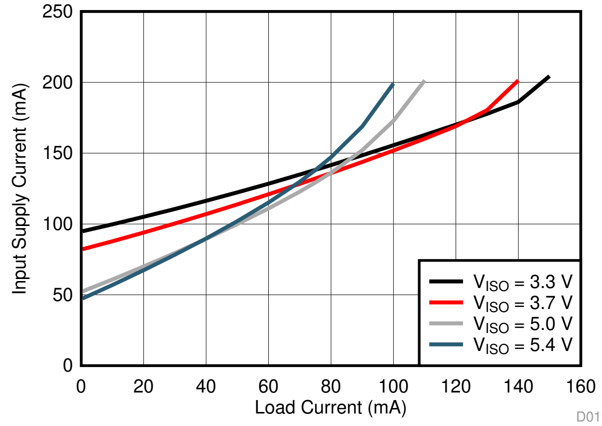
Figure 12. Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature

Typical Characteristics (continued)



T_A = 25ºC

Figure 13. Short-Circuit Supply Current (I_{VIN_SC}) vs Supply Voltage (V_{INP})



V_{INP} = 5.0 V T_A = 25ºC

Figure 14. Input Supply Current (I_{VINP}) vs Load Current (I_{ISO})

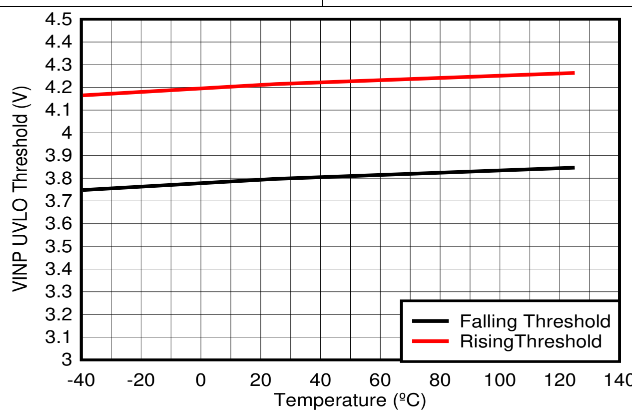


Figure 15. Typical V_{INP} UVLO Threshold vs Junction Temperature (T_J)

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The UCC12050 device integrates a high-efficiency, low-emissions isolated DC-DC converter. This approach provides typically 500 mW of clean, steady power across a 5000 V_{RMS} reinforced isolation barrier.

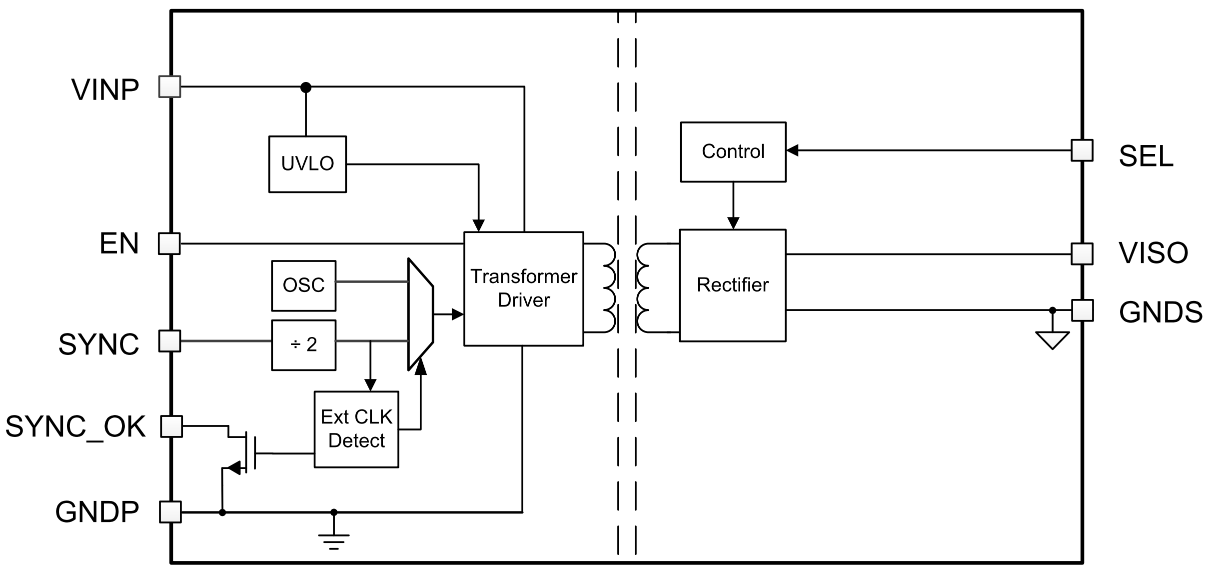
The integrated DC-DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The VINP supply is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side, rectified, and regulated to a level set by the SEL pin condition.

A fast feedback control loop monitors VISO and the output load, and ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the VINP supply, which ensures robust system performance under noisy conditions.

UCC12050 is suitable for applications that have limited board space and require more integration. These devices are also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Disable

Forcing EN low will disable the device, which greatly reduces the VINP power consumption. Pull high to enable normal device functionality. The EN pin has weak internal pull-down resistor, so the device will float to the disable state if the pin is left open.

Feature Description (continued)

7.3.2 UVLO, Power-Up, and Power-Down Behavior

The UCC1250 has an undervoltage lockout (UVLO) on the VINP power supply. Upon power-up, while the VINP voltage is below the threshold voltage V_{UVPR}, the primary side transformer driver is disabled, and VISO output is off. The output powers up once the threshold is met. Likewise, if VINP falls below V_{UVPF}, the converter will be disabled and there will be no output at VISO. Both UVLO threshold voltages have hysteresis to avoid chattering.

7.3.3 Thermal Shutdown

Thermal protection is also integrated to help prevent the device from getting damaged during overload and shortcircuit conditions on the isolated output. Under these conditions, the device temperature starts to increase. When the temperature goes above the threshold TSD_{THR}(typical 165ºC), thermal shutdown activates and the primary controller turns off which removes the energy supplied to the VISO load, which causes the device to cool off. When the junction temperature drops approximately 27ºC (TSD_{HYST})from the shutdown point, the device starts to function normally. If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care should be taken in the design to prevent the device junction temperatures from reaching such high values.

7.3.4 External Clocking and Synchronization

The UCC12050 has an internal oscillator trimmed to drive the transformer at 8.0 MHz. An external clock may be applied at the SYNC pin to override the internal oscillator. This external clock will be divided by 2, so the target range for the external clock signal at SYNC is 16 MHz ±10%. The SYNC_OK pin is asserted LOW if an no external SYNC clock or one that is outside of the operating range of the UCC12050 is detected. In this state, the external clock is ignored and the DC-DC converter is clocked by the device's internal oscillator. The pin is in high-impedance if a good clock is applied on SYNC.

When more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC/DC converters. The UCC12050 overcomes this interference by allowing devices to synchronize to one another. Synchronize multiple devices by connecting the SYNC pins of each device, taking care to minimize the capacitance of tracking. Stray capacitance (greater than 3 pF) may affect the switching frequency.

7.3.5 V_{ISO} Output Voltage Selection

The SEL pin is monitored during power-up — within the first 1 ms after applying VINP above the UVLO rising threshold or enabling via the EN pin — to detect the desired regulation voltage for the VISO output. Note that after this initial monitoring, the SEL pin no longer affects the VISO output level. In order to change the output mode selection, either the EN pin must be toggled or the VINP power supply must be cycled off and back on. Section Table 1 provides more details on the SEL pin functionality.

7.3.6 Electromagnetic Compatibility (EMC) Considerations

UCC12050 devices use emissions reduction schemes for the internal oscillator and advanced internal layout scheme to minimize radiated emissions at the system level.

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the UCC12050 incorporates many chip-level design improvements for overall system robustness.

7.4 Device Functional Modes

Table 1. Device Functional Modes

EN	SEL	Isolated Supply Output Voltage (V_{ISO}) Setpoint
HIGH	Shorted to VISO	5.0 V
HIGH	100 kΩ to VISO	5.4 V
HIGH	Shorted to GNDS	3.3 V
HIGH	100 kΩ to GNDS	3.7 V
HIGH	OPEN (1)	UNSUPPORTED
LOW	X	0 V

(1) The SEL pin has an internal weak pull-down resistance to ground, but leaving this pin open is not recommended.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC12050 device is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

8.2 Typical Application

Figure 16 shows the typical application schematic for the UCC12050 device supplying an isolated load.

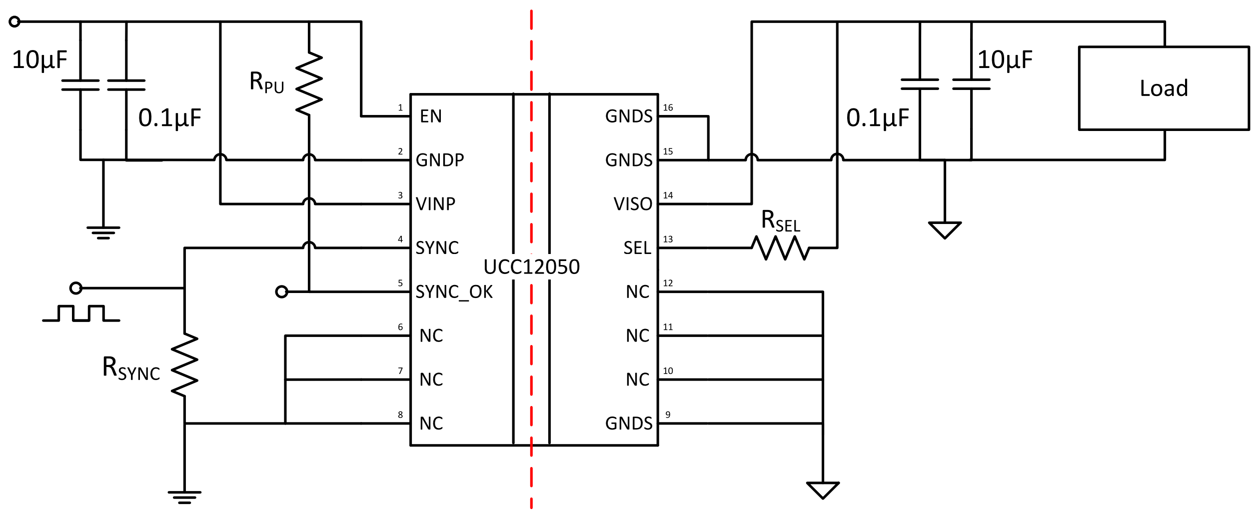


Figure 16. Typical Application Diagram

ADVANCE INFORMATION

Typical Application (continued)

8.2.1 Design Requirements

To design using UCC12050, a few simple design considerations must be evaluated. Table 2 shows some recommended values for a typical application. See Power Supply Recommendations and Layout sections to review other key design considerations for the UCC12050.

Table 2. Design Parameters

PARAMETER	RECOMMENDED VALUE
Input supply voltage, V_{INP}	4.5 - 5.5 V
Decoupling capacitance between V_{INP} and GNDP	10 µF
Decoupling capacitance between V_{ISO} and GNDS	10 µF
Optional additional capacitance on VISO or VINP to reduce high-frequency ripple	0.1 µF
Pull-up resistor from SYNC_OK to V_{INP}, R_{PU}	100 kΩ
Pull-up resistor from SEL to V_{ISO} for 5.0V output voltage mode, R_{SEL}	0 Ω
Pull-up resistor from SEL to V_{ISO} for 5.4V output voltage mode, R_{SEL}	100 kΩ
Optional SYNC signal impedance-matching resistor, R_{SYNC}	Match source — typical values are 50 Ω, 75 Ω, 100 Ω, or 1 kΩ
External clock signal applied on SYNC	16 MHz

8.2.2 Detailed Design Procedure

Place decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitor(s) between pin 3 (VINP) and pin 2 (GNDP). For the isolated output supply, place the capacitor(s) between pin 14 (VISO) and pin 15 (GNDS). This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits. The recommended capacitor value is 10 µF. Ensure the capacitor dielectric material is compatible with the target application temperature.

ADVANCE INFORMATION

9 Power Supply Recommendations

The recommended input supply voltage (VINP) for UCC12050 is between 4.5 V and 5.5 V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Local bypass capacitors should be placed between the VINP and GNDP pins at the input, and between VISO and GNDS at the isolated output supply. Low ESR, ceramic surface mount capacitors are recommended. It is further suggested that one place two such capacitors: one with a value of 10 µF for supply bypassing, and an additional 100-nF capacitor in parallel for high frequency filtering. The input supply must have an appropriate current rating to support output load required by the end application.

10 Layout

10.1 Layout Guidelines

The UCC12050 integrated isolated power solution simplifies system design and reduces board area usage. Proper PCB layout is important in order to achieve optimum performance. Here is a list of recommendations:

1. Place decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitor(s) between pin 3 (VINP) and pin 2 (GNDP). For the isolated output supply, place the capacitor(s) between pin 14 (VISO) and pin 15 (GNDS). This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.
2. Because the device does not have a thermal pad for heat-sinking, the device dissipates heat through the respective GND pins. Ensure that enough copper — preferably a connection to the ground plane — is present on all GNDP and GNDS pins for best heat-sinking.
3. If space and layer count allow, it is also recommended to connect the VINP, GNDP, VISO and GNDS pins to internal ground or power planes through multiple vias of adequate size. Alternatively, make traces for these nets as wide as possible to minimize losses.
4. TI also recommends grounding the no-connect pins (NC) to their respective ground planes. For pins 6, 7, and 8, connect to GNDP. For pins 10, 11, and 12, connect to GNDS. This will allow more continuous ground planes and larger thermal mass for heat-sinking.
5. A minimum of four layers is recommended to accomplish a low-EMI PCB design. Inner layers can be spaced closer than outer layers and used to create a high-frequency bypass capacitor between GNDP and GNDS to reduce radiated emissions. Ensure proper spacing, both inter-layer and layer-to-layer, is implemented to avoid reducing isolation capabilities. These spacings will vary based on the printed circuit board construction parameters, such as dielectric material and thickness.
6. Pay close attention to the spacing between primary ground plane (GNDP) and secondary ground plane (GNDS) on the PCB's outer layers. The effective creepage and or clearance of the system will be reduced if the two ground planes have a lower spacing than that of the UCC12050 package.
7. To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the UCC12050 device on the outer copper layers.

10.2 Layout Example

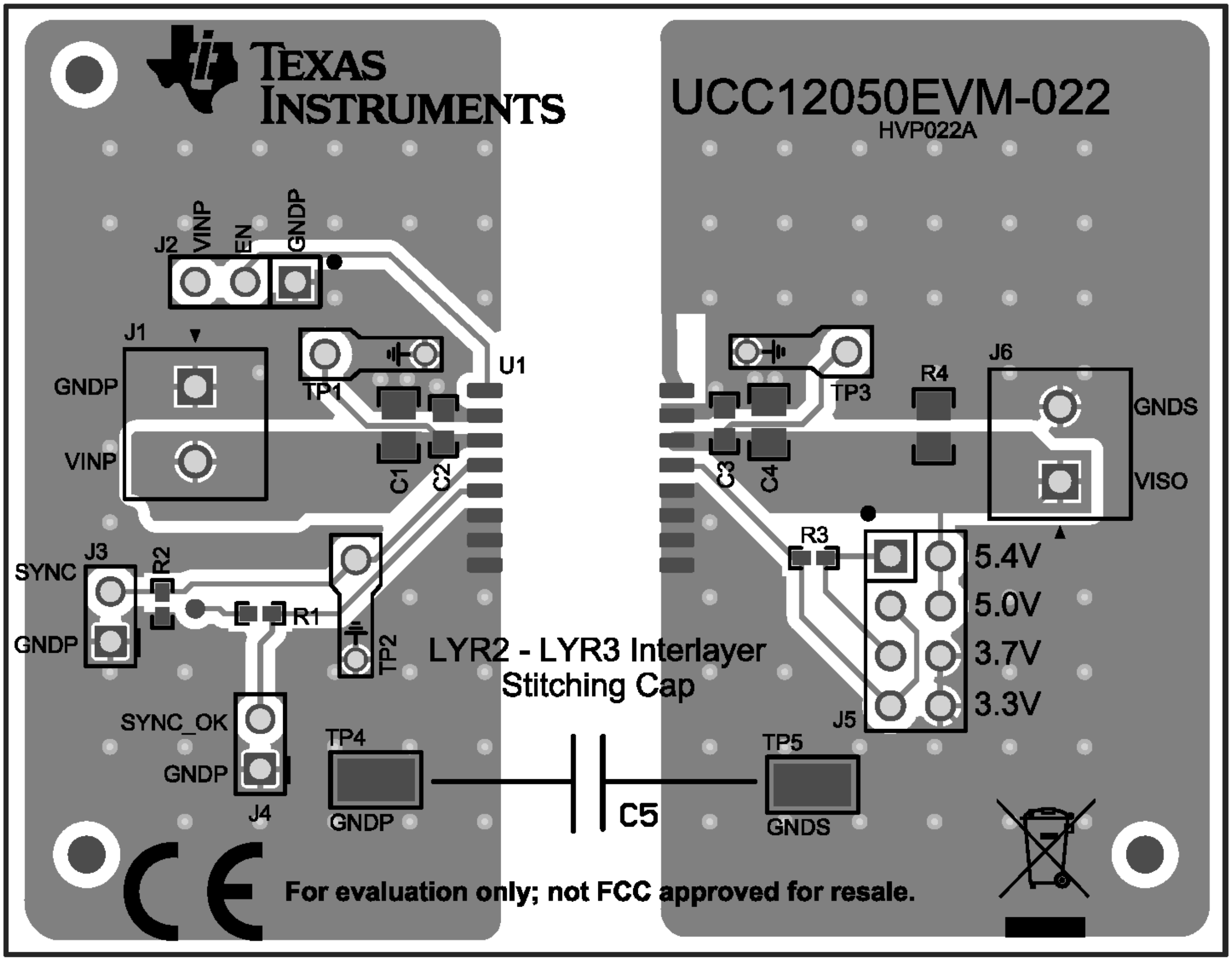


Figure 17. Layout Example

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- ***UCC12050 EVM User Guide***
- ***UCC12050 EMI Reduction Techniques Applications Note***

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical and Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

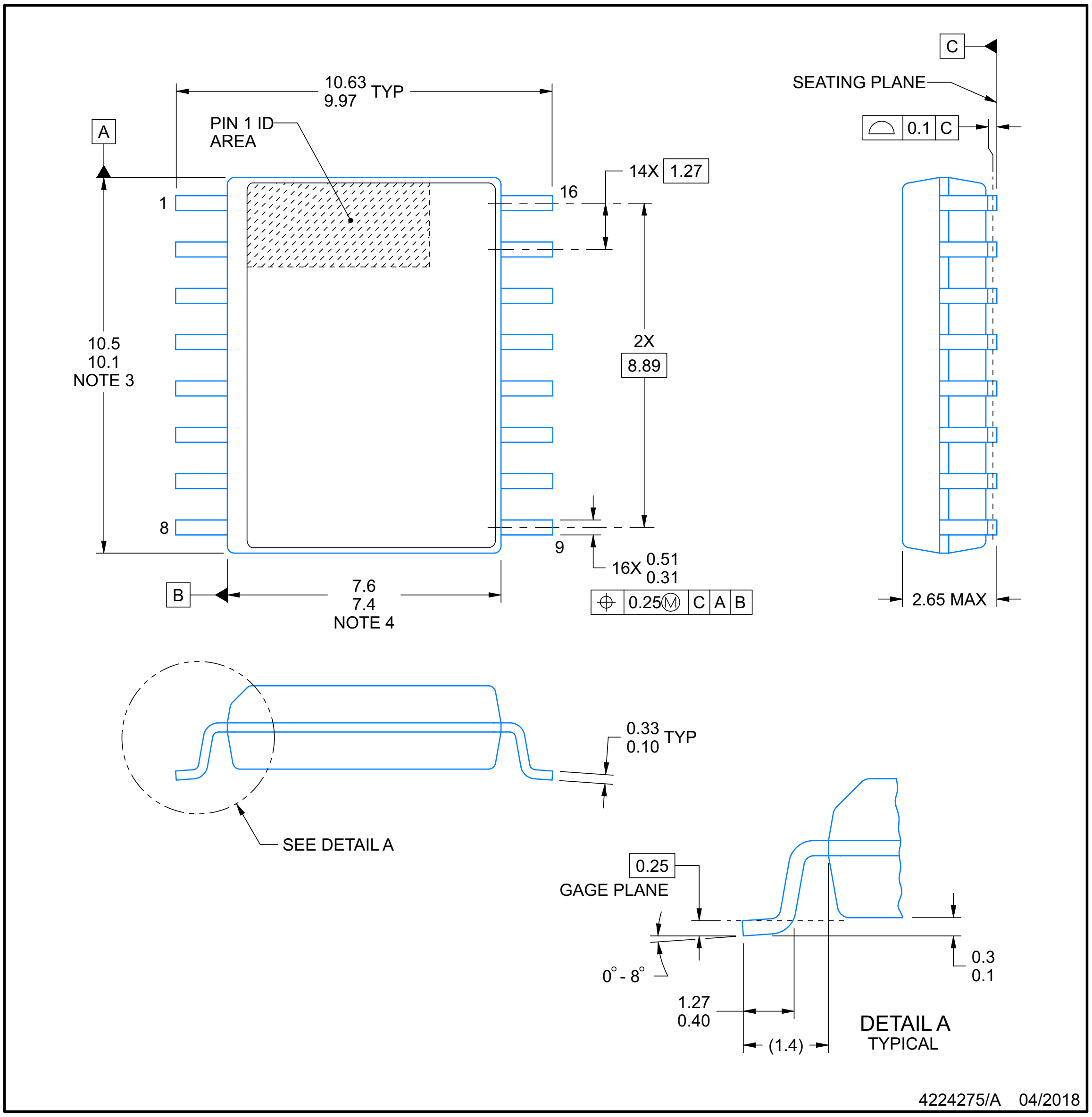
ADVANCE INFORMATION

PACKAGE OUTLINE

DVE0016A

SO-MOD - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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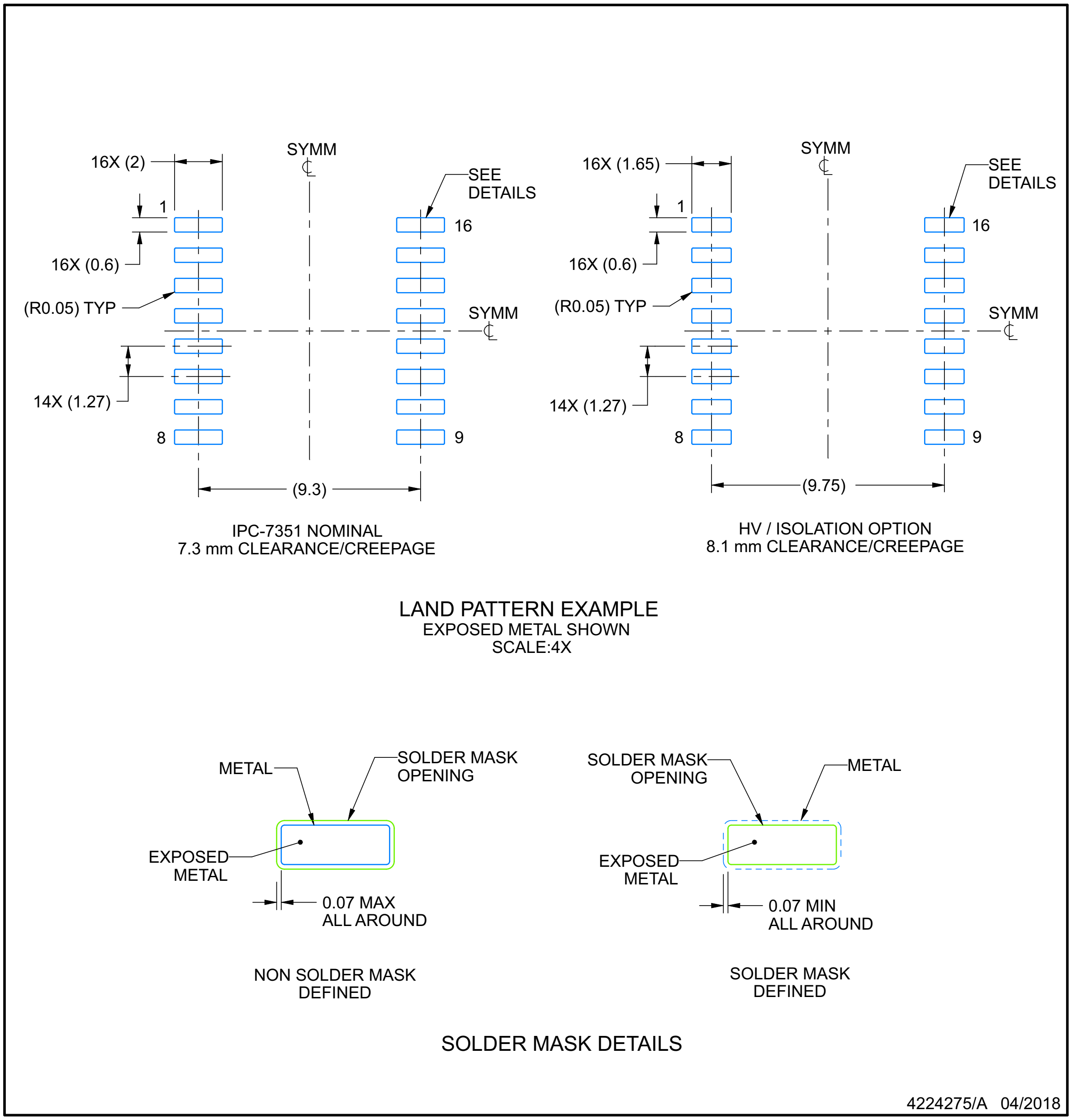
EXAMPLE BOARD LAYOUT

DVE0016A

SO-MOD - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

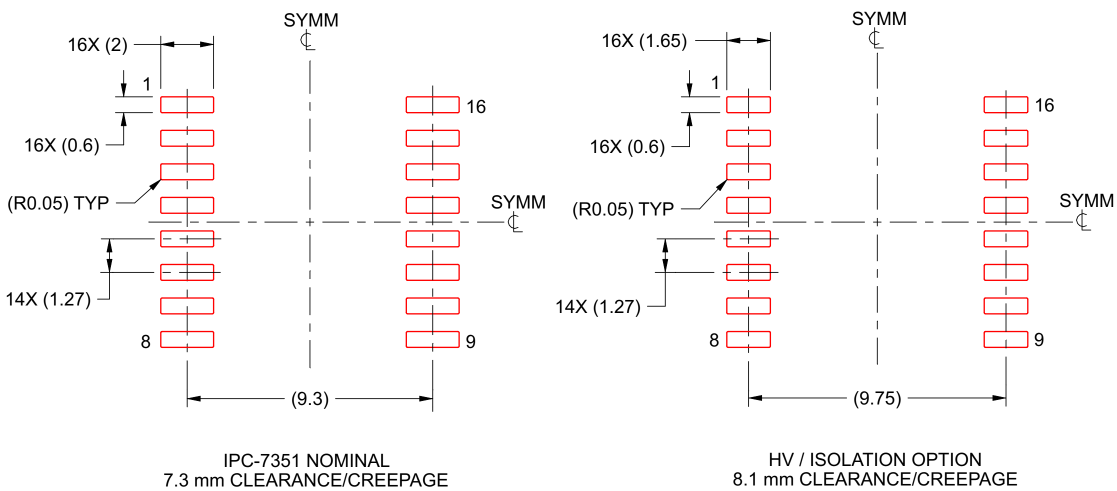
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DVE0016A

SO-MOD - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4224275/A 04/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC12050DVE	ACTIVE	SO-MOD	DVE	16	40	TBD	Call TI	Call TI	-40 to 125		Samples
UCC12050DVE	PREVIEW	SO-MOD	DVE	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC12050	
UCC12050DVER	PREVIEW	SO-MOD	DVE	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC12050	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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