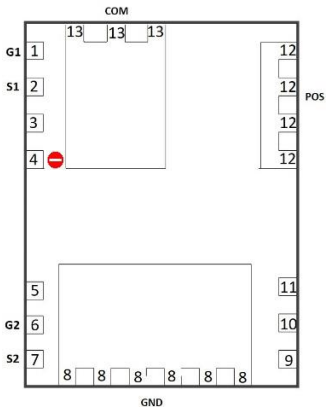
WiseGaN® platform – WI65100A2
Half bridge Power GaN IC 650 V E-mode GaN transistor
Preliminary datasheet

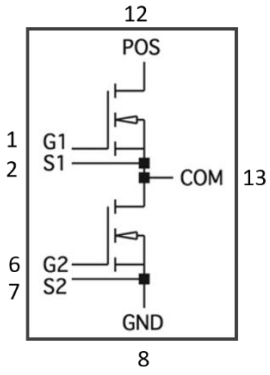
1. Features

- 650 V enhancement mode half bridge power switch
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 100 mΩ per switch
- $I_{DS(max)}$ = 10 A
- Low inductance PQFN PACKAGE
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10V)
- Very high switching frequency (> 1 MHz)
- Fast and controllable fall and rise times
- Integrated Source sense
- Reverse current capability
- Zero reverse recovery loss
- Small 6 x 8 mm² PCB footprint
- RoHS 6 compliant

PCB footprint



Symbol & Pinout



Pins 3, 4, 5, 9, 10, 11 not connected.

(Do not use Pin 4 for power)

2. Applications

- High efficiency power conversion
- High density power conversion
- AC-DC Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Small-Medium UPS
- Fast Battery Charging

Description

The WI65100A2 is an enhancement mode GaN-on silicon half bridge power circuit. The properties of GaN allow for high current, high voltage breakdown and high switching frequency.

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3. Absolute Maximum Ratings per transistor (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage - transient (note 1)	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case} = 25 °C) (note 2)	I_{DS}	10	A
Continuous Drain Current (T_{case} = 100 °C) (note 2)	I_{DS}	5	A
Pulse Drain Current (Pulse width 100 µs)	$I_{DS\ Pulse}$	20	A

(1) Pulse ≤ 1 µs

(2) Limited by saturation

4. Thermal Characteristics (Typical values)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	2	°C /W
Thermal Resistance (junction-to-ambient)	$R_{\Theta JA}$	45	°C /W

5. ESD Ratings

Parameter	Symbol	Max	Units
Human Body Model (JS-001-2014)	HBM	1 000	V
Charged Device Model (JS-002-2014)	CDM	1 000	V

6. Electrical Characteristics (Typical values at TJ = 25 °C, VGS = 6 V unless otherwise noted per transistor)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	650			V	V_{GS} = 0 V I_{DSS} = 1 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		100	110	mΩ	V_{GS} = 6 V, T_J = 25°C I_{DS} = 2 A
Drain-to-Source On Resistance	$R_{DS(on)}$		150		mΩ	V_{GS} = 6 V ,T_J = 150 °C I_{DS} = 2 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.2	1.4	1.5	V	V_{DS} = V_{GS} , Tj=25°C I_{DS} = 1 mA
Gate-to-Source Current	I_{GS}		10		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 400 V I_{DS} = 5 A
Reverse Drain-to-Source voltage	V_{rDS}		1.3		V	V_{GS}=0V,Tj=25°C I_{SD} = 1 mA
Drain-to-Source Leakage Current	I_{DSS}		0.1	5	µA	V_{DS} = 650 V V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		35	100	µA	V_{DS} = 650 V V_{GS} = 0 V T_J = 150 °C
Input Capacitance	C_{ISS}		100		pF	V_{DS} = 400 V V_{GS} = 0 V f = 100 kHz
Output Capacitance	C_{OSS}		15		pF	
Reverse Transfer Capacitance	C_{RSS}		10,5		pF	

(3) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(4) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

7. Characteristics Graphs

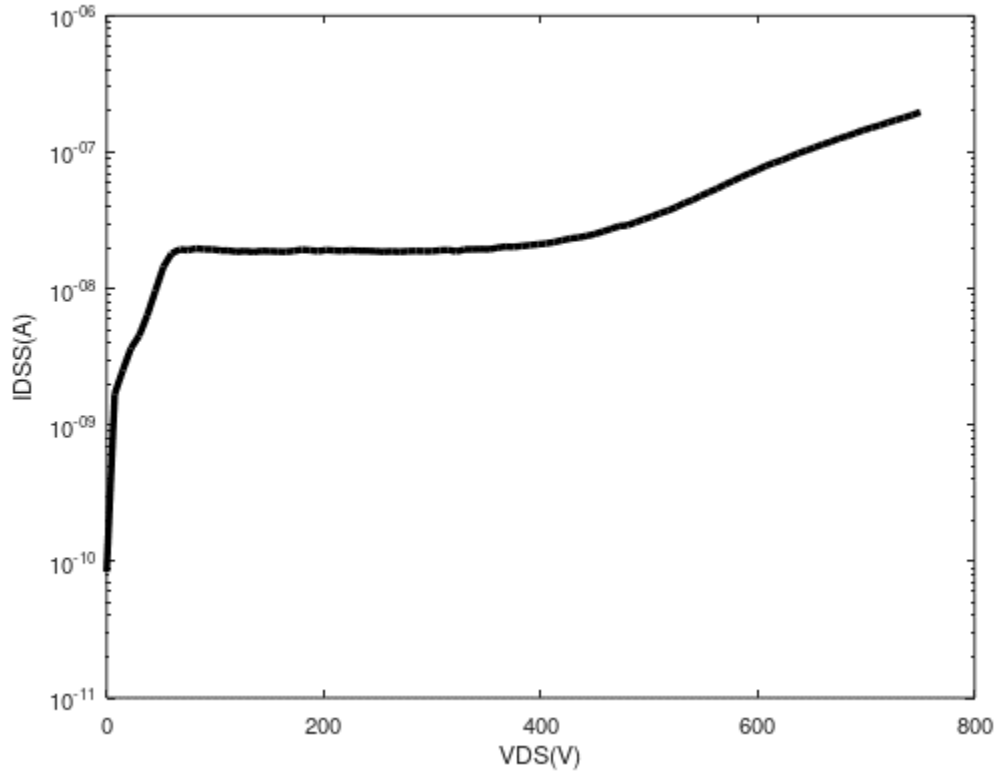


Figure 1 : Drain-to-source leakage current (I_{DSS}) vs. drain-to-source voltage (V_{DS}) @ 25°C

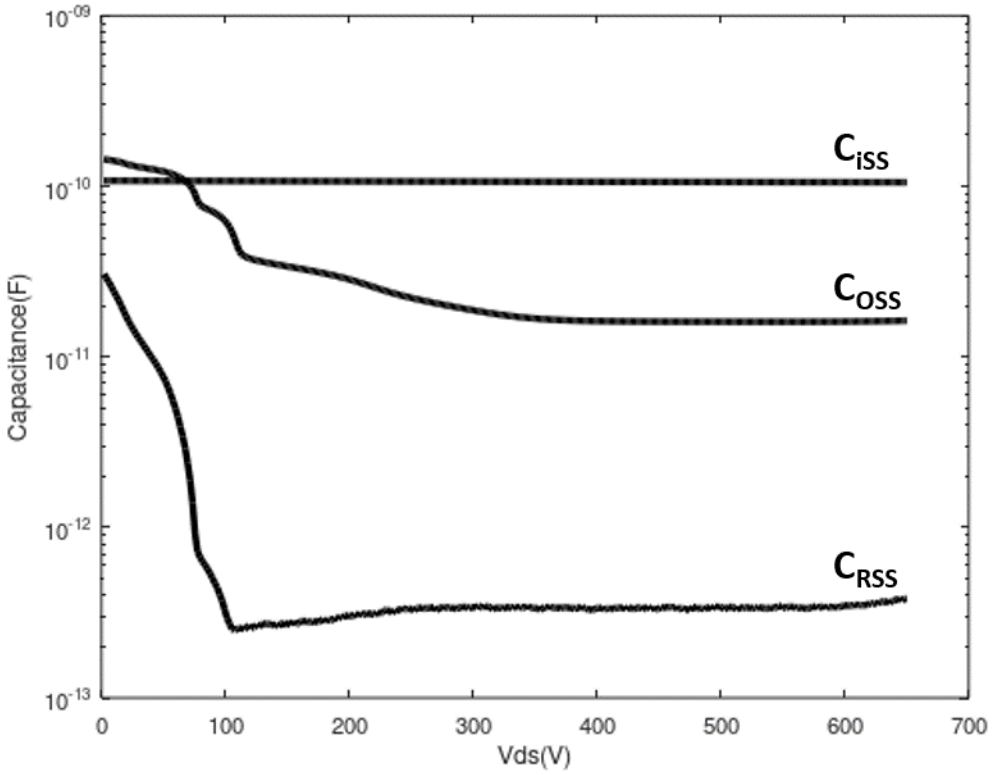


Figure 2 : Typical C_{OSS}, C_{ISS}, C_{RSS} vs V_{DS}

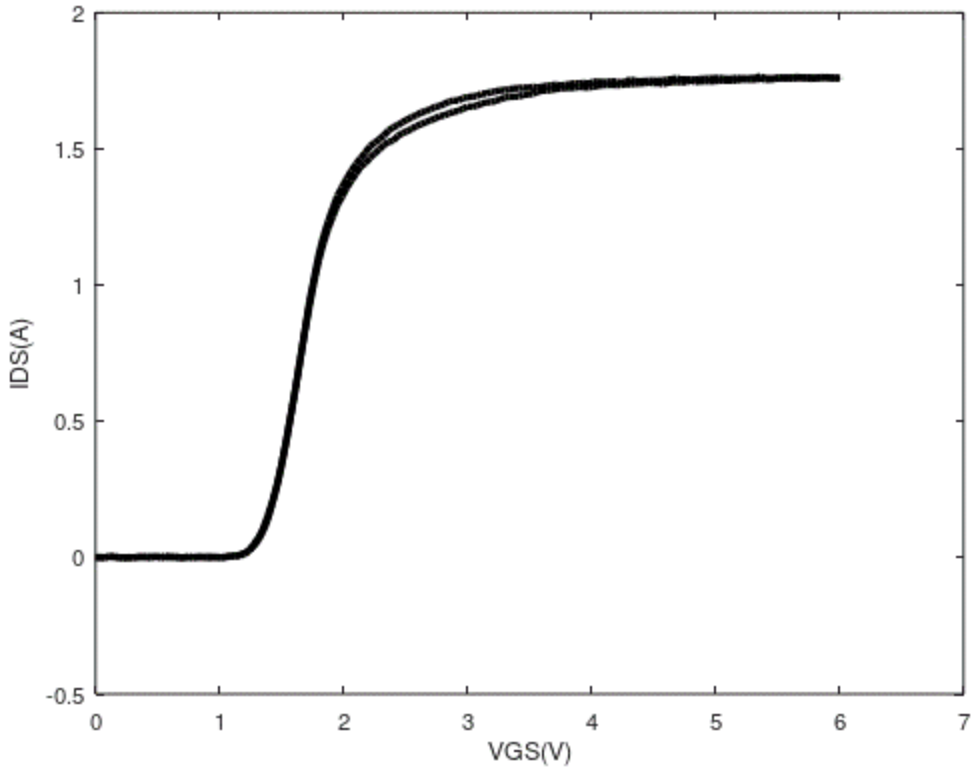


Figure 3 : Typical threshold voltage $I_{DS}=f(V_{GS})$ for V_{DS}=0,1V, T=25°C. Back & Reverse measurement to check V_T shift.

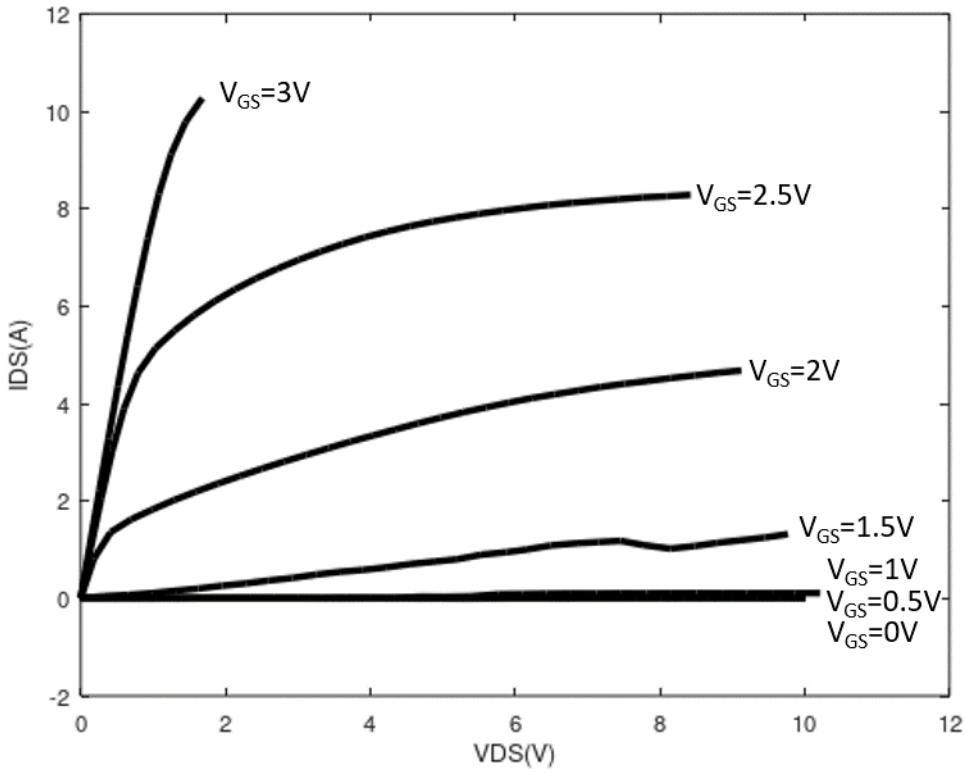
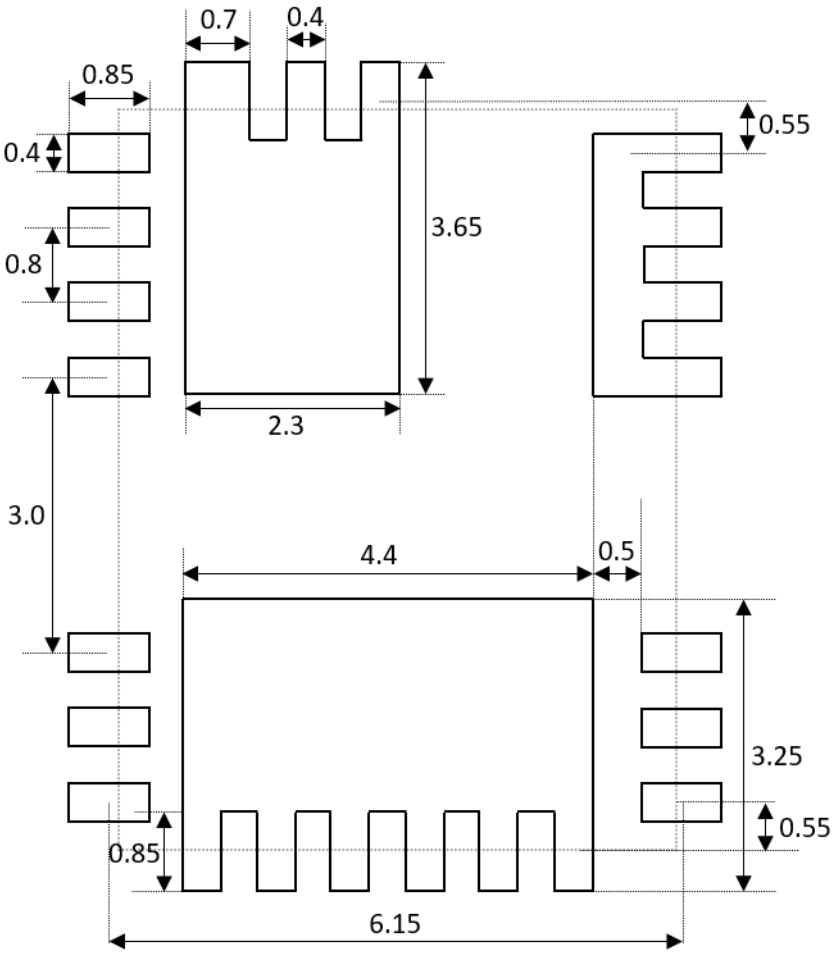


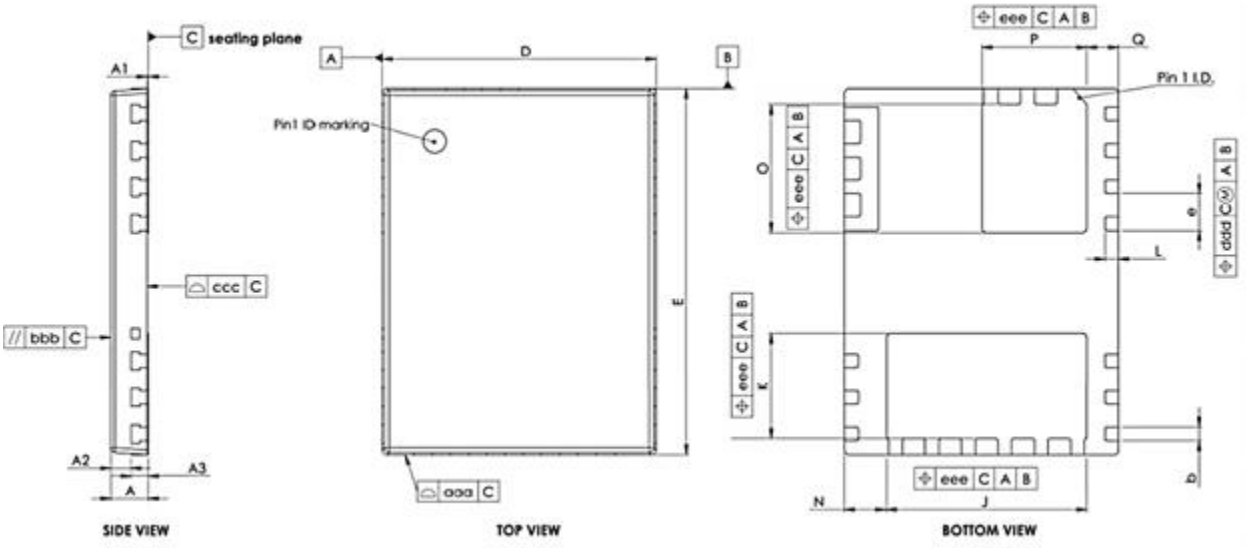
Figure 4 : Typical $I_{DS}=f(V_{DS}, V_{GS})$ curve. $R_{ON}=100\ m\Omega$

8. Recommended PCB Footprint



All dimensions are in mm

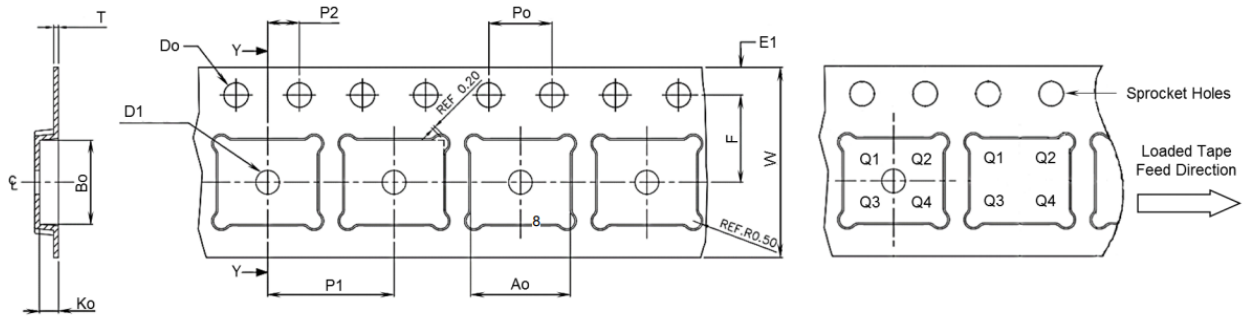
9. PQFN Package Outline



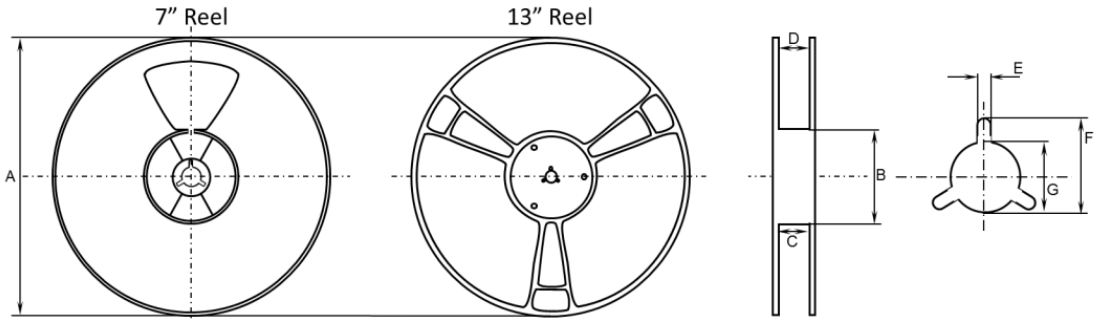
All dimensions are in mm

	Symbol	Min	Nom	Max		Symbol	Min	Nom	Max
Total Thickness	A	1.18	1.2	1.2	Lower EP Size	J	4.4	4.4	4.4
Stand off	A1	0.03	0.03	0.03		K	2.3	2.3	2.3
Mold thickness	A2	0.8	0.82	0.82	Lead length	L	0.3	0.3	0.3
L/F thickness	A3	0.381			Merged lead length	M			
Lead width	B	0.3			Package edge tolerance	aaa	0.1		
BODY Size	D	5.98	6	6.01	Mold Flatness	bbb	0.1		
	E	7.98	8	8.01	Coplanarity	ccc	0.08		
Lead pitch	e	0.8			Lead offset	ddd	0.1		
Upper EP Size	O	2.8	2.8	2.8	Exposed pad offset	eee	0.1		
	P	2.3	2.3	2.3	Lower EP left shift	N	0.9	0.9	0.9
					Upper EP right shift	Q	0.7	0.7	0.7

10. Tape and Reel Dimensions



Ao (mm)	Bo (mm)	Do (mm)	D1 (mm)	E1 (mm)	F (mm)	Ko (mm)	Po (mm)	P1 (mm)	P2 (mm)	T (mm)	W (mm)	Pin1 Quadrant
8.30 ± 0.1	6.30 ± 0.1	ϕ1.55 ± 0.05	min. ϕ1.50	1.75 ± 0.1	6.00 ± 0.1	1.20 ± 0.1	6.0 ± 0.1	10.00 ± 0.1	3.0 ± 0.1	0.30 ± 0.05	13.00 ± 0.1	Q1



	A (mm)	B (mm)	C (mm)	D (mm)	E (mm)	F (mm)	G (mm)
7" Reel	ϕ180.0 ± 1.5	ϕ62.0	12.4 +2.0 -0.0	Max. 18.4	2.3 ± 0.2	17.3 ± 0.2	ϕ13.0 +0.5 -0.2
13" Reel	ϕ330.0 ± 1.5	ϕ100.0 ± 1.5	12.4 +2.0 -0.0	Max. 18.4	2.2 ± 0.2	17.2 ± 0.2	ϕ13.0 +0.5 -0.2

11. Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
WI650100A2	6 x 8 mm PQFN	Tape-and-Reel	1000 5000	7" Reel 13" Reel	13mm