# Components choice:

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| --- | --- | --- | --- |
| **Capa decouplage** | **700V 10uF** | [C4AF7BW5100A3OK](https://www.mouser.be/ProductDetail/KEMET/C4AF7BW5100A3OK?qs=sGAEpiMZZMukHu%252BjC5l7YbZJogKwR3uATJUtAir2kIE%3D) | [C4AF7BW5100A3OK](https://www.mouser.be/ProductDetail/KEMET/C4AF7BW5100A3OK?qs=sGAEpiMZZMukHu%252BjC5l7YbZJogKwR3uATJUtAir2kIE%3D) |
| **LDO5V** |  |  |  |
| **ISO7821**  **DCDC & iso** | **Vussply max = 5.5V**  **Load current>130mA** |  |  |
| **Driver** | **Recom op.:**  **4-12V**  7.6-A/1.3-A Peak Sink and Source Drive Current |  | **Mouser:**  926-LM5114BMF/NOPB |
| **GAN66508B (switch)** | **Abs rating**  **VGS =+7V**  **VDS 650V**  **Recommended :**  **VGS 5-6V** |  | **En stock chez mouser: ref :** 499-GS66508B-E01-MR |
| **CAPAS decouplage**  **C5 – C10** | **C1218**  **1000V 10uF X7R** | C1812C104KDRACTU / C1812V104KDRACTU | 80-C1812C104KDRACTU |
| **Annexe:**  Driver lvds |  |  | 595-SN65LVDS31MDREP |
| **555**  **Generate double pulse** |  |  |  |

**12 Layout**

**12.1 Layout Guidelines**

A minimum of four layers is required to accomplish a low-EMI PCB design (see Figure 35). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.

* Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
* Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
* Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of

2 approximately 100 pF/in .

* Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
* Keep decoupling capacitors as close as possible to the VCC and VISO pins.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Because the device has no thermal pad to dissipate heat, the device dissipates heat through the respective GND pins. Ensure that enough copper is present on both GND pins to prevent the internal junction temperature of the device from rising to unacceptable levels.

The ISOW7821 integrated signal and power isolation device simplifies system design and reduces board area. The use of low-inductance micro-transformers in the ISOW7821 device necessitates the use of high frequency switching, resulting in higher radiated emissions compared to discrete solutions. The ISOW7821 device uses on- chip circuit techniques to reduce emissions compared to competing solutions. For further reduction in radiated emissions at system level, refer to the *Low-Emission Designs With ISOW7841 Integrated Signal and Power Isolator* application report.

**12.1.1 PCB Material**

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

**Layout Example**

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