

## ASR6601

# RFSW User Guide

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## About This Document

This document introduces the differences in hardware and software between single-pin and complementary-pin controlled RF switches (RFSW), helping customers design RF switches for the ASR6601 LPWAN SoC chip.

## Intended Readers

This document is mainly for engineers who use this chip to develop their own platform and products, for instance:

- PCB Hardware Development Engineer
- Software Engineer
- Technical Support Engineer

## Included Chip Models

The product models corresponding to this document are as follows.

| Model | Flash | SRAM | Core | Package | Frequency |
|---|---|---|---|---|---|
| ASR6601SE | 256 KB | 64 KB | 32-bit 48 MHz Arm China STAR-MC1 | QFN68, 8*8 mm | 150 ~ 960 MHz |
| ASR6601CB | 128 KB | 16 KB | 32-bit 48 MHz Arm China STAR-MC1 | QFN48, 6*6 mm | 150 ~ 960 MHz |
| ASR6601SER | 256 KB | 64 KB | 32-bit 48 MHz Arm China STAR-MC1 | QFN68, 8*8 mm | 150 ~ 960 MHz |
| ASR6601CBR | 128 KB | 16 KB | 32-bit 48 MHz Arm China STAR-MC1 | QFN48, 6*6 mm | 150 ~ 960 MHz |



## Copyright Notice

## Electrostatic Discharge (ESD) Warning

This product can be damaged by Electrostatic Discharge (ESD). When handling with this device, the people should be very careful to conduct the ESD protection to avoid any device damage caused by ESD event.

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## ASR Microelectronics Co., Ltd.

**Address**: 9F, Building 10, No. 399 Keyuan Road, Zhangjiang High-tech Park, Pudong New Area, Shanghai, 201203, China

**Homepage**: http://www.asrmicro.com/


## Revision History

| Date | Version | Release Notes |
|---|---|---|
| 2023.07 | V1.0.0 | First Release. |

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# 1. Overview

Both ASR650X and ASR6601 chips are based on SX1262, switching between TX and RX via RFSW. RFSW is divided into three categories depending on the control signals: the single-pin controlled switch, the complementary-pin controlled switch, and the single- and complementary-pin controlled switch. The first two categories are common, while the single- and complementary-pin controlled RFSW is less common. Generally, the SX1262's internal state machine automatically generates an interrupt signal DIO2 as the control signal for TX and RX switching, which makes the hardware circuit and software design the easiest if with a single-pin controlled RFSW. However, in practice, the complementary-pin controlled RFSW may be used, and the corresponding hardware circuit and software are significantly different from those of the single-pin controlled RFSW. Below are the differences in hardware and software between single-pin and complementary-pin controlled RFSWs.

## 1.1 Single-pin Controlled RFSWs

The following are the single-pin controlled RFSWs commonly used in LPWAN:

**Table 1-1 Commonly Used Single-pin Controlled RFSWs in LPWAN**

| Company | Part Number | Control Mode | Description | Truth Table | Power Supply |
|---|---|---|---|---|---|
| muRata | XMSSJR6G0BA-093 | Single-Pin Control | SOI CMOS SPDT Switch for 0.01~6.0 GHz | Single-Pin Control Logic:<br>CTL RF1 RF2<br>Low ON OFF<br>High OFF ON | 1.7~5.0V<br>3.0V TVP |
| Maxscend | MXD8625C | Single-Pin Control | SOI CMOS SPDT Switch for 0.1~3.0 GHz | Single-Pin Control Logic:<br>CTL RF1 RF2<br>Low ON OFF<br>High OFF ON | 2.5~3.0V<br>2.8V TVP |
| CanaanTek | CAN1630RW | Single-Pin Control | SOI CMOS SPDT Switch for 0.1~2.7 GHz | Single-Pin Control Logic:<br>CTL RF1 RF2<br>Low ON OFF<br>High OFF ON | 2.5~5.0V<br>2.85V TYP |
| Will | WS7802DE | Single-Pin Control | SOI CMOS SPDT up to 3 GHz | Single-Pin Control Logic:<br>CTL RF1 RF2<br>Low ON OFF<br>High OFF ON | 2.5~5.0V<br>2.8V TYP |
| RDA | RDASW293C | Single-Pin Control | SOI CMOS SPDT up to 6 GHz | Single-Pin Control Logic:<br>CTL RF1 RF2<br>Low ON OFF<br>High OFF ON | 2.4~4.2V<br>2.85V TYP |

Take muRata's XMSSJR6G0BA-093 as an example:


**Figure 1-1 XMSSJR6G0BA Diagram**

| Single-Pin Control Logic Truth | | | |
|---|---|---|---|
| VDD | CTL | RFC-RF1 | RFC-RF2 |
| VDD | LOW | ON | OFF |
| VDD | HIGH | OFF | ON |

**Table 1-2 XMSSJR6G0BA Truth Table**

**Note:**

1. *The pin order of RF1 (Port1) and RF2 (Port2) is different for different single-pin controlled RFSWs.*
2. *The packages of different RFSWs are different, which should be noted when replacing different RFSWs.*

## 1.2 Complementary-pin Controlled RFSWs

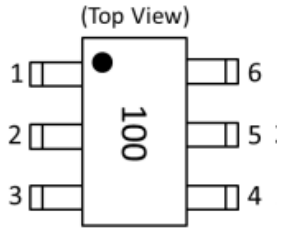
The following are the complementary-pin controlled RFSWs commonly used in LPWAN:

**Table 1-3 Commonly Used Complementary-pin Controlled RFSWs in LPWAN**

| Company | Part Number | Control Mode | Description | Truth Table | Power Supply |
|---|---|---|---|---|---|
| HexaWave | HWS408 | Complementary-Pin Control | This switch can be used in many wireless digital communication systems like IEEE 802.11b/g WLAN and Bluetooth for transmit/receive selection or antenna diversity function. | VC1 VC2 RFC-RF1 RFC-RF2<br>Low High ON OFF<br>High Low OFF ON | 1.8~6.0 V<br>3.0 V TYP |
| GSR | GSR1303S<br>GSR1370C | Complementary-Pin Control | a pHEMT GaAs SPDT operate frequency from DC to 3.0 GHz, application: Wireless LAN (IEEE 802.11b/g) & Bluetooth | VC1 VC2 RFC-RF1 RFC-RF2<br>Low High ON OFF<br>High Low OFF ON | 1.8~5.0 V<br>3.0 V TYP |
| CDK | CKRF2214MM66 | Complementary-Pin Control | a pHEMT GaAs SPDT operate frequency from 0.05 to 3.0 GHz, application: Wireless LAN (IEEE 802.11b/g) & Bluetooth | VC1 VC2 RFC-RF1 RFC-RF2<br>Low High ON OFF<br>High Low OFF ON | 1.8~5.0 V<br>3.0 V TYP |
| CDK | CKRF2179MM26 | Complementary-Pin Control | a pHEMT GaAs SPDT operate frequency from 0.05 to 3.0 GHz, application: Wireless LAN (IEEE 802.11b/g) & Bluetooth | VC1 VC2 RFC-RF1 RFC-RF2<br>Low High ON OFF<br>High Low OFF ON | 1.8~5.0 V<br>3.0 V TYP |
| NJRC | NJG1801K75 (TE1) | Complementary-Pin Control | a SPDT switch IC suited for switching transmit/receive signals at 802.11a/b/g/n/ac applications. | ON PATH VCTL1 VCTL2<br>PC-P1 L H<br>PC-P2 H L | 2.0~3.3 V<br>2.8 V TYP |
| CEL | UPG2214TK | Complementary-Pin Control | NEC's ½W LOW VOLTAGE L, S-BAND SPDT SWITCH<br>● L, S-band digital cellular and cordless telephones<br>● Bluetooth TM, W-LAN and WLL | Vcont1 Vcont2 IN-OUT1 IN-OUT2<br>Low High ON OFF<br>High Low OFF ON | 1.8~5.3 V<br>1.8 V, 3.0 V TYP |

| | | | | | |
|---|---|---|---|---|---|
| | | | ● Short Range Wireless | | |

Take CKRF2179MM26 as an example:




| Pin No. | Pin Name |
|---|---|
| 1 | RF1 |
| 2 | GND |
| 3 | RF2 |
| 4 | VC2 |
| 5 | RFC |
| 6 | VC1 |

**Figure 1-2 CKRF2179MM26 Diagram**

| Complementary-Pin Control Logic Truth | | | |
|---|---|---|---|
| VC1 | VC2 | RFC-RF1 | RFC-RF2 |
| LOW | HIGH | ON | OFF |
| HIGH | LOW | OFF | ON |

**Table 1-4 CKRF2179MM26 Truth Table**

## 1.3 Single and Complementary-pin Controlled RFSWs

The following are the single and complementary-pin controlled RFSWs commonly used in LPWAN:

**Table 1-5 Commonly Used Single and Complementary-pin Controlled RFSWs in LPWAN**

| Company | Part Number | Control Mode | Description | Truth Table | Power Supply |
|---|---|---|---|---|---|
| Peregine | PE4259 | Both | SPDT High Power UltraCMOS™10 MHz-3.0 GHz RF Switch | **Single-Pin Control Logic:**<br>CTRL RFC-RF1 RFC-RF2<br>High ON OFF<br>Low OFF ON<br>**Complementary-Pin Control Logic:**<br>nCTRL CTRL RFC-RF1 RFC-RF2<br>Low High ON OFF<br>High Low OFF ON | 1.8~3.3 V<br>3.0 V TVP |

For example, PE4259 can be used as both a single-pin controlled RFSW and a complementary-pin controlled RFSW, as follows:

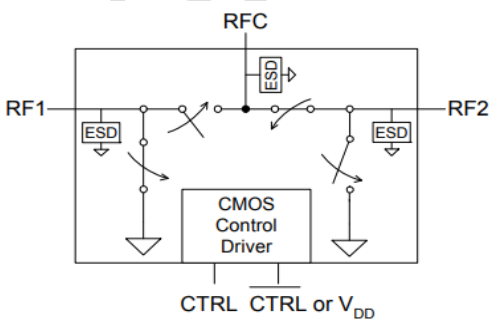



**Figure 1-3 PE4259 Functional Block Diagram**

| Single-Pin Control Logic Truth | | | |
|---|---|---|---|
| VDD | CTL | RFC-RF1 | RFC-RF2 |
| VDD | LOW | OFF | ON |
| VDD | HIGH | ON | OFF |
| **Complementary-Pin Control Logic Truth** | | | |
| nCTRL | CTRL | RFC-RF1 | RFC-RF2 |
| LOW | HIGH | ON | OFF |
| HIGH | LOW | OFF | ON |

**Table 1-6 PE4259 Truth Table**

# 2. Design of Single-pin Controlled RFSWs

We recommend you to use single-pin controlled RFSWs, which are used for reference design of the official ASR module and on which the SDK of ASR650X and ASR6601 chips are all based.

The following is an example of the hardware design of the ASR6601SE single-pin controlled RFSW. Its model is murata's XMSSJR6G0BA-093. The ASR6601's ANT_SW_CTRL (i.e., SX1262's DIO2 signal) is connected to the RFSW's CTRL (pin6) to control the TX and RX switching. GPIO10 is connected to VDD (pin4) of RFSW, which can be turned off in deep sleep mode to prevent it from leakage (leakage for XMSSJR6G0BA is about 5 uA). The control logic of RFSW is as follows:

**Table 2-1 Control Logic of Single-pin Controlled RFSWs**

| Mode | VDD (pin4) | CTRL (pin6) |
|---|---|---|
| TX | HIGH | HIGH |
| RX | HIGH | LOW |
| Deep Sleep | LOW | LOW |

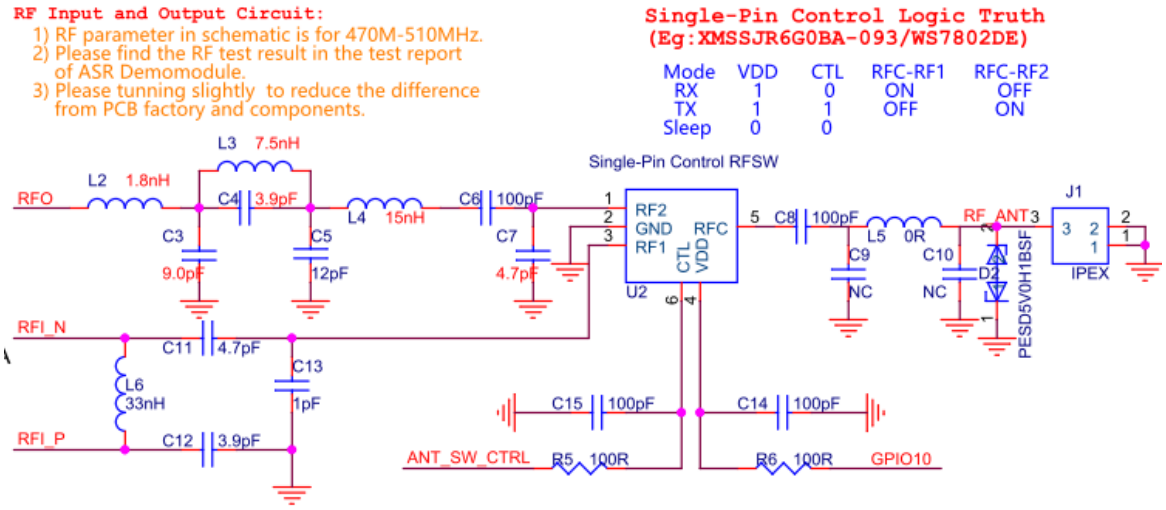



**Figure 2-1 Single-pin Controlled RFSW Schematic Reference Design**

For **software design**, please refer to the default SDK.

# 3. Design of Complementary-pin Controlled RFSWs

## 3.1 Design Scheme I for Complementary-pin Controlled RFSWs

**Hardware design:** ANT_SW_CTRL (i.e. DIO2 signal of SX1262) generates a complementary controlled signal through an inverter, controlling VC1 and VC2 of the complementary-pin controlled RFSW with its complementary signal for TX and RX switching.

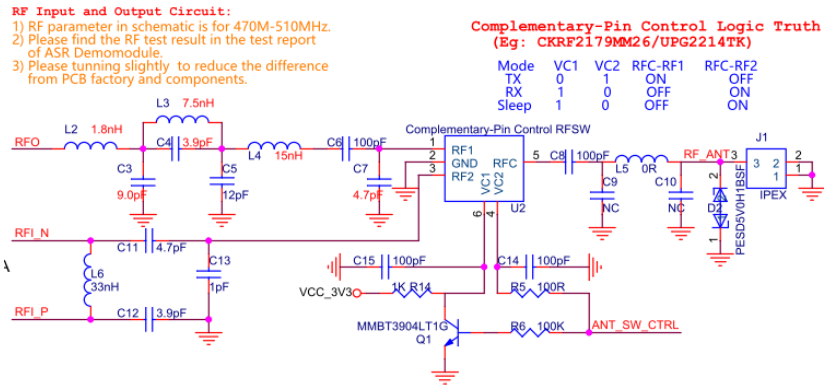



**Figure 3-1 Hardware Design Scheme I for Complementary-pin Controlled RFSWs**

**Software design:** Use the default SDK. No software modifications are required.

## 3.2 Design Scheme II for Complementary-pin Controlled RFSWs

**Hardware design:** ANT_SW_CTRL (i.e. DIO2 signal of SX1262) and a GPIO are used to control VC1 and VC2 of the complementary-pin controlled RFSW for TX and RX switching.

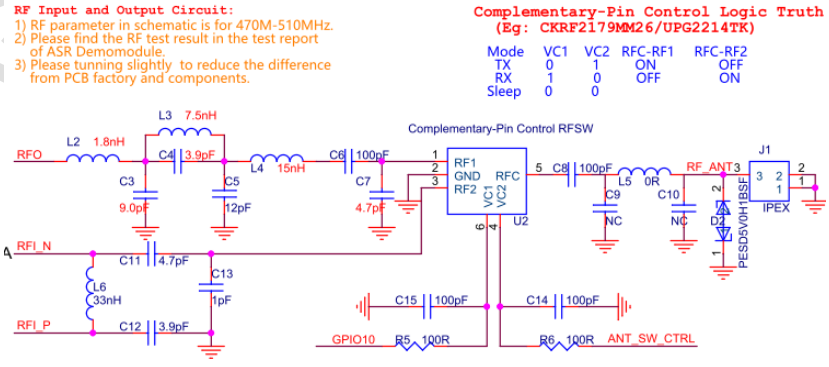



**Figure 3-2 Hardware Design Scheme II for Complementary-pin Controlled RFSWs**

**Software design:** Based on the default ASR6601 SDK, the software should be modified according to the following control logic:

**Table 3-1 Control Logic of Hardware Design Scheme II for Complementary-pin Controlled RFSWs**

| Mode | VC1 (pin6) GPIO10 | VC2 (pin4) ANT_SW_CTRL |
|---|---|---|
| TX | Low | High |
| RX | High | Low |
| Deep Sleep | Low | Low |
| *Note: ANT_SW_CTRL is the DIO2 of SX1262.* | | |

The *SX126xCheckDeviceReady* function in the sx126x.c file should be modified by modifying the code as follows, with newly added code marked in blue:

```
void SX126xCheckDeviceReady( void )
{
    if( ( SX126xGetOperatingMode( ) == MODE_SLEEP ) || ( SX126xGetOperatingMode( ) == MODE_RX_DC ) )
    {
        SX126xWakeup( );
        // Switch is turned off when device is in sleep mode and turned on is all other modes
        SX126xAntSwOn( );
    }
    if (SX126xGetOperatingMode( ) == MODE_RX)
    {
        SX126xAntSwOn();
    }
    else if (SX126xGetOperatingMode( ) == MODE_TX)
    {
        SX126xAntSwOff();
    }
    SX126xWaitOnBusy( );
}
```

**Note:**

*ANT_SW_CTRL (DIO2) is controllable by the SX1262's internal state machine and is uncontrollable by software. GPIO10 is controllable by software.*



## 3.3 Design Scheme III for Complementary-pin Controlled RFSWs

**Hardware design:** 2 GPIOs are used to control VC1 and VC2 of the complementary-pin controlled RFSW for TX and RX switching.

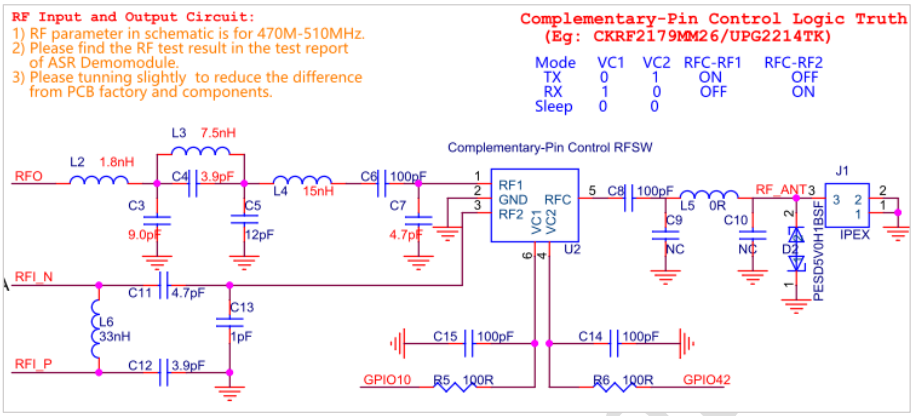



**Figure 3-3 Hardware Design Scheme III for Complementary-pin Controlled RFSWs**

**Software design:** Based on the default ASR6601 SDK, the software should be modified according to the following control logic:

**Table 3-2 Control Logic of Hardware Design Scheme III for Complementary-pin Controlled RFSWs**

| Mode | VC1 (pin6) GPIO10 | VC2 (pin4) GPIO42 |
|---|---|---|
| TX | Low | High |
| RX | High | Low |
| Deep Sleep | Low | Low |
| *Note: Other GPIOs can also be used at customers' convenience, with the software modified accordingly.* | | |

The *SX126xCheckDeviceReady* function in the sx126x.c file should be modified by modifying the code as follows, with newly added code marked in blue:

```
void SX126xCheckDeviceReady( void )
{
    if( ( SX126xGetOperatingMode( ) == MODE_SLEEP ) || ( SX126xGetOperatingMode( ) == MODE_RX_DC ) )
    {
        SX126xWakeup( );
        // Switch is turned off when device is in sleep mode and turned on is all other modes
        SX126xAntSwOn( );
    }
    if (SX126xGetOperatingMode( ) == MODE_TX) {
        gpio_init(GPIOA, GPIO_PIN_10, GPIO_MODE_OUTPUT_PP_LOW);
        gpio_init(GPIOC, GPIO_PIN_10, GPIO_MODE_OUTPUT_PP_HIGH);
    } else if (SX126xGetOperatingMode( ) == MODE_RX) {
        gpio_init(GPIOA, GPIO_PIN_10, GPIO_MODE_OUTPUT_PP_HIGH);
        gpio_init(GPIOC, GPIO_PIN_10, GPIO_MODE_OUTPUT_PP_LOW);
    }
    SX126xWaitOnBusy( );
}
```

In addition, the functions *SX126xAntSwOn* and *SX126xAntSwOff* in the sx1262-board.c file should be modified by deleting the code of the *SX126xAntSwOn* function, and modifying the code of the *SX126xAntSwOff* function to set GPIO10 and GPIO42 to output low level. The modified code is as follows.

```
void SX126xAntSwOn( void )
{

}

void SX126xAntSwOff( void )
{
    gpio_init(GPIOA, GPIO_PIN_10, GPIO_MODE_OUTPUT_PP_LOW);
    gpio_init(GPIOC, GPIO_PIN_10, GPIO_MODE_OUTPUT_PP_LOW);
}
```

**Notice:**

*Use GPIO10 and GPIO42 (or other GPIOs, with the software modified accordingly) to control VC1 and VC2 of RFSW, both of which are uncontrollable by software. ANT_SW_CTRL (DIO2) is discarded.*

## 3.4 Comparison of Design Schemes for Complementary-pin Controlled RFSWs

**Table 3-3 Comparison of Design Schemes for Complementary-pin Controlled RFSWs**

| Number | Description | Advantages and Disadvantage | Is Recommended |
|---|---|---|---|
| Scheme II | Use ANT_SW_CTRL (i.e. DIO2 signal of SX1262) and a GPIO to control VC1 and VC2 of the complementary-pin controlled RFSW | **Advantage:** In terms of hardware, the control signals of the complementary-pin controlled RFSW are compatible with the single-pin controlled RFSW circuit, requiring only software modifications according to the corresponding logic.<br>**Disadvantage:** ANT_SW_CTRL is uncontrollable by software and a GPIO is required. | Recommended |
| Scheme III | Use 2 GPIOs to control VC1 and VC2 of the complementary-pin controlled RFSW | **Advantages:** Two GPIOs are used as the control signals of the complementary-pin controlled RFSW, which allows flexible control and adaptation to different hardware solutions.<br>**Disadvantages:** Two GPIOs are needed, requiring software modifications according to the corresponding logic. | Moderately recommended |
| Scheme I | A control signal complementary to ANT_SW_CTRL (i.e., the DIO2 signal of SX1262) is generated via an inverter to control VC1 and VC2 of the complementary pin controlled RFSW with ANT_SW_CTRL. | **Advantages:** The control logic of the complementary-pin controlled RFSW is mainly implemented through hardware (inverter), no software modifications are required, and a GPIO can be spared.<br>**Disadvantages:** The complementary-pin controlled RFSW cannot be turned off, and there is leakage in both RFSW and inverter in deep sleep mode, which makes the solution unsuitable for applications with strict low-power requirements. | Not recommended |

