



HC32L07x Series

32-bit ARM® Cortex®-M0+ microcontrollers

Data sheet

Rev1.85 March 2025

Product Features

- 48MHz Cortex-M0+ 32-bit CPU
- HC32L072 / HC32L073 series with flexible power management system
 - 1.2μA @ 3V deep sleep mode: all clocks off, power-on reset valid, IO state retained, IO interrupt valid, all registers, RAM and CPU data saved
 - 1.6μA @3V deep sleep mode + RTC running
 - 9μA @32.768kHz low-speed run mode: CPU running, peripherals off, program running from FLASH
 - 40μA/MHz@3V@24MHz sleep mode: CPU stopped, peripherals off, main clock running
 - 140μA/MHz@3V@24MHz working mode: CPU running, peripherals off, program running from FLASH
 - 4μs Wake-up time, making mode switching more flexible and efficient, and the system more responsive
- 128K bytes of FLASH memory with erase and write protection function, supporting ISP, ICP, IAP
- 16K bytes of RAM memory with parity check to enhance system stability
- General I/O pins
- Clock, crystal oscillator
 - External high-speed crystal oscillator 8 ~ 32MHz
 - External low-speed crystal oscillator 32.768kHz
 - Internal high-speed clock 4/8/16/22.12/24MHz
 - Internal low-speed clock 32.8/38.4kHz
 - PLL clock 8 ~ 48MHz
 - Internal high-speed USB clock 48MHz
 - Hardware supports internal and external clock calibration and monitoring
- Timer/Counter
 - 3 general-purpose 16-bit timers, support 1 group of complementary PWM output, support double main frequency PWM output, support up to 96MHz PWM output
 - 1 advanced 16-bit timer, support 3-phase complementary PWM output, support double main frequency PWM output, support up to 96MHz PWM output
 - 3 high-performance 16-bit timer/counters, support PWM complementary, dead zone protection function
 - 1 ultra-low power pulse counter PCNT, with automatic timed wake-up function in low power mode, maximum timing up to 1024 seconds
 - 1 programmable 16-bit PCA, supporting 5-channel capture-compare,
- 5-channel PWM output
 - 2 low-power 16-bit timers, support cascading
 - 1 20-bit programmable watchdog circuit, built-in dedicated 10kHz oscillator provides WDT counting
- Communication interfaces
 - 4 UART standard communication interfaces
 - 2 LPUART low-power communication interfaces, can work in deep sleep mode
 - 2 SPI standard communication interfaces
 - 2 I2C standard communication interfaces
 - 2 I2S audio communication interfaces
 - 1 Crystal-less USB Full Speed Device
 - 1 CAN 2.0B standard communication interface
- Buzzer frequency generator, support complementary output
- Hardware perpetual calendar RTC module
- Hardware CRC-16/32 module
- Hardware 32-bit divider
- AES-128/192/256 hardware coprocessor
- TRNG True Random Number Generator
- 2-channel DMAC
- 4*52 / 6*50 / 8*48 LCD driver (073 series only)
- Globally unique 10-byte ID number
- 12-bit 1Msps sampling high-speed and high-precision SARADC, built-in op amp, can measure high output impedance signals
- 2-channel 12-bit 500Ksps DAC
- Integrated 5 multi-function operational amplifiers, two of which can be used as output buffers for 2 DACs
- Integrated 3-channel voltage comparator with 6-bit DAC and programmable comparison reference
- Integrated low voltage detector, configurable 16-step comparison voltage, can monitor port voltage and power supply voltage
- SWD debugging solution, providing full-function debugger
- Operating conditions: -40 ~ 85°C, 1.8 ~ 5.5V
- Package: LQFP100/ 64/ 48, QFN32

Supported models:

| | |
|----------------------|---------------------|
| HC32L072PATA-LQFP100 | HC32L072KATA-LQFP64 |
| HC32L072JATA-LQ48 | HC32L072FAUA-QN32TR |
| HC32L073PATA-LQFP100 | HC32L073KATA-LQFP64 |
| HC32L073JATA-LQ48 | |

Disclaimer

- ★ Xiaohua Semiconductor Co., Ltd. (hereinafter referred to as "XHSC") reserves the right to change, correct, enhance, and modify Xiaohua Semiconductor products and/or this document at any time without prior notice. Users can obtain the latest relevant information before placing an order. XHSC products are sold in accordance with the sales terms and conditions stated in the basic purchase and sales contract.
- ★ Customers are solely responsible for selecting appropriate XHSC products for their applications, and for designing, validating, and testing their applications to ensure that they meet the applicable standards and any safety, security, or other requirements.
- ★ XHSC hereby acknowledges that no license to any intellectual property rights is granted, either expressly or impliedly.
- ★ Resale of XHSC products on terms different from those set forth herein will void any warranty provided by XHSC with respect to such products.
- ★ Any graphics or words with "®" or "™" logo are trademarks of XHSC. All other product or service names displayed on XHSC products are the property of their respective owners.
- ★ The information in this notice supersedes and replaces the information in previous versions.

©2025 Xiaohua Semiconductor Co., Ltd. All rights reserved

Table of contents

| | |
|--|----------|
| Product Features | 2 |
| Disclaimer | 3 |
| Table of contents | 4 |
| List of Tables | 7 |
| List of Figures | 8 |
| 1 Introduction | 9 |
| 1.1 32-bit Cortex M0+ core | 10 |
| 1.2 128K Byte FLASH | 10 |
| 1.3 16K Byte RAM | 10 |
| 1.4 Clock System | 10 |
| 1.5 Operating Modes | 11 |
| 1.6 Real-time Clock RTC | 11 |
| 1.7 Port Controller GPIO | 11 |
| 1.8 Interrupt Controller NVIC | 12 |
| 1.9 Reset Controller RESET | 13 |
| 1.10 DMA Controller DMAC | 13 |
| 1.11 Timer TIM | 14 |
| 1.12 Pulse Counter PCNT | 15 |
| 1.13 Watchdog Timer WDT | 16 |
| 1.14 Universal Synchronous Asynchronous Receiver Transmitter UART0~UART3 | 16 |
| 1.15 Low power synchronous asynchronous receiver and transmitter LPUART0~LPUART1 | 17 |
| 1.16 Serial Peripheral Interface SPI | 17 |
| 1.17 I2C Bus | 18 |
| 1.18 Audio Interface I2S | 18 |
| 1.19 USB2.0 full speed module | 18 |
| 1.20 Controller Area Network CAN | 18 |
| 1.21 Crystal-less USB Clock Calibrator CTS | 19 |
| 1.22 Buzzer | 19 |
| 1.23 Clock Calibration Module CLKTRIM | 19 |
| 1.24 Device Electronic Signature | 19 |
| 1.25 Cyclic Redundancy Check CRC | 19 |
| 1.26 Hardware Divider Module HDIV | 19 |
| 1.27 Advanced Encryption Standard Module AES | 20 |
| 1.28 True Random Number Generator TRNG | 20 |

| | |
|--|-----------|
| 1.29 Analog-to-Digital Converter ADC | 20 |
| 1.30 Digital-to-Analog Converter DAC | 21 |
| 1.31 Analog Comparator VC | 21 |
| 1.32 Low Voltage Detector LVD | 21 |
| 1.33 Operational Amplifier OPA | 21 |
| 1.34 Liquid Crystal Controller LCD | 21 |
| 1.35 Embedded Debug System | 22 |
| 1.36 Programming Modes | 22 |
| 1.37 Security | 22 |
| 2 Product Lineup | 23 |
| 2.1 Product Naming | 23 |
| 2.2 Functionality | 24 |
| 3 Pin Configuration and Function | 25 |
| 3.1 Pin Configuration Diagram | 25 |
| 3.2 Pin Function Description | 32 |
| 3.3 Module signal description | 42 |
| 4 Functional Block Diagram..... | 45 |
| 5 Memory Map | 46 |
| 6 Typical application circuit diagram | 48 |
| 7 Electrical characteristics | 49 |
| 7.1 Test conditions | 49 |
| 7.1.1 Minimum and maximum values | 49 |
| 7.1.2 Typical values | 49 |
| 7.2 Absolute Maximum Ratings | 50 |
| 7.3 Operating conditions | 51 |
| 7.3.1 General operating conditions | 51 |
| 7.3.2 Operating conditions during power-on and power-off | 51 |
| 7.3.3 Embedded reset and LVD module features | 52 |
| 7.3.4 Built-in reference voltage | 54 |
| 7.3.5 Supply current characteristics | 54 |
| 7.3.6 Wake-up time from low power modes | 58 |
| 7.3.7 External clock source characteristics | 59 |
| 7.3.8 Internal clock source characteristics | 64 |
| 7.3.9 PLL Characteristics | 66 |
| 7.3.10 Memory characteristics | 66 |

| | |
|--|-----------|
| 7.3.11 EFT Characteristics | 66 |
| 7.3.12 ESD characteristics | 67 |
| 7.3.13 I/O Port Characteristics | 67 |
| 7.3.14 RESETB Pin Characteristics..... | 71 |
| 7.3.15 ADC Characteristics | 72 |
| 7.3.16 VC Characteristics | 74 |
| 7.3.17 OPA Features | 74 |
| 7.3.18 LCD Controller..... | 75 |
| 7.3.19 DAC Characteristics | 75 |
| 7.3.20 TIM timer characteristics | 76 |
| 7.3.21 Communication interfaces..... | 78 |
| 8 Packaging Information | 84 |
| 8.1 Package Dimensions | 84 |
| 8.2 Pad Diagram | 88 |
| 8.3 Marking Description..... | 92 |
| 8.4 Package Thermal Resistance..... | 93 |
| 9 Ordering Information | 94 |
| Version Revision History | 95 |

List of Tables

| | |
|--|----|
| Table 3-1 Module Signal Description | 42 |
| Table 7-1 Voltage Characteristics | 50 |
| Table 7-2 Current Characteristics | 50 |
| Table 7-3 Temperature Characteristics | 51 |
| Table 7-4 General Operating Conditions | 51 |
| Table 7-5 Power-on and Power-off Operating Conditions | 51 |
| Table 7-6 POR/Brown Out | 52 |
| Table 7-7 LVD Module Characteristics | 53 |
| Table 7-8 Operating Current Characteristics | 54 |
| Table 7-9 Port Output Characteristics | 67 |
| Table 7-10 Advanced Timer (ADVTIM) Characteristics | 76 |
| Table 7-11 General Timer Characteristics | 76 |
| Table 7-12 PCA Characteristics | 77 |
| Table 7-13 Low Power Timer Characteristics | 77 |
| Table 7-14 WDT Characteristics | 77 |
| Table 7-15 I2C Interface Characteristics | 78 |
| Table 7-16 SPI Interface Characteristics ⁽¹⁾⁽²⁾ | 79 |
| Table 8-1 Thermal Resistance Coefficient Table of Each Package | 93 |

List of Figures

| | |
|---|----|
| Figure 3-1 Pin configuration diagram | 31 |
| Figure 7-1 POR/Brown Out diagram | 52 |
| Figure 7-2 Output port VOH/VOL measured curve | 68 |
| Figure 7-3 I2C interface timing | 78 |
| Figure 7-4 SPI timing diagram (master mode) | 80 |
| Figure 7-5 SPI timing diagram (slave mode cpha=0) | 80 |
| Figure 7-6 SPI timing diagram (slave mode cpha=1) | 81 |
| Figure 7-7 I2S slave timing diagram | 83 |
| Figure 7-8 I2S master timing diagram | 83 |

1 Introduction

The HC32L072/HC32L073 series is an ultra-low power, wide voltage range MCU designed to extend the battery life of portable measurement systems. It integrates a 12-bit 1Msps high-precision SARADC, 2 12-bit DACs, and integrates comparators, op amps, built-in high-performance PWM timers, LCD displays, multiple UARTs, SPI, I2C, I2S, USB, CAN and other rich communication peripherals, built-in AES, TRNG and other information security modules, with high integration, high anti-interference, high reliability and ultra-low power consumption. The core of this product adopts the Cortex-M0+ core, with mature Keil & IAR debugging and development software, supports C language and assembly language, assembly instructions.

Ultra-low power MCU typical applications

- Sensor applications, IoT applications
- Smart meters, wireless modules, thermostats, shelf labels
- Smart transportation, alarm systems
- Smart homes, medical equipment

1.1 32-bit Cortex M0+ core

The ARM® Cortex®-M0+ processor is derived from the Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhystone MIPS/MHz. At the same time, it has added a number of new designs, improved debugging and tracing capabilities, reduced the number of instruction cycles (IPCs) per instruction, improved two-stage pipelines for Flash access, and incorporated energy-saving and power-reduction technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debuggers.

The Cortex-M0+ includes a hardware debugging circuit that supports a 2-pin SWD debugging interface.

ARM Cortex-M0+ features:

| | |
|------------------------|---|
| Instruction set | Thumb/ Thumb-2 |
| Pipeline | 2-stage pipeline |
| Performance efficiency | 2.46 CoreMark/ MHz |
| Performance efficiency | 0.95 DMIPS/ MHz in Dhystone |
| Interrupts | 32 fast interrupts |
| Interrupt priority | Configurable 4-level interrupt priority |
| Enhanced instructions | Single-cycle 32-bit multiplier |
| Debug | Serial-wire debug port, supports 4 hard interrupts (break point) and 2 watch points (watch point) |

1.2 128K Byte FLASH

Built-in fully integrated FLASH controller, no external high voltage input is required, high voltage is generated by the fully built-in circuit for programming. Supports ISP, IAP, ICP functions.

1.3 16K Byte RAM

RAM data will be retained according to different power consumption modes selected by customers. Comes with hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

1.4 Clock System

A configurable high-precision internal clock RCH with a frequency of 4~24MHz. When configured at 24MHz, the wake-up time from low-power mode to working mode is 4us, and the frequency deviation is small within the full voltage and temperature range, so there is no need to connect an expensive high-frequency crystal.

An external crystal oscillator XTH with a frequency of 8~32MHz.

An external crystal oscillator XTL with a frequency of 32.768kHz.

An internal clock RCL with a frequency of 32.8/38.4kHz.

A PLL with an output frequency of 8~48MHz.

1.5 Operating Modes

- 1) Active Mode: CPU is running and peripheral function modules are running.
- 2) Sleep Mode: CPU stops running and peripheral function modules are running.
- 3) Deep Sleep Mode: CPU stops running, high-speed clock stops, and low-power function modules are running.

1.6 Real-time Clock RTC

RTC (Real Time Counter) is a register that supports BCD data. It uses a 32.768kHz crystal oscillator as its clock and can realize the perpetual calendar function. The interrupt cycle can be configured as year/month/day/hour/minute/second. 24/12 hour time mode, hardware automatically corrects leap year. It has precision compensation function, with the highest accuracy of 0.96ppm. The internal temperature sensor or external temperature sensor can be used for precision compensation, and the year/month/day/hour/minute/second can be adjusted by software +1/-1, with the minimum adjustable accuracy of 1 second.

The RTC calendar recorder used to indicate time and date will not clear the retained value when the MCU is reset due to external factors. It is the best choice for measuring equipment that requires a permanent high-precision real-time clock.

1.7 Port Controller GPIO

Up to 86 GPIO ports can be provided, some of which are multiplexed with analog ports. Each port is controlled by an independent control register bit and supports FAST IO. Support edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU from various deep sleep modes to working modes. Support position, clear, and position clear operations. Support Push-Pull CMOS push-pull output and Open-Drain output. Built-in pull-up resistors and pull-down resistors, with Schmitt trigger input filtering function. The output drive capability is configurable, and the maximum current drive capability supports 18mA. All general IOs can support external asynchronous interrupts.

1.8 Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in nested vector interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs; it has four interrupt priority levels, can handle complex logic, and can perform real-time control and interrupt processing.

The 32 interrupt entry vector addresses are:

| Interrupt vector number | Interrupt Source |
|-------------------------|------------------|
| [0] | GPIO_PA |
| [1] | GPIO_PB |
| [2] | GPIO_PC/GPIO_PE |
| [3] | GPIO_PD/GPIO_PF |
| [4] | DMAC |
| [5] | TIM3 |
| [6] | UART0/UART2 |
| [7] | UART1/UART3 |
| [8] | LPUART0 |
| [9] | LPUART1 |
| [10] | SPI0/I2S0 |
| [11] | SPI1/I2S1 |
| [12] | I2C0 |
| [13] | I2C1 |
| [14] | TIM0 |
| [15] | TIM1 |
| [16] | TIM2 |
| [17] | LPTIM0/LPTIM1 |
| [18] | TIM4 |
| [19] | TIM5 |
| [20] | TIM6 |
| [21] | PCA |
| [22] | WDT |
| [23] | RTC |
| [24] | ADC/DAC |
| [25] | PCNT |
| [26] | VC0/VC1/VC2/ LVD |
| [27] | USB |
| [28] | CAN |
| [29] | LCD |
| [30] | RAM FLASH |
| [31] | CLKTRIM /CTS |

1.9 Reset Controller RESET

This product has 7 reset signal sources. Each reset signal can make the CPU run again. Most registers will be reset and the program counter PC will point to the starting address.

| | Reset Source |
|-----|---------------------------------------|
| [0] | Power-on reset POR BOR |
| [1] | External reset pin reset |
| [2] | WDT reset |
| [3] | PCA reset |
| [4] | Cortex-M0+ LOCKUP hardware reset |
| [5] | Cortex-M0+ SYSRESETREQ software reset |
| [6] | LVD reset |

1.10 DMA Controller DMAC

The DMAC (Direct Memory Access Controller) function block can transfer data at high speed without going through the CPU. Using DMAC can improve system performance.

- DMAC is equipped with an independent bus, so DMAC can perform transfer operations even when the CPU bus is used.
- It consists of 2 channels and can perform 2 independent DMA transfers.
- The transfer destination address, transfer source address, transfer data size, transfer request source and transfer mode can be set, and the start of transfer operation, forced termination of transfer and suspension of transfer can be controlled for each channel.
- The start, forced termination and suspension of batch transfers for all channels can be controlled.
- When multiple channels are operated simultaneously, the priority of the operating channel can be selected by a fixed method or a round-robin method.
- Supports hardware DMA transfer using peripheral interrupt signals.
- Complies with the system bus (AHB) and supports 32-bit address space (4GB).

1.11 Timer TIM

| Type | Name | Bit Width | Prescaler | Count Direction | PWM | Capture | Complementary Output |
|----------------------------|--------|-----------|----------------------------|---------------------------|------|---------|----------------------|
| General purpose timer | TIM0 | 16/32 | 1/2/4/8/16/ 32/64/256 | Up Down Up and down | 2 | 2 | 1 |
| | TIM1 | 16/32 | 1/2/4/8/16/ 32/64/256 | Up Down Up and down | 2 | 2 | 1 |
| | TIM2 | 16/32 | 1/2/4/8/16/ 32/64/256 | Up Down Up and down | 2 | 2 | 1 |
| | TIM3 | 16/32 | 1/2/4/8/16/ 32/64/256 | Up Down Up and down | 6 | 6 | 3 |
| Low Power Timer | LPTIM0 | 16 | 1/2/4/8/16/ 32/64/256 | Up | None | None | None |
| | LPTIM1 | 16 | 1/2/4/8/16/ 32/64/256 | Up | None | None | None |
| Programmable Counter Array | PCA | 16 | 2/4/8/16/32 | Up | 5 | 5 | None |
| Advanced Timer | TIM4 | 16 | 1/2/4/8/16/ 64/256/1024 | Up Down Up and down | 2 | 2 | 1 |
| | TIM5 | 16 | 1/2/4/8/16/ 64/256/1024 | Up Down Up and down | 2 | 2 | 1 |
| | TIM6 | 16 | 1/2/4/8/16/ 64/256/1024 | Up Down Up and down | 2 | 2 | 1 |

The general timer includes four timers TIM0/1/2/3.

General timer features:

- PWM independent output, complementary output
- Capture input
- Dead zone control
- Brake control
- Edge-aligned, symmetrical center-aligned and asymmetrical center-aligned PWM outputs
- Quadrature encoding counting function
- Single pulse mode
- External counting function

TIM0/1/2 have the same functions. TIM0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reload function or a 32-bit timer/counter without reload function. Each timer of TIM0/1/2 has 2 capture and compare functions, which can generate 2 independent PWM outputs or 1 group of PWM complementary outputs. It has a dead zone control function.

TIM3 is a multi-channel general-purpose timer with all the functions of TIM0/1/2, which can generate 3 groups of PWM complementary outputs or 6 independent PWM outputs, and up to 6 input captures. It has a dead zone control function.

Low-power timer LPTIM is an asynchronous 16-bit timer/counter, which can still time/count through internal low-speed RC or external low-speed crystal oscillator after the system clock is turned off. The system can be woken up in low-power mode through interrupts.

PCA (Programmable Counter Array) supports up to 5 16-bit capture/compare modules. The timer/counter can be used as a general clock count/event counter with capture/compare functions. Each module of the PCA can be independently programmed to provide input capture, output comparison or pulse width modulation. In addition, module 4 has an additional watchdog timer mode.

The Advanced Timer contains three timers TIM4/5/6. TIM4/5/6 are high-performance counters with the same functions. They can be used to count and generate clock waveforms in different forms. One timer can generate a complementary pair of PWM or independent 2-way PWM outputs, and can capture external inputs for pulse width or period measurement.

The basic functions and features of the Advanced Timer are shown in the table:

| | |
|-----------------|--|
| Waveform Mode | Sawtooth wave, triangle wave |
| Basic Functions | • Incremental and decremental counting direction |
| | • Software synchronization |
| | • Hardware synchronization |
| | • Cache function |
| | • Quadrature encoding counting |
| | • General PWM output |
| | • Protection mechanism |
| | • AOS associated action |
| Interrupt Type | Count compare match interrupt |
| | Count period match interrupt |
| | Dead time error interrupt |

1.12 Pulse Counter PCNT

The PCNT (Pulse Counter) module is used to count external pulses, supporting single and dual (quadrature coded and non-cross coded) pulses. It can count without software involvement in low-power sleep mode.

Pulse Counter Features:

- 16-bit counter with reload function
- Single-channel pulse counting

- Dual-channel non-quadrature pulse counting
- Dual-channel quadrature pulse counting, no missing codes
- Up/down count overflow interrupt
- Pulse timeout interrupt
- 4 decoding error interrupts, non-quadrature pulse mode
- 1 direction change interrupt, quadrature pulse mode
- Multi-level pulse width filtering
- Configurable input pulse polarity
- Support low power mode counting
- Support wake-up of MCU in low power mode
- Support any pulse edge spacing not less than 1 counting clock cycle
- With automatic timed wake-up function in low power mode, the maximum timer is 1024 seconds

1.13 Watchdog Timer WDT

WDT (Watch Dog Timer) is a configurable 20-bit timer that provides reset in case of MCU abnormality; built-in 10kHz low-speed clock input as counter clock. In debug mode, you can choose to pause or continue running; only writing a specific sequence can restart WDT.

1.14 Universal Synchronous Asynchronous Receiver Transmitter UART0~UART3

4 Universal Asynchronous Receiver/Transmitter, UART0~UART3.

Basic functions of UART:

- Half-duplex and full-duplex transmission
- 8/ 9-Bit transmission data length
- Hardware parity check
- 1/ 1.5/ 2-Bit stop bit
- Four different transmission modes
- 16-Bit baud rate generator
- Multi-machine communication
- Hardware address recognition
- DMAC hardware transmission handshake
- Hardware flow control
- Support single-line mode

1.15 Low power synchronous asynchronous receiver and transmitter **LPUART0~LPUART1**

2 Low Power Universal Asynchronous Receiver/Transmitter (LPUART0/LPUART1) that can work in low power mode.

LPUART basic functions:

- Transmission clock SCLK (SCLK can select XTL, RCL and PCLK)
- Transmit and receive data in system low power mode
- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity check
- 1/1.5/2-Bit stop bit
- Four different transmission modes
- 16-Bit baud rate generator
- Multi-machine communication
- Hardware address recognition
- DMAC hardware transmission handshake
- Hardware flow control
- Support single-line mode

1.16 Serial Peripheral Interface SPI

2 synchronous serial interface (Serial Peripheral Interface)

SPI basic features:

- Can be configured as a master or slave through programming
- Four-wire transmission mode, full-duplex communication
- 7 configurable baud rates in master mode
- The maximum division factor of master mode is PCLK/2, and the maximum communication rate is 16Mbps
- The maximum division factor of slave mode is PCLK/4, and the maximum communication rate is 12Mbps
- Configurable serial clock polarity and phase
- Interrupts support
- 8-bit data transmission, high bits are transmitted first and low bits later
- Support DMA software/hardware access

1.17 I2C Bus

2 I2C, using serial synchronous clock, can realize data transmission at different rates between devices.

I2C basic features:

- Supports four working modes: master send/receive, slave send/receive
- Supports three working rates: standard (100Kbps)/fast (400Kbps)/high speed (1Mbps)
- Supports 7-bit addressing function
- Supports noise filtering function
- Supports broadcast address
- Supports interrupt status query function

1.18 Audio Interface I2S

2 I2S audio communication interfaces

- Support Philips/MSB/LSB/PCM modes
- Support MCK output
- Support 5 audio sampling rates: 48, 44.1, 32, 16, 8 kHz
- Support 3 data lengths: 16, 24, 32 Bit
- Support 2 frame lengths: 16, 32 Bit
- Support DMA data transmission
- Support full-duplex transmission and reception (2 I2S cooperation)
- Support master transmission and reception
- Support slave transmission and reception

1.19 USB2.0 full speed module

The USB Full Speed (USBFS) controller provides a USB communication solution for portable devices. The USBFS controller supports device mode and has a full-speed PHY integrated inside the chip. The full-speed (FS, 12Mb/s) transceiver is supported in device mode. The USBFS controller supports all four transfer modes defined by the USB2.0 protocol (control transfer, bulk transfer, interrupt transfer, and isochronous transfer).

1.20 Controller Area Network CAN

The CAN communication interface module is equipped with 512 bytes of RAM for storing the sent and received data. It supports the CAN2.0B protocol specified in ISO11898-1 and the TTCAN protocol specified in ISO11898-4.

1.21 Crystal-less USB Clock Calibrator CTS

The clock calibration timer can adjust and calibrate the RCH48M clock frequency for use with Crystal-less USB. It can also adjust and calibrate the clock frequency of other RC oscillators, and can also be used as a general-purpose timer.

1.22 Buzzer

The 4 general-purpose timers and 2 low-power timers have multiplexed outputs to provide programmable drive frequencies for the buzzer. The buzzer port can provide 18mA of sink current, complementary output, and does not require additional transistors.

1.23 Clock Calibration Module CLKTRIM

Built-in clock calibration module, can calibrate the internal RC clock through the external accurate crystal clock, can also use the internal RC clock to check whether the external crystal clock is working properly.

Basic features of clock calibration:

- Calibration mode
- Monitoring mode
- 32-bit reference clock counter can load initial value
- 32-bit calibrated clock counter can configure overflow value
- 6 reference clock sources
- 6 calibrated clock sources
- Support interrupt mode

1.24 Device Electronic Signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. The UID address is: 0x00100E74 - 0x00100E7D.

1.25 Cyclic Redundancy Check CRC

CRC16 complies with the polynomial $x^{16} + x^{12} + x^5 + 1$ given in ISO/IEC13239.

CRC32 complies with the polynomial $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ given in ISO/IEC13239.

1.26 Hardware Divider Module HDIV

HDIV (Hardware Divider) is a 32-bit signed/unsigned integer hardware divider.

Basic features of HDIV hardware divider:

- Configurable signed/unsigned integer division calculation

- 32-bit dividend, 16-bit divisor
- Output 32-bit quotient and 32-bit remainder
- Division by zero warning flag, division operation end flag
- 10 clock cycles to complete a division operation
- Writing the divisor register triggers the start of the division operation
- Automatically wait for the calculation to end when reading the quotient register/remainder register

1.27 Advanced Encryption Standard Module AES

AES (The Advanced Encryption Standard) is a new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on October 2, 2000. The block length of AES is fixed at 128 bits, and the key length supports 128/192/256 bits.

1.28 True Random Number Generator TRNG

TRNG is a true random number generator used to generate true random numbers.

1.29 Analog-to-Digital Converter ADC

12-bit successive approximation analog-to-digital converter with monotonicity and no missing codes. The sampling rate reaches 1Msps when working at 24MHz ADC clock. The reference voltage can be selected from the on-chip precision voltage (1.5V or 2.5V) or from the external input or power supply voltage. 40 input channels, including 36 external pin inputs, 1 internal temperature sensor voltage, 1 1/3 power supply voltage, and 2 DAC outputs. Built-in configurable input signal amplifier to detect high output impedance signals.

SAR ADC basic features:

- 12-bit conversion accuracy
- 1Msps conversion speed
- 40 input channels, including 36 external pin inputs, 1 internal temperature sensor voltage, 1 1/3 AVCC voltage, 2 DAC outputs
- 4 reference sources: AVCC voltage, ExRef pin, built-in 1.5V reference voltage, built-in 2.5V reference voltage
- ADC voltage input range: 0~Vref
- 4 conversion modes: single conversion, sequential scan continuous conversion, queue scan continuous conversion, continuous conversion accumulation
- Input channel voltage threshold monitoring
- Software configurable ADC conversion rate
- Built-in signal amplifier, can convert high-impedance signals
- Support on-chip external devices to automatically trigger ADC conversion, effectively reduce chip power consumption and improve the real-time performance of conversion

1.30 Digital-to-Analog Converter DAC

2-channel 12Bit 500Ksps DAC, capable of digital-to-analog conversion.

1.31 Analog Comparator VC

Built-in 3 VCs, chip pin voltage monitoring/comparison circuits. 16 configurable positive external input channels, 11 configurable negative external input channels; 4 internal negative input channels, including 1 internal temperature sensor voltage, 1 built-in BGR 2.5V reference voltage, and 1 64-stage resistor divider. VC output can be used for general timer TIM0/1/2/3, low power timer LPTIM and programmable counter array PCA capture, gating, and external counting clock. Asynchronous interrupts can be generated based on rising/falling edges to wake up the MCU from low power mode. Configurable software anti-shake function.

1.32 Low Voltage Detector LVD

Detect the chip power supply voltage or chip pin voltage. 16-level voltage monitoring value (1.8 ~ 3.3V). Asynchronous interrupt or reset can be generated according to the rising/falling edge. With hardware hysteresis circuit and configurable software anti-shake function.

LVD basic features:

- 4 monitoring sources, AVCC, PC13, PB08, PB07;
- 16-level threshold voltage, 1.8~3.3V optional;
- 8 trigger conditions, high level, rising edge, falling edge combination;
- 2 trigger results, reset, interrupt;
- 8-level filter configuration to prevent false triggering;
- Hysteresis function, strong anti-interference.

1.33 Operational Amplifier OPA

OPA0/ 1/ 2 modules can be flexibly configured and are suitable for simple filter and buffer applications. The OPA3/4 module can be used as a DAC buffer or configured as an op amp.

1.34 Liquid Crystal Controller LCD

Note: Only for HC32L073 series.

The LCD controller is a digital controller/driver for monochrome passive liquid crystal displays (LCDs) with up to 8 common terminals (COM) and 48 segment terminals (SEG) to drive 208 (4x52) or 384 (8x48) LCD picture elements. Capacitive or resistive voltage division can be selected, and internal resistor voltage division is supported. Internal resistor voltage division can adjust the contrast. Supports DMA hardware data transfer.

LCD Basic Features:

- Highly flexible frame rate control
- Supports static, 1/2, 1/3, 1/4, 1/6 and 1/8 duty cycles

- Supports 1/2, 1/3 bias
- LCD data RAM with up to 16 registers
- LCD contrast can be configured by software
- 3 drive waveform generation methods: internal resistor voltage division, external resistor voltage division, external capacitor voltage division.
The power consumption of the internal resistor voltage division method can be configured by software to match the capacitor charge required by the LCD panel.
- Supports low power mode: LCD controller can display in Active, Sleep, DeepSleep mode
- Configurable frame interrupt
- Support LCD flashing function and configurable multiple flashing frequencies
- Unused LCD segments and common pins can be configured as digital or analog functions

1.35 Embedded Debug System

Embedded debugging solution, providing a full-featured real-time debugger, with standard and mature Keil/IAR debugging and development software. Supports 4 hard breakpoints and multiple soft breakpoints.

1.36 Programming Modes

Supports two programming modes: online programming and offline programming.

Supports two programming protocols: ISP protocol and SWD protocol.

Supports unified programming interface: ISP protocol and SWD protocol share SWD port.

When reset, BOOT0 (PF11) pin is high level, the chip works in ISP programming mode, and FLASH can be programmed through ISP.

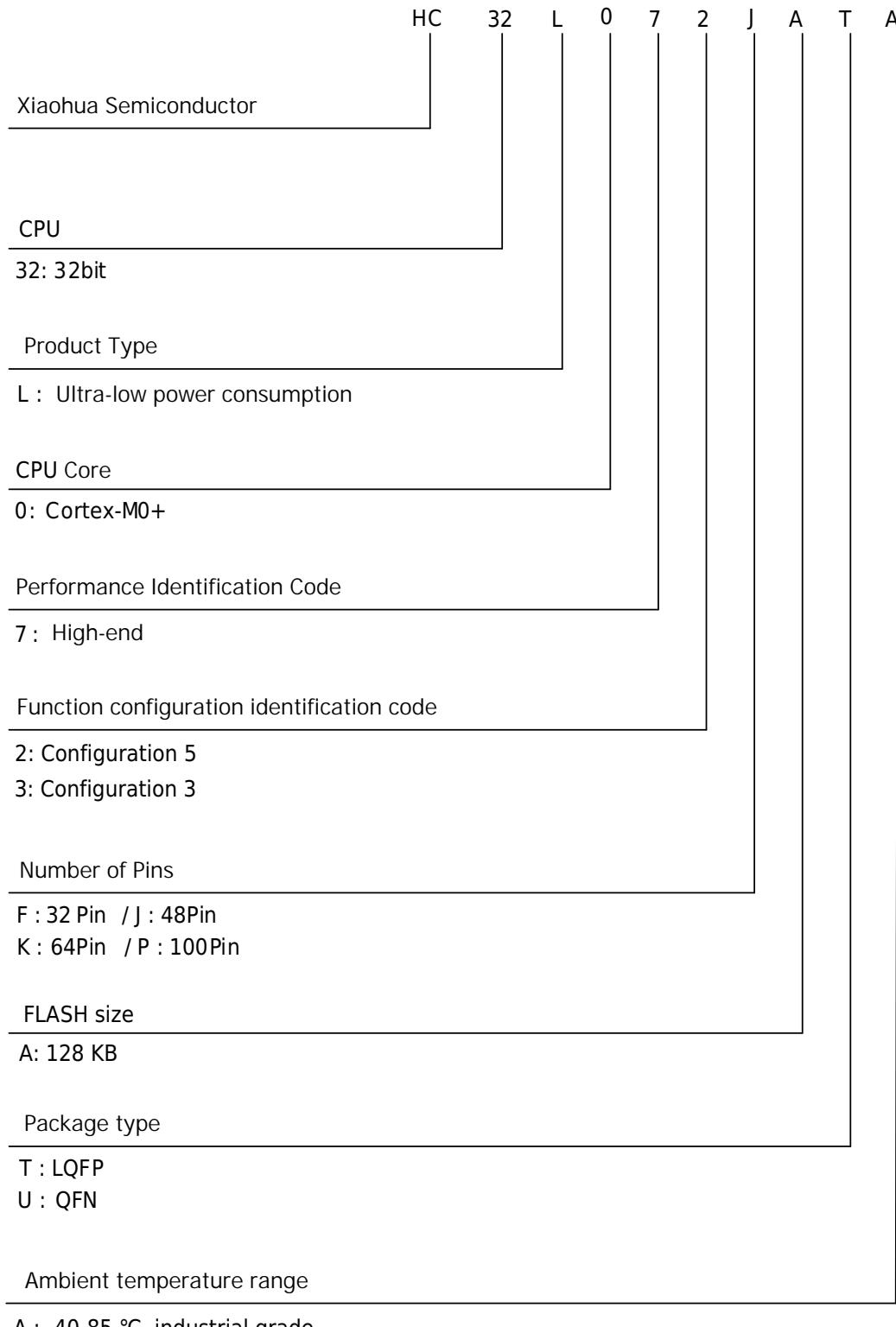
When reset, BOOT0 (PF11) pin is low level, the chip works in user mode, the chip executes the program code in FLASH, and Flash can be programmed through SWD protocol.

1.37 Security

Encrypted embedded debugging solution with full-featured real-time debugger.

2 Product Lineup

2.1 Product Naming



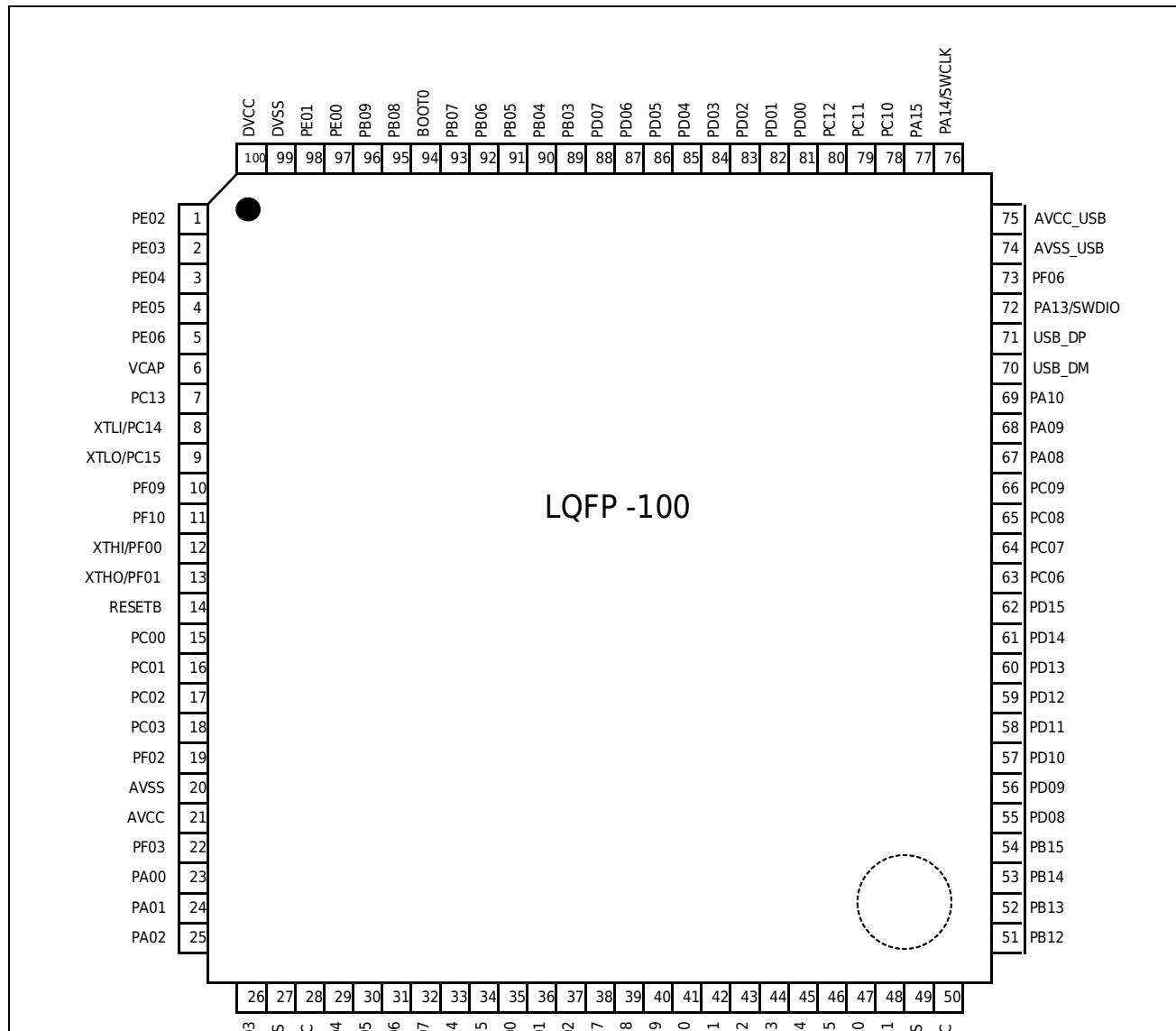
2.2 Functionality

| Product Name | L072PATA | L073PATA | L072KATA | L073KATA | L072JATA | L073JATA | L072FAUA | | | | | | |
|-----------------------------|---|------------------------|----------|--|----------|--|----------|--|--|--|--|--|--|
| Number of Pins | 100 | | 64 | | 48 | | 32 | | | | | | |
| GPIO pins | 86 | | 50 | 52 | 36 | 38 | 22 | | | | | | |
| CPU | Core | Cortex M0+ | | | | | | | | | | | |
| | Frequency | 48MHz | | | | | | | | | | | |
| Power supply voltage range | 1.8 ~5.5V | | | | | | | | | | | | |
| Temperature rang | -40 ~ 85°C | | | | | | | | | | | | |
| Debug function | SWD debug interface | | | | | | | | | | | | |
| Unique identification code | Support | | | | | | | | | | | | |
| 通信接口 | UART0/1/2/3 LPUART0/1 SPI0/1 I2C0/1 I2S0/1 | | | UART0/1 LPUART0/1 SPI0/1 I2C0/1 I2S0/1 | | UART0/1 LPUART0 SPI0 I2C0 I2S0 | | | | | | | |
| Communication interfaces | General purpose timer TIM0/1/2/3 Advanced timer TIM4/5/6 Low power timer LPTIMO/1 | | | | | | | | | | | | |
| 12-bit A/D converter | 24ch | | 23ch | | 17ch | | 10ch | | | | | | |
| 12-bit D/A converter | 2ch | | 2ch | | 2ch | | 2ch | | | | | | |
| Analog voltage comparator | VC0/1/2 | | | | | | | | | | | | |
| Operational amplifier | 5 | | 5 | | 3 | | 1 | | | | | | |
| USB | Support | | Support | Not support | Support | Not support | Support | | | | | | |
| CAN | Support | | | | | | | | | | | | |
| Real-time clock | Support | | | | | | | | | | | | |
| Port interrupt | 86 | 50 | 52 | 36 | 38 | 22 | | | | | | | |
| Low voltage detection reset | 1 | | | | | | | | | | | | |
| Clock | Internal high speed oscillator | RCH 4/8/16/22.12/24MHz | | | | | | | | | | | |
| | Internal low speed oscillator | RCL 32.8/38.4kHz | | | | | | | | | | | |
| | PLL | 8~48MHz | | | | | | | | | | | |
| | External high speed crystal | 8~32MHz | | | | | | | | | | | |
| Buzzer | Max 6ch | | | | | | | | | | | | |
| Flash Security Protection | Support | | | | | | | | | | | | |
| RAM Parity | Support | | | | | | | | | | | | |

3 Pin Configuration and Function

3.1 Pin Configuration Diagram

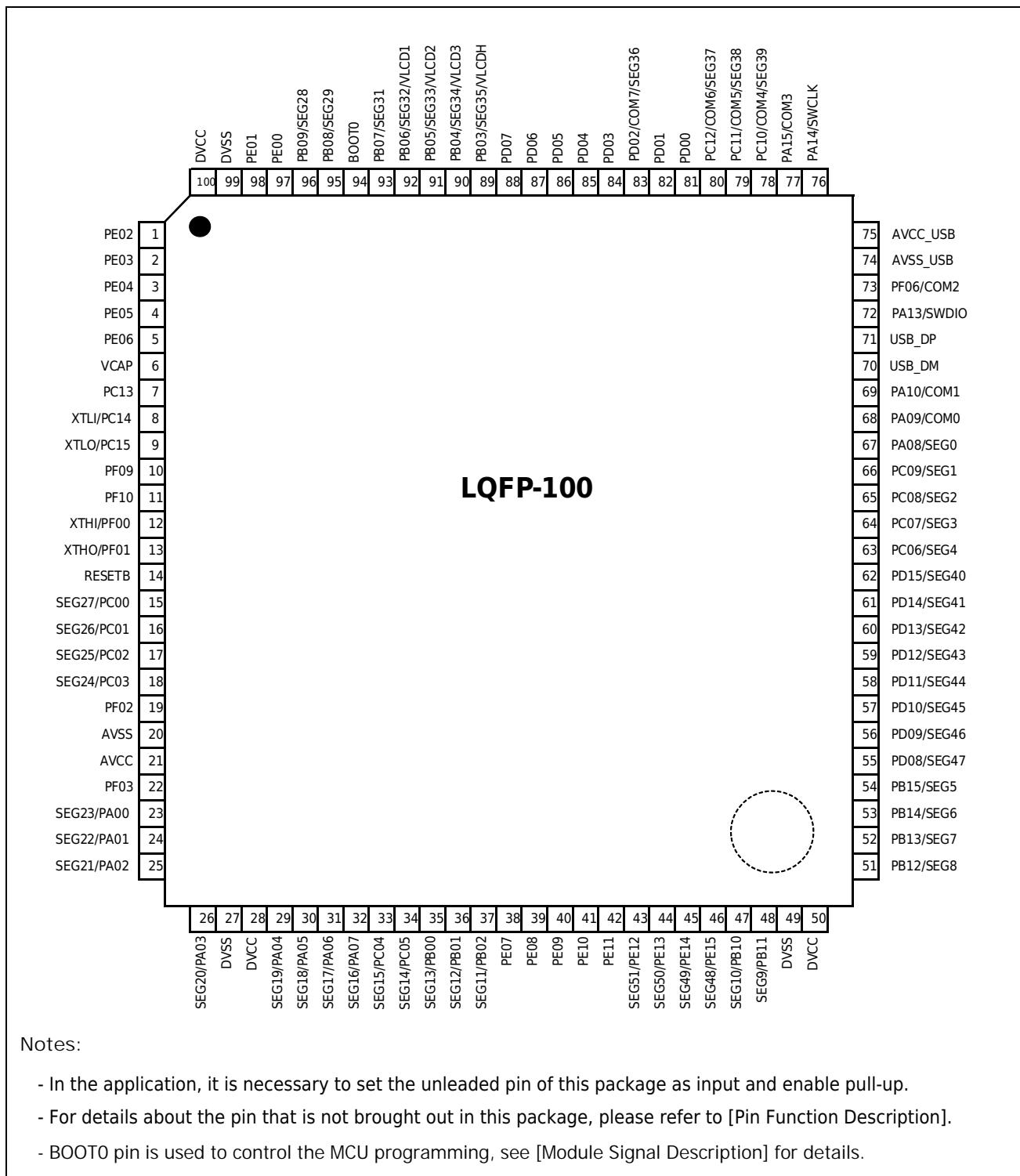
HC32L072PATA



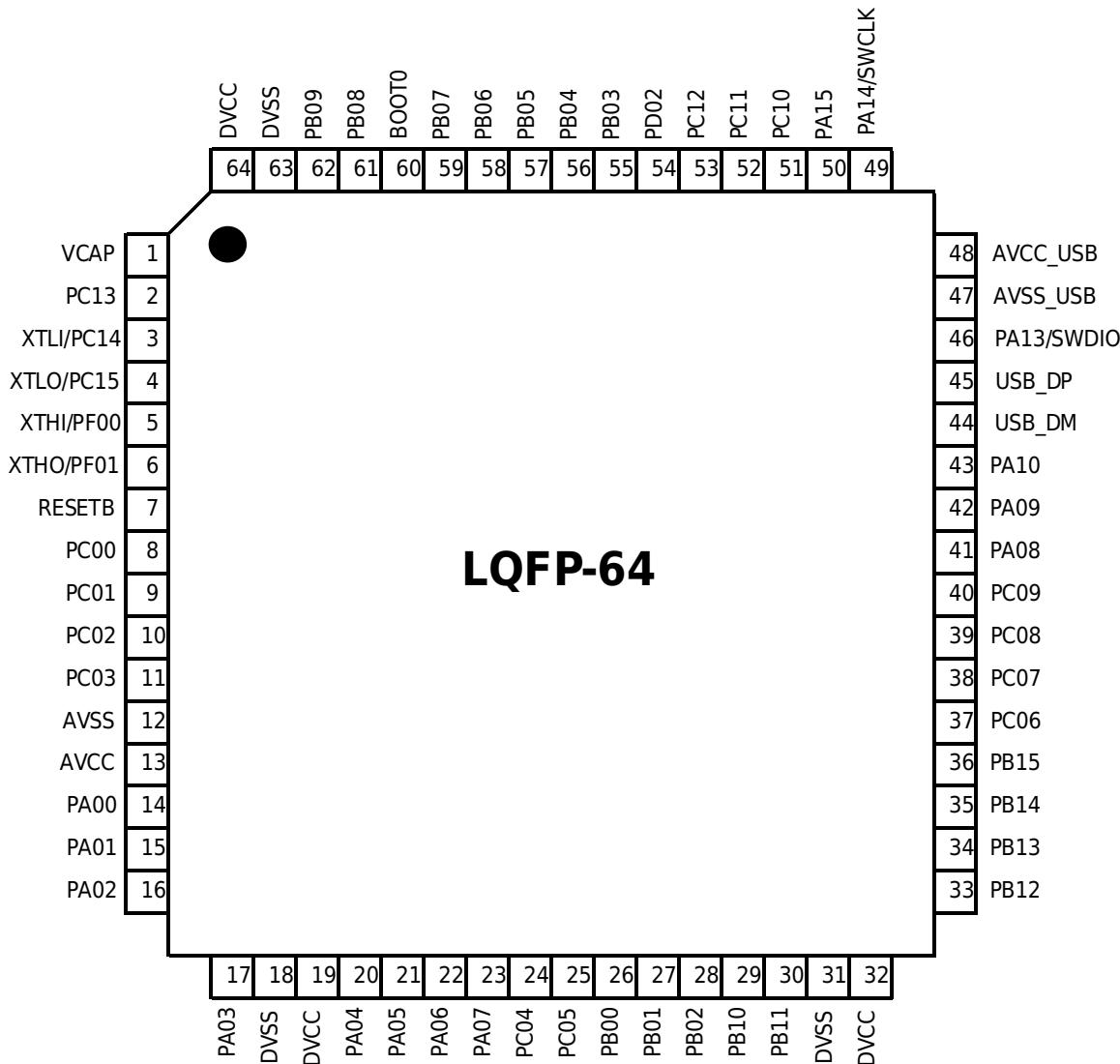
Notes:

- In the application, it is necessary to set the unlead pin of this package as input and enable pull-up.
- For details about the pin that is not brought out in this package, please refer to [Pin Function Description].
- BOOT0 pin is used to control the MCU programming, see [Module Signal Description] for details.

HC32L073PATA



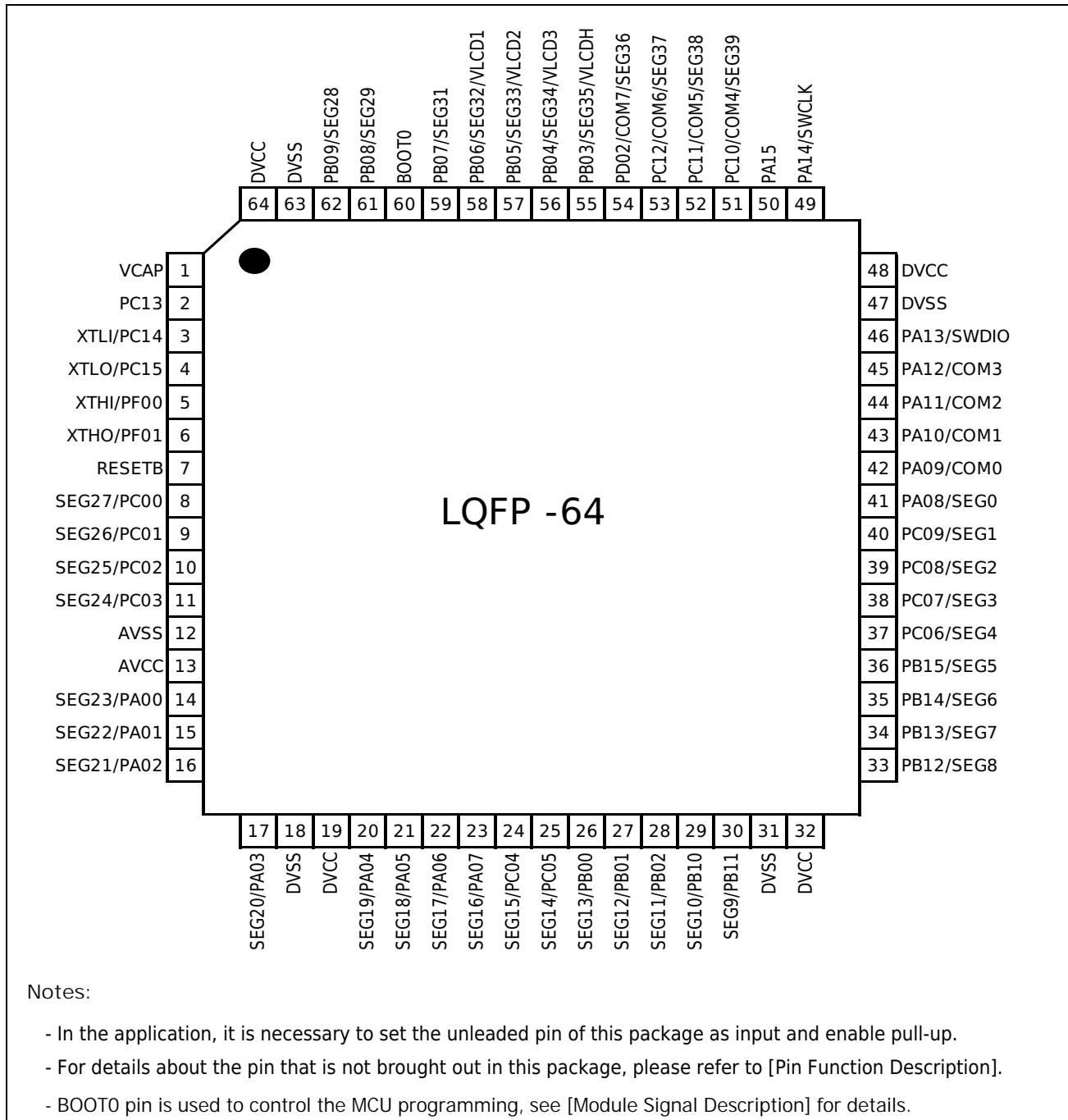
HC32L072KATA



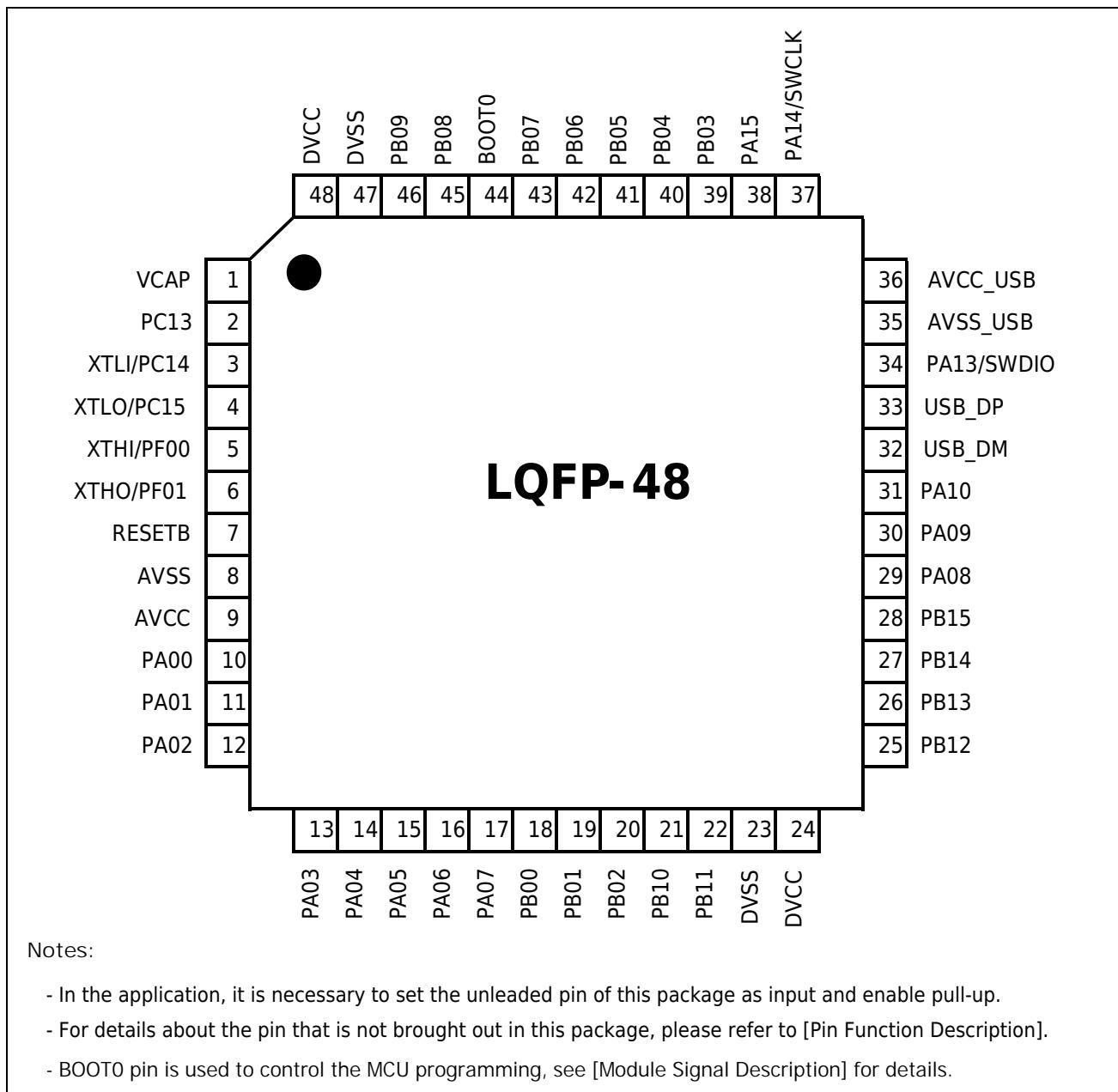
Notes:

- In the application, it is necessary to set the unlead pin of this package as input and enable pull-up.
 - For details about the pin that is not brought out in this package, please refer to [Pin Function Description].
 - BOOT0 pin is used to control the MCU programming, see [Module Signal Description] for details.

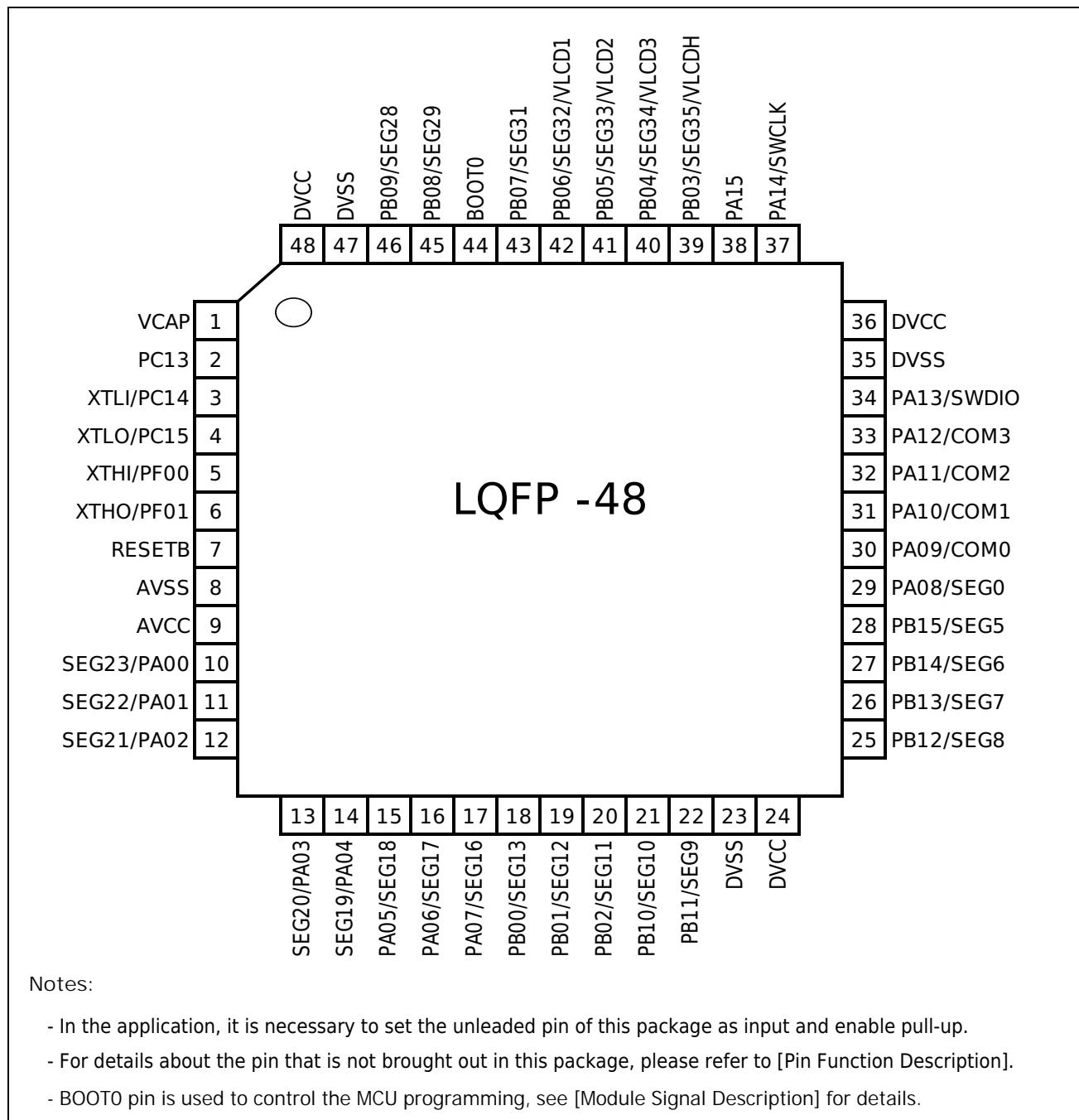
HC32L073KATA



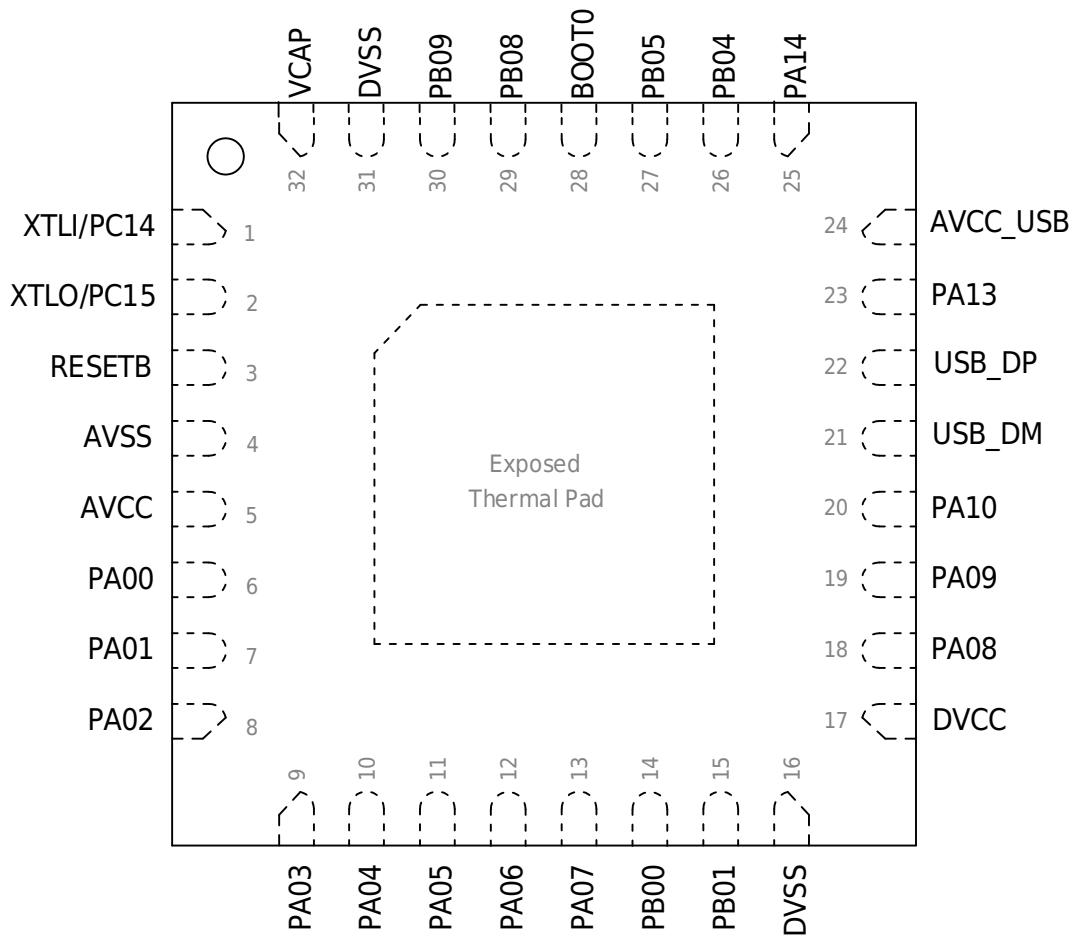
HC32L072JATA



HC32L073JATA



HC32L072FAUA



Notes:

- In the application, it is necessary to set the unlead pin of this package as input and enable pull-up.
- For details about the pin that is not brought out in this package, please refer to [Pin Function Description].
- BOOT0 pin is used to control the MCU programming, see [Module Signal Description] for details.

Figure 3-1 Pin Configuration

3.2 Pin Function Description

| LQFP100 | LQFP64 | LQFP48 | QFN32 | NAME | DIGITAL | ANALOG |
|---------|--------|--------|-------|--------|---|---|
| 1 | | | | PE02 | PCA_ECI | |
| 2 | | | | PE03 | PCA_CH0 | |
| 3 | | | | PE04 | PCA_CH1 | |
| 4 | | | | PE05 | PCA_CH2 | |
| 5 | | | | PE06 | PCA_CH3 | |
| 6 | 1 | 1 | 32 | VCAP | | |
| 7 | 2 | 2 | | PC13 | RTC_1HZ TIM3_CH1B I2S0_SCK | LVD0 |
| 8 | 3 | 3 | 1 | PC14 | | XTLI |
| 9 | 4 | 4 | 2 | PC15 | | XTLO |
| 10 | | | | PF09 | TIM0_CHA | |
| 11 | | | | PF10 | TIM0_CHB | |
| 12 | 5 | 5 | | PF00 | I2C0_SDA CRS_SYNC UART1_TXD | XTHI |
| 13 | 6 | 6 | | PF01 | I2C0_SCL UART1_RXD | XTHO |
| 14 | 7 | 7 | 3 | RESETB | | |
| 15 | 8 | | | PC00 | LPTIMO_GATE PCNT_S0 UART1_CTS UART2_RTS I2S0_MCK | AIN10, VC0_INP0 VC1_INN0 SEG27 |
| 16 | 9 | | | PC01 | LPTIMO_TOG TIM5_CHB UART1_RTS PCNT_S0FO UART2_CTS I2S0_SD | AIN11 VC0_INP1 VC1_INN1 SEG26 |
| 17 | 10 | | | PC02 | SPI1_MISO LPTIMO_TOGN PCNT_S1 UART2_RXD | AIN12, VC0_INP2 VC1_INN2 SEG25 |
| 18 | 11 | | | PC03 | SPI1_MOSI LPTIMO_EXT LPTIMO_TOGN PCNT_S1FO UART2_TXD | AIN13 VC0_INP3 VC1_INN3 SEG24 |
| 19 | | | | PF02 | | |
| 20 | 12 | 8 | 4 | AVSS | | |
| 21 | 13 | 9 | 5 | AVCC | | |
| 22 | | | | PF03 | | |
| 23 | 14 | 10 | 6 | PA00 | UART1_CTS LPUART1_RXD TIM0_ETR VC0_OUT TIM1_CHA TIM3_ETR TIM0_CHA | AIN0 VC0_INP4 VC0_INN0 VC1_INP0 VC1_INN4 SEG23 |

| LQFP100 | LQFP64 | LQFP48 | QFN32 | NAME | DIGITAL | ANALOG |
|---------|--------|--------|-------|------|---|--|
| 24 | 15 | 11 | 7 | PA01 | UART1_RTS LPUART1_RXD TIM0_CHB TIM1_ETR TIM1_CHB HCLK_OUT SPI1_MOSI | AIN1 VC0_INP5 VC0_INN1 VC1_INP1 VC1_INN5 SEG22 |
| 25 | 16 | 12 | 8 | PA02 | UART1_TXD TIM0_CHA VC1_OUT TIM1_CHA TIM2_CHA PCLK_OUT SPI1_MISO | AIN2 VC0_INP6 VC0_INN2 VC1_INP2 SEG21 |
| 26 | 17 | 13 | 9 | PA03 | UART1_RXD TIM0_GATE TIM1_CHB TIM2_CHB SPI1_CS TIM3_CH1A TIM5_CHA | AIN3 VC0_INP7 VC0_INN3 VC1_INP3 SEG20 |
| 27 | 18 | | | DVSS | | |
| 28 | 19 | | | DVCC | | |
| | | | | PF04 | | |
| | | | | PF05 | | |
| 29 | 20 | 14 | 10 | PA04 | SPI0_CS UART1_TXD PCA_CH4 TIM2_ETR TIM5_CHA LVD_OUT TIM3_CH2B | AIN4 VC0_INP8 VC0_INN4 VC1_INP4 OP3_OUT DAC0_OUT SEG19 |
| 30 | 21 | 15 | 11 | PA05 | SPI0_SCK TIM0_ETR PCA_ECI TIM0_CHA TIM5_CHB XTL_OUT XTH_OUT | AIN5 VC0_INP9 VC0_INN5 VC1_INP5 VC2_INP0 VC2_INN0 OP4_OUT DAC1_OUT SEG18 |
| 31 | 22 | 16 | 12 | PA06 | SPI0_MISO PCA_CH0 TIM3_BK TIM1_CHA VC0_OUT TIM3_GATE LPUART0_CTS | AIN6 VC0_INP10 VC0_INN6 OP4_INN SEG17 |
| 32 | 23 | 17 | 13 | PA07 | SPI0_MOSI PCA_CH1 HCLK_OUT TIM3_CH0B TIM2_CHA VC1_OUT TIM4_CHB | AIN7 VC0_INP11 VC0_INN7 OP4_INP SEG16 |
| 33 | 24 | | | PC04 | LPUART0_RXD TIM2_ETR IR_OUT VC2_OUT I2SO_WS | AIN14 VC0_INN8 SEG15 |

| LQFP100 | LQFP64 | LQFP48 | QFN32 | NAME | DIGITAL | ANALOG |
|---------|--------|--------|-------|------|--|--|
| 34 | 25 | | | PC05 | LPUART0_RXD TIM6_CHB PCA_CH4 I2S0_SDIN | AIN15 VC0_INN9 OP3_INN SEG14 |
| 35 | 26 | 18 | 14 | PB00 | PCA_CH2 TIM3_CH1B LPUART0_TXD TIM5_CHB RCH_OUT RCL_OUT PLL_OUT | AIN8 VC1_INN6 OP3_INP SEG13 |
| 36 | 27 | 19 | 15 | PB01 | PCA_CH3 PCLK_OUT TIM3_CH2B TIM6_CHB LPUART0_RTS VC2_OUT TCLK_OUT | AIN9/EXVREF VC1_INP6 VC1_INN7 VC2_INP1 VC2_INN1 SEG12 |
| 37 | 28 | 20 | | PB02 | LPTIM0_TOG PCA_ECI LPUART1_TXD TIM4_CHA TIM1_BK TIM0_BK TIM2_BK | AIN16, VC1_INP7 VC1_INN8 OP2_INN SEG11 |
| 38 | | | | PE07 | TIM3_ETR LPTIM1_GATE | |
| 39 | | | | PE08 | TIM3_CH0B LPTIM1_EXT | OP2_OUT4 |
| 40 | | | | PE09 | TIM3_CH0A LPTIM1_TOG | VC2_INP2 OP2_OUT3 |
| 41 | | | | PE10 | TIM3_CH1B LPTIM1_TOGN | VC2_INP3 OP2_OUT2 |
| 42 | | | | PE11 | TIM3_CH1A | VC2_INP4 VC2_INN2 OP2_OUT1 |
| 43 | | | | PE12 | TIM3_CH2B SPI0_CS UART3_CTS | OP1_OUT4 SEG51 |
| 44 | | | | PE13 | TIM3_CH2A SPI0_SCK UART3_RTS | VC2_INP5 OP1_OUT3 SEG50 |
| 45 | | | | PE14 | TIM3_CH0B SPI0_MISO UART3_RXD | VC2_INP6 OP1_OUT2 SEG49 |
| 46 | | | | PE15 | TIM3_BK SPI0_MOSI UART3_TXD | AIN23, VC2_INP7 VC2_INN3 OP1_OUT1 SEG48 |
| 47 | 29 | 21 | | PB10 | I2C1_SCL SPI1_SCK TIM1_CHA LPUART0_TXD TIM3_CH1A LPUART1_RTS UART1_RTS | AIN17, VC1_INP8 OP2_INP SEG10 |
| 48 | 30 | 22 | | PB11 | I2C1_SDA TIM1_CHB LPUART0_RXD TIM2_GATE TIM6_CHA | AIN18, VC2_INP8 VC2_INN4 OP2_OUT SEG9 |

| LQFP100 | LQFP64 | LQFP48 | QFN32 | NAME | DIGITAL | ANALOG |
|---------|--------|--------|-------|------|---|--|
| | | | | | LPUART1_CTS UART1_CTS | |
| 49 | 31 | 23 | 16 | DVSS | | |
| 50 | 32 | 24 | 17 | DVCC | | |
| 51 | 33 | 25 | | PB12 | SPI1_CS TIM3_BK LPUART0_RXD TIM0_BK LPUART0_RTS TIM6_CHA | AIN19 VC1_INP9 OP1_INN SEG8 |
| 52 | 34 | 26 | | PB13 | SPI1_SCK I2C1_SCL TIM3_CH0B LPUART0_CTS TIM1_CHA TIM1_GATE TIM6_CHB | AIN20 VC1_INP10 OP1_INP SEG7 |
| 53 | 35 | 27 | | PB14 | SPI1_MISO I2C1_SDA TIM3_CH1B TIM0_CHA RTC_1HZ LPUART0_RTS TIM1_BK | AIN21, VC1_INP11 VC2_INP9 VC2_INN5 OP1_OUT SEG6 |
| 54 | 36 | 28 | | PB15 | SPI1_MOSI TIM3_CH2B TIM0_CHB TIM0_GATE LPUART1_RXD | AIN22, OP0_INN SEG5 |
| 55 | | | | PD08 | LPUART0_RXD I2S0_SCK | OP0_OUT4 SEG47 |
| 56 | | | | PD09 | LPUART0_RXD I2S0_MCK | VC2_INP10 OP0_OUT3 SEG46 |
| 57 | | | | PD10 | LPUART0_RXD I2S0_SD | VC2_INP11 VC2_INN6 OP0_OUT2 SEG45 |
| 58 | | | | PD11 | LPUART0_CTS I2S0_WS | VC2_INP12 VC2_INN7 OP0_OUT1 SEG44 |
| 59 | | | | PD12 | LPUART0_RTS UART2_RTS | SEG43 |
| 60 | | | | PD13 | UART2_RXD I2S0_SDIN | SEG42 |
| 61 | | | | PD14 | UART2_TXD | SEG41 |
| 62 | | | | PD15 | CRS_SYNC UART2_CTS | SEG40 |
| 63 | 37 | | | PC06 | PCA_CH0 TIM4_CHA TIM2_CHA LPTIM1_GATE UART3_RXD I2S1_SCK | OP0_INP SEG4 |
| 64 | 38 | | | PC07 | PCA_CH1 TIM5_CHA TIM2_CHB LPTIM1_EXT UART3_RXD I2S1_MCK | VC2_INP13 VC2_INN8 OP0_OUT SEG3 |

| LQFP100 | LQFP64 | LQFP48 | QFN32 | NAME | DIGITAL | ANALOG |
|---------|--------------|--------------|-------|-------|--|--------|
| 65 | 39 | | | PC08 | PCA_CH2 TIM6_CHA TIM2_ETR LPTIM1_TOG UART3_CTS I2S1_SD | SEG2 |
| 66 | 40 | | | PC09 | PCA_CH3 TIM4_CHB TIM1_ETR LPTIM1_TOGN UART3_RTS I2S1_WS | SEG1 |
| 67 | 41 | 29 | 18 | PA08 | UART0_RXD TIM3_CH0A CRS_SYNC CAN_STBY TIM1_GATE TIM4_CHA TIM3_BK | SEG0 |
| 68 | 42 | 30 | 19 | PA09 | UART0_RXD TIM3_CH1A TIM0_BK I2C0_SCL HCLK_OUT TIM5_CHA | COM0 |
| 69 | 43 | 31 | 20 | PA10 | UART0_RXD TIM3_CH2A TIM2_BK I2C0_SDA TIM2_GATE PCLK_OUT TIM6_CHA | COM1 |
| | 44 (L073) | 32 (L073) | | PA11 | UART0_CTS TIM3_GATE I2C1_SCL CAN_RX VC0_OUT SPI0_MISO TIM4_CHB | COM2 |
| | 45 (L073) | 33 (L073) | | PA12 | UART0_RTS TIM3_ETR I2C1_SDA CAN_TX VC1_OUT SPI0_MOSI PCNT_SO | COM3 |
| 70 | 44 (L072) | 32 (L072) | 21 | USBDM | | |
| 71 | 45 (L072) | 33 (L072) | 22 | USBDP | | |
| 72 | 46 | 34 | 23 | PA13 | IR_OUT UART0_RXD LVD_OUT TIM3_ETR RTC_1HZ PCNT_S1 VC2_OUT | SWDIO |
| 73 | | | | PF06 | I2C1_SCL LPUART1_CTS UART0_CTS | COM2 |
| | | | | PF07 | I2C1_SDA LPUART1_RTS UART0_RTS | |
| | 47 (L073) | 35 (L073) | | DVSS | | |

| LQFP100 | LQFP64 | LQFP48 | QFN32 | NAME | DIGITAL | ANALOG |
|---------|-----------|-----------|-------|----------|---|---------------------------------------|
| | 48 (L073) | 36 (L073) | | DVCC | | |
| 74 | 47 (L072) | 35 (L072) | | AVSS_USB | | |
| 75 | 48 (L072) | 36 (L072) | 24 | AVCC_USB | | |
| 76 | 49 | 37 | 25 | PA14 | UART1_TXD UART0_TXD TIM3_CH2A LVD_OUT RCH_OUT RCL_OUT PLL_OUT | SWCLK |
| 77 | 50 | 38 | | PA15 | SPI0_CS UART1_RXD LPUART1_RTS TIM0_ETR TIM0_CHA TIM3_CH1A | COM3 |
| 78 | 51 | | | PC10 | LPUART1_RXD LPUART0_RXD PCA_CH2 | COM4/ SEG39 |
| 79 | 52 | | | PC11 | LPUART1_RXD LPUART0_RXD PCA_CH3 PCNT_SOFO | COM5/ SEG38 |
| 80 | 53 | | | PC12 | LPUART0_RXD LPUART1_RXD PCA_CH4 PCNT_S1FO | COM6/ SEG37 |
| 81 | | | | PD00 | CAN_RX SPI1_CS | |
| 82 | | | | PD01 | CAN_TX SPI1_SCK | |
| 83 | 54 | | | PD02 | PCA_ECI LPUART0_RTS TIM1_ETR | COM7/ SEG36 |
| 84 | | | | PD03 | UART1_CTS SPI1_MISO LPTIM1_TOG I2S1_SCK | |
| 85 | | | | PD04 | UART1_RTS SPI1_MOSI LPTIM1_TOGN I2S1_MCK | |
| 86 | | | | PD05 | UART1_RXD LPTIM1_GATE CAN_STBY I2S1_SD | |
| 87 | | | | PD06 | UART1_RXD LPTIM1_EXT I2S1_WS | |
| 88 | | | | PD07 | UART1_RXD I2S1_SDIN | |
| 89 | 55 | 39 | | PB03 | SPI0_SCK TIM0_CHB TIM1_GATE TIM3_CH0A LPTIM0_GATE XTL_OUT XTH_OUT | VC1_INN9 SEG35/VLCDH |
| 90 | 56 | 40 | 26 | PB04 | SPI0_MISO PCA_CH0 TIM2_BK | VC0_INP12 VC1_INP12 SEG34/VLCD3 |

| LQFP100 | LQFP64 | LQFP48 | QFN32 | NAME | DIGITAL | ANALOG |
|---------|--------|--------|-------|------------|--|--|
| | | | | | UART0_CTS TIM2_GATE TIM3_CH0B LPTIM0_EXT | |
| 91 | 57 | 41 | 27 | PB05 | SPI0_MOSI TIM1_BK PCA_CH1 LPTIM0_GATE PCNT_S0 UART0_RTS | VC0_INP13 SEG33/ VLCD2 |
| 92 | 58 | 42 | | PB06 | I2C0_SCL UART0_RXD TIM1_CHB TIM0_CHA LPTIM0_EXT TIM3_CH0A LPTIM0_TOG | VC0_INP14 VC1_INP14 SEG32/ VLCD1 |
| 93 | 59 | 43 | | PB07 | I2C0_SDA UART0_RXD TIM2_CHB LPUART1_CTS TIM0_CHB LPTIM0_TOGN PCNT_S1 | VC1_INP15 LVD2 SEG31 |
| 94 | 60 | 44 | 28 | BOOT0/PF11 | | SEG30 |
| 95 | 61 | 45 | 29 | PB08 | I2C0_SCL TIM1_CHA CAN_RX TIM2_CHA TIM0_GATE TIM3_CH2A UART0_RXD | LVD1 SEG29 |
| 96 | 62 | 46 | 30 | PB09 | I2C0_SDA IR_OUT SPI1_CS TIM2_CHA CAN_TX TIM2_CHB UART0_RXD | SEG28 |
| 97 | | | | PE00 | TIM1_CHA | |
| 98 | | | | PE01 | TIM2_CHA | |
| 99 | 63 | 47 | 31 | DVSS | | |
| 100 | 64 | 48 | | DVCC | | |

The digital function of each pin is controlled by the PSEL bit field, see the table below for details.

| PxSEL | | | | | | | |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| PA00 | UART1_CTS | LPUART1_TXD | TIM0_ETR | VC0_OUT | TIM1_CHA | TIM3_ETR | TIM0_CHA |
| PA01 | UART1 RTS | LPUART1_RXD | TIM0_CHB | TIM1_ETR | TIM1_CHB | HCLK_OUT | SPI1_MOSI |
| PA02 | UART1_TXD | TIM0_CHA | VC1_OUT | TIM1_CHA | TIM2_CHA | PCLK_OUT | SPI1_MISO |
| PA03 | UART1_RXD | TIM0_GATE | TIM1_CHB | TIM2_CHB | SPI1_CS | TIM3_CH1A | TIM5_CHA |
| PA04 | SPI0_CS | UART1_TXD | PCA_CH4 | TIM2_ETR | TIM5_CHA | LVD_OUT | TIM3_CH2B |
| PA05 | SPI0_SCK | TIM0_ETR | PCA_ECI | TIM0_CHA | TIM5_CHB | XTL_OUT | XTH_OUT |
| PA06 | SPI0_MISO | PCA_CH0 | TIM3_BK | TIM1_CHA | VC0_OUT | TIM3_GATE | LPUART0_CTS |
| PA07 | SPI0_MOSI | PCA_CH1 | HCLK_OUT | TIM3_CH0B | TIM2_CHA | VC1_OUT | TIM4_CHB |
| PA08 | UART0_TXD | TIM3_CH0A | CRS_SYNC | CAN_STBY | TIM1_GATE | TIM4_CHA | TIM3_BK |
| PA09 | UART0_TXD | TIM3_CH1A | TIM0_BK | I2C0_SCL | | HCLK_OUT | TIM5_CHA |
| PA10 | UART0_RXD | TIM3_CH2A | TIM2_BK | I2C0_SDA | TIM2_GATE | PCLK_OUT | TIM6_CHA |
| PA11 | UART0_CTS | TIM3_GATE | I2C1_SCL | CAN_RX | VC0_OUT | SPI0_MISO | TIM4_CHB |
| PA12 | UART0_RTS | TIM3_ETR | I2C1_SDA | CAN_TX | VC1_OUT | SPI0_MOSI | PCNT_SO |
| PA13 | IR_OUT | UART0_RXD | LVD_OUT | TIM3_ETR | RTC_1HZ | PCNT_S1 | VC2_OUT |
| PA14 | UART1_TXD | UART0_TXD | TIM3_CH2A | LVD_OUT | RCH_OUT | RCL_OUT | PLL_OUT |
| PA15 | SPI0_CS | UART1_RXD | LPUART1_RTS | TIM0_ETR | TIM0_CHA | TIM3_CH1A | |
| PB00 | PCA_CH2 | TIM3_CH1B | LPUART0_TXD | TIM5_CHB | RCH_OUT | RCL_OUT | PLL_OUT |
| PB01 | PCA_CH3 | PCLK_OUT | TIM3_CH2B | TIM6_CHB | LPUART0_RTS | VC2_OUT | TCLK_OUT |
| PB02 | LPTIMO_TOG | PCA_ECI | LPUART1_TXD | TIM4_CHA | TIM1_BK | TIM0_BK | TIM2_BK |
| PB03 | SPI0_SCK | TIM0_CHB | TIM1_GATE | TIM3_CH0A | LPTIMO_GATE | XTL_OUT | XTH_OUT |
| PB04 | SPI0_MISO | PCA_CH0 | TIM2_BK | UART0_CTS | TIM2_GATE | TIM3_CH0B | LPTIMO_EXT |
| PB05 | SPI0_MOSI | | TIM1_BK | PCA_CH1 | LPTIMO_GATE | PCNT_SO | UART0_RTS |
| PB06 | I2C0_SCL | UART0_TXD | TIM1_CHB | TIM0_CHA | LPTIMO_EXT | TIM3_CH0A | LPTIMO_TOG |
| PB07 | I2C0_SDA | UART0_RXD | TIM2_CHB | LPUART1_CTS | TIM0_CHB | LPTIMO_TOGN | PCNT_S1 |
| PB08 | I2C0_SCL | TIM1_CHA | CAN_RX | TIM2_CHA | TIM0_GATE | TIM3_CH2A | UART0_TXD |
| PB09 | I2C0_SDA | IR_OUT | SPI1_CS | TIM2_CHA | CAN_TX | TIM2_CHB | UART0_RXD |
| PB10 | I2C1_SCL | SPI1_SCK | TIM1_CHA | LPUART0_TXD | TIM3_CH1A | LPUART1_RTS | UART1_RTS |
| PB11 | I2C1_SDA | TIM1_CHB | LPUART0_RXD | TIM2_GATE | TIM6_CHA | LPUART1_CTS | UART1_CTS |
| PB12 | SPI1_CS | TIM3_BK | LPUART0_TXD | TIM0_BK | | LPUART0_RTS | TIM6_CHA |
| PB13 | SPI1_SCK | I2C1_SCL | TIM3_CH0B | LPUART0_CTS | TIM1_CHA | TIM1_GATE | TIM6_CHB |
| PB14 | SPI1_MISO | I2C1_SDA | TIM3_CH1B | TIM0_CHA | RTC_1HZ | LPUART0_RTS | TIM1_BK |
| PB15 | SPI1_MOSI | TIM3_CH2B | TIM0_CHB | TIM0_GATE | | | LPUART1_RXD |
| PC00 | LPTIMO_GATE | PCNT_SO | UART1_CTS | UART2_RTS | I2S0_MCK | | |
| PC01 | LPTIMO_TOG | TIM5_CHB | UART1_RTS | PCNT_S0FO | I2S0_SD | UART2_CTS | |
| PC02 | SPI1_MISO | LPTIMO_TOGN | PCNT_S1 | UART2_RXD | | | |
| PC03 | SPI1_MOSI | LPTIMO_EXT | LPTIMO_TOGN | PCNT_S1FO | UART2_TXD | | |

| PxSEL | | | | | | | |
|-------|-------------|-------------|-------------|-------------|-----------|-----------|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| PC04 | LPUART0_TXD | TIM2_ETR | IR_OUT | VC2_OUT | I2S0_WS | | |
| PC05 | LPUART0_RXD | TIM6_CHB | PCA_CH4 | | I2S0_SDIN | | |
| PC06 | PCA_CH0 | TIM4_CHA | TIM2_CHA | LPTIM1_GATE | I2S1_SCK | UART3_RXD | |
| PC07 | PCA_CH1 | TIM5_CHA | TIM2_CHB | LPTIM1_EXT | I2S1_MCK | UART3_TXD | |
| PC08 | PCA_CH2 | TIM6_CHA | TIM2_ETR | LPTIM1_TOG | I2S1_SD | UART3_CTS | |
| PC09 | PCA_CH3 | TIM4_CHB | TIM1_ETR | LPTIM1_TOGN | I2S1_WS | UART3_RTS | |
| PC10 | LPUART1_TXD | LPUART0_RXD | PCA_CH2 | | | | |
| PC11 | LPUART1_RXD | LPUART0_RXD | PCA_CH3 | PCNT_S0FO | | | |
| PC12 | LPUART0_RXD | LPUART1_RXD | PCA_CH4 | PCNT_S1FO | | | |
| PC13 | | RTC_1HZ | TIM3_CH1B | | I2S0_SCK | | |
| PC14 | | | | | | | |
| PC15 | | | | | | | |
| PD00 | CAN_RX | SPI1_CS | | | | | |
| PD01 | CAN_TX | SPI1_SCK | | | | | |
| PD02 | PCA_ECI | LPUART0_RTS | TIM1_ETR | | | | |
| PD03 | UART1_CTS | SPI1_MISO | LPTIM1_TOG | I2S1_SCK | | | |
| PD04 | UART1_RTS | SPI1_MOSI | LPTIM1_TOGN | I2S1_MCK | | | |
| PD05 | UART1_RXD | LPTIM1_GATE | CAN_STBY | I2S1_SD | | | |
| PD06 | UART1_RXD | LPTIM1_EXT | | I2S1_WS | | | |
| PD07 | UART1_RXD | | | I2S1_SDIN | | | |
| PD08 | LPUART0_RXD | I2S0_SCK | | | | | |
| PD09 | LPUART0_RXD | I2S0_MCK | | | | | |
| PD10 | LPUART0_RXD | I2S0_SD | | | | | |
| PD11 | LPUART0_CTS | I2S0_WS | | | | | |
| PD12 | LPUART0_RTS | UART2_RTS | | | | | |
| PD13 | UART2_RXD | I2S0_SDIN | | | | | |
| PD14 | UART2_RXD | | | | | | |
| PD15 | CRS_SYNC | UART2_CTS | | | | | |
| PE00 | TIM1_CHA | | | | | | |
| PE01 | TIM2_CHA | | | | | | |
| PE02 | PCA_ECI | | | | | | |
| PE03 | PCA_CH0 | | | | | | |
| PE04 | PCA_CH1 | | | | | | |
| PE05 | PCA_CH2 | | | | | | |
| PE06 | PCA_CH3 | | | | | | |
| PE07 | TIM3_ETR | LPTIM1_GATE | | | | | |
| PE08 | TIM3_CH0B | LPTIM1_EXT | | | | | |

| PxSEL | | | | | | | |
|----------|-----------|-------------|-----------|----------|----------|----------|----------|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| PE09 | TIM3_CH0A | LPTIM1_TOG | | | | | |
| PE10 | TIM3_CH1B | LPTIM1_TOGN | | | | | |
| PE11 | TIM3_CH1A | | | | | | |
| PE12 | TIM3_CH2B | SPI0_CS | UART3_CTS | | | | |
| PE13 | TIM3_CH2A | SPI0_SCK | UART3_RTS | | | | |
| PE14 | TIM3_CH0B | SPI0_MISO | UART3_RXD | | | | |
| PE15 | TIM3_BK | SPI0_MOSI | UART3_TXD | | | | |
| PF00 | I2C0_SDA | CRS_SYNC | UART1_TXD | | | | |
| PF01 | I2C0_SCL | | UART1_RXD | | | | |
| PF02 | | | | | | | |
| PF03 | | | | | | | |
| PF04 | | | | | | | |
| PF05 | | | | | | | |
| PF06 | I2C1_SCL | LPUART1_CTS | UART0_CTS | | | | |
| PF07 | I2C1_SDA | LPUART1_RTS | UART0_RTS | | | | |
| PF09 | TIM0_CHA | | | | | | |
| PF10 | TIM0_CHB | | | | | | |
| PF11 | | | | | | | |

3.3 Module signal description

Table 3-1 Module signal description

| Module | Pin Name | Description |
|---|---------------|---|
| Power supply | DVCC | Digital power supply |
| | AVCC | Analog power supply |
| | DVSS | Digital ground |
| | AVSS | Analog ground |
| | AVCC_USB | USB module power supply (not more than 3.6V, see [Electrical Characteristics] for details) |
| | AVSS_USB | USB module ground |
| | VCAP | LDO core power supply output (for internal circuit use only, external decoupling capacitor of not less than 1uF is required) |
| ISP | BOOT0 | When reset, the BOOT0 (PF11) pin is high, the chip works in ISP programming mode, and the FLASH can be programmed through the ISP protocol. When reset, the BOOT0 (PF11) pin is low, the chip works in user mode, the chip executes the program code in the FLASH, and the FLASH can be programmed through the SWD protocol. |
| ADC | AIN0~AIN35 | AIN0~AIN35 ADC input channel 0~35 |
| | ADC_VREF | ADC external reference voltage |
| VC | VCIN0~VCIN15 | VC input 0~15 |
| | VC0_OUT | VC0 comparison output |
| | VC1_OUT | VC1 comparison output |
| | VC2_OUT | VC2 comparison output |
| LVD | LVDIN0 | Voltage detection input 0 |
| | LVDIN1 | Voltage detection input 1 |
| | LVDIN2 | Voltage detection input 2 |
| | LVD_OUT | Voltage detection output |
| OPA $x=0,1,2,3,4$ | OPx_INN | OPA negative input |
| | OPx_INP | OPA positive input |
| | OPx_OUTy | OPA output |
| LCD $x=0~7$ $y=0-52$ $z=1,2,3,H$ | COMx | LCD common output |
| | SEGY VLCDZ | LCD segment output External resistor mode, external capacitor mode use pins |
| UART $x=0,1,2,3$ | UARTx_TXD | UARTx data transmitter |
| | UARTx_RXD | UARTx data receiver |
| | UARTx_CTS | UARTx CTS |
| | UARTx_RTS | UARTx RTS |
| LPUART $x=0,1$ | LPUARTx_TXD | LPUART data transmitter |
| | LPUARTx_RXD | LPUART data receiver |
| | LPUARTx_CTS | LPUART CTS |
| | LPUARTx_RTS | LPUART RTS |

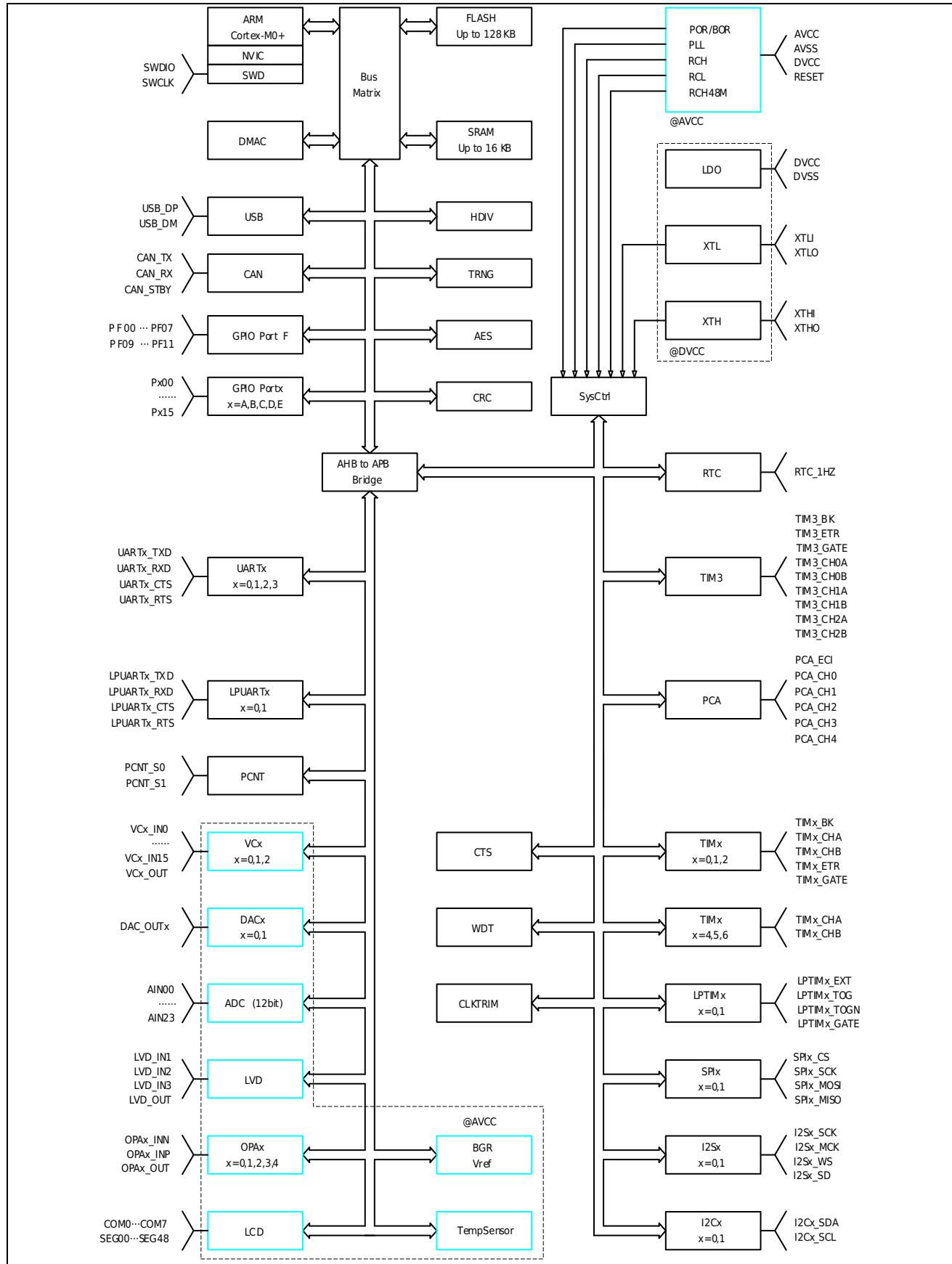
| Module | Pin Name | Description |
|--|-------------|--|
| I2Sx x=0,1 | I2Sx_CK | I2Sx_CK I2S module clock signal |
| | I2Sx_WS | I2Sx_WS I2S module word select signal |
| | I2Sx_MCK | I2Sx_MCK I2S module master mode clock output |
| | I2Sx_SD | I2Sx_SD I2S module data input and output |
| USB | USB_DP | USB data signal |
| | USB_DM | USB data signal |
| CAN | CAN_TX | CAN TX output signal |
| | CAN_RX | CAN RX input signal |
| | CAN_STBY | CAN STBY signal |
| CTS | CTS_SYNC | CTS external synchronization signal |
| SPI x=0,1 | SPIx_MISO | SPI module master input slave output data signal |
| | SPIx_MOSI | SPI module master output slave input data signal |
| | SPIx_SCK | SPI module clock signal |
| | SPIx_CS | SPI chip select |
| I2C x=0,1 | I2Cx_SDA | I2C module data signal |
| | I2Cx_SCL | I2C module clock signal |
| General purpose timer TIMx x=0,1,2 | TIMx_CHA | Timer capture input compare output A |
| | TIMx_CHB | Timer capture input compare output B |
| | TIMx_ETR | Timer external count input signal |
| | TIMx_GATE | Timer gate signal |
| General purpose timer TIM3 y=0,1,2 | TIM3_CHyA | Timer capture input compare output A |
| | TIM3_CHyB | Timer capture input compare output B |
| | TIM3_ETR | Timer external count input signal |
| | TIM3_GATE | Timer gate signal |
| Low Power Timer LPTIMx x=0,1 | LPTIMx_TOG | The toggle output signal of LPTimer |
| | LPTIMx_TOGN | The toggle output inverse signal of LPTimer |
| | LPTIMx_EXT | The external count input signal of LPTimer |
| | LPTIMx_GATE | The gate signal of LPTimer |
| Programmable Counter Array (PCA) | PCA_ECI | External clock input signal |
| | PCA_CH0 | Capture input/compare output/PWM output 0 |
| | PCA_CH1 | Capture input/compare output/PWM output 1 |
| | PCA_CH2 | Capture input/compare output/PWM output 2 |
| | PCA_CH3 | Capture input/compare output/PWM output 3 |
| | PCA_CH4 | Capture input/compare output/PWM output 4 |
| PCNT | PCNT_S0 | PCNT Pulse count input 0 |
| | PCNT_S1 | PCNT Pulse count input 1 |
| Advanced Timer | TIM4_CHA | Advanced Timer4 compare output/capture input A |
| | TIM4_CHB | Advanced Timer4 compare output/capture input B |

| Module | Pin Name | Description |
|--------|----------|--|
| | TIM5_CHA | Advanced Timer5 Compare Output/Capture Input A |
| | TIM5_CHB | Advanced Timer5 Compare Output/Capture Input B |
| | TIM6_CHA | Advanced Timer6 Compare Output/Capture Input A |
| | TIM6_CHB | Advanced Timer6 Compare Output/Capture Input B |

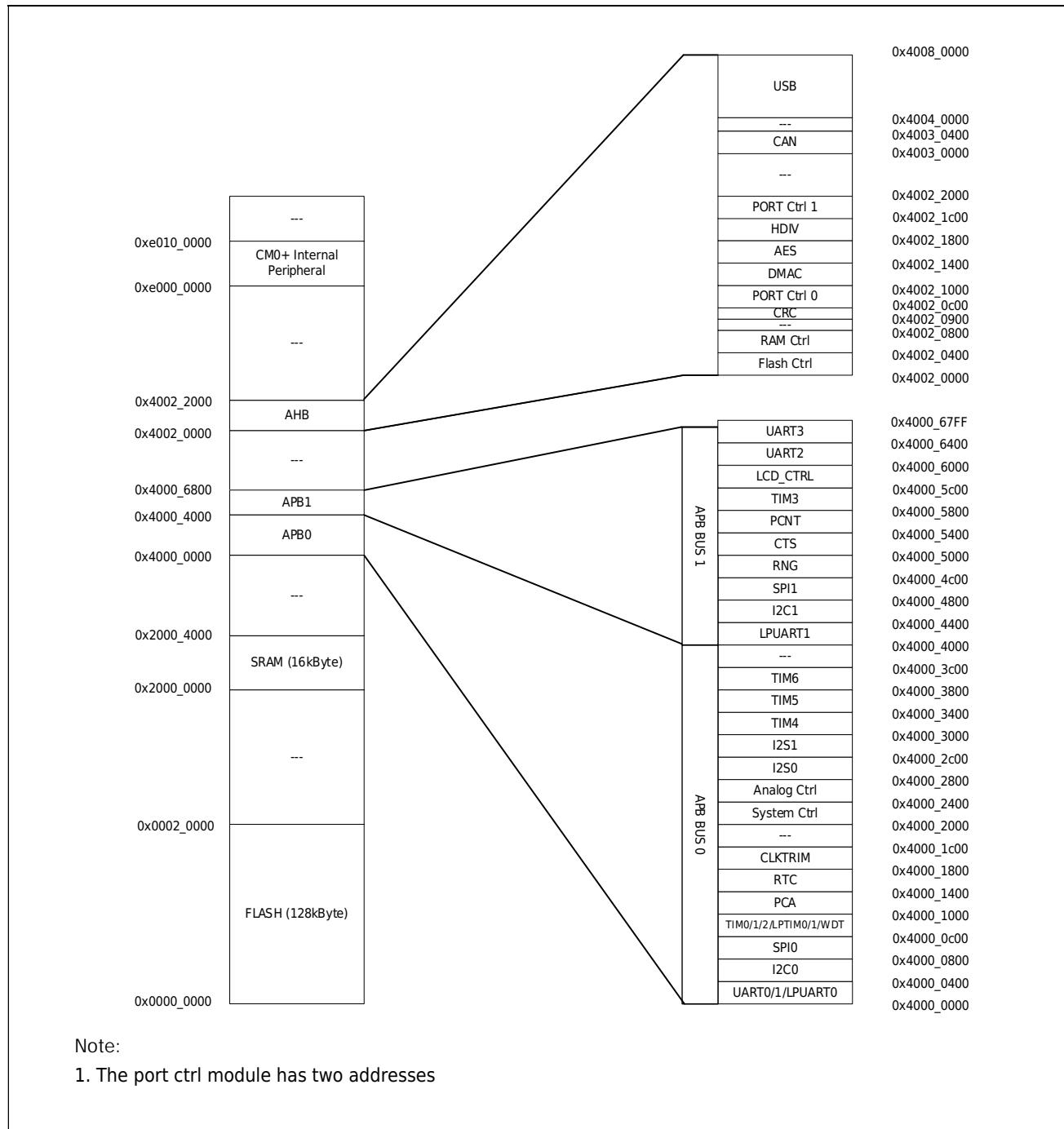
Note:

- The IO ports are reset to input high-impedance state, and the sleep mode and deep sleep mode retain the previous port status.

4 Functional Block Diagram

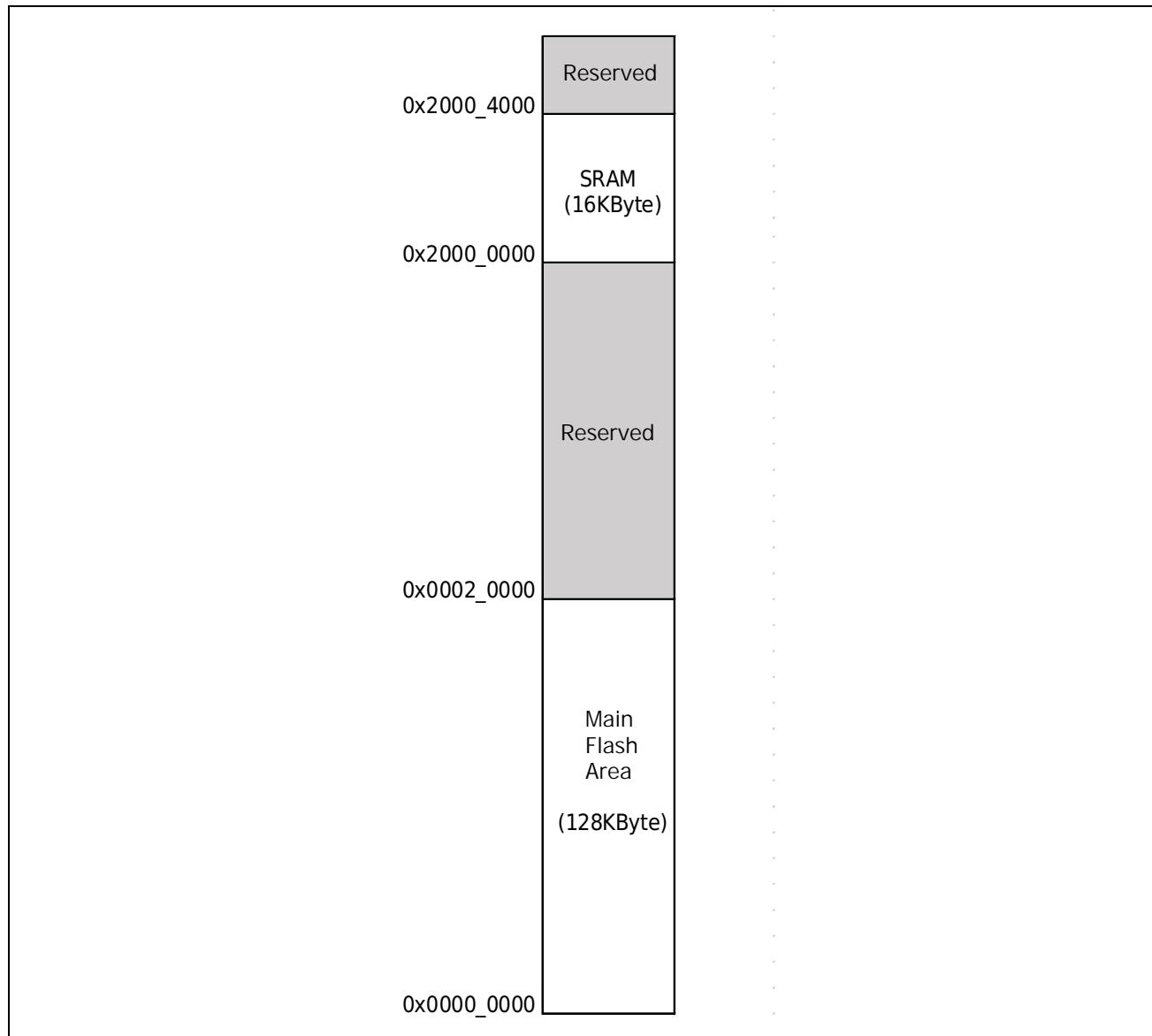


5 Memory Map

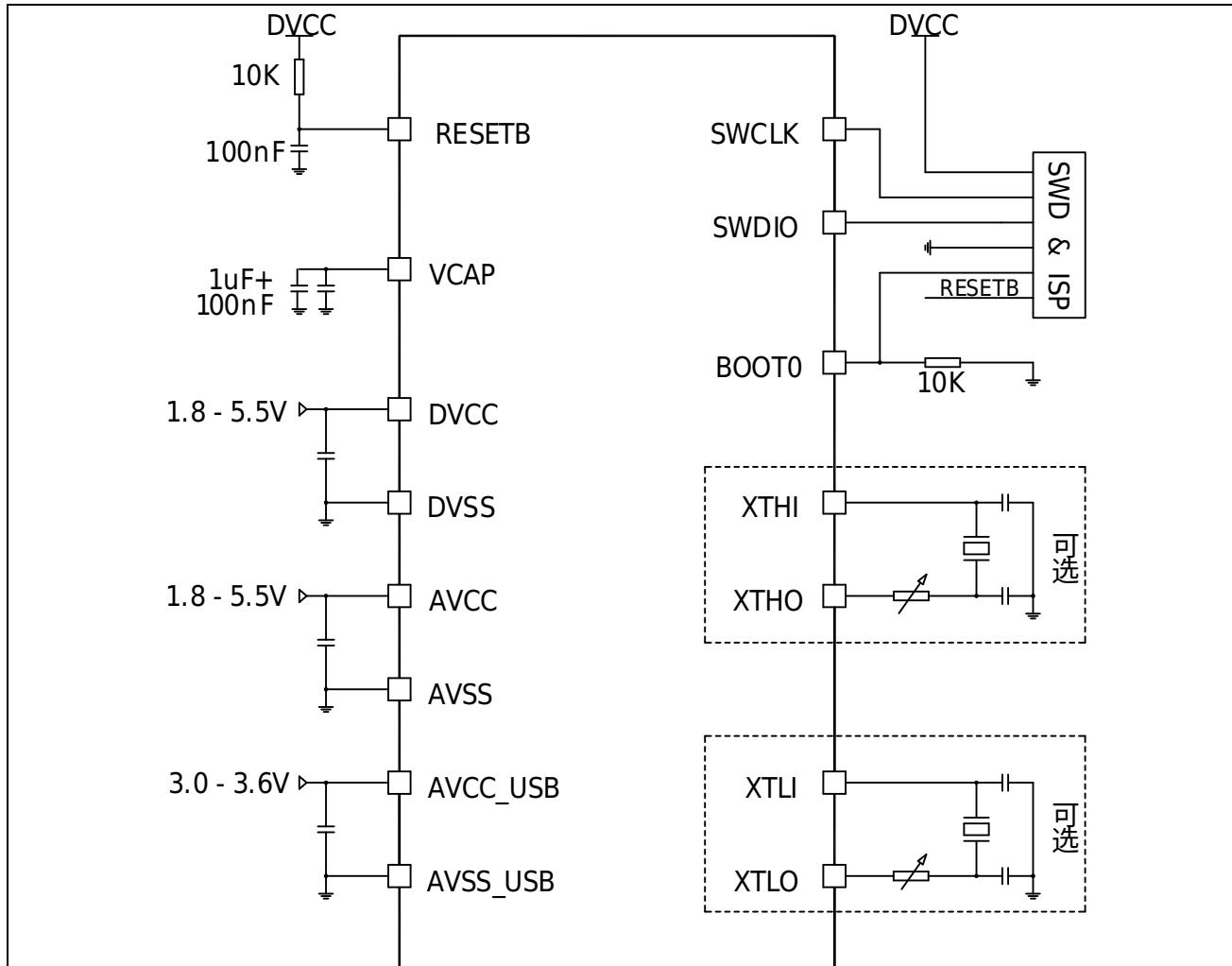


Note:

1. The port ctrl module has two addresses



6 Typical application circuit diagram



Notes:

- AVCC and DVCC voltages must be the same.
- When powering AVCC_USB, the voltages of AVCC and DVCC should not be less than AVCC_USB.
- When the USB function is not used, it is recommended that the AVCC_USB pin be left floating or grounded.
- Each power supply requires a decoupling capacitor, which should be placed as close to the corresponding power pin as possible.

7 Electrical characteristics

7.1 Test conditions

Unless otherwise specified, all voltages are referenced to VSS.

7.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values are guaranteed under the worst-case ambient temperature, supply voltage and clock frequency conditions by testing 100% of the products at ambient temperature $T_A=25^\circ\text{C}$ and $T_A=T_{\text{Amax}}$ (T_{Amax} matches the selected temperature range) on the production line.

The notes below each table indicate that the data are obtained through comprehensive evaluation, design simulation and/or process characteristics, and are not tested on the production line; based on comprehensive evaluation, the minimum and maximum values are obtained by taking the average value of the sample test and then adding or subtracting three times the standard distribution (average $\pm 3\Sigma$).

7.1.2 Typical values

Unless otherwise specified, typical data is based on $T_A = 25^\circ\text{C}$ and $VCC = 3.3\text{V}$ ($1.8\text{V} \leq VCC \leq 5.5\text{V}$ voltage range). These data are only for design guidance and are not tested.

The typical ADC accuracy value is obtained by sampling a standard batch and testing it under all temperature ranges. The error of 95% of the products is less than or equal to the given value (average $\pm 2\Sigma$).

7.2 Absolute Maximum Ratings

If the load applied to the device exceeds the value given in the "Absolute Maximum Ratings" table, it may cause permanent damage to the device. This is just the maximum load that can be tolerated, and it does not mean that the functional operation of the device is correct under this condition. The long-term operation of the device under the maximum value condition will affect the reliability of the device.

Table 7-1 Voltage characteristics

| Symbol | Description | Min | Max | Unit |
|-----------------------|---|---|-----------|------|
| VCC - VSS | External main supply voltage (including AVCC and DVCC) ⁽¹⁾ | -0.3 | 5.5 | V |
| AVCC_USB | USB module supply voltage ⁽²⁾ | 3.0 | 3.6 | V |
| V _{IN} | Input voltage on other pins ⁽³⁾ | VSS-0.3 | VCC + 0.3 | V |
| ΔVCCx | Voltage difference between different supply pins | | 50 | mV |
| VSSx - VSS | Voltage difference between different ground pins | | 50 | mV |
| V _{ESD(HBM)} | Electrostatic Discharge Voltage (Human Body Model) | Refer to Absolute Maximum Electrical Parameters | | V |

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to the power supply system within the external allowable range.
2. AVCC_USB cannot be higher than AVCC/DVCC 0.3V.
3. I_{INJ(PIN)} must never exceed its limit, that is, ensure that V_{IN} does not exceed its maximum value. If it is not possible to ensure that V_{IN} does not exceed its maximum value, it is also necessary to ensure that I_{INJ(PIN)} does not exceed its maximum value under external limits. When V_{IN}>V_C, there is a forward injection current; when V_{IN}<V_S, there is a reverse injection current.

Table 7-2 Current characteristics

| Symbol | Description | Max ⁽¹⁾ | Unit |
|--|--|--------------------|------|
| I _{VCC} | Total current through DVCC/AVCC power supply line (supply current) ⁽¹⁾ | 300 | mA |
| I _{VSS} | I _{VSS} Total current through VSS ground line (source current) ⁽¹⁾ | 300 | mA |
| I _{IO} | Output current sinking on any I/O and control pins | 25 | mA |
| | Output current sourcing on any I/O and control pins | -25 | mA |
| I _{INJ(PIN)} ^{(2) (3)} | Injection current at RESETB pin | +/-5 | mA |
| | Injection current at XTH1 pin of XTH and XTL1 pin of XTL | +/-5 | mA |
| | Injection current at other pins ⁽⁴⁾ | +/-5 | mA |
| ΣI _{INJ(PIN)} ⁽²⁾ | Total injection current at all I/O and control pins ⁽⁴⁾ | +/-25 | mA |

1. All power supply (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to the power supply system within the external allowable range.
2. I_{INJ(PIN)} must never exceed its limit, that is, ensure that V_{IN} does not exceed its maximum value. If it is not possible to ensure that V_{IN} does not exceed its maximum value, it is also necessary to ensure that I_{INJ(PIN)} does not exceed its maximum value externally. When V_{IN}>V_C, there is a forward injection current; when V_{IN}<V_S, there is a reverse injection current.
3. Reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of ΣI_{INJ(PIN)} is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum value of ΣI_{INJ(PIN)} on the 4 I/O ports of the device.

Table 7-3 Temperature Characteristics

| Symbol | Description | Value | Unit |
|------------------|------------------------------|-------------|------|
| T _{STG} | Storage temperature range | -65 ~ + 150 | °C |
| T _J | Maximum junction temperature | 105 | °C |

7.3 Operating conditions

7.3.1 General operating conditions

Table 7-4 General operating conditions

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---------------------|--------------------------------|--------------------------------------|----------|------|------|
| f _{HCLK} | Internal AHB clock frequency | | 0 | 48 | MHz |
| f _{PCLK0} | Internal APB0 clock frequency | | 0 | 48 | MHz |
| f _{PCLK1} | Internal APB1 clock frequency | | 0 | 48 | MHz |
| DVCC | Digital part operating voltage | AVCC_USB=0V | 1.8 | 5.5 | V |
| AVCC ⁽¹⁾ | Analog part operating voltage | | 1.8 | 5.5 | V |
| DVCC | Digital part operating voltage | AVCC_USB>3.0V | AVCC_USB | 5.5 | V |
| AVCC ⁽¹⁾ | Analog part operating voltage | | AVCC_USB | 5.5 | V |
| AVCC_USB | USB module supply voltage | | 3.0 | 3.6 | V |
| P _D | Power dissipation TA=85°C | LQFP100 | | 476 | mW |
| | Power dissipation TA=85°C | LQFP64 | | 455 | mW |
| | Power dissipation TA=85°C | LQFP48 | | 364 | mW |
| | Power dissipation TA=85°C | QFN32 | | 556 | mW |
| T _A | Ambient temperature | Maximum power consumption | -40 | 85 | °C |
| | | Low power consumption ⁽²⁾ | -40 | 105 | °C |
| T _J | Junction temperature range | | -40 | 105 | °C |

1. AVCC and DVCC voltages must be the same.

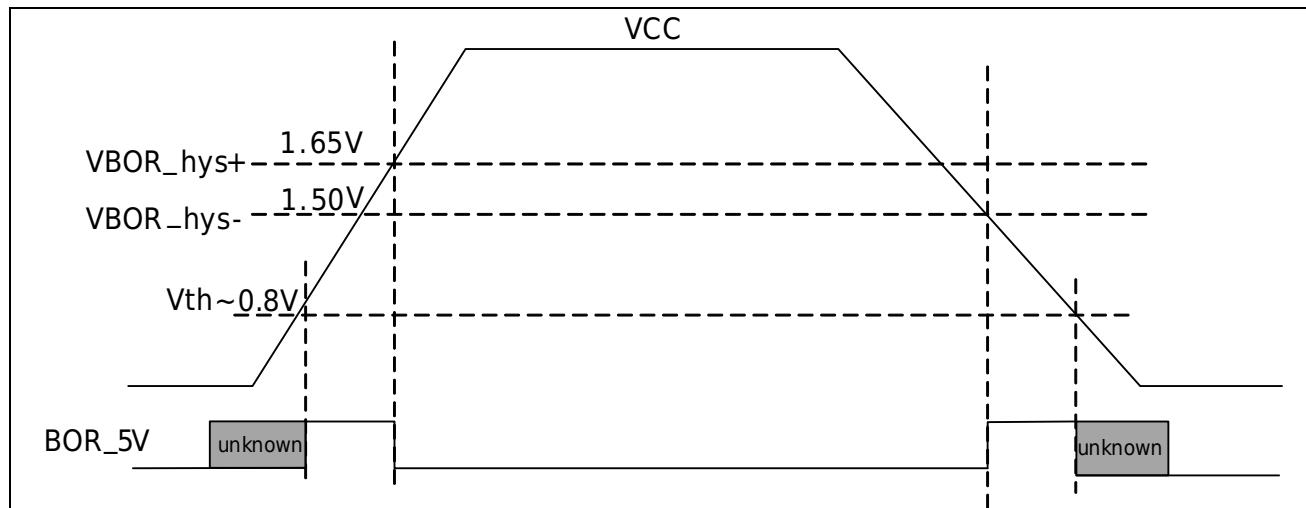
2. In the state of lower power dissipation, TA can be extended to this range as long as T_J does not exceed T_{Jmax}.

7.3.2 Operating conditions during power-on and power-off

Table 7-5 Power-on and power-off operating conditions

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|------------------|------------------|------------|------|------|------|
| t _{VCC} | VCC rising rate | | 0 | 5 | V/μs |
| t _{VCC} | VCC falling rate | | 10 | 5 | V/μs |

7.3.3 Embedded reset and LVD module features



1. Guaranteed by design, not tested in production.

Figure 7-1 POR/Brown Out diagram

Table 7-6 POR/Brown Out

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|---|------------|------|------|------|------|
| Vpor | POR release voltage (power-on process) BOR detection voltage (power-off process) | | 1.45 | 1.50 | 1.65 | V |

Table 7-7 LVD module characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|--------------------|------|-------|------|------|
| Vex | External input voltage range | | 0 | | VCC | V |
| Vlevel | Detection Threshold | LVD_CR.VTDS=0000 | 1.7 | 1.8 | 1.9 | |
| | | LVD_CR.VTDS =0001 | 1.8 | 1.9 | 2.0 | |
| | | LVD_CR.VTDS =0010 | 1.9 | 2.0 | 2.1 | |
| | | LVD_CR.VTDS =0011 | 2.0 | 2.1 | 2.2 | |
| | | LVD_CR.VTDS =0100 | 2.1 | 2.2 | 2.3 | |
| | | LVD_CR.VTDS=0101 | 2.2 | 2.3 | 2.4 | |
| | | LVD_CR.VTDS=0110 | 2.3 | 2.4 | 2.5 | |
| | | LVD_CR.VTDS=0111 | 2.4 | 2.5 | 2.6 | |
| | | LVD_CR.VTDS=1000 | 2.5 | 2.6 | 2.7 | |
| | | LVD_CR.VTDS=1001 | 2.6 | 2.7 | 2.8 | |
| | | LVD_CR.VTDS=1010 | 2.7 | 2.8 | 2.9 | |
| | | LVD_CR.VTDS=1011 | 2.8 | 2.9 | 3.0 | |
| | | LVD_CR.VTDS=1100 | 2.9 | 3.0 | 3.1 | |
| | | LVD_CR.VTDS=1101 | 3.0 | 3.1 | 3.2 | |
| | | LVD_CR.VTDS=1110 | 3.1 | 3.2 | 3.3 | |
| | | LVD_CR.VTDS=1111 | 3.2 | 3.3 | 3.4 | |
| Icomp | Power consumption | | | 0.12 | | µA |
| Tresponse | Response time | | | 80 | | µs |
| Tsetup | Settling Time | | | 400 | | µs |
| Vhyste | Hysteresis voltage | | | 40 | | mV |
| Tfilter | Filter time | LVD_debounce = 000 | | 7 | | |
| | | LVD_debounce = 001 | | 14 | | |
| | | LVD_debounce = 010 | | 28 | | |
| | | LVD_debounce = 011 | | 112 | | |
| | | LVD_debounce = 100 | | 450 | | |
| | | LVD_debounce = 101 | | 1800 | | |
| | | LVD_debounce = 110 | | 7200 | | |
| | | LVD_debounce = 111 | | 28800 | | |

7.3.4 Built-in reference voltage

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------------|--|------------------------------|-------|------|-------|------------------|
| V _{REF25} | Internal 2.5V Reference Voltage | Normal temperature 25°C 3.3V | 2.475 | 2.5 | 2.525 | V |
| V _{REF25} | Internal 2.5V Reference Voltage | -40 ~ 85°C 2.8 ~ 5.5V | 2.463 | 2.5 | 2.525 | V ^[1] |
| V _{REF15} | Internal 1.5V Reference Voltage | Normal temperature 25°C 3.3V | 1.485 | 1.5 | 1.515 | V |
| V _{REF15} | Internal 1.5V Reference Voltage | -40 ~ 85°C 1.8 ~ 5.5V | 1.477 | 1.5 | 1.519 | V ^[1] |
| T _{Coeff} | Internal 2.5V 1.5V temperature coefficient | -40 ~ 85°C | | | 120 | ppm/°C |

1. The data is based on characterization results and is not tested in production.

7.3.5 Supply current characteristics

Current consumption is a composite indicator of many parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, program location in memory, and executed code.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level - VCC or VSS (no load).
- All peripherals are turned off unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of fHCLK (0 wait cycles for 0~24MHz, 1 wait cycle for 24~48MHz).
- When the peripherals are turned on: fPCLK0 = fHCLK, fPCLK1 = fHCLK.

Table 7-8 Operating current characteristics

| Symbol | Parameter | Conditions | | | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit |
|---------------------|--|---------------------------------|-------------------------------------|--------|--------------------|--------------------|------|
| IDD (AVCC_USB) | | Active | | | 4 | | mA |
| IDD (Run in RAM) | All peripherals clock ON, Run while(1) in RAM | Vcap=1.5V Vcc=3.3V TA=2xC | RCH clock source | 4M | 990 | | µA |
| | | | | 8M | 1960 | | |
| | | | | 16M | 3870 | | |
| | | | | 22.12M | 5360 | | |
| | | | | 24M | 5780 | | |
| | | | PLL RCH4M to xxM clock source | 32M | 7910 | | |
| | | | | 48M | 11770 | | |
| | All peripherals clock OFF, Run while(1) in RAM | Vcap=1.5V Vcc=3.3V TA=2xC | RCH clock source | 4M | 340 | | µA |
| | | | | 8M | 650 | | |
| | | | | 16M | 1240 | | |
| | | | | 22.12M | 1700 | | |
| | | | | 24M | 1840 | | |
| | | | PLL RCH4M to xxM clock source | 32M | 2690 | | |
| | | | | 48M | 3950 | | |
| | | | | 4M | 820 | | µA |

| Symbol | Parameter | Conditions | | | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit |
|----------------------------|---|---|-------------------------------------|--------------------|--------------------|--------------------|---------|
| I_{DD} (Run CoreMark) | All peripherals clock OFF, Run CoreMark in Flash | Vcap=1.5V V _{CC} =3.3V T _A =2xC | RCH clock source | 8M | 1550 | | μA |
| | | | | 16M | 2980 | | |
| | | | | 22.12M | 4000 | | |
| | | | | 24M | 4320 | | |
| | | | PLL RCH4M to xxM | 48M FlashWait=1 | 6810 | | |
| | | Vcap=1.5V V _{CC} =1.8-5.5V T _A =N40-85°C | RCH clock source | 4M | 1330 | 1800 | |
| | | | | 8M | 2490 | 3430 | |
| | | | | 16M | 4990 | 6570 | |
| | | | | 22.12M | 6760 | 8960 | |
| | | | | 24M | 7260 | 9680 | |
| I_{DD} (Run mode) | All peripherals clock ON, Run while(1) in Flash | Vcap=1.5V V _{CC} =1.8-5.5V T _A =N40C- 85°C | PLL RCH4M to xxM clock source | 16M | 5270 | 6550 | μA |
| | | | | 24M | 7390 | 9260 | |
| | | | | 32M FlashWait=1 | 9200 | 10640 | |
| | | | | 40M FlashWait=1 | 11350 | 13150 | |
| | | | | 48M FlashWait=1 | 13470 | 15750 | |
| | | Vcap=1.5V V _{CC} =1.8-5.5V T _A =N40-85°C | PLL RCH8M to xxM clock source | 16M | 5350 | 6620 | μA |
| | | | | 24M | 7460 | 9390 | |
| | | | | 32M FlashWait=1 | 9250 | 10740 | |
| | | | | 40M FlashWait=1 | 11380 | 13290 | |
| | | | | 48M FlashWait=1 | 13560 | 15850 | |
| | All peripherals clock OFF, Run while(1) in Flash | Vcap=1.5V V _{CC} =1.8-5.5V T _A =N40-85°C | RCH clock source | 4M | 670 | 1080 | μA |
| | | | | 8M | 1190 | 1990 | |
| | | | | 16M | 2280 | 3580 | |
| | | | | 22.12M | 3070 | 4790 | |
| | | | | 24M | 3290 | 5120 | |
| | | Vcap=1.5V V _{CC} =1.8-5.5V T _A =N40-85°C | PLL RCH4M to xxM clock source | 16M | 2560 | 3530 | μA |
| | | | | 24M | 3450 | 4780 | |
| | | | | 32M FlashWait=1 | 3950 | 4670 | |
| | | | | 40M FlashWait=1 | 4800 | 5710 | |
| | | | | 48M FlashWait=1 | 5680 | 6780 | |
| | | Vcap=1.5V V _{CC} =1.8-5.5V T _A =N40-85°C | PLL RCH8M to xxM clock source | 16M | 2620 | 3610 | μA |
| | | | | 24M | 3510 | 4860 | |
| | | | | 32M FlashWait=1 | 4010 | 4730 | |
| | | | | 40M FlashWait=1 | 4850 | 5760 | |
| | | | | 48M FlashWait=1 | 5730 | 6850 | |

| Symbol | Parameter | Conditions | | | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit |
|--------------------------|---|--|--------------------------------------|--------------------|--------------------|--------------------|---------|
| I_{DD} (Sleep mode) | All peripherals clock ON | Vcap=1.5V Vcc=1.8-5.5V TA=N40-85°C | RCH clock source | 4M | 840 | 950 | μA |
| | | | | 8M | 1640 | 1880 | |
| | | | | 16M | 3240 | 3680 | |
| | | | | 22.12M | 4490 | 5120 | |
| | | | | 24M | 4850 | 5570 | |
| | | Vcap=1.5V Vcc=1.8-5.5V TA=N40-85°C | PLL RCH4M to xxM clock source | 16M | 3550 | 4070 | μA |
| | | | | 24M | 5060 | 5770 | |
| | | | | 32M FlashWait=1 | 6680 | 7640 | |
| | | | | 40M FlashWait=1 | 8300 | 9510 | |
| | | | | 48M FlashWait=1 | 9920 | 11370 | |
| | | Vcap=1.5V Vcc=1.8-5.5V TA=N40-85°C | PLL RCH8M to xxM clock source | 16M | 3620 | 4120 | μA |
| | | | | 24M | 5120 | 5850 | |
| | | | | 32M FlashWait=1 | 6740 | 7710 | |
| | | | | 40M FlashWait=1 | 8340 | 9580 | |
| | | | | 48M FlashWait=1 | 9980 | 11430 | |
| | All peripherals clock OFF | Vcap=1.5V Vcc=1.8-5.5V TA=N40-85°C | RCH clock source | 4M | 180 | 230 | μA |
| | | | | 8M | 330 | 390 | |
| | | | | 16M | 600 | 690 | |
| | | | | 22.12M | 820 | 930 | |
| | | | | 24M | 880 | 1000 | |
| | | Vcap=1.5V Vcc=1.8-5.5V TA=N40-85°C | PLL RCH4M to xxM clock source | 16M | 900 | 1020 | μA |
| | | | | 24M | 1110 | 1260 | |
| | | | | 32M FlashWait=1 | 1410 | 1610 | |
| | | | | 40M FlashWait=1 | 1730 | 1970 | |
| | | | | 48M FlashWait=1 | 2040 | 2330 | |
| | All peripherals clock ON, Run while(1) in Flash | Vcap=1.5V Vcc=1.8-5.5V | XTL32K clock source Driver=0x0 | 16M | 960 | 1090 | μA |
| | | | | 24M | 1170 | 1330 | |
| | | | | 32M FlashWait=1 | 1470 | 1670 | |
| | | | | 40M FlashWait=1 | 1780 | 2030 | |
| | | | | 48M FlashWait=1 | 2100 | 2390 | |
| | | | | TA=N40-25C | 14 | 19 | |
| I_{DD} (LP Run) | All peripherals clock ON, Run while(1) in Flash | Vcap=1.5V Vcc=1.8-5.5V | XTL32K clock source Driver=0x0 | TA=50C | 15 | 20 | μA |
| | | | | TA=85C | 21 | 28 | |
| | | | | TA=N40-25C | 9 | 13 | |
| | All peripherals clock OFF, Run while(1) in Flash | Vcap=1.5V Vcc=1.8-5.5V | XTL32K clock source Driver=0x0 | TA=50C | 10 | 14 | μA |
| | | | | TA=85C | 16 | 22 | |

| Symbol | Parameter | Conditions | | | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit |
|---------------------------------|--|--|--------------------------------------|------------|--------------------|--------------------|---------|
| I_{DD} (LP Sleep) | All peripherals clock ON | Vcap=1.5V V _{CC} =1.8-5.5V | XTL32K clock source Driver=0x0 | TA=N40-25C | 9 | 10 | μA |
| | | | | TA=50C | 10 | 11 | |
| | | | | TA=85C | 16 | 18 | |
| | All peripherals clock OFF | Vcap=1.5V V _{CC} =1.8-5.5V | XTL32K clock source Driver=0x0 | TA=N40-25C | 4 | 4 | μA |
| | | | | TA=50C | 5 | 5 | |
| | | | | TA=85C | 11 | 13 | |
| | LpTimer+RTC+32 K clk ON, Other clk OFF | Vcap=1.5V V _{CC} =1.8-5.5V | XTL32K clock source Driver=0x0 | TA=N40-25C | 4 | 4 | μA |
| | | | | TA=50C | 5 | 6 | |
| | | | | TA=85C | 11 | 13 | |
| I_{DD} (DeepSleep mode) | RTC+WDT+LPT+ XTL32K +DeepSleep | Vcap=1.5V V _{CC} =1.8-5.5V | XTL32K Driver=0x0 | TA=N40-25C | 1750 | 2040 | nA |
| | | | | TA=50C | 2460 | 2990 | |
| | | | | TA=85C | 6940 | 8620 | |
| | LPT+XTL32K +DeepSleep | Vcap=1.5V V _{CC} =1.8-5.5V | XTL32K Driver=0x0 | TA=N40-25C | 1630 | 1910 | nA |
| | | | | TA=50C | 2340 | 2850 | |
| | | | | TA=85C | 6810 | 8510 | |
| | RTC+XTL32K +DeepSleep | Vcap=1.5V V _{CC} =1.8-5.5V | XTL32K Driver=0x0 | TA=N40-25C | 1590 | 1870 | nA |
| | | | | TA=50C | 2300 | 2810 | |
| | | | | TA=85C | 6800 | 8470 | |
| | XTL32K +DeepSleep | Vcap=1.5V V _{CC} =1.8-5.5V | XTL32K Driver=0x0 | TA=N40-25C | 1580 | 1860 | nA |
| | | | | TA=50C | 2290 | 2790 | |
| | | | | TA=85C | 6750 | 8410 | |
| | IRC32K +DeepSleep | Vcap=1.5V V _{CC} =1.8-5.5V | | TA=N40-25C | 1570 | 1830 | nA |
| | | | | TA=50C | 2270 | 2750 | |
| | | | | TA=85C | 6750 | 8410 | |
| | WDT +DeepSleep | Vcap=1.5V V _{CC} =1.8-5.5V | | TA=N40-25C | 1300 | 1520 | nA |
| | | | | TA=50C | 1990 | 2430 | |
| | | | | TA=85C | 6410 | 8020 | |
| | DeepSleep | Vcap=1.5V V _{CC} =1.8-5.5V | | TA=N40-25C | 1190 | 1400 | nA |
| | | | | TA=50C | 1880 | 2310 | |
| | | | | TA=85C | 6330 | 7970 | |

1. If no other conditions are specified, the Typ value is measured at 25°C & VCC = 3.3V.

2. If no other conditions are specified, the Max value is the maximum value in the range of VCC = 1.8-5.5V & Temperature = N40 - 85°C.

3. The data is based on the characterization results and is not tested in production.

7.3.6 Wake-up time from low power modes

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used during wake-up depends on the current operating mode:

- Sleep mode: The clock source is the RCH oscillator
- Deep sleep mode: The clock source is the RCH oscillator used when entering deep sleep

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|-------------------------|---------------------------|-----|-----|-----|------|
| T _{wu} | Sleep mode wake-up time | | | 1.8 | | μs |
| | Deep sleep wake-up time | F _{MCLK} = 4MHz | | 9.0 | | μs |
| | | F _{MCLK} = 8MHz | | 6.0 | | μs |
| | | F _{MCLK} = 16MHz | | 5.0 | | μs |
| | | F _{MCLK} = 24MHz | | 4.0 | | μs |

1. The wake-up time is measured from the wake-up event to the first instruction read by the user program.

7.3.7 External clock source characteristics

7.3.7.1 External high-speed clock input

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|--|------------|--------|-----|--------|------|
| f _{XTH_ext} | User external clock frequency ⁽¹⁾ | | 0 | 8 | 32 | MHz |
| V _{XTHH} | Input pin high level voltage | | 0.7VCC | | VCC | V |
| V _{XTHL} | Input pin low level voltage | | VSS | | 0.3VCC | V |
| T _{r(XTH)} | Rise time ⁽¹⁾ | | | | 20 | ns |
| T _{f(XTH)} | Fall time ⁽¹⁾ | | | | 20 | ns |
| T _{w(XTH)} | Input high or low time ⁽¹⁾ | | 16 | | | ns |
| C _{in(XTH)} | Input capacitance ⁽¹⁾ | | | 5 | | pF |
| Duty | Duty cycle | | 40 | | 60 | % |
| I _L | Input leakage current | | | | ±1 | µA |

1. Guaranteed by design, not tested in production.

7.3.7.2 External low speed clock input

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|--|------------|--------|--------|--------|------|
| f _{XTL_ext} | User external clock frequency ⁽¹⁾ | | 0 | 32.768 | 1000 | kHz |
| V _{XTLH} | Input pin high level voltage | | 0.7VCC | | VCC | V |
| V _{XTLL} | Input pin low level voltage | | VSS | | 0.3VCC | V |
| T _{r(XTL)} | Rise time ⁽¹⁾ | | | | 50 | ns |
| T _{f(XTL)} | Fall time ⁽¹⁾ | | | | 50 | ns |
| T _{w(XTL)} | Input high or low time ⁽¹⁾ | | 450 | | | ns |
| C _{in(XTL)} | Input capacitance ⁽¹⁾ | | | 5 | | pF |
| Duty | Duty cycle | | 30 | | 70 | % |
| I _L | Input leakage current | | | | ±1 | µA |

1. Guaranteed by design, not tested in production.

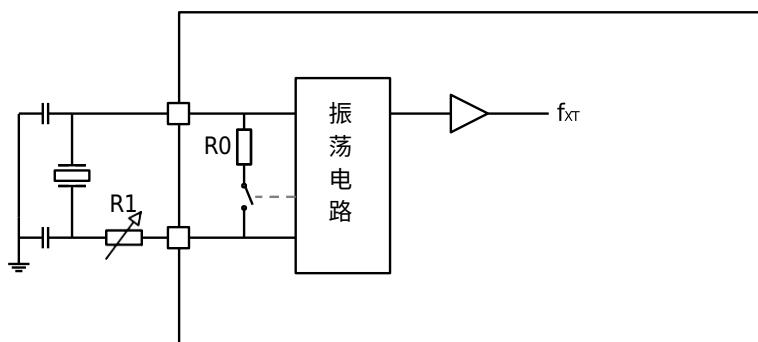
7.3.7.3 High-speed external clock XTH

The high-speed external clock (XTH) can be generated using an 8~32MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitors must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed parameters of the crystal resonator (frequency, package, accuracy, etc.), please consult the corresponding manufacturer.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|------------------|--|-----|-------|-----|----------|
| F_{CLK} | Frequency | - | 8 | - | 32 | MHz |
| ESR_{CLK} | ESR range | 32MHz | - | - | 60 | Ω |
| | | 24MHz | - | - | 80 | |
| | | 16MHz | - | - | 100 | |
| | | 8MHz | - | - | 120 | |
| $C_{LX}^{(3)}$ | Load Capacitance | Configured as required by the crystal manufacturer. | 4 | 12 | 20 | pF |
| Duty | Duty Cycle | - | 40 | 50 | 60 | % |
| $I_{dd}^{(4)}$ | Current | XTH_CR[3:0]=0b1111 | - | 1000 | - | μA |
| | | XTH_CR[3:0]=0b1110 | - | 600 | - | |
| | | XTH_CR[3:0]=0b1010 | - | 370 | - | |
| | | XTH_CR[3:0]=0b0110 | - | 300 | - | |
| | | XTH_CR[3:0]=0b0010 | - | 160 | - | |
| g_m | Transconductance | XTH_CR[3:0]=0b1111 | - | 11.75 | - | mA/V |
| | | XTH_CR[3:0]=0b1110 (32MHz, 24MHz Recommended value) | - | 6.34 | - | |
| | | XTH_CR[3:0]=0b1101 | - | 4.38 | - | |
| | | XTH_CR[3:0]=0b1100 | - | 3.38 | - | |
| | | XTH_CR[3:0]=0b1011 | - | 7.41 | - | |
| | | XTH_CR[3:0]=0b1010 (16MHz Recommended value) | - | 4.01 | - | |
| | | XTH_CR[3:0]=0b1001 | - | 2.77 | - | |
| | | XTH_CR[3:0]=0b1000 | - | 2.14 | - | |
| | | XTH_CR[3:0]=0b0111 | - | 5.59 | - | |
| | | XTH_CR[3:0]=0b0110 (12MHz Recommended value) | - | 3.01 | - | |
| | | XTH_CR[3:0]=0b0101 | - | 2.08 | - | |
| | | XTH_CR[3:0]=0b0100 | - | 1.60 | - | |
| | | XTH_CR[3:0]=0b0011 | - | 2.50 | - | |
| | | XTH_CR[3:0]=0b0010 (8MHz Recommended value) | - | 1.30 | - | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|--------------|--|-----|------|-----|------|
| | | XTH_CR[3:0]=0b0001 | - | 0.93 | - | |
| | | XTH_CR[3:0]=0b0000 | - | 0.72 | - | |
| T _{start} ⁽⁵⁾ | Startup time | 32MHz, CL=16pF @ XTH_CR[3:0]=0b1110 | - | 500 | - | μs |
| | | 8MHz, CL=16pF @ XTH_CR[3:0]=0b0010 | - | 2 | - | ms |

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
 2. Derived from comprehensive evaluation, not tested in production.
 3. CLx refers to the load capacitance CL1 and CL2 of the two pins of XTAL. For CL1 and CL2, it is recommended to use high-quality ceramic capacitors designed for high-frequency applications and select a crystal or resonator that meets the requirements. Usually CL1 and CL2 have the same parameters. Crystal manufacturers usually give the parameters of the load capacitance as a series combination of CL1 and CL2. When selecting CL1 and CL2, the parameters such as the frequency and ESR of the crystal should be considered, and the capacitance of the PCB and MCU pins should be taken into account.
 4. The current varies with the selection of frequency and drive capability. The higher the frequency and the stronger the drive capability, the greater the current consumption.
- T_{start} is the start-up time, which is measured from the software enabling XTH until a stable 32MHz/8MHz oscillation is obtained. This value is measured with a standard crystal resonator at XTH_CR[5:4] = 0b10 and may vary greatly depending on the crystal manufacturer and model.



Note:

- It is recommended to configure the crystal matching capacitor according to the requirements of the crystal manufacturer's technical manual. If the crystal manufacturer specifies the load capacitance, the matching capacitor should be twice the load capacitance specified by the crystal manufacturer. If the crystal manufacturer specifies the matching capacitor, the matching capacitor specified by the crystal manufacturer can be used directly.
- The chip has integrated feedback resistor R0.
- The damping resistor R1 is optional. The resistance value depends on the crystal characteristics and is 0Ω by default.

7.3.7.4 Low-speed external clock XTL

The low-speed external clock (XTL) can be generated using an oscillator composed of a 32.768kHz crystal/ceramic resonator. The information given in this section is based on typical external components and the results obtained through comprehensive characteristic evaluation. In the application, the resonator and load capacitors must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed parameters of the crystal resonator (frequency, package, accuracy, etc.), please consult the corresponding manufacturer.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|------------------|---|-----|--------|-----|------|
| F_{CLK} | Frequency | - | - | 32.768 | - | kHz |
| ESR_{CLK} | ESR range | - | - | - | 60 | kΩ |
| $C_{Lx}^{(2)}$ | Load Capacitance | Configured as required by the crystal manufacturer. | 8 | 12 | 20 | pF |
| DC_{ACLK} | Duty Cycle | - | 30 | 50 | 70 | % |
| $I_{dd}^{(3)}$ | Current | XTL_CR[3:0]=0b1111 | - | 1330 | - | nA |
| | | XTL_CR[3:0]=0b1011 | - | 1230 | - | |
| | | XTL_CR[3:0]=0b0111 | - | 1140 | - | |
| | | XTL_CR[3:0]=0b0011 | - | 1050 | - | |
| | | XTL_CR[3:0]=0b1110 | - | 630 | - | |
| | | XTL_CR[3:0]=0b1010 (推荐值) | - | 580 | - | |
| | | XTL_CR[3:0]=0b0110 | - | 530 | - | |
| | | XTL_CR[3:0]=0b0010 | - | 490 | - | |
| g_m | Transconductance | XTL_CR[3:0]=0b1111 | - | 14.64 | - | μA/V |
| | | XTL_CR[3:0]=0b1011 | - | 13.17 | - | |
| | | XTL_CR[3:0]=0b0111 | - | 11.67 | - | |
| | | XTL_CR[3:0]=0b0011 | - | 10.15 | - | |
| | | XTL_CR[3:0]=0b1110 | - | 7.37 | - | |
| | | XTL_CR[3:0]=0b1010 (推荐值) | - | 6.62 | - | |
| | | XTL_CR[3:0]=0b0110 | - | 5.87 | - | |
| | | XTL_CR[3:0]=0b0010 | - | 5.10 | - | |
| $T_{start}^{(4)}$ | Startup time | ESR=30kΩ $C_L=12pF$ XTL_CR[3:0]=0b1010 | - | 2000 | - | ms |

1. Derived from comprehensive evaluation, not tested in production.

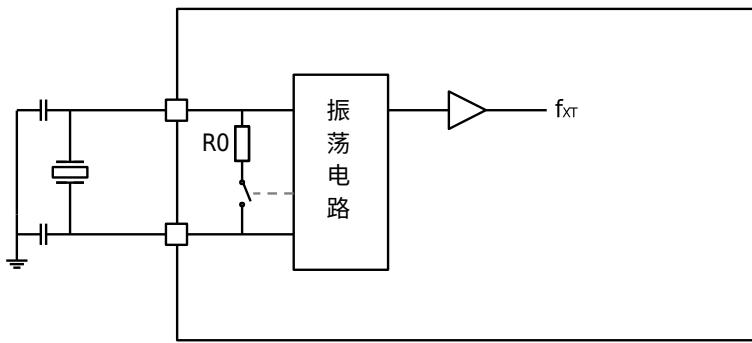
2. CLX refers to the load capacitance of the two pins of XTAL. The user must select the capacitance of the capacitor according to the requirements of the crystal manufacturer.

If the crystal manufacturer gives the capacitance of the load capacitance, the capacitance of the matching capacitor should be twice the capacitance of the load capacitance given by the crystal manufacturer. If the crystal manufacturer gives the capacitance of the matching capacitor, the capacitance of the matching capacitor given by the crystal manufacturer can be used directly.

Example: When the crystal manufacturer gives the crystal load capacitance of 8pF, the capacitance of the matching capacitor should be 16pF. Considering the distributed capacitance between the PCB and the MCU pin, it is recommended to select a matching capacitor with a capacitance of 15pF or 12pF.

When the crystal manufacturer specifies a matching capacitor of 12pF for the crystal, the matching capacitor should be 12pF. Considering the distributed capacitance between the PCB and the MCU pin, it is recommended to select a matching capacitor with a capacitance of 10pF or 8pF.

3. Select a high-quality oscillator with a small ESR value (such as MSIV-TIN32.768kHz). You can optimize the current consumption by adjusting the XTL_CR[3:0] setting value. The current consumption is proportional to the transconductance (gm) provided by the circuit.
4. Tstart is the start-up time, which is measured from the software enabling XTL until a stable 32768 oscillation is obtained. This value is measured on a standard crystal resonator with the settings of XTL_CR[3:0]=0b1010 and XTL_CR[5:4]=0b11, and it may vary greatly depending on the crystal manufacturer and model.



Notes:

- It is recommended to configure the crystal matching capacitor according to the requirements of the crystal manufacturer's technical manual.
If the crystal manufacturer specifies the load capacitance value, the matching capacitor value should be twice the load capacitance value specified by the crystal manufacturer.
If the crystal manufacturer specifies the matching capacitor value, the matching capacitor value specified by the crystal manufacturer can be used directly.
- The feedback resistor R0 is integrated in the chip.

7.3.8 Internal clock source characteristics

7.3.8.1 Internal RCH Oscillator

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|---------------------------|--|------|-------------------------------------|------|------|
| Dev | RCH Oscillator Accuracy | User trimming step for given VCC and TA conditions | | 0.25 | | % |
| | | VCC = 1.8 ~ 5.5V T _{AMB} = -40 ~ 85°C | -3.5 | | +3.5 | % |
| | | VCC = 1.8 ~ 5.5V T _{AMB} = -20 ~ 85°C | -2.5 | | +2.5 | % |
| | | VCC = 1.8 ~ 5.5V T _{AMB} = -20 ~ 50°C | -2.0 | | +2.0 | % |
| F _{CLK} | Frequency | | 4.0 | 4.0 8.0 16.0 22.12 24.0 | 24.0 | MHz |
| I _{CLK} | Power consumption | F _{MCLK} = 4MHz | | 80 | | µA |
| | | F _{MCLK} = 8MHz | | 100 | | µA |
| | | F _{MCLK} = 16MHz | | 120 | | µA |
| | | F _{MCLK} = 24MHz | | 140 | | µA |
| DC _{CLK} | Duty Cycle ⁽¹⁾ | | 45 | 50 | 55 | % |

1. Derived from comprehensive evaluation, not tested in production.

7.3.8.2 Internal RCL Oscillator

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|---------------------------|--|-----|----------------|-----|------|
| Dev | RCL Oscillator Accuracy | User trimming step for given VCC and TA conditions | | 0.5 | | % |
| | | VCC = 1.8 ~ 5.5V T _{AMB} = -40 ~ 85°C T _{AMB} = -40°C ~ 85°C | -5 | | +5 | % |
| | | VCC = 1.8 ~ 5.5V T _{AMB} = -20 ~ 50°C | -3 | | +3 | % |
| F _{CLK} | Frequency | | | 38.4 32.768 | | kHz |
| T _{CLK} | Startup time | | | 150 | | µs |
| DC _{CLK} | Duty Cycle ⁽¹⁾ | | 25 | 50 | 75 | % |
| I _{CLK} | Power consumption | | | 0.35 | | µA |

1. Derived from comprehensive evaluation, not tested in production.

7.3.8.3 Internal low speed clock 10k oscillator

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|------------------------------------|---|-----|-----|-----|------|
| V | Operation voltage | - | 1.8 | | 5.5 | V |
| Dev | Oscillator Accuracy ⁽¹⁾ | VCC = 1.8 ~ 5.5V T _{AMB} = -20 ~ 50°C | -50 | - | 50 | % |
| F _{CLK} | Frequency | VCC=3.3v T _{AMB} = 25°C | | 10 | | KHz |

1. Derived from comprehensive evaluation, not tested in production.

7.3.8.4 Internal USB-specific RCH48M oscillator

| Parameter | Description | Min | Typ | Max | Units | Condition |
|---------------------------|---|---------------------|------|--------------------|-------|-------------------------------|
| DVCC | Analog 5V Supply | 1.8 | 3.3 | 5.5 | V | |
| T | Junction Temperature | -40 | 27 | 105 | deg C | |
| F _{RCH48M} | Frequency | - | 48 | - | MHz | - |
| TRIM | RCH48M user-trimming step | 0.06 ⁽²⁾ | 0.12 | 0.2 ⁽²⁾ | % | - |
| DUC _{RCH48M} | Duty cycle | 45 ⁽²⁾ | - | 55 ⁽²⁾ | % | - |
| ACC _{RCH48M} | Accuracy of the RCH48M oscillator(factory calibrated) | 6 ⁽³⁾ | - | 6 ⁽³⁾ | % | T _A =-40 to 105 °C |
| | | TBD ⁽³⁾ | - | TBD ⁽³⁾ | % | T _A =-10 to 85 °C |
| | | TBD ⁽³⁾ | - | TBD ⁽³⁾ | % | T _A =0 to 70 °C |
| | | 2 ⁽³⁾ | - | 2 ⁽³⁾ | % | T _A =25 °C |
| t _{su} (RCH48M) | RCH48M oscillator startup time | - | - | 20 ⁽²⁾ | μs | |
| I _{DDA} (RCH48M) | RCH48M oscillator power consumption | - | 270 | 350 ⁽²⁾ | μA | |

1. AVCC=3.3V, T_A=-40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

7.3.9 PLL Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|------------------------|----------------------|-----|-----|-----|-------|
| Fin ⁽¹⁾ | Input clock | | 4 | 4 | 24 | MHz |
| | Input clock duty cycle | | 40 | | 60 | % |
| Fout | Output frequency | | 8 | - | 48 | MHz |
| Duty ⁽¹⁾ | Output duty cycle | | 48% | - | 52% | |
| Tlock ⁽¹⁾ | Lock time | Input frequency 4MHz | - | 100 | 200 | μs |

1. Derived from comprehensive evaluation, not tested in production.

7.3.10 Memory characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------|-------------------------|--|-----|-----|-----|---------|
| ECFLASH | Endurance | Regulator voltage=1.5V, T _{AMB} = 25°C | 20 | | | kcycles |
| RET _{FLASH} | Data retention time | T _{AMB} = 85°C, after 20 kcycles | 20 | | | Years |
| T _b _prog | Programming time (byte) | | 22 | | 30 | μs |
| T _w _prog | Programming time (word) | | 40 | | 52 | μs |
| T _p _erase | Page Erase Time | | 4 | | 5 | ms |
| T _m _erase | Full chip erase time | | 30 | | 40 | ms |

7.3.11 EFT Characteristics

Chip reset can restore the system to normal operation.

| Symbol | Level/Type |
|-----------------------------|-------------|
| EFT to IO (IEC61000-4-4) | Class:4 (A) |
| EFT to Power (IEC61000-4-4) | Class:4 (A) |

Software Recommendations

The software process must include controls for program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Corrupted critical data (control registers, etc.)

When performing EFT testing, interference that exceeds application requirements can be applied directly to the chip power supply or IO. When unexpected actions are detected, the software part is strengthened to prevent unrecoverable errors.

7.3.12 ESD characteristics

Using specific measurement methods, the chip is stressed to determine its performance in terms of electrical sensitivity.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------------|--------------------------|------------|-----|-----|-----|-------|
| V _{ESD_{HBM}} | ESD @ Human Body Mode | | | 4 | | kV |
| V _{ESD_{CDM}} | ESD @ Charge Device Mode | | | 1 | | kV |
| V _{ESD_{MM}} | ESD @ machine Mode | | | 200 | | V |
| I _{latchup} | Latch up current | | | 200 | | mA |

7.3.13 I/O Port Characteristics

7.3.13.1 Output Characteristics - Ports

Table 7-9 Port output characteristics

| Symbol | Parameter | Conditions | Min | Max | Units |
|------------------|--|--|----------|----------|-------|
| V _{OH} | High level output voltage Source Current | Sourcing 4 mA, VCC = 3.3 V (see Note 1) | VCC-0.25 | | V |
| | | Sourcing 8 mA, VCC = 3.3 V (see Note 2) | VCC-0.6 | | V |
| V _{OL} | Low level output voltage Sink Current | Sinking 5 mA, VCC = 3.3 V (see Note 1) | | VSS+0.25 | V |
| | | Sinking 14 mA, VCC = 3.3 V (see Note 2) | | VSS+0.6 | V |
| V _{OHD} | High level output voltage Double source Current | Sourcing 8 mA, VCC = 3.3 V (see Note 1) | VCC-0.25 | | V |
| | | Sourcing 18 mA, VCC = 3.3V (see Note 2) | VCC-0.6 | | V |
| V _{OLD} | Low level output voltage Double Sink Current | Sinking 8 mA, VCC = 3.3 V (see Note 1) | | VSS+0.25 | V |
| | | Sinking 18 mA, VCC = 3.3 V (see Note 2) | | VSS+0.6 | V |

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed 40 mA to satisfy the maximum specified voltage drop.
 2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed 100 mA to satisfy the maximum specified voltage drop.

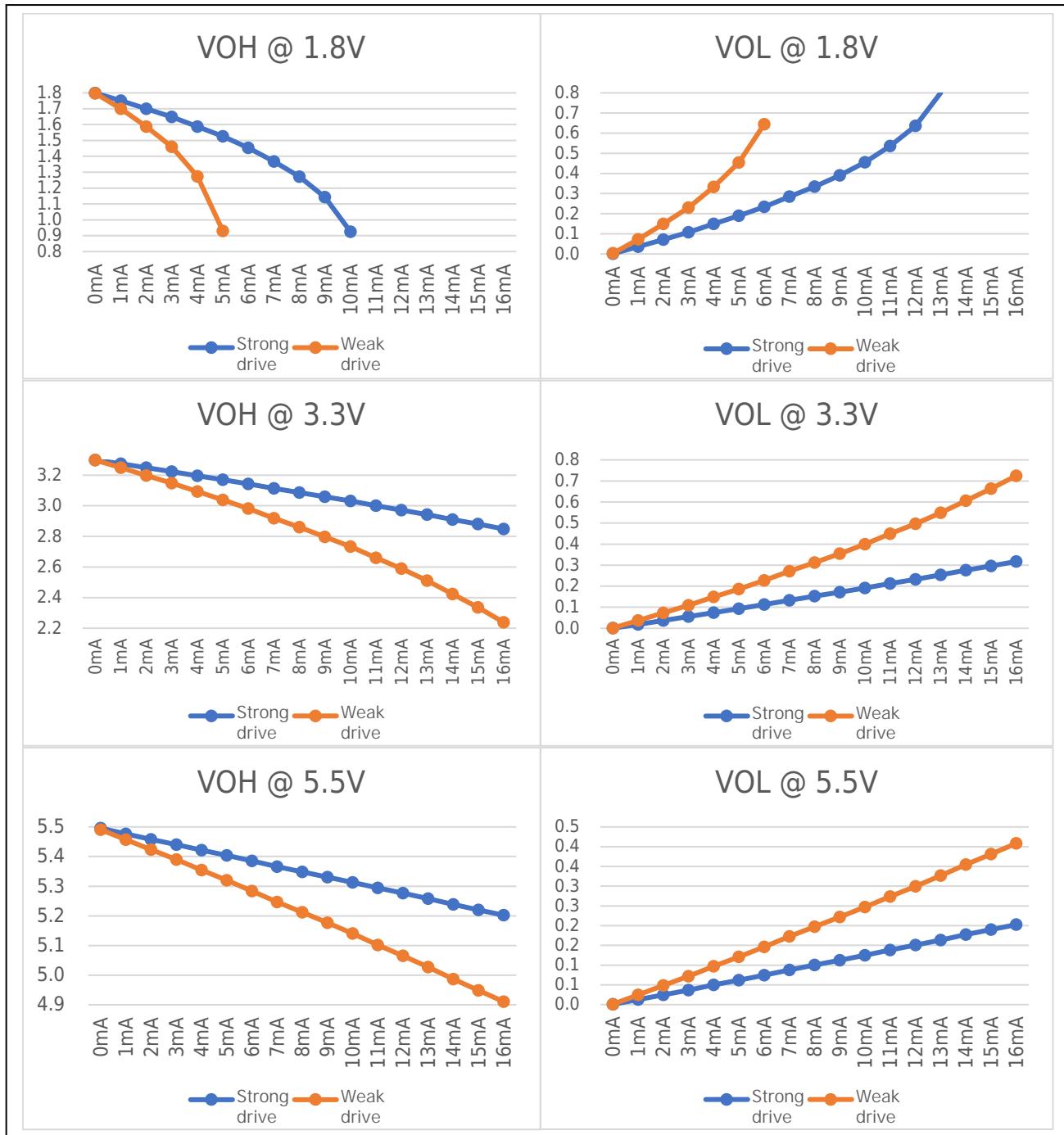


Figure 7-2 Output port VOH/VOL measured curve

7.3.13.2 Input characteristics - ports PA, PB, PC, PD, PE, PF

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------|--|------------------------------|--------|-----|--------|-------|
| V_{IH} | Positive-going input threshold voltage | VCC=1.8V | 0.7VCC | | | V |
| | | VCC=3.3V | 0.7VCC | | | V |
| | | VCC=5.5V | 0.7VCC | | | V |
| V_{IL} | Negative-going input threshold voltage | VCC=1.8V | | | 0.3VCC | V |
| | | VCC=3.3V | | | 0.3VCC | V |
| | | VCC=5.5V | | | 0.3VCC | V |
| $V_{hys(1)}$ | Input voltage hysteresis ($V_{IH} - V_{IL}$) | VCC=1.8V | | 0.3 | | V |
| | | VCC=3.3V | | 0.4 | | V |
| | | VCC=5.5V | | 0.6 | | V |
| $R_{pullhigh}$ (GPIO) | Pullup resistor | Pullup enabled VCC=3.3V | | 80 | | kΩ |
| $R_{pulllow}$ (GPIO) | Pulldown resistor | Pulldown enabled VCC=3.3V | | 40 | | kΩ |
| C_{input} | Input capacitance | | | 5 | | pf |

1. Derived from comprehensive evaluation, not tested in production.

7.3.13.3 Input characteristics - USB_DP, USB_DM

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------|--|----------------------|-------------|-----|-------------|-------|
| V_{IH} | Positive-going input threshold voltage | AVCC_USB = 3.0 ~ 3.6 | 0.7AVCC_USB | | | V |
| V_{IL} | Negative-going input threshold voltage | | | | 0.3AVCC_USB | V |
| $V_{hys(1)}$ | Input voltage hysteresis ($V_{IH} - V_{IL}$) | | | 0.3 | | V |
| $R_{pullhigh}$ | Pullup resistor | Transmitting | 1425 | | 3090 | Ohm |
| | | Idle | 900 | | 1575 | |
| C_{input} | Input capacitance | | | 5 | | pf |

1. Derived from comprehensive evaluation, not tested in production.

7.3.13.4 Port External Input Sampling Requirements - Timer Gate/Timer Clock

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------|--------------------------------------|---|------|-----|--------|-------|
| t(int) | External interrupt timing | External trigger signal for the interrupt flag (see Note 1) | 1.8V | 30 | | ns |
| | | | 3.3V | 30 | | ns |
| | | | 5.5V | 30 | | ns |
| t(cap) | Timer capture timing | Timer4/5/6 capture pulse width Fsystem = 4MHz | 1.8V | 0.5 | | μs |
| | | | 3.3V | 0.5 | | μs |
| | | | 5.5V | 0.5 | | μs |
| t(clk) | Timer clock frequency applied to pin | Timer0/1/2/4/5/6 external clock input Fsystem = 4MHz | 1.8V | | PCLK/2 | MHz |
| | | | 3.3V | | PCLK/2 | MHz |
| | | | 5.5V | | PCLK/2 | MHz |
| t(pca) ⁽²⁾ | PCA clock frequency applied to pin | PCA external clock input Fsystem = 4MHz | 1.8V | | PCLK/8 | MHz |
| | | | 3.3V | | PCLK/8 | MHz |
| | | | 5.5V | | PCLK/8 | MHz |

NOTES: 1. The external signal sets the interrupt flag every time the minimum t_(int) parameters are met. It may be set even with trigger signals shorter than t_(int).

2. Derived from comprehensive evaluation, not tested in production.

7.3.13.5 Port leakage characteristics - PA, PB, PC, PD, PE, PF

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------|-----------------|-------------------------------------|-----|-----|-----|-------|
| I _{lkg(Px,y)} | Leakage current | V _(Px,y) (see Note 1, 2) | | ±50 | | nA |

NOTES: 1. The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.

2. The port pin must be selected as input.

7.3.14 RESETB Pin Characteristics

The RESETB pin input driver uses CMOS technology and is connected to a pull-up resistor that cannot be disconnected.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|------------------------------------|-----------------------------------|--------|-----|---------|-------|
| VIL(RESETB) ⁽¹⁾ | Input low level voltage | | -0.3 | | 0.3VCC | V |
| VIH(RESETB) | Input high level voltage | | 0.7VCC | | VCC+0.3 | V |
| V _{hys} (RESETB) | Schmitt trigger voltage hysteresis | | | 200 | | mV |
| R _{PU} | Weak pull-up equivalent resistance | V _{IN} = V _{SS} | | 80 | | KΩ |
| T _F (RESETB) ⁽¹⁾ | Input filtered pulse | | | | 2 | μs |
| T _{NF} (RESETB) ⁽¹⁾ | Input unfiltered pulse | | 10 | | | μs |

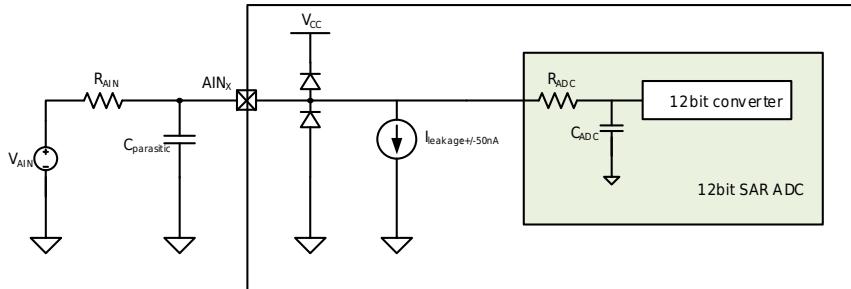
1. Guaranteed by design, not tested in production.

7.3.15 ADC Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------------|---|--|-----|------|-----------------------|--------|
| V _{ADCIN} | Input voltage range | Single ended | 0 | | V _{ADCREFIN} | V |
| V _{ADCREFIN} | Input range of external reference voltage | Single ended | 0 | | AVCC | V |
| DEV _{AVCC/3} | AVCC/3 accuracy | | | 3 | | % |
| I _{ADC1} | Active current including reference generator and buffer | 200Ksps | | 2 | | mA |
| I _{ADC2} | Active current without reference generator and buffer | 1Msps | | 0.5 | | mA |
| C _{ADCIN} | ADC input capacitance | | | 16 | 19.2 | pF |
| R _{ADC} ⁽¹⁾ | ADC sampling switch impedance | | | 1.5 | | kΩ |
| R _{AIN} ⁽¹⁾ | ADC external input resistor ⁽²⁾ | | | | 100 | kΩ |
| F _{ADCCLK} | ADC clock Frequency | | | | 24M | Hz |
| T _{ADCSTART} | Startup time of reference generator and ADC core | | | 30 | | μs |
| T _{ADCCONV} | Conversion time | | 20 | 24 | 28 | cycles |
| ENOB | Effective Bits | 1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF | | 10.3 | | Bit |
| | | 1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC | | 10.3 | | Bit |
| | | 200Ksps@VCC>=1.8V REF=internal 1.5V | | 9.4 | | Bit |
| | | 200Ksps@VCC>=2.8V REF=internal 2.5V | | 9.4 | | Bit |
| SNR | Signal to Noise Ratio | 1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF | | 68.2 | | dB |
| | | 1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC | | 68.2 | | dB |
| | | 200Ksps@VCC>=1.8V REF=internal 1.5V | | 60 | | dB |
| | | 200Ksps@VCC>=2.8V REF=internal 2.5V | | 60 | | dB |
| DNL ⁽¹⁾ | Differential non-linearity | 200Ksps; VREF=EXREF/AVCC | -1 | | 1 | LSB |
| INL ⁽¹⁾ | Integral non-linearity | 200Ksps; VREF=EXREF/AVCC | -3 | | 3 | LSB |
| E _o | Offset error | | | 0 | | LSB |
| E _g | Gain error | | | 0 | | LSB |

1. Guaranteed by design, not tested in production.

2. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} = \frac{M}{F_{ADC} * C_{ADC} * (N+1) * \ln(2)} - R_{ADC}$$

Among them, FADC is the ADC clock frequency, and the register ADC_CR0<3:2> can set its relationship with PCLK, as shown in the following table.

The following table shows the relationship between the ADC clock frequency FADC and the PCLK division ratio:

| ADC_CR0<3:2> | N |
|--------------|---|
| 00 | 1 |
| 01 | 2 |
| 10 | 4 |
| 11 | 8 |

M is the number of sampling cycles, which is set by register ADC_CR0<13:12>.

The following table shows the relationship between sampling time tsa and ADC clock frequency FADC:

| ADC_CR0<13:12> | M |
|----------------|----|
| 00 | 4 |
| 01 | 6 |
| 10 | 8 |
| 11 | 12 |

The following table shows the relationship between the ADC clock frequency FADC and the external resistor RAIN (under the condition of M=12 and sampling error of 0.5LSB):

| R_AIN(kΩ) | F_ADC(kHz) |
|-----------|------------|
| 10 | 5600 |
| 30 | 2100 |
| 50 | 1300 |
| 80 | 820 |
| 100 | 660 |
| 120 | 550 |
| 150 | 450 |

For the above typical applications, it should be noted that:

- Minimize the parasitic capacitance CPARACITIC of the ADC input port AINX;
- In addition to considering the RAIN value, if the internal resistance of the signal source VAIN is large, it also needs to be taken into consideration.

7.3.16 VC Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------|---|--|-----|--|---------|-------|
| Vin | Input voltage range | | 0 | | 5.5 | V |
| Vincom | Input common mode range | | 0 | | VCC-0.2 | V |
| Voffset | Input offset | Normal temperature 25°C 3.3V | -10 | | +10 | mV |
| Icomp | Comparator's current | VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11 | | 0.3 1.2 10 20 | | µA |
| Tresponse | Comparator's response time when one input cross another | VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11 | | 20 5 1 0.2 | | µs |
| Tsetup | Comparator's setup time when ENABLE. Input signals unchanged. | VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11 | | 20 5 1 0.2 | | µs |
| Twarmup | From main bandgap enable to Temp sensor voltage, ADC internal 1.5V, 2.5V reference stable | | | 20 | | µs |
| Tfilter | Digital filter time | VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111 | | 7 14 28 112 450 1800 7200 28800 | | µs |

7.3.17 OPA Features

OPA: (AVCC=2.2 ~ 5.5 V, AVSS=0 V, Ta=- 40 ~ +85°C)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|-------------------------------------|--|-----|-----|----------|-------|
| Vi | Input voltage | | 0 | - | AVCC | V |
| Vo | Output voltage ⁽¹⁾ | | 0.1 | - | AVCC-0.2 | V |
| Io | Output Current ⁽¹⁾ | | | | 2.2 | mA |
| RL | Load resistance ⁽¹⁾ | | 5K | | | Ohm |
| Tstart | Initialization time ⁽²⁾ | | | | 20 | µs |
| Vio | Input offset voltage | ViC=AVCC/2, Vo=AVCC/2, RL=5kΩ, RS=50 pF | | ±6 | | mV |
| PM | Phase Margin ⁽¹⁾ | ViC=AVCC/2, Vo=AVCC/2 RL=5kΩ, CL=50pF | | 80 | - | deg |
| UGBW | Unity gain bandwidth ⁽¹⁾ | ViC=AVCC/2, Vo=AVCC/2 RL=5kΩ, CL=50pF | | 9.3 | | MHz |
| SR | Slew rate ⁽¹⁾ | RL=5kΩ, CL=50pF | | 8 | | V/µs |

1. Guaranteed by design, not tested in production.

2. Need to set BGR_CR<0>=1 at the same time.

7.3.18 LCD Controller

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------|--------------------------------|-----------------------------------|-----|-----------|----------------|----------|
| I_{LCD} | Operating current | VCC=3.3V, external capacitor mode | | 0.2 | | μA |
| | | VCC=3.3V, external resistor mode | | 0.2 | | μA |
| | | VCC=3.3V, internal resistor mode | | 3.3 | | μA |
| R_H | Low drive resistance | | | 1M | | Ω |
| R_L | High drive resistance | | | 360K | | Ω |
| V_{LCDH} | LCD adjustable maximum voltage | | | | VCC | V |
| V_{LCD3} | LCD maximum voltage | | | | V_{LCDH} | V |
| V_{LCD2} | LCD 2/3 voltage | | | | 2/3 V_{LCDH} | V |
| V_{LCD1} | LCD 1/3 voltage | | | | 1/3 V_{LCDH} | V |
| V_{LCD0} | LCD minimum voltage | | 0 | | | V |
| ΔV_{xx} | LCD voltage deviation | $T_A=-40\sim85^\circ C$ | | $\pm 5\%$ | | |

7.3.19 DAC Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------|--------------------------------------|--------------------------------------|-----|---------|-----|---------|
| V_{DACOUT} | Output voltage range | AVCC voltage reference, single ended | 0 | | Vcc | V |
| V_{DACCm} | Output common mode voltage range | | 0 | | Vcc | V |
| I_{DAC} | Active current | 500KSamples/s | | 15 | | μA |
| SR_{DAC} | Sample rate | | | | 500 | Ksps |
| $t_{DACCONV}$ | Conversion time | | 2 | | | μs |
| $t_{DACSETTLE}$ | Setting time | | | 5 | | μs |
| SNR_{DAC} | Signal to Noise Ratio | | | 59 | | dB |
| $SNDR_{DAC}$ | Signal to Noise and Distortion Ratio | | | 57 | | dB |
| $SFDR_{DAC}$ | Spurious Free Dynamic Range | | | 56 | | dB |
| $V_{DACOFFSET}$ | Offset voltage | w/o buffer | | 2 | | mV |
| DNL_{DAC} | Differential non-linearity | | | ± 1 | | LSB |
| INL_{DAC} | Integral non-linearity | | | ± 5 | | LSB |

7.3.20 TIM timer characteristics

有关输入输出复用功能引脚（输出比较、输入捕获、外部时钟、PWM 输出）的特性详情，参见下表。

表 7-10 高级定时器 (ADVTIM) 特性

| Symbol | Parameter | Conditions | Min | Typ | Units |
|------------------|-------------------------|--------------------|--------|----------------|--------------|
| t_{res} | 定时器分辨时间 | | 1 | | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | 20.8 | | ns |
| f_{ext} | 外部时钟频率 | | 0 | $f_{TIMCLK}/2$ | MHz |
| | | $f_{TIMCLK}=48MHz$ | 0 | 24 | MHz |
| Res_{Tim} | 定时器分辨率 | | | 16 | 位 |
| $T_{counter}$ | 选择内部时钟时，16 位计数器 时钟周期 | | 1 | 65536 | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | 0.0208 | 1363 | μs |
| T_{MAX_COUNT} | 最大可能计数 | | | 67108864 | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | | 1.4 | s |

1. 由设计保证，不在生产中测试。

表 7-11 通用定时器特性

| 符号 | 参数 | 条件 | 最小值 | 最大值 | 单位 |
|------------------|-------------------------|--------------------|--------|----------------|--------------|
| t_{res} | 定时器分辨时间 | | 1 | | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | 20.8 | | ns |
| f_{ext} | 外部时钟频率 | | 0 | $f_{TIMCLK}/2$ | MHz |
| | | $f_{TIMCLK}=48MHz$ | 0 | 24 | MHz |
| Res_{Tim} | 定时器分辨率 | | | 16 | 位 |
| | | 模式 0 自由计数 | | 32 | 位 |
| $T_{counter}$ | 选择内部时钟时，16 位计数器 时钟周期 | | 1 | 65536 | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | 0.0208 | 1363 | μs |
| T_{MAX_COUNT} | 最大可能计数 | | | 16777216 | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | | 349.5 | ms |

1. 由设计保证，不在生产中测试。

表 7-12 PCA 特性

| 符号 | 参数 | 条件 | 最小值 | 最大值 | 单位 |
|------------------|---------------------|--------------------|--------|----------------|--------------|
| t_{res} | 定时器分辨时间 | | 1 | | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | 20.8 | | ns |
| f_{ext} | 外部时钟频率 | | 0 | $f_{TIMCLK}/2$ | MHz |
| | | $f_{TIMCLK}=48MHz$ | 0 | 24 | MHz |
| Res_{Tim} | 定时器分辨率 | | | 16 | 位 |
| $T_{counter}$ | 选择内部时钟时，16 位计数器时钟周期 | | 1 | 65536 | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | 0.0208 | 1363 | μs |
| T_{MAX_COUNT} | 最大可能计数 | | | 2097152 | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | | 43.69 | ms |

1. 由设计保证，不在生产中测试。

表 7-13 低功耗定时器特性

| 符号 | 参数 | 条件 | 最小值 | 最大值 | 单位 |
|------------------|---------------------|--------------------|--------|----------------|--------------|
| t_{res} | 定时器分辨时间 | | 1 | | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | 20.8 | | ns |
| f_{ext} | 外部时钟频率 | | 0 | $f_{TIMCLK}/2$ | MHz |
| | | $f_{TIMCLK}=48MHz$ | 0 | 24 | MHz |
| Res_{Tim} | 定时器分辨率 | | | 16 | 位 |
| $T_{counter}$ | 选择内部时钟时，16 位计数器时钟周期 | | 1 | 65536 | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | 0.0208 | 1363 | μs |
| T_{MAX_COUNT} | 最大可能计数 | | | 16777216 | t_{TIMCLK} |
| | | $f_{TIMCLK}=48MHz$ | | 349.53 | ms |

1. 由设计保证，不在生产中测试。

表 7-14 WDT 特性

| 符号 | 参数 | 条件 | 最小值 | 最大值 | 单位 |
|-----------|----------|--------------------|-----|-------|----|
| t_{res} | WDT 溢出时间 | $f_{WDTCLK}=10kHz$ | 1.6 | 52000 | ms |

1. 由设计保证，不在生产中测试。

7.3.21 Communication interfaces

7.3.21.1 I2C Features

I2C 接口特性如下表：

表 7-15 I2C 接口特性

| 符号 | 参数 | 标准模式 (100K) | | 快速模式 (400K) | | 高速模式 (1M) | | 单位 |
|---------|-----------------|-------------|-----|-------------|-----|-----------|-----|----|
| | | 最小值 | 最大值 | 最小值 | 最大值 | 最小值 | 最大值 | |
| tSCLL | SCL 时钟低时间 | 4.7 | | 1.25 | | 0.5 | | μs |
| tSCLH | SCL 时钟高时间 | 4.0 | | 0.6 | | 0.26 | | μs |
| tsu.SDA | SDA 建立时间 | 250 | | 100 | | 50 | | ns |
| tHD.SDA | SDA 保持时间 | 0 | | 0 | | 0 | | μs |
| tHD.STA | 开始条件保持时间 | 2.5 | | 0.625 | | 0.25 | | μs |
| tsu.STA | 重复的开始条件建立时间 | 2.5 | | 0.6 | | 0.25 | | μs |
| tsu.STO | 停止条件建立时间 | 0.25 | | 0.25 | | 0.25 | | μs |
| tBUF | 总线空闲(停止条件至开始条件) | 4.7 | | 1.3 | | 0.5 | | μs |

- 由设计保证，不在生产中测试。

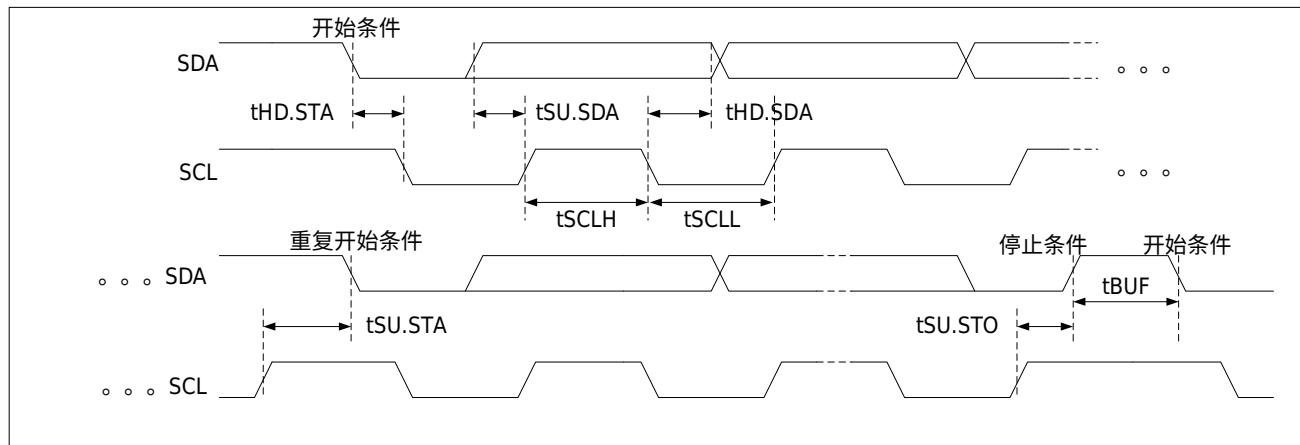


图 7-3 I2C 接口时序

7.3.21.2 SPI Features

表 7-16 SPI 接口特性^{(1) (2)}

| 符号 | 参数 | 条件 | 最小值 | 最大值 | 单位 |
|---------------|------------------------|-------------------------------------|------------------------|-------------------|----|
| $t_c(SCK)$ | 串行时钟的周期 ⁽³⁾ | 主机发送模式 $f_{PCLK} = 32\text{MHz}$ | 62.5 | - | ns |
| | | 主机接收模式 $f_{PCLK} = 48\text{MHz}$ | 160 | - | ns |
| | | 从机发送模式 $f_{PCLK} = 48\text{MHz}$ | 160 | - | ns |
| | | 从机接收模式 $f_{PCLK} = 48\text{MHz}$ | 84 | - | ns |
| $t_w(SCKH)$ | 串行时钟的高电平时间 | 主机模式 | $0.45 \times t_c(SCK)$ | - | ns |
| | | 从机模式 | $0.45 \times t_c(SCK)$ | - | ns |
| $t_w(SCKL)$ | 串行时钟的低电平时间 | 主机模式 | $0.45 \times t_c(SCK)$ | - | ns |
| | | 从机模式 | $0.45 \times t_c(SCK)$ | - | ns |
| $t_{su(SSN)}$ | 从机选择的建立时间 | 从机模式 | $0.45 \times t_c(SCK)$ | - | ns |
| $t_h(SSN)$ | 从机选择的保持时间 | 从机模式 | $0.45 \times t_c(SCK)$ | - | ns |
| $t_v(MO)$ | 主机数据输出的生效时间 | - | - | 3 | ns |
| $t_h(MO)$ | 主机数据输出的保持时间 | - | 2 | - | ns |
| $t_v(SO)$ | 从机数据输出的生效时间 | - | - | $20+1.5*T_{PCLK}$ | ns |
| $t_h(SO)$ | 从机数据输出的保持时间 | - | $10+0.5*T_{PCLK}$ | - | ns |
| $t_{su(MI)}$ | 主机数据输入的建立时间 | - | 10 | - | ns |
| $t_h(MI)$ | 主机数据输入的保持时间 | - | 2 | - | ns |
| $t_{su(SI)}$ | 从机数据输入的建立时间 | - | 10 | - | ns |
| $t_h(SI)$ | 从机数据输入的保持时间 | - | 2 | - | ns |

1. 由设计保证，不在生产中测试。
2. 数据基于VCC=3.0V条件给出。
3. 主机模式最大分频系数为PCLK/2，从机模式最大分频系数为PCLK/4。

SPI 接口信号的波形和时序参数如下：

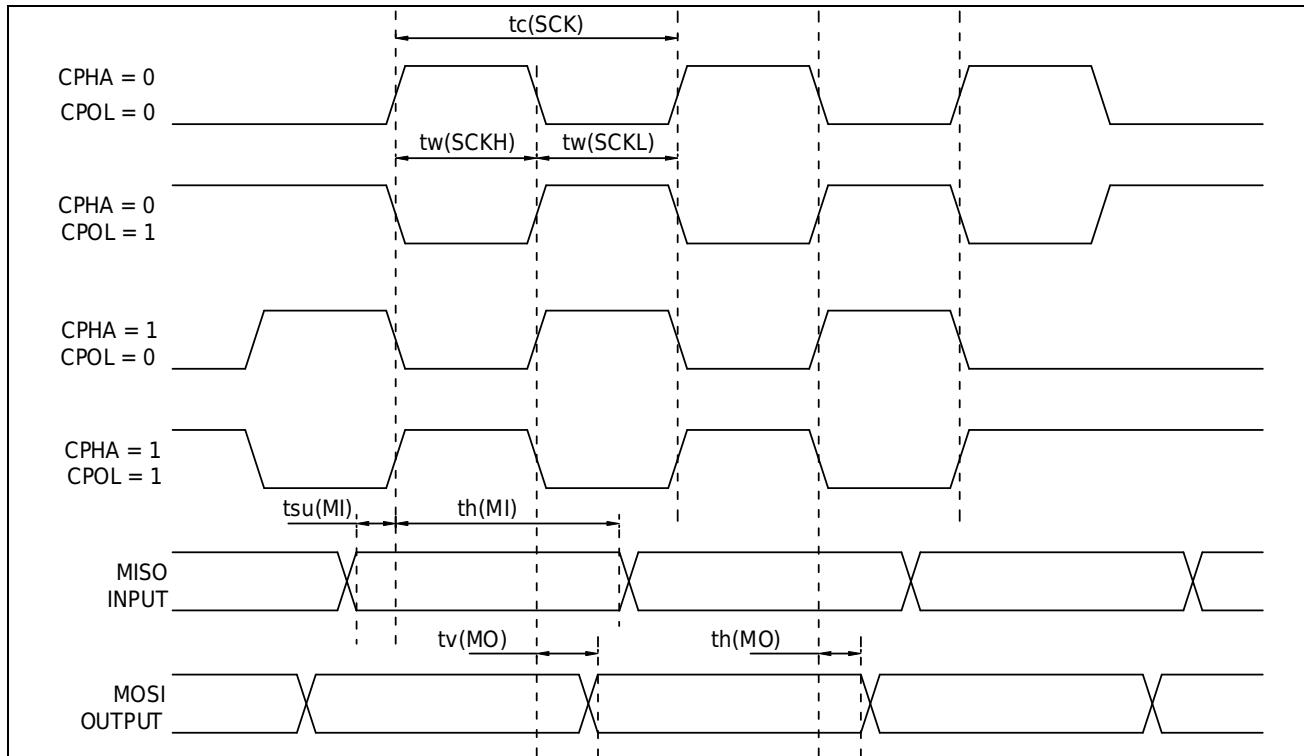


图 7-4 SPI 时序图 (主机模式)

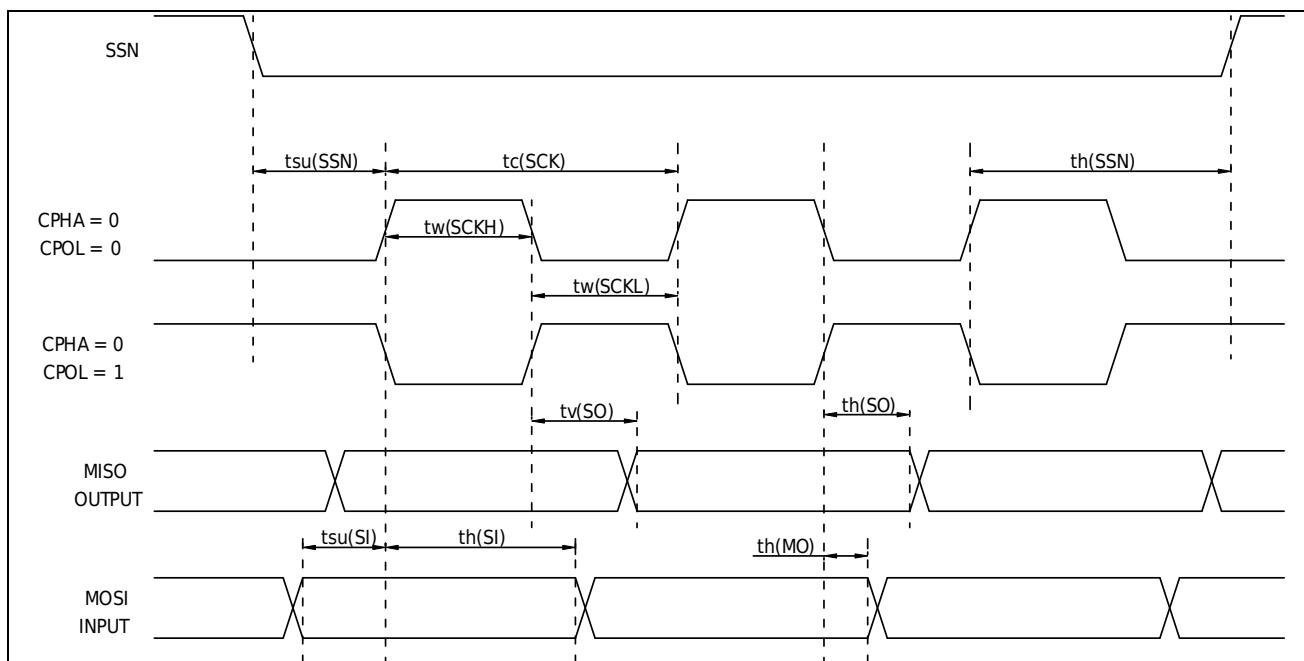


图 7-5 SPI 时序图 (从机模式 cpha=0)

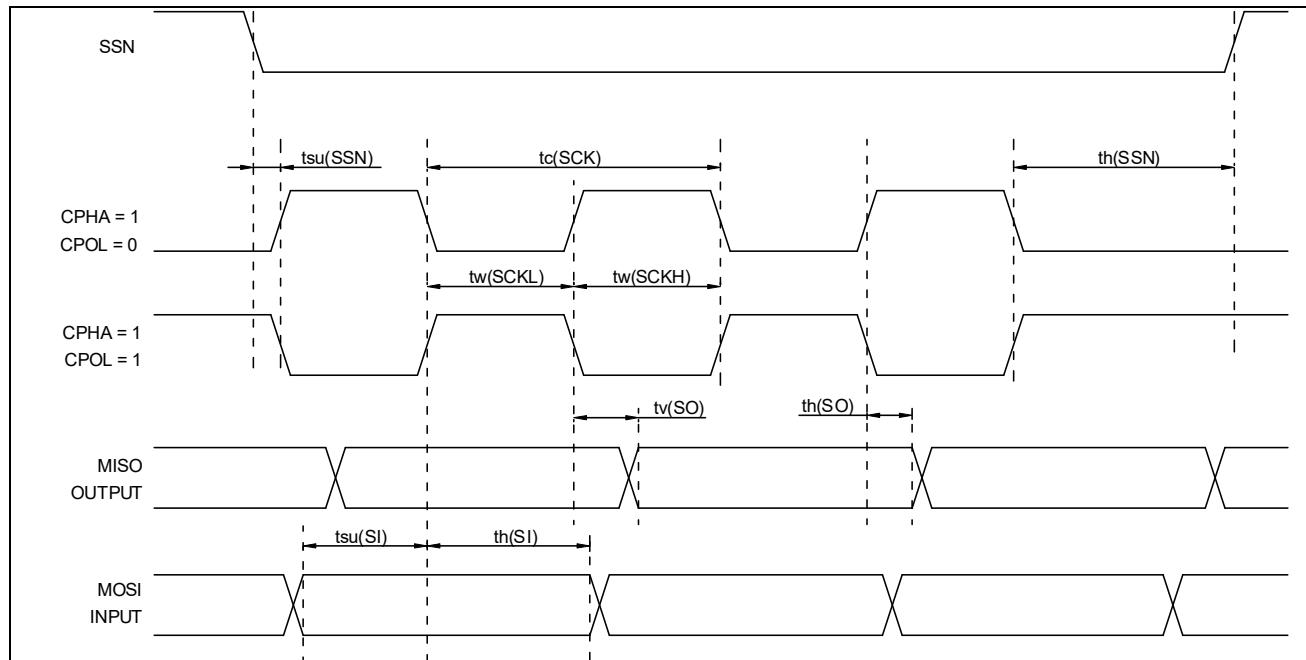
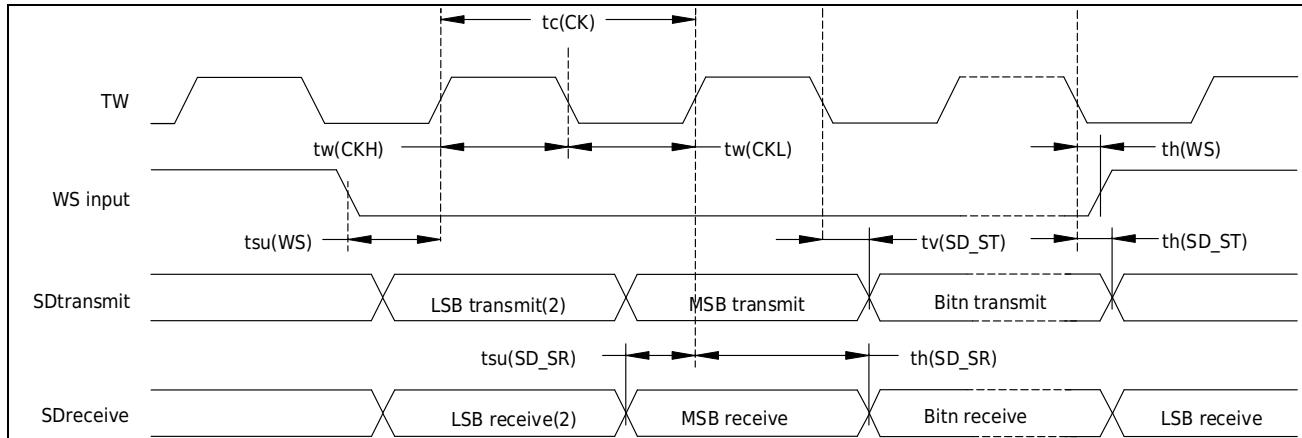


图 7-6 SPI 时序图 (从机模式 cpha=1)

7.3.21.3 I2S Features⁽¹⁾

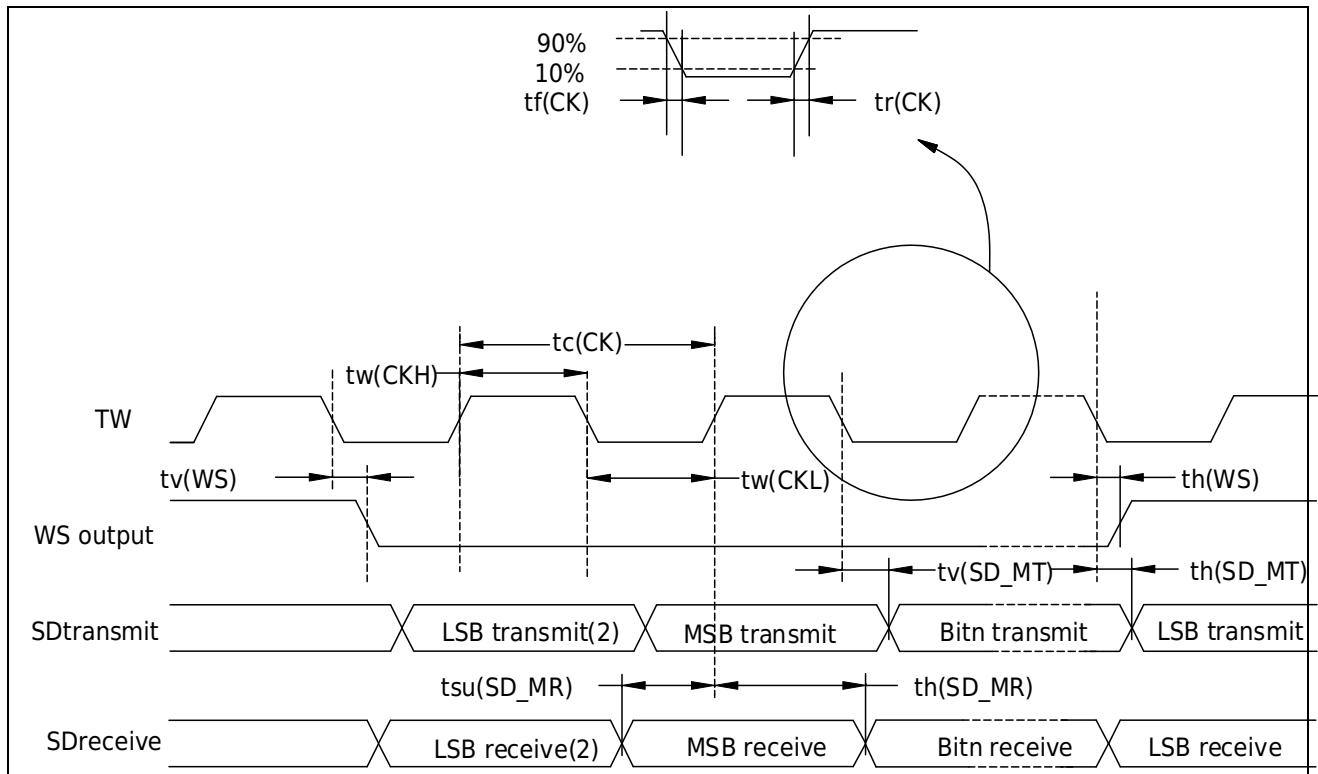
| 符号 | 参数 | 条件 | 最小值 | 最大值 | 单位 |
|------------------------------|-------------|---|-------|-------|-----|
| f_{ck} | I2S 时钟频率 | Master mode (data:16bits, audio freq 48kHz) | 1.597 | 1.601 | MHz |
| | | Slave mode | 0 | 6.5 | |
| $t_{r(ck)}$ | I2S 时钟上升时间 | Capacitive load $C_L=15\text{pF}$ | - | 10 | ns |
| $T_{f(ck)}$ | I2S 时钟下降时间 | | - | 12 | |
| $t_{w(ckh)}$ | I2S 时钟高电平时间 | Master $f_{pclk}=16\text{MHz}$, audio freq 48kHz | 306 | - | |
| $t_{w(cki)}$ | I2S 时钟低电平时间 | | 312 | - | |
| $t_{v(ws)}$ | WS 有效时间 | Master mode | 2 | - | |
| $T_h(ws)$ | WS 保持时间 | Master mode | 2 | - | |
| $T_{su(ws)}$ | WS 建立时间 | Slave mode | 7 | - | |
| $T_h(ws)$ | WS 保持时间 | Slave mode | 0 | - | |
| Duty(sck) | 从模式时钟占空比 | Slave mode | 25 | 75 | % |
| $T_{su(SD_MR)}$ | SD 输入建立时间 | Master receiver | 6 | - | ns |
| $T_{su(SD_SR)}$ | | Slave receiver | 2 | - | |
| $T_h(SD_MR)$ ⁽²⁾ | SD 输入保持时间 | Master receiver | 4 | - | |
| $T_h(SD_SR)$ ⁽²⁾ | | Slave receiver | 0.5 | - | |
| $T_v(SD_MR)$ ⁽²⁾ | SD 输出建立时间 | Master transmitter | - | 4 | |
| $T_v(SD_SR)$ ⁽²⁾ | | Slave transmitter | - | 20 | |
| $T_h(SD_MR)$ | SD 输出保持时间 | Master transmitter | 0 | - | |
| $T_h(SD_SR)$ | | Slave transmitter | 13 | - | |

1. 由设计保证，不在生产中测试。
2. 与 F_{PCLK} 相关，例如 $F_{PCLK}=10\text{M}$ $T_{PCLK}=1/F_{PCLK}=100\text{ns}$



1. Measurement points are done at CMOS levels: $0.3 \times V_{DDIOX}$ and $0.7 \times V_{DDIOX}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

图 7-7 I2S slave timing diagram



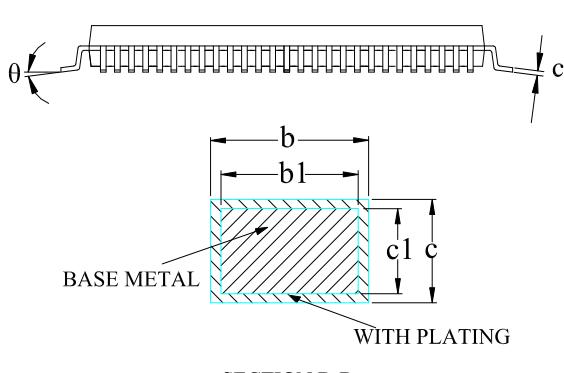
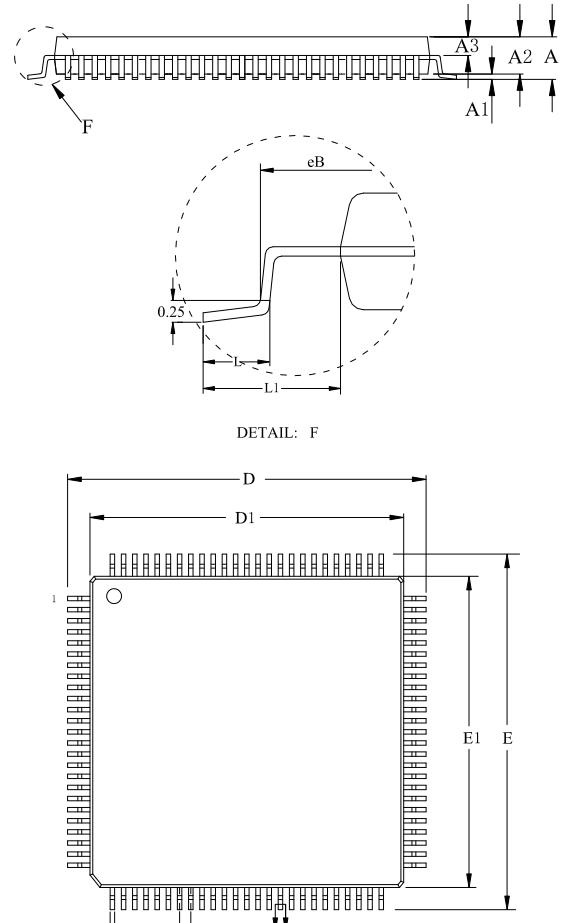
1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

图 7-8 I2S master timing diagram

8 Packaging Information

8.1 Package Dimensions

LQFP100 package

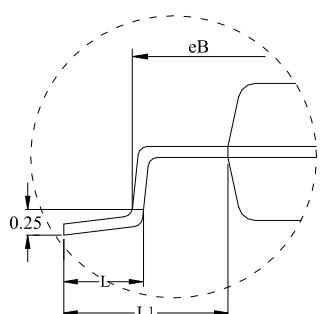
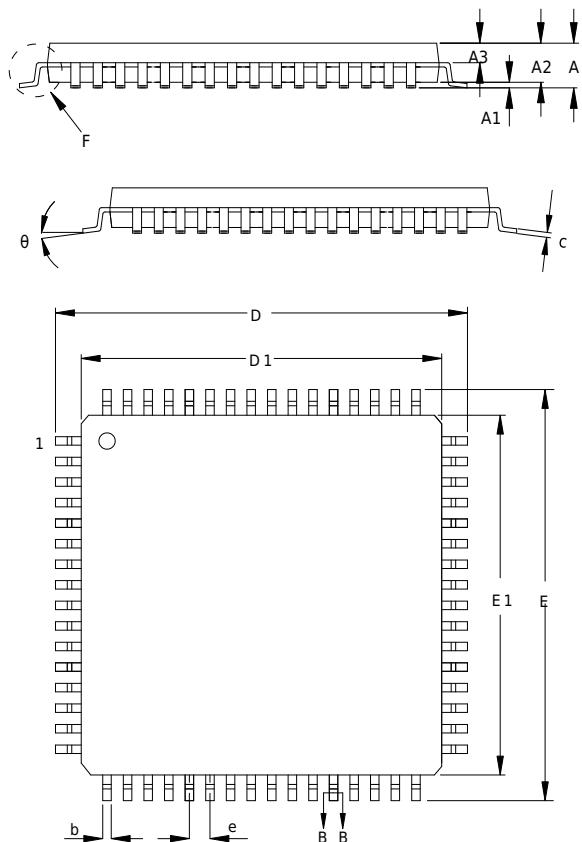


| Symbol | 14 x 14 Millimeter | | |
|--------|--------------------|-------|-------|
| | Min | Nom | Max |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | -- | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | -- | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.90 | 14.00 | 14.10 |
| eB | 15.05 | -- | 15.35 |
| e | 0.50BSC | | |
| L | 0.45 | -- | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | -- | 7° |

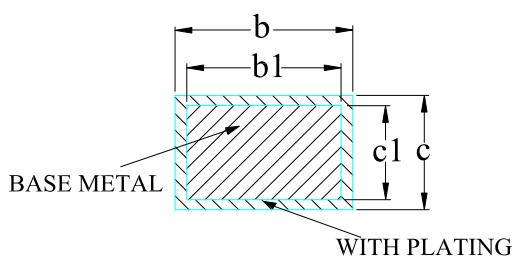
NOTE

- Dimensions "D1" and "E1" do not include mold flash.

LQFP64 package



DETAIL: F



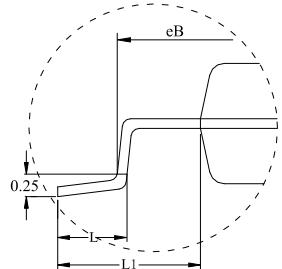
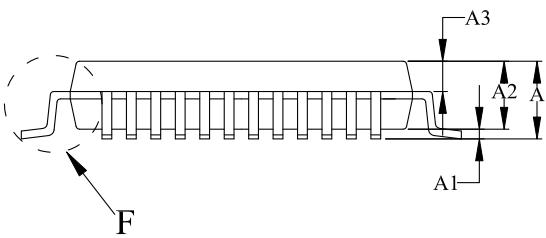
SECTION B-B

| Symbol | 10 x 10 Millimeter | | |
|----------|--------------------|-------|-------|
| | Min | Nom | Max |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | -- | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | -- | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 11.80 | 12.00 | 12.20 |
| D1 | 9.90 | 10.00 | 10.10 |
| E | 11.80 | 12.00 | 12.20 |
| E1 | 9.90 | 10.00 | 10.10 |
| eB | 11.05 | -- | 11.25 |
| e | 0.50BSC | | |
| L | 0.45 | -- | 0.75 |
| L1 | 1.00REF | | |
| θ | 0° | -- | 7° |

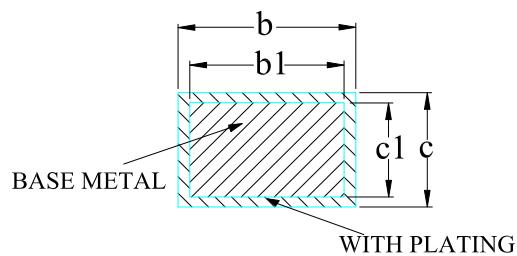
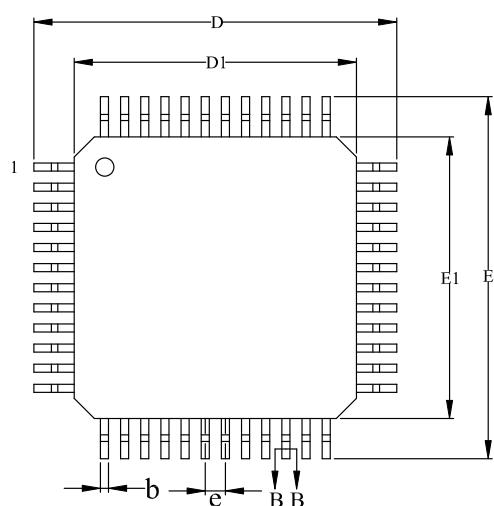
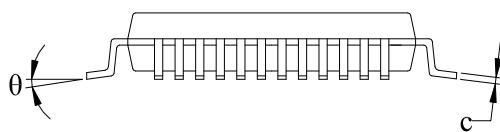
NOTE

- Dimensions "D1" and "E1" do not include mold flash.

LQFP48 package



DETAIL: F



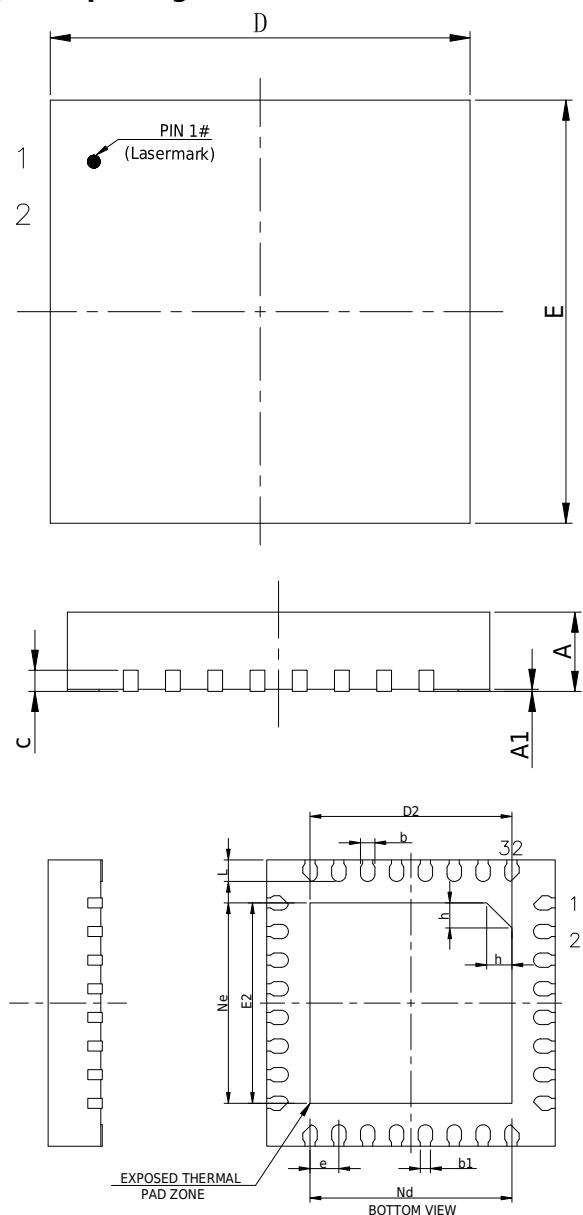
SECTION B-B

| Symbol | 7 x 7 Millimeter | | |
|----------|------------------|------|------|
| | Min | Nom | Max |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | -- | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | -- | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| e_B | 8.10 | -- | 8.25 |
| e | 0.50BSC | | |
| L | 0.40 | -- | 0.65 |
| L_1 | 1.00REF | | |
| θ | 0 | -- | 7° |

NOTE

- Dimensions "D1" and "E1" do not include mold flash.

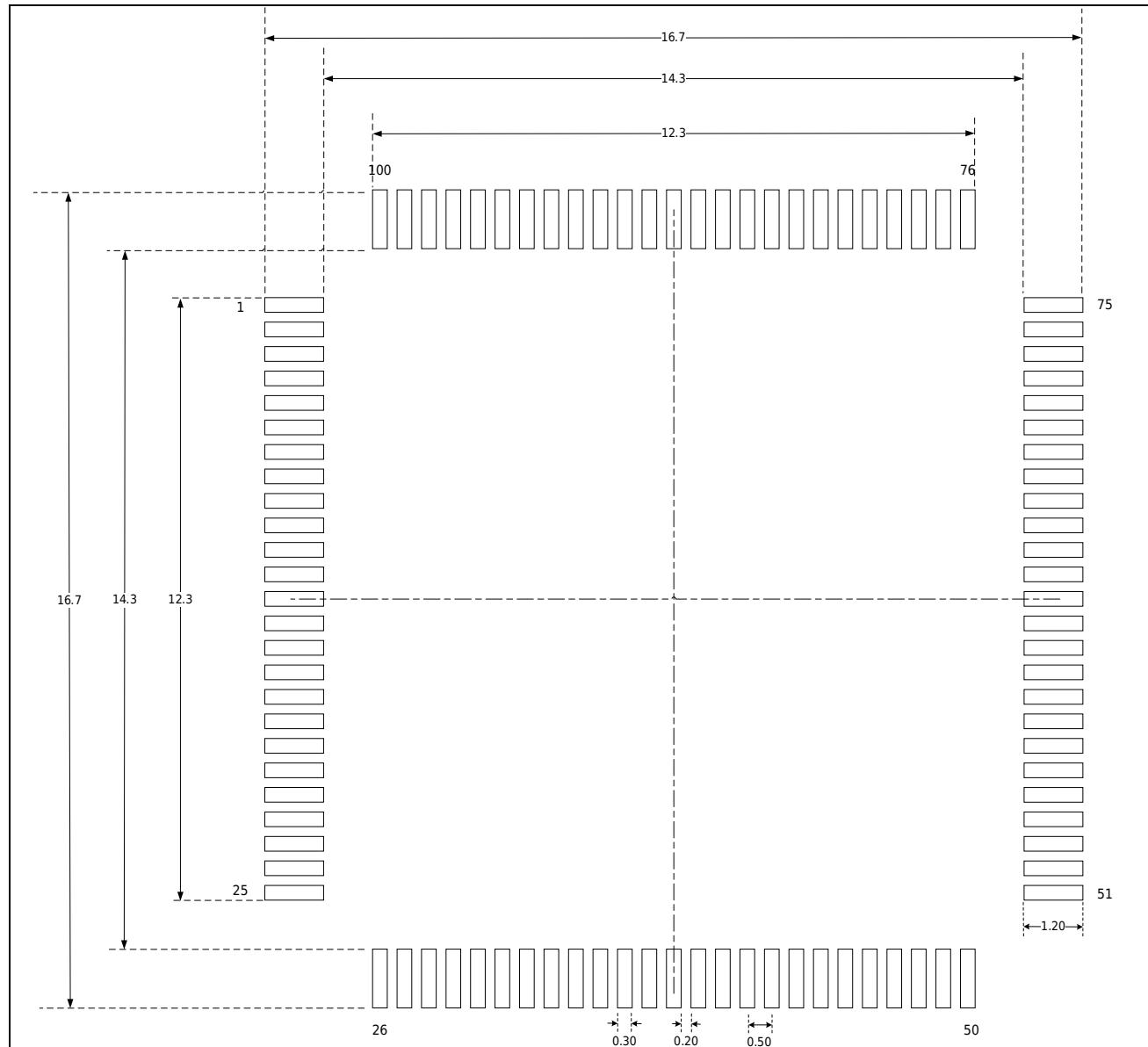
QFN32 package



| Symbol | 5 x 5 Millimeter | | |
|----------|------------------|------|------|
| | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| b1 | 0.16REF | | |
| c | 0.18 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.70 | 3.80 | 3.90 |
| e | 0.50BSC | | |
| Ne | 3.50BSC | | |
| Nd | 3.50BSC | | |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 3.70 | 3.80 | 3.90 |
| L | 0.25 | 0.30 | 0.35 |
| h | 0.30 | 0.35 | 0.40 |
| L/F 载体尺寸 | 4.10 x 4.10 | | |

8.2 Pad Diagram

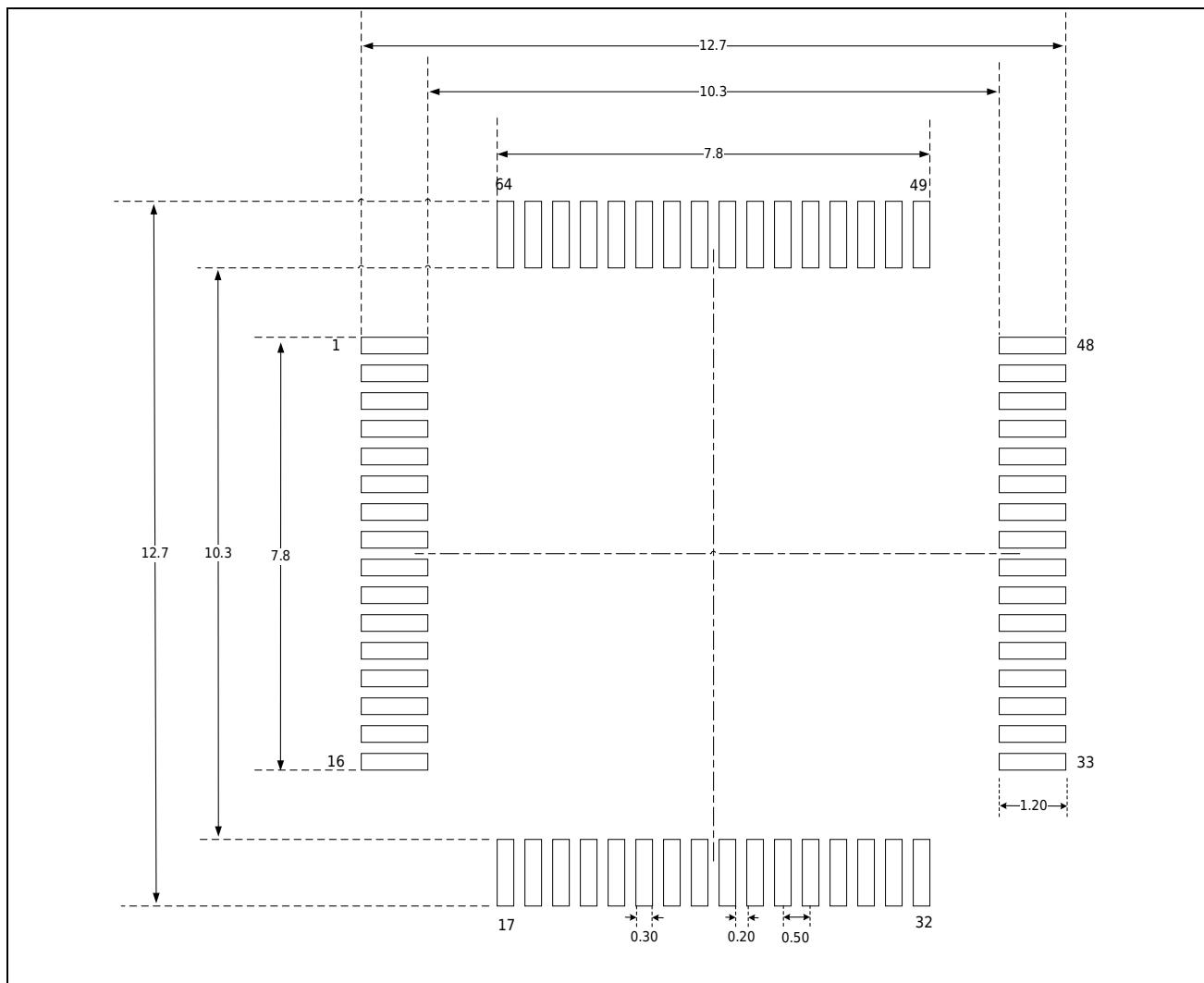
LQFP100 package (14mm x 14mm)



NOTE

- Dimensions are expressed in millimeters.
 - 尺寸仅做参考。

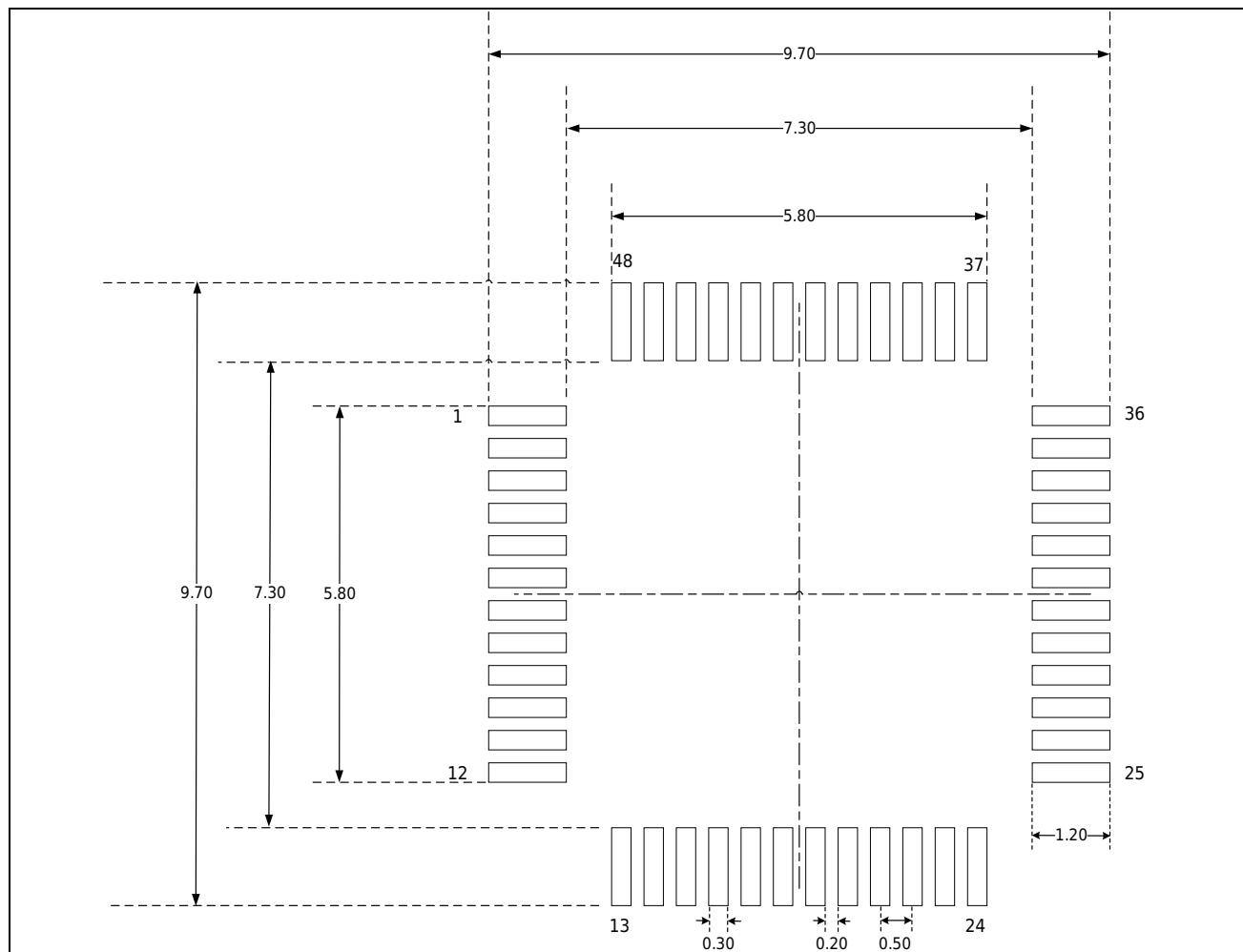
LQFP64 package (10mm x 10mm)



NOTE

- Dimensions are expressed in millimeters.
- 尺寸仅做参考。

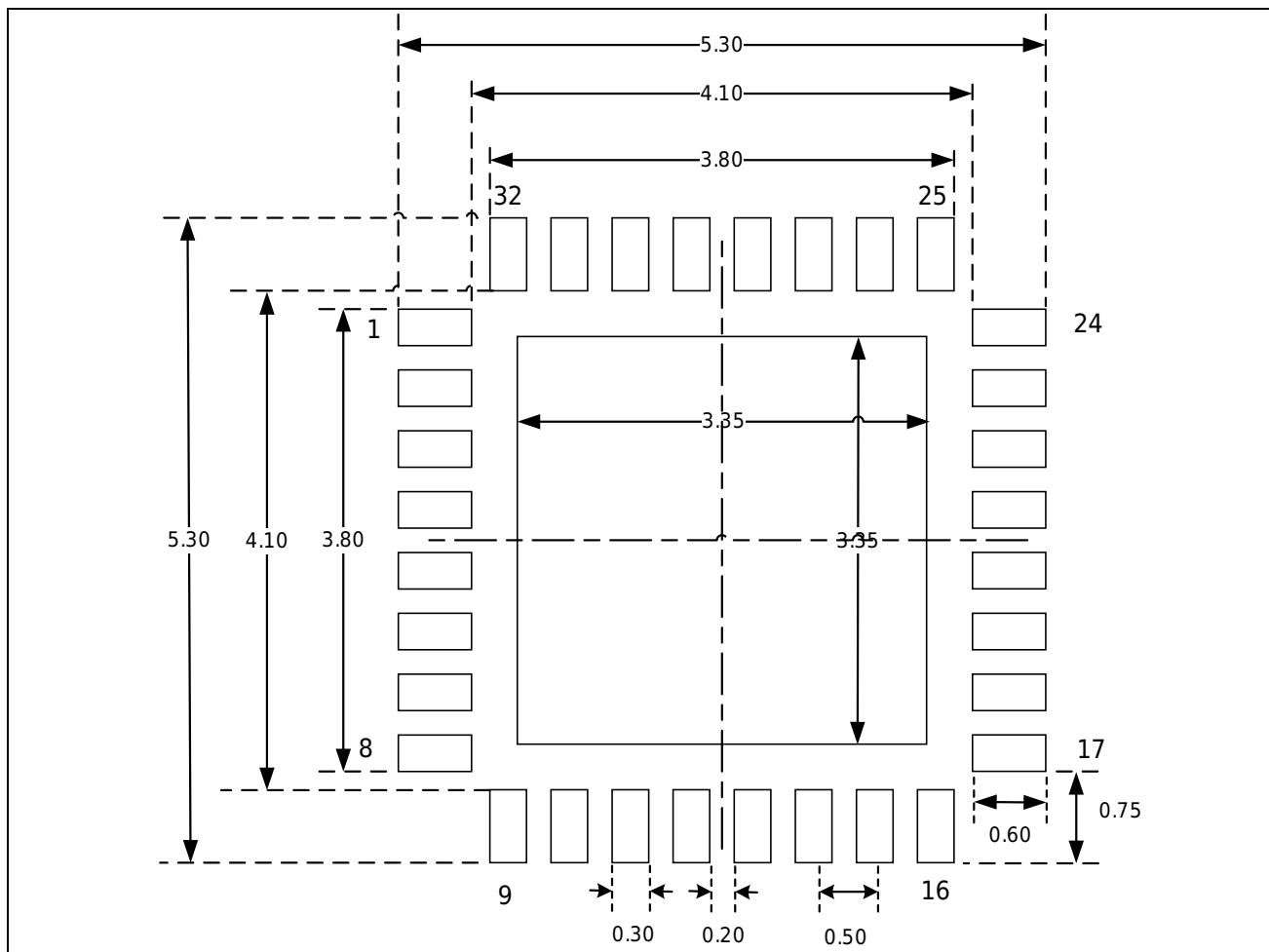
LQFP48 package (7mm x 7mm)



NOTE

- Dimensions are expressed in millimeters.
- 尺寸仅做参考。

QFN32 package (5mm x 5mm)



NOTE

- Dimensions are expressed in millimeters.
 - 尺寸仅做参考。

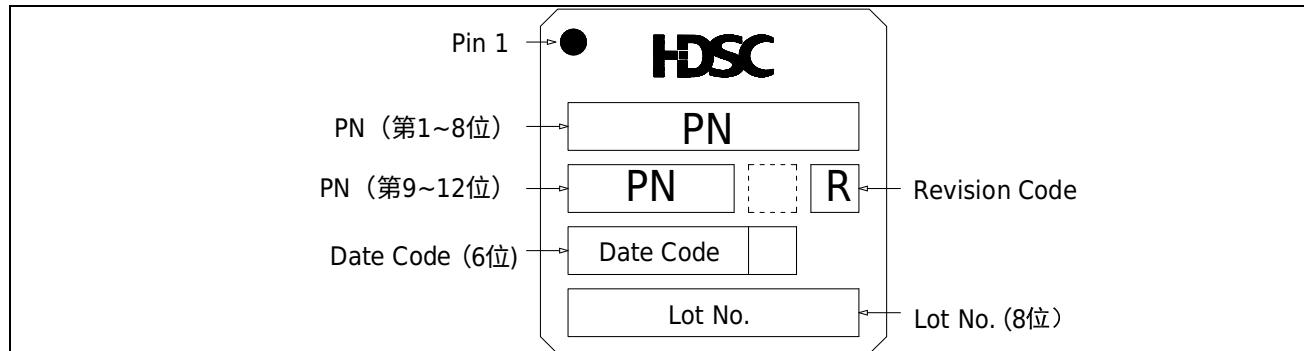
8.3 Marking Description

以下给出各封装正面丝印的 Pin 1 位置和信息说明。

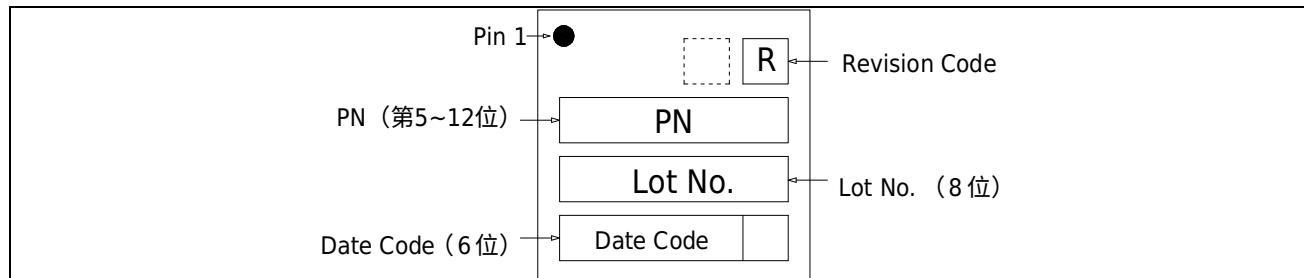
LQFP100 package (14mm x 14mm)

LQFP64 package (10mm x 10mm)

LQFP48 package (7mm x 7mm)



QFN32 package (5mm x 5mm)



注意：

- 上图空白框表示与生产相关的可选标记，本节不作说明。

8.4 Package Thermal Resistance

When the packaged chip works at a specified working environment temperature, the junction temperature T_j ($^{\circ}\text{C}$) on the chip surface can be calculated according to the following formula:

$$T_j = T_{\text{amb}} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip works, in $^{\circ}\text{C}$;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, in $^{\circ}\text{C}/\text{W}$;
- P_D is equal to the sum of the chip's internal power consumption and I/O power consumption, in W. The chip's internal power consumption is the product's $\text{IDD} \times \text{VDD}$, and the I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually, this part is very small and can be ignored.

When the chip works at a specified working environment temperature, the junction temperature T_j on the chip surface must not exceed the maximum allowable junction temperature T_J of the chip.

表 8-1 各封装热阻系数表

| Package Type and Size | Thermal Resistance Junction-ambient Value (θ_{JA}) | Unit |
|-----------------------------------|---|-----------------------------|
| LQFP100 14mm x 14mm / 0.5mm pitch | 50 +/- 10% | $^{\circ}\text{C}/\text{W}$ |
| LQFP64 10mm x 10mm / 0.5mm pitch | 65 +/- 10% | $^{\circ}\text{C}/\text{W}$ |
| LQFP48 7mm x 7mm / 0.5mm pitch | 75 +/- 10% | $^{\circ}\text{C}/\text{W}$ |
| QFN32 5mm x 5mm / 0.5mm pitch | 42 +/- 10% | $^{\circ}\text{C}/\text{W}$ |

9 Ordering Information

| Part Number | | HC32L072PATA-LQFP100 | HC32L072KATA-LQFP64 | HC32L072JATA-LQ48 | HC32L072FAUA-QN32TR | HC32L073PATA-LQFP100 | HC32L073KATA-LQFP64 | HC32L073JATA-LQ48 |
|-------------------|-----------|----------------------|---------------------|-------------------|---------------------|----------------------|---------------------|-------------------|
| Memory (bytes) | Flash | 128K | 128K | 128K | 128K | 128K | 128K | 128K |
| | RAM | 16K | 16K | 16K | 16K | 16K | 16K | 16K |
| I/O | | 86 | 50 | 36 | 22 | 86 | 52 | 38 |
| TIMER | GTIMER | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| | ATIMER | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | LPTIMER | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | PCNT | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | UART | 4 | 4 | 2 | 2 | 4 | 4 | 2 |
| | LPUART | 2 | 2 | 2 | 1 | 2 | 2 | 2 |
| | I2C | 2 | 2 | 2 | 1 | 2 | 2 | 2 |
| | SPI | 2 | 2 | 2 | 1 | 2 | 2 | 2 |
| | USB | ✓ | ✓ | ✓ | ✓ | ✓ | - | - |
| | CAN | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | I2S | 2 | 2 | 2 | 1 | 2 | 2 | 2 |
| Analog | ADC*12bit | 24ch | 23ch | 17ch | 10ch | 24ch | 23ch | 17ch |
| | DAC*12bit | 2ch | 2ch | 2ch | 2ch | 2ch | 2ch | 2ch |
| | OP | 5 | 5 | 3 | 1 | 5 | 5 | 3 |
| | Comp | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Display | LCD | - | - | - | - | 4*52/6*50/8*48 | 4*40/6*38/8*36 | 4*26 |
| Security | AES | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| LVD | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| LVR | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Votage | Vdd | 1.8~5.5V | 1.8~5.5V | 1.8~5.5V | 1.8~5.5V | 1.8~5.5V | 1.8~5.5V | 1.8~5.5V |
| Package | | LQFP100(14*14) | LQFP64(10*10) | LQFP48(7*7) | QFN32(5*5) | LQFP100(14*14) | LQFP64(10*10) | LQFP48(7*7) |
| Shipping form | | Tray | Tray | Tray | Tape | Tray | Tray | Tray |
| Product thickness | | 1.6mm | 1.6mm | 1.6mm | 0.75mm | 1.6mm | 1.6mm | 1.6mm |
| Pad spacing | | 0.5mm | 0.5mm | 0.5mm | 0.5mm | 0.5mm | 0.5mm | 0.5mm |

Before ordering, please contact the sales office for the latest mass production information.

Version Revision History

| Version | Date | Description |
|---------|------------|---|
| Rev1.00 | 2019/11/18 | First draft published. |
| Rev1.10 | 2019/12/25 | Updated the following information: ① Added QFN32 package; ② Typical application circuit diagram; ③ Illustrations and precautions for high-speed external clock XTH and low-speed external clock XTL; ④ Silkscreen description; ⑤ General working conditions description; ⑥ Ordering information. |
| Rev1.20 | 2020/04/10 | Updated the following information: ① Pin function description; ② Added AVCC/3 accuracy in ADC characteristics; ③ 44/45/47/48pin changes for HC32L073KATA; ④ 32/33/35/36pin changes for HC32L073JATA. |
| Rev1.30 | 2020/05/29 | Updated the following information: ① Corrected typos in 7.3.7.2; ② Added LCD controller; ③ RCL oscillator accuracy in 7.3.8.2; ④ Added low power timer description in Product Features. |
| Rev1.40 | 2020/06/30 | Updated the following information: ① Added I2S information in the pin function description; ② Corrected LPTIM to LPTIMO, LPTIMx_ETR to LPTIMx_EXT; ③ Unified the pin function names. |
| Rev1.50 | 2020/07/31 | Updated the following information: ① Added Sections 7.3.20, 7.3.21, 8.2, and 8.4; ② 7.3.11 Levels; ③ 7.3.13.2 Values of VIH and VIL. |
| Rev1.60 | 2020/09/30 | Updated the following information: ① Functional block diagram; ② Added SPI features and I2S features (1); ③ 1.4 description; ④ 7.3.14 VIL and VIH; ⑤ Added 7.3.13.3; ⑥ The number of OPAs for HC32L072FAUA is 1. |
| Rev1.70 | 2021/05/31 | Updated the following information: ① Modified the statement; ② Corrected the ANALOG function of PB04 in the pin function description; ③ tHD STA and tSU STO parameters in the I2C characteristics; ④ Data retention period in the memory characteristics; ⑤ Added the gm parameter in the external clock source characteristics. |
| Rev1.80 | 2022/03/09 | Company Logo updated. |
| Rev1.81 | 2022/08/13 | Updated the following information: ① 3.2 Pin function description, deleted the PF01 function mapping of TIM4_CHB; ② 7.3.14 RESETB pin characteristics, input filter pulse time modification. |
| Rev1.82 | 2023/06/21 | Updated the following information: ① The APB1 address range error in the storage area mapping diagram was modified. |
| Rev1.83 | 2024/06/25 | Updated the following information: ① Modified the number of ADC and VC channels in 1.29 and 1.31, deleted the 1.2V related description, and deleted the 1.2V related description in 7.3.16; ② Modified the storage temperature range in Table 7-3 Temperature Characteristics; ③ Added the "7.3.8.3 Internal Low-Speed Clock 10k Oscillator" section. |
| Rev1.84 | 2024/12/12 | Updated the following information: ① Updated the contents of chapters "7.3.7.3 High-speed external clock XTH" and "7.3.7.4 Low-speed external clock XTL". |
| Rev1.85 | 2025/03/28 | Updated the following information: ① Updated the relevant parameters in Table 7-16 SPI interface characteristics; ② Modified the maximum value of the input filtered pulse and the minimum value of the input non-filtered pulse in 7.3.14 RESETB pin characteristics. |