XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

32-bit microcontrollers

HC32L07x_F072 Series Notes

Application Notes

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Target customers

Product range	Product Model	Product range	Product Model
L Series	HC32L072 HC32L073	**F Series**	HC32F072

statement

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1 Summary

This document mainly introduces the precautions and workarounds for using the HC32L07x/ HC32F072 series chips.

2 Notes on HC32L07x/ HC32F072 Series

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2.1 System and Clock Considerations

2.1.1 The VCAP pin is not VBAT and cannot be connected to a power source. For the minimum capacitance to be connected, refer to the data sheet of each model.

ÿ Application Notes

a. VCAP is the core voltage filter pin and must be grounded through a capacitor. It cannot be used for other functions or left floating.

Note: Please refer to the data sheet of each series for the minimum allowable capacitance of each series.

b. Place the capacitor as close to the VCAP pin as possible.

2.1.2 Each DVCC and AVCC pin needs to be equipped with a decoupling capacitor, as close to the corresponding pin as possible.

ÿ Application Notes

Each DVCC and AVCC pin needs to be equipped with a decoupling capacitor as close to the corresponding power pin as possible.

The actual situation is determined.

2.1.3 BOOT pin: High level when powered on or reset, ISP programming mode; low level when powered on or reset,

User Mode

ÿ Application Notes

a. When in user mode, the BOOT pin must be a low level input when powered on or reset.

BOOT pin status, when input low level, directly enter the user main program, when input high level, enter the boot program (for ISP mode)

(UART) burning).

Note: If the BOOT pin is not at a low level during power-on or reset, the user main program cannot be entered.

b. It is not recommended to use the BOOT pin for other functions.

c. If you want to use the BOOT pin as a GPIO, please note that the BOOT peripheral circuit can keep the pin in the low state when powering on or resetting.

Pull status.

2.1.4 The NRESET pin has a weak pull-up internally, but from the perspective of system reliability, it is still recommended to connect an external reset circuit.

ÿ Application Notes

Inside the MCU, NRESET has a weak pull-up, but from the perspective of system reliability, it is still recommended to refer to the data sheet for the recommended circuit external reset

Circuit.

2.1.5 Causes of SWD interface failure

ÿ Reason description

a. The user main program enters deep sleep mode as soon as it is powered on.

b. Burn the user program and encrypt it. After the burning is completed and the device is powered on or reset again, SWD cannot be connected.

c. The chip cannot be connected and downloaded using SWD again due to an incorrect program.

d. Immediately after reset, the SWD interface is changed to the GPIO interface, causing the emulator or programmer to fail to connect.

ÿ Recovery Method

a. Use the online programming tool to erase the user program on the MCU using the chip erase method.

b. Use the offline programming tool to configure a normal sample, select chip erase and no encryption, and then download the program once.

c. For the above three situations a, c, d, during the debugging phase: you can add a delay of more than 1s at the beginning of main to

The next time you power on or reset, you can burn the program again through the SWD interface; or at the beginning of main by detecting an IO input

The external level determines whether to continue executing subsequent programs.

2.1.6 The UART pins used by the ISP mode of the MCU are fixed

ÿ Application Notes

a. This series ISP pin and SWD pin are multiplexed.

For details, please refer to the user manual of the online programmer or offline programmer.

2.1.7 I/O port voltage cannot be greater than Vcc

ÿ Application Notes

a. All I/O voltages cannot be greater than VCC.

Note: Engineers like to use PC+USB-UART+Serial Port Debug Assistant to view the data sent by UART.

If the voltage level is greater than the MCU power supply voltage VCC, there will be problems.

b. When the I/O pin is powered on before Vcc, or when the I/O pin is powered but Vcc is not, the voltage injected from the I/O pin will also

This may cause the MCU to run, but may not run properly. If this situation cannot be avoided, it is recommended to connect a suitable

The resistor limits the voltage and current injected into the MCU to prevent the MCU from operating in such a situation.

2.1.8 Chip Encryption

ÿ Application Notes

a. After the chip is encrypted, it cannot be simulated or downloaded. It is necessary to use the ISP interface and an online or offline programmer to perform a chip erase operation.

Simulation and downloading can then be resumed.

b. The encryption and decryption of this series is limited in number. After 64 cycles of encryption and decryption, the chip can no longer encrypt and decrypt.

2.1.9 External crystal oscillator circuit

ÿ Application Notes

a. The external crystal oscillator unit and matching capacitors should be as close to the chip as possible.

b. The external crystal oscillator signal line should be as short as possible. The line width should not be too thin, and the thinnest should not be less than the width of the chip pin.

c. There should be a complete ground cover on the layer adjacent to the crystal oscillator local circuit.

d. A ground wire should be used as a guard ring around the external crystal oscillator. The ground ring wire needs to be fully grounded (through ground holes) to reduce Mutual interference between external crystal oscillator signal and other signals.

e. The crystal oscillator circuit should pay attention to the cleanness of the local signal and avoid external interference. Try not to route wires near the crystal oscillator circuit or in adjacent layers, especially It is not allowed to run high-speed lines, power lines, clock lines, etc.

f. In harsh application environments, such as humid environments, in order to reduce the oscillation problem caused by leakage, it is necessary to place the crystal in the external oscillator area. Add coatings, such as conformal coatings, to the PCB boards.

2.1.10 XTH If a passive crystal oscillator is used

If you choose a passive crystal oscillator, it is recommended to choose a low ESR 16MHz~32MHz crystal.

2.1.11 XTH Configuration

ÿ Application Notes

a. In the program, the XTHI/XTHO pins should be set to analog functions.

b. After the program detects that the XTH stable flag is set, it needs to wait at least 10ms before using the XTH clock as the system clock or PLL clock source.

c. The external crystal oscillator should be matched with appropriate matching capacitors and have appropriate driving capability. If necessary, a current limiting resistor can be connected in series to the XTH_OUT pin.

2.1.12 XTL Configuration

ÿ Application Notes

a. In the program, the XTLI/XTLO pins should be set to analog functions.

b. If power consumption permits, XTL should use high drive capability, but the higher the drive capability, the greater the power consumption.

2.1.13 Frequency switching when using internal RCH needs to follow the steps described in the manual

ÿ Application Notes

Solution 1: When switching RCH, you must first adjust the HCLK frequency division, then gradually increase it, or gradually decrease it, and then adjust the HCLK frequency division.

The process of frequency cannot be completed in one step.

Solution 2: First switch to RCL as the system clock, then change the RCH frequency, and then switch back to RCH as the system clock.

Otherwise, it may affect the operation of user programs.

Please refer to the System Controller chapter of the reference manual for each family and the relevant application notes for details.

2.1.14 Notes on using external input clock

ÿ Application Notes

a. When using XTH external input (from XTHI), you need to set the XTHI pin as a digital input and SYSCTRL0.XTHEN to

1. At the same time, the XTHO pin is prohibited from being used as a GPIO and needs to be configured as an analog state;

When using XTL external input (from XTLI), you need to set the XTLI pin as digital input and SYSCTRL0.XTLEN to 1.

At the same time, the XTLO pin cannot be used as GPIO and needs to be configured as analog state.

2.2 Reset Controller

2.2.1 Reset flag needs to be initialized after power on

ÿ Application Notes

The bits of the reset flag register other than POR5V and POR15V are in an uncertain state after power-on and need to be initialized and cleared by software.

2.2.2 The corresponding control bit of the reset module needs to be written as 0 first and then as 1

ÿ Application Notes

To reset a peripheral module using the peripheral module reset control register, you need to write the corresponding bit control bit to 0 first and then to 1.

2.3 Flash

2.3.1 Address of internal Flash erase and write functions

ÿ Application Notes

Flash erase and write functions need to be within the Flash address range of 0~32K and cannot exceed it, or run in RAM, otherwise execute

Errors will occur during erase and write operations.

For details, refer to the application note: FLASH operation instructions.

2.3.2 Flash instruction fetch wait cycle

ÿ Application Notes

When HCLK ÿ 24 MHz: FLASH_CR.WAIT=0

24MHz ÿ HCLK ÿ 48MHz: FLASH_CR.WAIT=1

2.3.3 Flash erase and write operation time parameter configuration

ÿ Application Notes

The configuration of the FLASH erase-related time parameter register is strongly related to HCLK and should comply with the reference manual requirements.

2.4 Ultra-low power consumption

2.4.1 ADC processing before entering ultra-low power consumption

ÿ Application Notes

Before entering ultra-low power consumption, you need to turn off BGR first, then turn off ADC_EN, and then turn off the ADC peripheral clock to further reduce the power consumption in the ultra-low power consumption state.

2.4.2 I/O processing before entering ultra-low power consumption

ÿ Application Notes

a. For chips that are not packaged with the maximum PIN, refer to the maximum package and set the unpackaged pins to a fixed digital level (such as pull-up

For example, the 48pin of L136 should be set as 64pin, and the unpackaged

The pins.

b. The unused floating pins should also be processed as above.

c. The analog signal pins such as ADC that are already connected to the external circuit do not require additional processing during standby.

d. Output pins, for external circuits, should avoid sourcing or sinking current when in standby mode.

e. If you want to reduce standby power consumption, you can also refer to the above processing.

f. L07x/ F07x If the USB module is not used, the USB related pins can be grounded to achieve lower power consumption.

2.4.3 Re-debugging and re-burning after entering ultra-low power consumption

ÿ Application Notes

After entering ultra-low power mode, the SWD interface will be invalid and needs to be re-awakened or reset before burning the code before entering ultra-low power mode.

Or erase the original code.

Therefore, it is recommended that during the debugging phase, before entering DeepSleep, you can use a certain length of delay or while query, etc.

Waiting for the valid level and other methods to delay the time of entering DeepSleep again, so that it can be burned again. Or use online or offline programming

The serial port mode of the programmer will replace or erase the original program.

2.4.4 XTH as system clock, need to enter DeepSleep mode

ÿ Application Notes

When the external high-speed (passive) clock XTH is used as the system clock, before entering DeepSleep mode, you need to set it to use the internal high-speed clock after waking up.

Clock function (such as WAKEUPBYRCH or WAKEUPCLK control bit in SYSCTRL_CRx register), after waking up, the system runs at the internal high-speed clock, and then enables and switches XTH according to the steps required by the reference manual.

2.4.5 PLL as system clock, need to enter DeepSleep mode

ÿ Application Notes

When PLL is used as the system clock, before entering DeepSleep mode, you need to switch the system clock to the internal high-speed clock (such as RCH).

And turn off BGR. After waking up, the system runs at the internal high-speed clock, and then you need to use software to switch the system clock to the PLL clock.

2.5 ADC

2.5.1 Analog power pin processing

ÿ Application Notes

a. AVCC/DVCC/AVSS/DVSS separation is recommended to improve ADC accuracy.

b. AVCC needs to be the same voltage as DVCC.

c. When using the internal reference voltage, AVCC must be greater than the internal reference voltage +0.3V.

d. The external reference voltage REF must not be greater than AVCC.

2.5.2 Operating Voltage and Sampling Rate

ÿ Application Notes

The sampling rate of the ADC has requirements on the operating voltage. For details, please refer to the ADC section of the reference manual.

2.5.5 The voltage of the ADC signal cannot exceed the ADC reference voltage

ÿ Application Notes

The input voltage of the ADC pin cannot exceed the ADC reference voltage.

2.5.6 Effective methods to improve ADC sampling accuracy

ÿ Application Notes

a. If a more accurate reference voltage can be provided externally, it is recommended to use an external reference voltage;

b. Reduce the sampling signal impedance;

c. For signals with small changes, try to reduce the sampling rate as much as possible while meeting the sampling time requirements;

d. Avoid using the internal follower BUF when the signal impedance is appropriate or the signal strength is sufficient;

e. Turn off unused digital circuits as much as possible during ADC sampling;

f. I/Os in the same group or I/Os with ADC functions should not be reused as high-frequency output or input signal pins.

2.5.7 Notes on using ADC 1Msps sampling rate

ÿ Application Notes

When the ADC uses a 1 Msps sampling rate, it is necessary to comprehensively consider factors such as the driving capability of the sampled signal and the external input impedance.

Please refer to the relevant description in the data sheet.

When the driving capability of the sampled signal is weak, the external input impedance is large, and the sampling rate is too high, the channel with a large voltage difference before and after scanning the sampling will be

When there are voltage spikes on some channels, or the ADC sampling value is inaccurate during single or scan sampling, you need to consider reducing the sampling rate.

Measures such as increasing the sampling rate, enhancing the driving capability of the sampled signal or reducing the input impedance can be taken.

2.6 LCD

2.6.1 For screens with higher driving capability or power consumption requirements, external resistor or capacitor mode needs to be selected

ÿ Application Notes

a. For LCD applications that require higher driving capability, or applications with poor display quality using 8COM, it is recommended to use the external resistor mode.

This mode can provide stronger driving capability.

b. For LCD applications with higher power consumption requirements, the external capacitor mode can be considered.

2.6.2 COM2/COM3 of LCD packaged in L073-LQFP100 needs to be remapped to PF6 and PA15

ÿ Application Notes

The COM2/COM3 pins of the HC32L073PATA-LQFP100 package are different from those of other MCU series, and the configuration is slightly different.

Remapped to PF6 and PA15.

2.6.3 Due to BOOT pin limitation, all SEGs cannot be used

ÿ Application Notes

The I/O of the BOOT pin is the SEG30 function. If other SEG pins are sufficient, it is recommended not to use the BOOT pin as the SEG function.

2.7 BGR

2.7.1 BGR related modules

ÿ Application Notes

a. When using ADC/OPA/PLL, VC high power consumption mode, you need to turn on the BGR module first. After turning on the BGR, it takes a period of time to stabilize.

For specific times, please refer to the reference or data manual.

2.8 I2C

2.8.1 At I2C 1M rate, the time of THD.STA and TSU.STO does not conform to the standard protocol, and the time of other rates is redundant.

The rest is smaller

ÿ Application Notes

At high speed (1M rate), the time of THD.STA and TSU.STO does not conform to the standard protocol, and the time redundancy at other rates is also small.

Please refer to the data sheet of each model.

2.9 SPI

2.9.1 Bit0 and bit1 of SPI_CR2 register cannot be written to 0

ÿ Application Notes

Please refer to the reference manual. Bit0 and bit1 of SPI_CR2 cannot be written to 0 and must remain 1.

2.10 LVD

2.10.1 The LVD input is connected to the negative phase of the LVD comparator, and the reference voltage is connected to the positive phase of the LVD comparator.

ÿ Application Notes

The LVD input is connected to the negative phase of the LVD comparator, and the reference voltage is connected to the positive phase of the LVD comparator.

A trigger occurs when the monitored voltage changes from above the threshold voltage to below the threshold voltage.

2.11 WDT

2.11.1 Stopping Problem after WDT is Enabled

ÿ Application Notes

The WDT of the MCU models listed in the table cannot be stopped after it is started, so after entering the ultra-low power state, it is necessary to wake up and feed the dog periodically.

2.11.2 The WDT clock uses a dedicated 10K clock. It is recommended that the WDT counter count value reaches half of the overflow value before Clear WDT

ÿ Application Notes

The WDT of the MCU models listed in the table uses a dedicated 10K clock. It is recommended to use it when the count value of the WDT counter reaches the overflow value.

Clear WDT before half of the time.

2.12 GPIO

2.12.1 SWD pin multiplexing as GPIO

ÿ Application Notes

a. The SWD pin is in SWD function by default after power-on or reset. If you want to change it to GPIO function, you need to

The switch is set in SYSCTRL.CR1. Note that the write protection register must be operated before switching. The driver library of each model provides an interface for operation.

Port function.

b. Once it is changed to GPIO, the SWD function cannot be used. Therefore, in the code development stage, it is best to add a software delay before switching.

The change must be made immediately after power-on or reset, otherwise the next SWD mode programming or simulation will fail to download the code.

c. Changing SWD to I/O does not encrypt the chip and cannot prevent others from reading the code on the chip.

To encrypt, you need to select the [Chip Encryption] function when configuring the offline programmer or using the online programming tool to burn.

2.12.2 GPIO is directly connected to the external interface. If there is live plugging and unplugging, a protection circuit is required.

ÿ Application Notes

If the MCU's I/O is used as an external interface pin, the pin is directly connected to the interface and may be plugged and unplugged while powered, such as UART.

Add a protection circuit between the interface and the MCU to avoid damaging the MCU.

2.12.3 When IO is used as GPI function, there is no input filtering

ÿ Application Notes

a. When the pins of the MCU series are used as GPIO digital inputs, they do not contain input hardware filtering functions.

When this happens, you need to consider whether to configure a hardware input filter circuit outside the MCU.

b. When I/O is multiplexed as other IP function pins, please refer to the reference manual of each series model to see whether there is filtering.

2.12.4 IO internal pull-up and pull-down resistors

The internal pull-up and pull-down resistors are MOS resistors. Under 3.3V and 5V power supply conditions, the resistance values are different. If the user needs precise pull-up and pull-down,

Or when pulling up or down with a small resistance, you need to consider adding a pull-up or pull-down resistor outside the chip.

2.12.5 GPIO number corresponding to BOOT pin

ÿ Application Notes

a. The GPIO pin number corresponding to the BOOT pin of this series of MCUs is PF11.

c. It is not recommended to use the BOOT pin for other functions. If used for other functions, please note that the peripheral circuit of BOOT can

Leave this pin pulled down.

d. When processing the floating IO state before entering ultra-low power consumption, pay attention to the processing method of the BOOT pin. The BOOT pin is externally connected

The resistor is pulled down to ground.

2.13 DMA

2.13.1 For MCUs with DMA function, if you want to output data from GPIO via DMA, you need to set the GPIO bus to AHB bus (GPIO_CTRL2.ahb_sel)

ÿ Application Notes

The GPIO input/output value register has two bus control modes: FAST IO and AHB mode.

To output, you need to set the GPIO bus to AHB bus (GPIO_CTRL2.ahb_sel).

2.14 VC

2.14.1 Only VC0 and VC1 support the resistor voltage divider function

ÿ Application Notes

This series of MCUs has more than 2 VC comparators, but only VC0 and VC1 support resistor voltage division as the negative input function.

2.14.2 Notes on using internal filter time

ÿ Application Notes

The filtering function inside the VC of this series of MCU uses the counting clock RC150K clock, which has low precision.

The filter time set by the filter may have a large deviation, which needs to be considered when designing and using. If necessary, the input signal can be used with an external filter.

Wave circuit.

2.15 OPA

2.15.1 OPA does not have zero calibration function

ÿ Application Notes

This series of MCUs with OPA function do not have the zero calibration function.

2.16 USB

2.16.1 USB_DP and USB_DM cannot be reused as IO functions

ÿ Application Notes

This series of MCUs has USB function, and its USB pins are dedicated pins and cannot be reused as GPIO.

2.17 Timer

2.17.1 General purpose timer M23CR register usage notes

ÿ Application Notes

The DIR bit in the M23CR register of the general timer TIM0/1/2/3 can be written only in sawtooth mode, and is read-only and disabled in other modes.

Stop writing.

Note: ARM processors use a "Load-Store architecture", so any write operation to a register bit will be written to the CPU.

The instruction is ultimately expressed as a write operation to all bits of the register.

When using it, please follow one of the following principles:

1) The M23CR register is only configured during initialization. Do not write to it at other times.

2) In non-sawtooth mode, after the timer is enabled, if any write operation is performed on any bit other than DIR in this register, the timer must be avoided.

Number of overflow and underflow points.

2.18 RTC

2.18.1 Notes on reading and writing the RTC counter register by setting RTC_CR1.WAIT

For L07x series only:

ÿ Application Notes

When using the RTC_CR1.WAIT setting to read and write the RTC counter register, the alarm interrupt and periodic interrupt must be avoided. It is recommended to operate in the RTC interrupt function and avoid being interrupted by other high-priority interrupts.

Note: ARM processors use a "Load-Store architecture", so any write operation to a register bit will be written to the CPU.

The instruction is ultimately expressed as a write operation to all bits of the register.

Version Revision History

Version Number	Revision Date	Revision Content
Rev1.00	2023/04/28	Initial version released.
Rev1.01	2023/05/25	1) Added “Timer” section. 2) In the “I2C” section, “THO.STA” was changed to “THD.STA”.
Rev1.02	2024/04/19	1) "System and Clock Considerations" chapter: Added precautions for using external input clocks. 2) “ADC” chapter: added the precautions for using ADC 1 Msps sampling rate. 3) "BGR" chapter: Modify the description of BGR related module precautions. 4) "GPIO" section: Delete "When the external crystal oscillator is not in use, the pin can be used as GPIO" Precautions content. 5) “VC” chapter: Added the precautions for using the internal filter time of VC. 6) Added RTC_CR1.WAIT precautions in the “RTC” chapter.
Rev1.03	2024/09/02	1) System and Clock section: Modify the recommended frequency range of XTH if a passive crystal oscillator is used. 2) Ultra-low power consumption section: Added XTH as system clock, which requires entering DeepSleep mode; To add PLL as the system clock, you need to enter DeepSleep mode.
Rev1.04	2025/02/20	In the "System and Clock Considerations" section, modified the description of "Precautions for Using External Input Clocks".