XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32F072 Series

32-bit ARM® Cortex®-M0+ Microcontroller

Datasheet

Rev1.85 March 2025

Features

- 48MHz Cortex-M0+ 32-bit CPU platform
- HC32F072 series has a flexible power management system, Low power performance:
  - 5μA @ 3V Deep-sleep mode: all clocks off, power-on reset active, IO state retained, IO interrupt active, all registers, RAM and CPU data save state power consumption
  - 12μA@32.768 kHz low speed working mode: CPU running, peripherals off, running program from FLASH
  - 40μA/MHz@3V@24MHz sleep mode: CPU stop, peripherals off, main clock running
  - 140μA/MHz@3V@24MHz working mode: CPU running, peripherals off, running program from FLASH
  - 4μs wake-up time makes mode switching more flexible and efficient, and the system reacts more quickly
- 128K byte FLASH memory, with erase and write protection function, support ISP, ICP, IAP
- 16K bytes RAM memory with parity check to enhance system stability
- General I/O pins (86IO/100PIN, 50IO/64PIN, 36IO/48PIN, 25IO/32PIN)
- Clock, crystal
  - External high-speed crystal oscillator 8 - 32MHz
  - External low-speed crystal 32.768kHz
  - Internal high-speed clock 4/8/16/22.12/24MHz
  - Internal low-speed clock 32.8/38.4kHz
  - PLL clock 8 - 48MHz
  - Internal high-speed USB clock 48MHz
  - Hardware supports internal and external clock calibration and monitoring
- Timer/counter
  - 3 general-purpose 16-bit timers, support 1 set of complementary PWM output, support 2 times main frequency PWM output, support up to 96MHz PWM output
  - 1 advanced 16-bit customizer, supports 3-phase complementary PWM output, supports 2 times main frequency PWM output, supports up to 96MHz PWM output
  - 3 high-performance 16-bit timers/counters, support PWM complementary, dead zone protection function
  - 1 programmable 16-bit timer PCA, support 5-channel capture and compare, 5-channel PWM output
  - 1 20-bit programmable watchdog circuit, built-in dedicated 10kHz oscillator to provide WDT counting
- Communication Interface
  - 4-channel UART standard communication interface
  - 2-channel LPUART low power communication interface, can work in deep sleep mode
  - 2-channel SPI standard communication interface
  - 2-channel I2C standard communication interface
  - 2-channel I2S audio communication interface
  - 1 channel Crystal-less USB Full Speed Device
  - 1 channel CAN 2.0B standard communication interface
- Buzzer frequency generator, support complementary output
- Hardware CRC-16/32 module
- Hardware 32-bit divider
- AES-128/192/256 hardware coprocessor
- TRNG true random number generator
- 2- channel DMAC
- Globally unique 10-byte ID number
- 12-bit 1Msps sampling high-speed and high-precision SARADC, built-in operational amplifier, can measure high output impedance signals
- 2-channel 12-bit 500Ksps DAC
- Integrate 5 multi-function operational amplifiers, of which two OPAs can be used as the output buffer of 2-channel DACs
- Integrated 3-channel voltage comparators with 6-bit DAC and programmable comparison reference
- Integrated low voltage detector, can be configured with 16-step comparison voltage, can monitor port voltage and power supply voltage
- SWD debugging solution, providing a full-featured debugger
- Working conditions: -40 ~ 85 ℃, 1.8 ~ 5.5V
- Package form: LQFP100/64/48,QFN32

Support Model

HC32F072PATA-LQFP100	HC32F072KATA-LQFP64
HC32F072JATA-LQ48	HC32F072FAUA-QN32TR

Statement

★ Xiaohua Semiconductor Co., Ltd. (hereinafter referred to as "XHSC") reserves the right to change, correct, enhance, modify Xiaohua Semiconductor products and / or this document at any time without prior notice. Users can get the latest information before placing orders. XHSC products are sold in accordance with the terms and conditions of sale set forth in the Basic Contract for Purchase and Sales.

★ It is the customer's responsibility to select the appropriate XHSC product for your application and to design, validate and test your application to ensure that your application meets the appropriate standards and any safety, security or other requirements. The customer shall be solely responsible for this.

★ XHSC hereby acknowledges that no intellectual property license has been granted by express or implied means.

★ The resale of XHSC Products shall be invalidated by any warranty commitment of XHSC to such Products if its terms are different from those set forth herein.

★ Any graphics or words marked “®” or “™”are trademarks of XHSC. All other products or services shown on XHSC products are the property of their respective owners.

★ Information in this notification replaces and replaces information in previous versions.

Table of Contents

Table Index

Graph Index

1 Introduction

The HC32F072 series is a general MCU with a wide voltage operating range. Integrate 12-bit 1Msps high-precision SARADC, 2 12-bit DACs and integrated comparator, operational amplifier, built-in high-performance PWM timer, multiple UART, SPI, I2C, I2S, USB, CAN and other rich communications It has built-in information security modules such as AES and TRNG, which have the characteristics of high integration, high anti-interference, and high reliability. The core of this product adopts the Cortex-M0+ core, cooperates with mature Keil & IAR debugging and development software, supports C language, assembly language, and assembly instructions.

General MCU typical applications

It can be widely used in various market applications: such as human-computer interaction, handheld devices, game peripherals, printers, video intercom and other smart home applications.

1.1 32-bit CORTEX M0+ core

The ARM® Cortex®-M0+ processor is derived from Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhrystone MIPS/MHz. At the same time, a number of new designs have been added to improve debugging and tracing capabilities, reduce the number of each instruction cycle (IPC) and improve the two-stage pipeline for Flash access, and incorporate energy-saving and consumption-reducing technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debugger.

Cortex-M0+ includes a hardware debugging circuit that supports 2-pin SWD debugging interface.

ARM Cortex-M0+ features:

Instruction Set	Thumb / Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark / MHz
Performance efficiency	0.95 DMIPS / MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports 4 hard interrupts (break points) and 2 watch points (watch points)

1.2 128K Byte FLASH

Built-in fully integrated FLASH controller, no need for external high voltage input, high voltage generated by the fully built-in circuit for programming Support ISP, IAP, ICP functions.

1.3 16K Byte RAM

According to different power consumption modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

1.4 Clock system

A high-precision internal clock RCH with a configurable frequency of 4-24MHz. Under the configuration of 24MHz, the wake-up time from low power consumption mode to working mode is 4μs, and the frequency deviation within the full voltage and full temperature range is small, and it is not necessary to connect an expensive high-frequency crystal.

An external crystal oscillator XTH with a frequency of 8-32MHz.

An external crystal XTL with a frequency of 32.768kHz.

An internal clock RCL with a frequency of 32.8/38.4kHz.

A PLL with 8-48MHz output frequency.

1.5 Operating mode

1) Active Mode: CPU running, peripheral function modules running.
2) Sleep Mode: The CPU stops running, and the peripheral function modules run.
3) Deep sleep Mode: The CPU stops running, the high-speed clock stops, and the low-power function modules run.

1.6 Port controller GPIO

It can provide up to 86 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by independent control register bits and supports FAST IO. Supports edge-triggered interrupt and level-triggered interrupt, which can wake up the MCU to work mode from various deep sleep modes. Support position, clear, and clear operations. Support Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 18mA. All general-purpose IOs can support external asynchronous interrupts.

1.7 Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs; it has four interrupt priority levels, can handle complex logic, and can perform real-time control and interrupt processing.

The 32 interrupt entry vector addresses are:

Interrupt vector number	Interrupt source
[0]	GPIO_PA
[1]	GPIO_PB
[2]	GPIO_PC/GPIO_PE
[3]	GPIO_PD/GPIO_PF
[4]	DMAC
[5]	TIM3
[6]	UART0/UART2
[7]	UART1/UART3
[8]	LPUART0
[9]	LPUART1
[10]	SPI0/I2S0
[11]	SPI1/I2S1
[12]	I2C0
[13]	I2C1
[14]	TIM0
[15]	TIM1
[16]	TIM2
[17]	Reserve
[18]	TIM4
[19]	TIM5
[20]	TIM6
[21]	PCA
[22]	WDT
[23]	Reserve
[24]	ADC/DAC
[25]	Reserve
[26]	VC0/VC1/VC2/ LVD
[27]	USB
[28]	CAN
[29]	Reserve
[30]	RAM FLASH
[31]	CLKTRIM /CTS

1.8 Reset controller RESET

This product has 7 reset signal sources, each reset signal can make the CPU run again, most of the registers will be reset again, and the program counter PC will point to the starting address.

	Reset source
[0]	Power-on and power-down reset POR BOR
[1]	External Reset Pin reset
[2]	WDT reset
[3]	PCA reset
[4]	Cortex-M0+ LOCKUP hardware reset
[5]	Cortex-M0+ SYSRESETREQ software reset
[6]	LVD reset

1.9 DMA controller DMAC

The DMAC (Direct Memory Access Controller) function block can transmit data at high speed without passing through the CPU. Using DMAC can improve system performance.

- The DMAC is equipped with an independent bus, so even when the CPU bus is used, the DMAC can also perform transfer operations.
- Composed of 2 channels, capable of performing 2 independent DMA transfers.
- The transmission destination address, transmission source address, transmission data size, transmission request source, and transmission mode can be set, and the transmission operation start of each channel, the forced termination of transmission and the suspension of transmission can be controlled.
- It can control the start, forcibly terminate and pause of batch transmission of all channels.
- When multiple channels are operated at the same time, a fixed method or a cyclic method can be used to select the priority of the operating channel.
- Supports hardware DMA transfer using peripheral interrupt signals.
- Comply with system bus (AHB) and support 32-bit address space (4GB).

1.10 Timer TIM

Types of	Name	Bit width	Prescaler	Counting direction	PWM	capture	Complementary output
Universal timer	TIM0	16/32	1/2/4/8/16 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	TIM1	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	TIM2	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	2	2	1
	TIM3	16/32	1/2/4/8/16/ 32/64/256	Up count/ Count down/ Up and down count	6	6	3
Programmable counting array	PCA	16	2/4/8/16/32	Up count	5	5	No
Advanced timer	TIM4	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1
	TIM5	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1
	TIM6	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1

The general timer includes four timers TIM0/1/2/3.

General timer features

- PWM independent output, complementary output
- Capture input
- Dead zone control
- Brake control
- Edge alignment, symmetric center alignment and asymmetric center alignment PWM output
- Quadrature code counting function
- Single pulse mode
- External counting function

TIM0/1/2 have exactly the same function. TIM0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. Each timer of TIM0/1/2 has 2 channels of capture and comparison function, which can generate 2 channels of independent PWM output or 1 group of complementary PWM outputs. With dead zone control function.

TIM3 is a multi-channel general-purpose timer with all the functions of TIM0/1/2. It can generate 3 sets of complementary PWM outputs or 6 independent PWM outputs, and up to 6 input captures. With dead zone control function.

PCA (Programmable Counter Array) supports up to 5 16-bit capture/compare modules. The timer/counter can be used as a common clock count/event counter capture/compare function. Each module of PCA can be independently programmed to provide input capture, output comparison or pulse width modulation. In addition, module 4 has an additional watchdog timer mode.

Advanced Timer Advanced Timer contains three timers TIM4/5/6. TIM4/5/6 is a high-performance counter with the same function, which can be used to count and generate different forms of clock waveforms. One timer can generate a complementary pair of PWM or independent 2- way PWM output, which can capture external input for pulse width or Period measurement.

The basic functions and features of Advanced Timer are shown in the table:

Waveform mode	Sawtooth wave, triangular wave
Basic functions	• Direction of increments and decrements
	• Software synchronization
	• Hardware synchronization
	• Cache function
	• Orthogonal coding count
	• General PWM output
	• Protection mechanism
	• AOS related actions
Interrupt type	Count comparison match interrupt
	Count cycle match interrupt
	Dead time error interrupt

1.11 Watchdog WDT

WDT (Watch Dog Timer) is a configurable 20-bit timer that provides reset in the case of MCU abnormality; built-in 10kHz low-speed clock input is used as the counter clock. In debug mode, you can choose to pause or continue to run; WDT can only be restarted by writing a specific sequence.

1.12 Universal synchronous asynchronous transceiver UART0 ~ UART3

4-channel universal synchronous asynchronous receiver/transmitter (Universal Asynchronous Receiver/Transmitter), UART0~UART3.

Basic functions of universal UART:

- Half-duplex and full-duplex transmission

- 8/9-Bit transmission data length
- Hardware parity
- 1/1.5/2-Bit stop bit
- Four different transmission modes
- 16-Bit baud rate counter
- Multi-machine communication
- Hardware address recognition
- DMAC hardware transmission handshake
- Hardware flow control
- Support single line mode

1.13 Low power synchronous asynchronous transceiver LPUART0 ~ LPUART1

2-channel synchronous asynchronous transceiver (Low Power Universal Asynchronous Receiver/Transmitter) that can work in low power consumption mode, LPUART0/LPUART1.

Basic functions of LPUART:

- Transmission clock SCLK (SCLK can choose XTL, RCL and PCLK)
- Send and receive data in system low power mode
- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity
- 1/1.5/2-Bit stop bit
- Four different transmission modes
- 16-Bit baud rate counter
- Multi-machine communication
- Hardware address recognition
- DMAC hardware transmission handshake
- Hardware flow control
- Support single line mode

1.14 Serial Peripheral Interface SPI

2-channel synchronous serial interface (Serial Peripheral Interface)

Basic characteristics of SPI:

- Can be configured as master or slave through programming
- Four-wire transmission mode, full duplex communication
- Host mode 7 kinds of baud rate configurable

- The maximum frequency division factor of the host mode is PCLK/2, and the maximum communication rate is 16M bps
- The maximum frequency division factor of slave mode is PCLK/4, and the maximum communication rate is 12M bps
- Configurable serial clock polarity and phase
- Support interrupt
- 8-bit data transmission, first transmit high bit and then low bit
- Support DMA software/hardware access

1.15 I2C bus

Two-way I2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic characteristics of I2C:

- Support four working modes of master sending/receiving and slave sending/receiving
- Support standard (100Kbps) / fast (400Kbps) / high speed (1Mbps) three working rates
- Support 7-bit addressing function
- Support noise filtering function
- Support broadcast address
- Support interrupt status query function

1.16 Audio interface I2S

2-channel I2S audio communication interface

- Support Philip/MSB/LSB/PCM mode
- Support MCK output
- Supports 5 audio sampling rates: 48, 44.1, 32, 16, 8 kHz
- Support 3 kinds of data length: 16, 24, 32 Bit
- Support 2 frame lengths: 16, 32 Bit
- Support DMA data transfer
- Support full-duplex transmission and reception (2 I2S cooperation)
- Support master sending and receiving
- Support slave sending and receiving

1.17 USB 2.0 Full speed module

The USB Full Speed (USBFS) controller provides a set of USB communication solutions for portable devices. The USBFS controller supports device mode, and the chip integrates a full-speed PHY. Support full speed (FS, 12Mb/s) transceiver in device mode. The USBFS controller supports all four

transmission methods defined by the USB2.0 protocol (control transmission, batch transmission, interrupt transmission and synchronous transmission).

1.18 Controller Area Network CAN

The CAN communication interface module is equipped with 512 bytes of RAM to store the data sent and received. It supports the CAN2.0B protocol specified by ISO11898-1 and the TTCAN protocol specified by ISO11898-4.

1.19 Crystal-less USB clock calibrator CTS

The clock calibration timer can adjust and calibrate the clock frequency of RCH48M so as to provide it to Crystal-less USB. The clock frequency of other RC oscillations can also be adjusted and calibrated, and it can also be used as a general-purpose timer.

1.20 Buzzer

4 general-purpose timers function multiplexing output to provide programmable driving frequency for Buzzer. The buzzer port can provide 18mA sink current, complementary output, no additional transistor is needed.

1.21 Clock Trim Module CLKTRIM

The built-in clock calibration module can calibrate the internal RC clock through the external precise crystal oscillator clock, or use the internal RC clock to check whether the external crystal oscillator clock is working properly.

Basic features of clock calibration:

- Calibration mode
- Monitoring mode
- 32-bit reference clock counter can be loaded with initial value
- 32-bit clock counter to be calibrated with configurable overflow value
- 6 reference clock sources
- 6 clock sources to be calibrated
- Support interrupt mode

1.22 Device electronic signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. The UID addresses are: 0x0010 0E74 - 0x0010 0E7D.

1.23 Cyclic Redundancy Check CRC

CRC16 conforms to the polynomial given in ISO/IEC13239 $X^{16} + X^{12} + X^5 + 1$.

CRC32 conforms to the polynomial given in ISO/IEC13239 $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$.

1.24 Hardware divider Module HDIV

HDIV (Hardware Divider) is a 32-bit signed/unsigned integer hardware divider.

Basic characteristics of HDIV hardware divider:

- Configurable signed/unsigned integer division calculation
- 32-bit dividend, 16-bit divisor
- Output 32-bit quotient and 32-bit remainder
- Divide by zero warning flag, division end flag
- 10 clock cycles to complete a division operation
- Write the divisor register to trigger the start of the division operation
- Automatically wait for the end of the calculation when reading the quotient register/remainder register

1.25 Advanced Encryption Standard Module AES

AES (The Advanced Encryption Standard) is a new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on October 2, 2000. The packet length of AES is fixed at 128 Bit, and the key length supports 128/192/256 Bit.

1.26 True random number generator TRNG

TRNG is a true random number generator, used to generate true random numbers.

1.27 Analog-to-digital converter ADC

A 12-bit successive approximation analog-to-digital converter with monotonous and no missing codes, when working under a 24MHz ADC clock, the sampling rate reaches 1Msps. The reference voltage can be selected from the on-chip precision voltage (1.5V or 2.5V) or from an external input or power supply voltage. 40 input channels, including 36 external pin inputs, 1 -channel internal temperature sensor voltage, 1 -channel 1/3 power supply voltage, and 2 -channel DAC outputs. Built-in configurable input signal amplifier to detect high output impedance signals.

Basic characteristics of SAR ADC:

- 12-bit conversion accuracy;
- 1Msps conversion speed;

- 40 input channels, including 36 external pin inputs, 1 -channel internal temperature sensor voltage, 1 -channel 1/3 AVCC voltage, and 2-channel DAC outputs;
- 4 reference sources: AVCC voltage, ExRef pin, built-in 1.5V reference voltage, built-in 2.5V reference voltage;
- ADC voltage input range: 0~Vref;
- 4 conversion modes: single conversion, sequential scan continuous conversion, queue scanning continuous conversion, continuous conversion accumulation;
- Input channel voltage threshold monitoring;
- Software can configure ADC conversion rate;
- Built-in signal amplifier, can convert high impedance signal;
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion.

1.28 Digital-to-analog converter DAC

2-channel 12Bit 500Ksps DAC, can perform digital-to-analog conversion.

1.29 Analog comparator VC

Built-in 3-channel VC, chip pin voltage monitoring/comparison circuit. 16 configurable positive external input channels, 11 configurable negative external input channels; 4 internal negative input channels, including 1 internal temperature sensor voltage, 1 -channel built-in BGR 2.5V reference voltage, 1 channel 64-step resistor divider . VC output can be used for general-purpose timer TIM0/1/2/3 and programmable counting array PCA for capturing, gating, and external counting clock. An asynchronous interrupt can be generated according to the rising/falling edge to wake up the MCU from the low-power mode. Configurable software anti-shake function.

1.30 Low voltage detector LVD

Detect chip power supply voltage or chip pin voltage. 16-shift voltage monitoring values (1.8 - 3.3V). An asynchronous interrupt or reset can be generated based on the rising/falling edge. With hardware hysteresis circuit and configurable software anti-shake function.

LVD basic characteristics:

- 4 -channel monitoring sources, AVCC, PC13, PB08, PB07;
- 16-stage threshold voltage, 1.8-3.3V optional;
- 8 trigger conditions, combinations of high level, rising edge and falling edge;
- 2 trigger results, reset and interrupt;
- 8-stage filter configuration to prevent false triggering;
- With hysteresis function, strong anti-interference.

1.31 Operational Amplifier OPA

OPA0/1/2 modules can be flexibly configured and are suitable for simple filter and buffer applications. The OPA3/4 module can be used as a DAC buffer or configured as an operational amplifier.

1.32 Embedded debugging system

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development software. Support 4 hard breakpoints and multiple soft breakpoints.

1.33 Programming mode

Two programming modes are supported: online programming and offline programming.

Support two programming protocols: ISP protocol, SWD protocol.

Support unified programming interface: ISP protocol and SWD protocol share SWD port.

When reset, the BOOT0 (PF11) pin is high, the chip works in ISP programming mode, and FLASH can be programmed through ISP protocol.

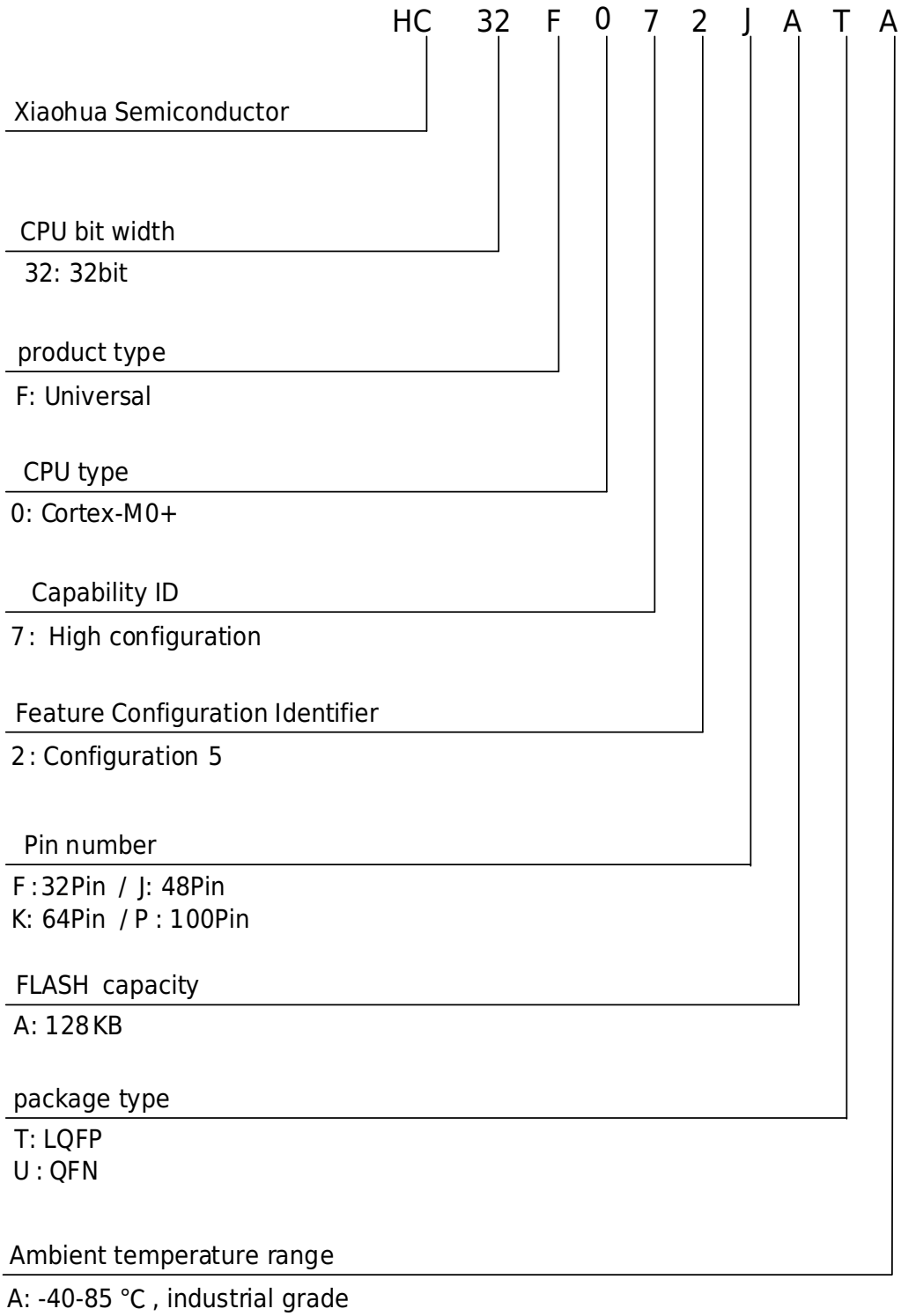
When reset, the BOOT0 (PF11) pin is low, the chip works in user mode, the chip executes the program code in FLASH, and the Flash can be programmed through the SWD protocol.

1.34 High security

Encrypted embedded debugging solution, providing a full-featured real-time debugger.

2 Product lineup

2.1 Product name



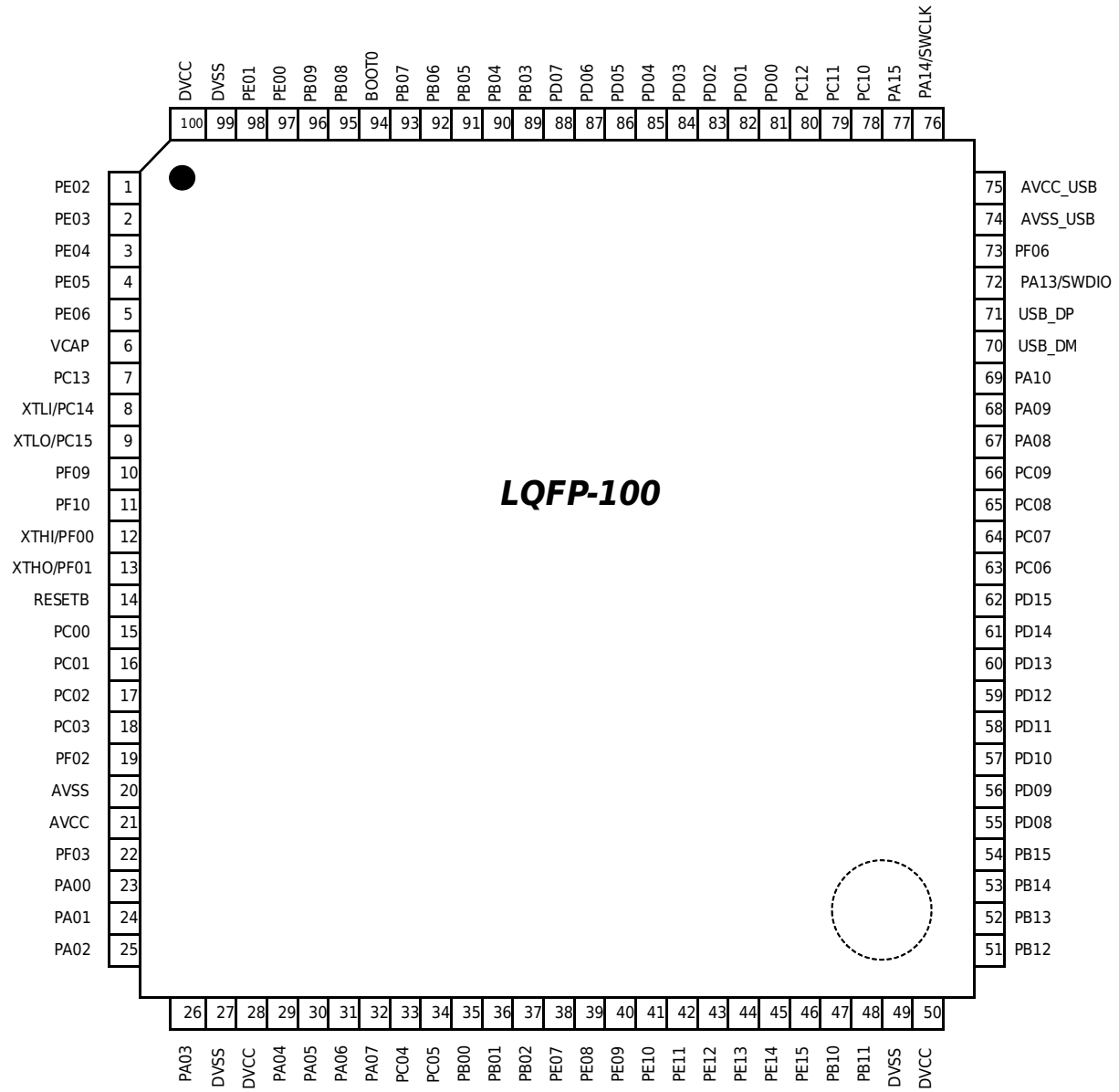
2.2 Function

Product name		HC32F072PATA	HC32F072KATA	HC32F072JATA	HC32F072FAUA
Pin number		100	64	48	32
GPIO pin number		86	50	36	25
CPU	Kernel	Cortex M0+			
	Frequency	48MHz			
Supply voltage range		1.8 ~5.5V			
Temperature range		-40 ~ 85℃			
Debug function		SWD debug interface			
Unique identification code		Support			
Communication Interface		UART0/1/2/3 LPUART0/1 SPI0/1 I2C0/1 I2S0/1		UART0/1 LPUART0/1 SPI0/1 I2C0/1 I2S0/1	UART0/1 LPUART0 SPI0 I2C0 I2S0
Timer		General timer TIM0/1/2/3 Advanced timer TIM4/5/6			
12-bit A/D converter		24ch	23ch	17ch	11ch
12-bit D/A converter		2ch	2ch	2ch	2ch
Analog voltage comparator		VC0/1/2			
Operational Amplifier		5	5	3	1
USB		Support			
CAN		Support			
Port interrupt		86	50	36	25
Low voltage detection reset		1			
Clock	Internal high-speed oscillator	RCH 4/8/16/22.12/24MHz			
	Internal low-speed oscillator	RCL 32.8/38.4kHz			
	PLL	8~48MHz			
	External high-speed crystal oscillator	8~32MHz			
buzzer		Max 4ch			
Flash security protection		Support			
RAM parity		Support			

3 Pin configuration and function

3.1 Pin Configuration Diagram

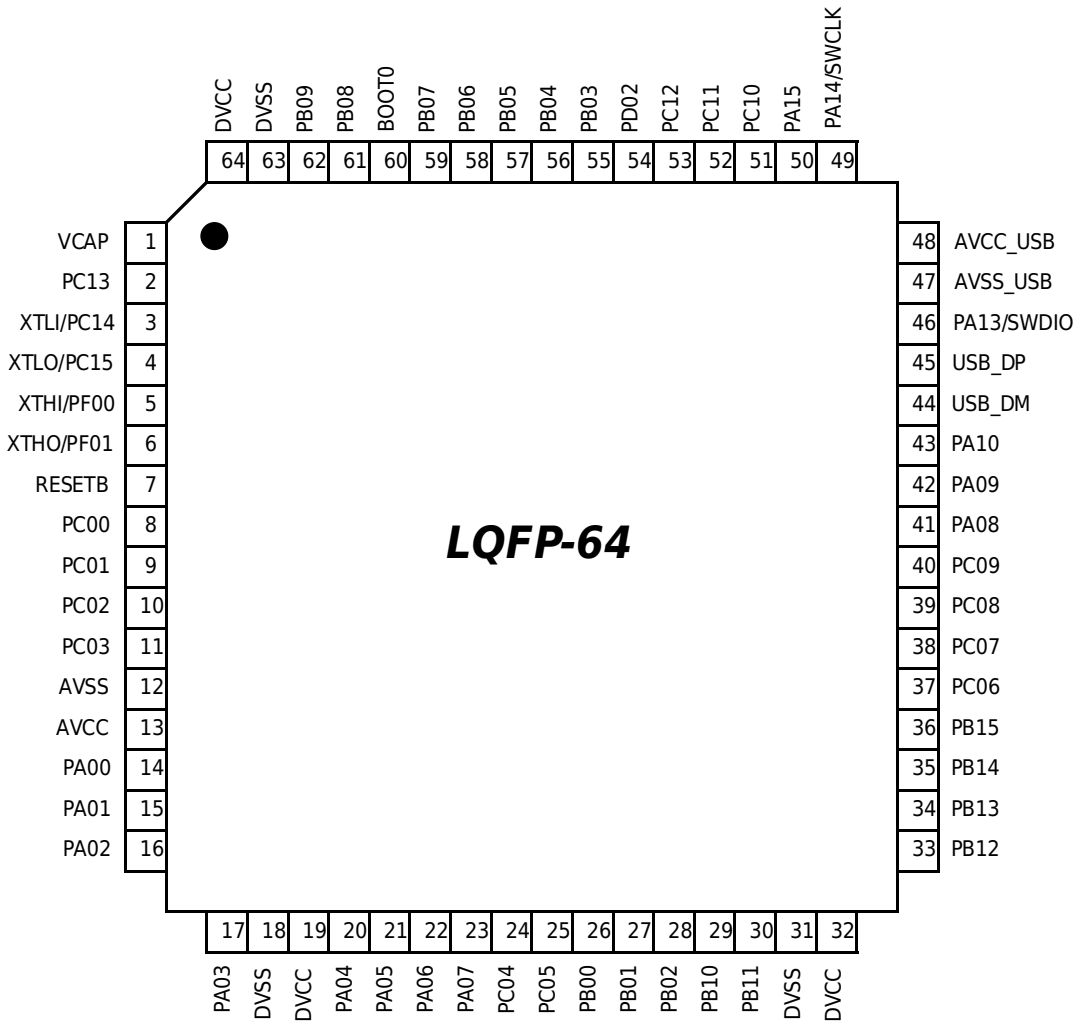
HC32F072PATA



Note:

- **In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.**
- **Please refer to Pin function description for the IO not drawn out of this package.**
- **The BOOT0 pin is used to control FLASH programming, see Module signal description for details.**

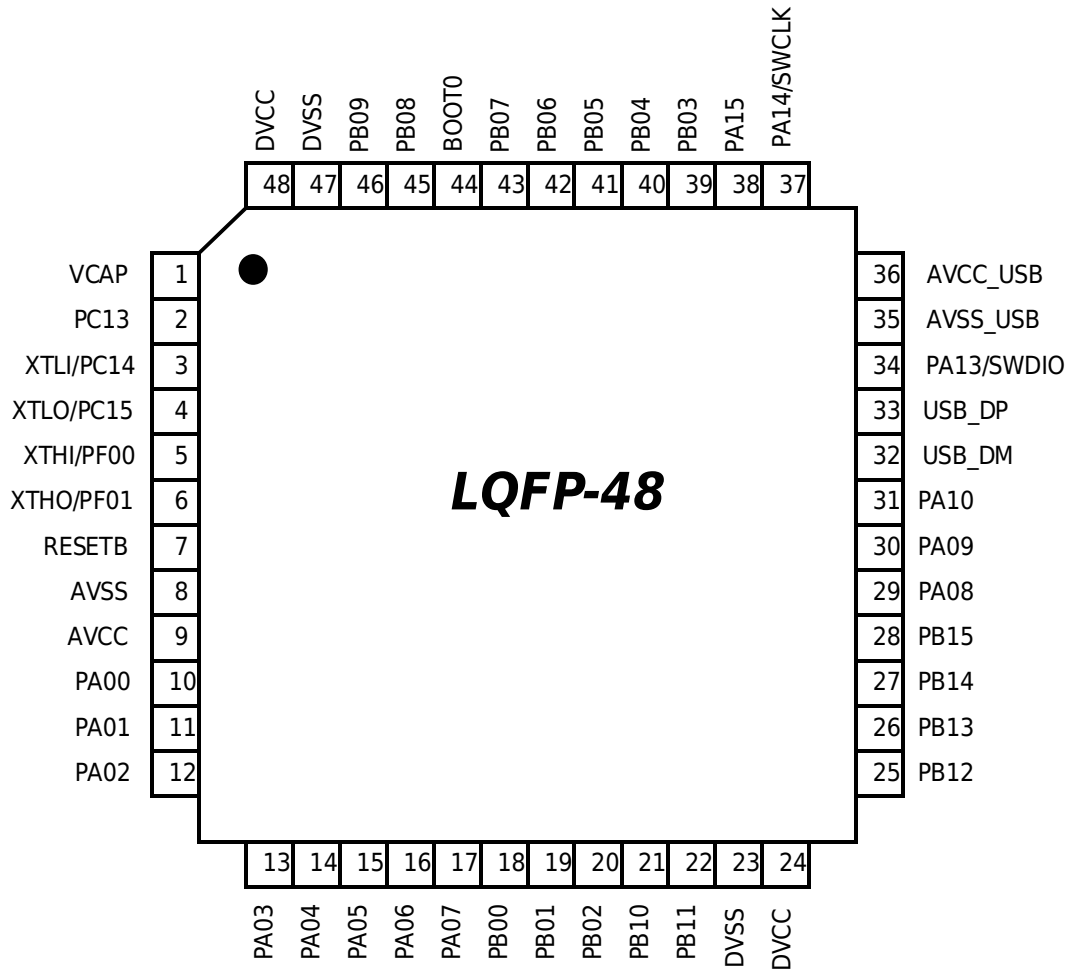
HC32F072KATA



Note:

- **In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.**
- **Refer to Pin function description for details about the IOs that are not drawn out in this package.**
- **The BOOT0 pin is used to control FLASH programming, see Module signal description for details.**

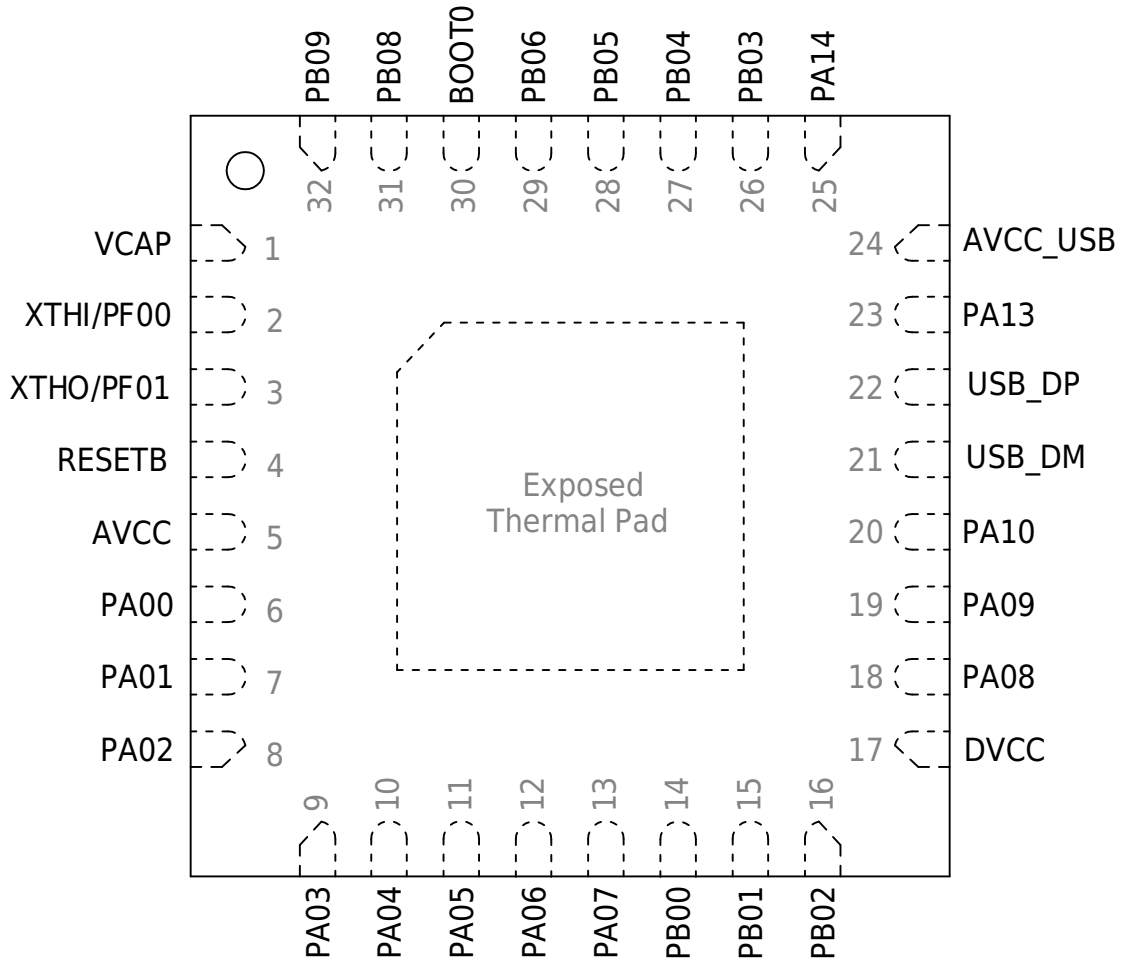
HC32F072JATA



Note:

- **In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.**
- **Refer to Pin function description for details about the IOs that are not drawn out in this package.**
- **The BOOT0 pin is used to control FLASH programming, see Module signal description for details.**

HC32F072FAUA



Note:

- **Exposed Thermal Pad needs to be connected to DVSS.**
- **In the application, it is necessary to set the unleaded IO pin of the package as input and enable the pull-up.**
- **Refer to Pin function description for details about the IOs that are not drawn out in this package.**
- **The BOOT0 pin is used to control FLASH programming, see Module signal description for details.**

Figure 3-1 Pin Configuration Diagram

3.2 Pin function description

LQFP100	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
1				PE02	PCA_ECI	
2				PE03	PCA_CH0	
3				PE04	PCA_CH1	
4				PE05	PCA_CH2	
5				PE06	PCA_CH3	
6	1	1	1	VCAP		
7	2	2		PC13	TIM3_CH1B I2S0_SCK	LVD0
8	3	3		PC14		XTLI
9	4	4		PC15		XTLO
10				PF09	TIM0_CHA	
11				PF10	TIM0_CHB	
12	5	5	2	PF00	I2C0_SDA CRS_SYNC UART1_TXD	XTHI
13	6	6	3	PF01	I2C0_SCL UART1_RXD	XTHO
14	7	7	4	RESETB		
15	8			PC00	UART1_CTS UART2_RTS I2S0_MCK	AIN10, VC0_INP0 VC1_INN0
16	9			PC01	TIM5_CHB UART1_RTS UART2_CTS I2S0_SD	AIN11 VC0_INP1 VC1_INN1
17	10			PC02	SPI1_MISO UART2_RXD	AIN12, VC0_INP2 VC1_INN2
18	11			PC03	SPI1_MOSI UART2_TXD	AIN13 VC0_INP3 VC1_INN3
19				PF02		
20	12	8		AVSS		
21	13	9	5	AVCC		
22				PF03		
23	14	10	6	PA00	UART1_CTS LPUART1_TXD TIM0_ETR VC0_OUT TIM1_CHA TIM3_ETR TIM0_CHA	AIN0 VC0_INP4 VC0_INN0 VC1_INP0 VC1_INN4
24	15	11	7	PA01	UART1_RTS LPUART1_RXD TIM0_CHB TIM1_ETR TIM1_CHB HCLK_OUT SPI1_MOSI	AIN1 VC0_INP5 VC0_INN1 VC1_INP1 VC1_INN5
25	16	12	8	PA02	UART1_TXD TIM0_CHA VC1_OUT TIM1_CHA TIM2_CHA	AIN2 VC0_INP6 VC0_INN2 VC1_INP2

LQFP100	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
					PCLK_OUT SPI1_MISO	
26	17	13	9	PA03	UART1_RXD TIM0_GATE TIM1_CHB TIM2_CHB SPI1_CS TIM3_CH1A TIM5_CHA	AIN3 VC0_INP7 VC0_INN3 VC1_INP3
27	18			DVSS		
28	19			DVCC		
				PF04		
				PF05		
29	20	14	10	PA04	SPI0_CS UART1_TXD PCA_CH4 TIM2_ETR TIM5_CHA LVD_OUT TIM3_CH2B	AIN4 VC0_INP8 VC0_INN4 VC1_INP4 OP3_OUT DAC0_OUT
30	21	15	11	PA05	SPI0_SCK TIM0_ETR PCA_ECI TIM0_CHA TIM5_CHB XTL_OUT XTH_OUT	AIN5 VC0_INP9 VC0_INN5 VC1_INP5 VC2_INP0 VC2_INN0 OP4_OUT DAC1_OUT
31	22	16	12	PA06	SPI0_MISO PCA_CH0 TIM3_BK TIM1_CHA VC0_OUT TIM3_GATE LPUART0_CTS	AIN6 VC0_INP10 VC0_INN6 OP4_INN
32	23	17	13	PA07	SPI0_MOSI PCA_CH1 HCLK_OUT TIM3_CH0B TIM2_CHA VC1_OUT TIM4_CHB	AIN7 VC0_INP11 VC0_INN7 OP4_INP
33	24			PC04	LPUART0_TXD TIM2_ETR IR_OUT VC2_OUT I2S0_WS	AIN14 VC0_INN8
34	25			PC05	LPUART0_RXD TIM6_CHB PCA_CH4 I2S0_SDIN	AIN15 VC0_INN9 OP3_INN
35	26	18	14	PB00	PCA_CH2 TIM3_CH1B LPUART0_TXD TIM5_CHB RCH_OUT RCL_OUT PLL_OUT	AIN8 VC1_INN6 OP3_INP
36	27	19	15	PB01	PCA_CH3 PCLK_OUT TIM3_CH2B TIM6_CHB LPUART0_RTS VC2_OUT TCLK_OUT	AIN9/EXVREF VC1_INP6 VC1_INN7 VC2_INP1 VC2_INN1
37	28	20	16	PB02	PCA_ECI LPUART1_TXD TIM4_CHA	AIN16, VC1_INP7 VC1_INN8

LQFP100	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
					TIM1_BK TIM0_BK TIM2_BK	OP2_INN
38				PE07	TIM3_ETR	
39				PE08	TIM3_CH0B	OP2_OUT4
40				PE09	TIM3_CH0A	VC2_INP2 OP2_OUT3
41				PE10	TIM3_CH1B	VC2_INP3 OP2_OUT2
42				PE11	TIM3_CH1A	VC2_INP4 VC2_INN2 OP2_OUT1
43				PE12	TIM3_CH2B SPI0_CS UART3_CTS	OP1_OUT4
44				PE13	TIM3_CH2A SPI0_SCK UART3_RTS	VC2_INP5 OP1_OUT3
45				PE14	TIM3_CH0B SPI0_MISO UART3_RXD	VC2_INP6 OP1_OUT2
46				PE15	TIM3_BK SPI0_MOSI UART3_TXD	AIN23, VC2_INP7 VC2_INN3 OP1_OUT1
47	29	21		PB10	I2C1_SCL SPI1_SCK TIM1_CHA LPUART0_TXD TIM3_CH1A LPUART1_RTS UART1_RTS	AIN17, VC1_INP8 OP2_INP
48	30	22		PB11	I2C1_SDA TIM1_CHB LPUART0_RXD TIM2_GATE TIM6_CHA LPUART1_CTS UART1_CTS	AIN18, VC2_INP8 VC2_INN4 OP2_OUT
49	31	23		DVSS		
50	32	24	17	DVCC		
51	33	25		PB12	SPI1_CS TIM3_BK LPUART0_TXD TIM0_BK LPUART0_RTS TIM6_CHA	AIN19 VC1_INP9 OP1_INN
52	34	26		PB13	SPI1_SCK I2C1_SCL TIM3_CH0B LPUART0_CTS TIM1_CHA TIM1_GATE TIM6_CHB	AIN20 VC1_INP10 OP1_INP
53	35	27		PB14	SPI1_MISO I2C1_SDA TIM3_CH1B TIM0_CHA LPUART0_RTS TIM1_BK	AIN21, VC1_INP11 VC2_INP9 VC2_INN5 OP1_OUT
54	36	28		PB15	SPI1_MOSI TIM3_CH2B TIM0_CHB TIM0_GATE LPUART1_RXD	AIN22, OP0_INN
55				PD08	LPUART0_TXD I2S0_SCK	OP0_OUT4

LQFP100	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
56				PD09	LPUART0_RXD I2S0_MCK	VC2_INP10 OP0_OUT3
57				PD10	LPUART0_TXD I2S0_SD	VC2_INP11 VC2_INN6 OP0_OUT2
58				PD11	LPUART0_CTS I2S0_WS	VC2_INP12 VC2_INN7 OP0_OUT1
59				PD12	LPUART0_RTS UART2_RTS	
60				PD13	UART2_RXD I2S0_SDIN	
61				PD14	UART2_TXD	
62				PD15	CRS_SYNC UART2_CTS	
63	37			PC06	PCA_CH0 TIM4_CHA TIM2_CHA UART3_RXD I2S1_SCK	OP0_INP
64	38			PC07	PCA_CH1 TIM5_CHA TIM2_CHB UART3_TXD I2S1_MCK	VC2_INP13 VC2_INN8 OP0_OUT
65	39			PC08	PCA_CH2 TIM6_CHA TIM2_ETR UART3_CTS I2S1_SD	
66	40			PC09	PCA_CH3 TIM4_CHB TIM1_ETR UART3_RTS I2S1_WS	
67	41	29	18	PA08	UART0_TXD TIM3_CH0A CRS_SYNC CAN_STBY TIM1_GATE TIM4_CHA TIM3_BK	
68	42	30	19	PA09	UART0_TXD TIM3_CH1A TIM0_BK I2C0_SCL HCLK_OUT TIM5_CHA	COM0
69	43	31	20	PA10	UART0_RXD TIM3_CH2A TIM2_BK I2C0_SDA TIM2_GATE PCLK_OUT TIM6_CHA	COM1
				PA11	UART0_CTS TIM3_GATE I2C1_SCL CAN_RX VC0_OUT SPI0_MISO TIM4_CHB	
				PA12	UART0_RTS TIM3_ETR I2C1_SDA CAN_TX VC1_OUT SPI0_MOSI	
70	44	32	21	USBDM		

LQFP100	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
71	45	33	22	USBDP		
72	46	34	23	PA13	IR_OUT UART0_RXD LVD_OUT TIM3_ETR VC2_OUT	SWDIO
73				PF06	I2C1_SCL LPUART1_CTS UART0_CTS	
				PF07	I2C1_SDA LPUART1_RTS UART0_RTS	
74	47	35		AVSS_USB		
75	48	36	24	AVCC_USB		
76	49	37	25	PA14	UART1_TXD UART0_TXD TIM3_CH2A LVD_OUT RCH_OUT RCL_OUT PLL_OUT	SWCLK
77	50	38		PA15	SPI0_CS UART1_RXD LPUART1_RTS TIM0_ETR TIM0_CHA TIM3_CH1A	
78	51			PC10	LPUART1_TXD LPUART0_TXD PCA_CH2	COM4
79	52			PC11	LPUART1_RXD LPUART0_RXD PCA_CH3	COM5
80	53			PC12	LPUART0_TXD LPUART1_TXD PCA_CH4	COM6
81				PD00	CAN_RX SPI1_CS	
82				PD01	CAN_TX SPI1_SCK	
83	54			PD02	PCA_ECI LPUART0_RTS TIM1_ETR	COM7
84				PD03	UART1_CTS SPI1_MISO I2S1_SCK	
85				PD04	UART1_RTS SPI1_MOSI I2S1_MCK	
86				PD05	UART1_TXD CAN_STBY I2S1_SD	
87				PD06	UART1_RXD I2S1_WS	
88				PD07	UART1_TXD I2S1_SDIN	
89	55	39	26	PB03	SPI0_SCK TIM0_CHB TIM1_GATE TIM3_CH0A XTL_OUT XTH_OUT	VC1_INN9
90	56	40	27	PB04	SPI0_MISO PCA_CH0 TIM2_BK UART0_CTS TIM2_GATE TIM3_CH0B	VC0_INP12 VC1_INP12

LQFP100	LQFP64	LQFP48	QFN32	NAME	DIGITAL	ANALOG
91	57	41	28	PB05	SPI0_MOSI TIM1_BK PCA_CH1 UART0_RTS	VC0_INP13
92	58	42	29	PB06	I2C0_SCL UART0_TXD TIM1_CHB TIM0_CHA TIM3_CH0A	VC0_INP14 VC1_INP14
93	59	43		PB07	I2C0_SDA UART0_RXD TIM2_CHB LPUART1_CTS TIM0_CHB	VC1_INP15 LVD2
94	60	44	30	BOOT0/PF11		
95	61	45	31	PB08	I2C0_SCL TIM1_CHA CAN_RX TIM2_CHA TIM0_GATE TIM3_CH2A UART0_TXD	LVD1
96	62	46	32	PB09	I2C0_SDA IR_OUT SPI1_CS TIM2_CHA CAN_TX TIM2_CHB UART0_RXD	
97				PE00	TIM1_CHA	
98				PE01	TIM2_CHA	
99	63	47		DVSS		
100	64	48		DVCC		

The digital function of each pin is controlled by the PSEL bit field, as shown in the table below.

PxSEL							
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PA00	UART1_CTS	LPUART1_TXD	TIM0_ETR	VC0_OUT	TIM1_CHA	TIM3_ETR	TIM0_CHA
PA01	UART1_RTS	LPUART1_RXD	TIM0_CHB	TIM1_ETR	TIM1_CHB	HCLK_OUT	SPI1_MOSI
PA02	UART1_TXD	TIM0_CHA	VC1_OUT	TIM1_CHA	TIM2_CHA	PCLK_OUT	SPI1_MISO
PA03	UART1_RXD	TIM0_GATE	TIM1_CHB	TIM2_CHB	SPI1_CS	TIM3_CH1A	TIM5_CHA
PA04	SPI0_CS	UART1_TXD	PCA_CH4	TIM2_ETR	TIM5_CHA	LVD_OUT	TIM3_CH2B
PA05	SPI0_SCK	TIM0_ETR	PCA_ECI	TIM0_CHA	TIM5_CHB	XTL_OUT	XTH_OUT
PA06	SPI0_MISO	PCA_CH0	TIM3_BK	TIM1_CHA	VC0_OUT	TIM3_GATE	LPUART0_CTS
PA07	SPI0_MOSI	PCA_CH1	HCLK_OUT	TIM3_CH0B	TIM2_CHA	VC1_OUT	TIM4_CHB
PA08	UART0_TXD	TIM3_CH0A	CRS_SYNC	CAN_STBY	TIM1_GATE	TIM4_CHA	TIM3_BK
PA09	UART0_TXD	TIM3_CH1A	TIM0_BK	I2C0_SCL		HCLK_OUT	TIM5_CHA
PA10	UART0_RXD	TIM3_CH2A	TIM2_BK	I2C0_SDA	TIM2_GATE	PCLK_OUT	TIM6_CHA
PA11	UART0_CTS	TIM3_GATE	I2C1_SCL	CAN_RX	VC0_OUT	SPI0_MISO	TIM4_CHB
PA12	UART0_RTS	TIM3_ETR	I2C1_SDA	CAN_TX	VC1_OUT	SPI0_MOSI	
PA13	IR_OUT	UART0_RXD	LVD_OUT	TIM3_ETR			VC2_OUT
PA14	UART1_TXD	UART0_TXD	TIM3_CH2A	LVD_OUT	RCH_OUT	RCL_OUT	PLL_OUT
PA15	SPI0_CS	UART1_RXD	LPUART1_RTS	TIM0_ETR	TIM0_CHA	TIM3_CH1A	
PB00	PCA_CH2	TIM3_CH1B	LPUART0_TXD	TIM5_CHB	RCH_OUT	RCL_OUT	PLL_OUT
PB01	PCA_CH3	PCLK_OUT	TIM3_CH2B	TIM6_CHB	LPUART0_RTS	VC2_OUT	TCLK_OUT
PB02		PCA_ECI	LPUART1_TXD	TIM4_CHA	TIM1_BK	TIM0_BK	TIM2_BK
PB03	SPI0_SCK	TIM0_CHB	TIM1_GATE	TIM3_CH0A		XTL_OUT	XTH_OUT
PB04	SPI0_MISO	PCA_CH0	TIM2_BK	UART0_CTS	TIM2_GATE	TIM3_CH0B	
PB05	SPI0_MOSI		TIM1_BK	PCA_CH1			UART0_RTS
PB06	I2C0_SCL	UART0_TXD	TIM1_CHB	TIM0_CHA		TIM3_CH0A	
PB07	I2C0_SDA	UART0_RXD	TIM2_CHB	LPUART1_CTS	TIM0_CHB		
PB08	I2C0_SCL	TIM1_CHA	CAN_RX	TIM2_CHA	TIM0_GATE	TIM3_CH2A	UART0_TXD
PB09	I2C0_SDA	IR_OUT	SPI1_CS	TIM2_CHA	CAN_TX	TIM2_CHB	UART0_RXD
PB10	I2C1_SCL	SPI1_SCK	TIM1_CHA	LPUART0_TXD	TIM3_CH1A	LPUART1_RTS	UART1_RTS
PB11	I2C1_SDA	TIM1_CHB	LPUART0_RXD	TIM2_GATE	TIM6_CHA	LPUART1_CTS	UART1_CTS
PB12	SPI1_CS	TIM3_BK	LPUART0_TXD	TIM0_BK		LPUART0_RTS	TIM6_CHA
PB13	SPI1_SCK	I2C1_SCL	TIM3_CH0B	LPUART0_CTS	TIM1_CHA	TIM1_GATE	TIM6_CHB
PB14	SPI1_MISO	I2C1_SDA	TIM3_CH1B	TIM0_CHA		LPUART0_RTS	TIM1_BK
PB15	SPI1_MOSI	TIM3_CH2B	TIM0_CHB	TIM0_GATE			LPUART1_RXD
PC00			UART1_CTS	UART2_RTS	I2S0_MCK		
PC01		TIM5_CHB	UART1_RTS		I2S0_SD	UART2_CTS	
PC02	SPI1_MISO			UART2_RXD			
PC03	SPI1_MOSI				UART2_TXD		

PxSEL							
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PC04	LPUART0_TXD	TIM2_ETR	IR_OUT	VC2_OUT	I2S0_WS		
PC05	LPUART0_RXD	TIM6_CHB	PCA_CH4		I2S0_SDIN		
PC06	PCA_CH0	TIM4_CHA	TIM2_CHA		I2S1_SCK	UART3_RXD	
PC07	PCA_CH1	TIM5_CHA	TIM2_CHB		I2S1_MCK	UART3_TXD	
PC08	PCA_CH2	TIM6_CHA	TIM2_ETR		I2S1_SD	UART3_CTS	
PC09	PCA_CH3	TIM4_CHB	TIM1_ETR		I2S1_WS	UART3_RTS	
PC10	LPUART1_TXD	LPUART0_TXD	PCA_CH2				
PC11	LPUART1_RXD	LPUART0_RXD	PCA_CH3				
PC12	LPUART0_TXD	LPUART1_TXD	PCA_CH4				
PC13			TIM3_CH1B		I2S0_SCK		
PC14							
PC15							
PD00	CAN_RX	SPI1_CS					
PD01	CAN_TX	SPI1_SCK					
PD02	PCA_ECI	LPUART0_RTS	TIM1_ETR				
PD03	UART1_CTS	SPI1_MISO		I2S1_SCK			
PD04	UART1_RTS	SPI1_MOSI		I2S1_MCK			
PD05	UART1_TXD		CAN_STBY	I2S1_SD			
PD06	UART1_RXD			I2S1_WS			
PD07	UART1_TXD			I2S1_SDIN			
PD08	LPUART0_TXD	I2S0_SCK					
PD09	LPUART0_RXD	I2S0_MCK					
PD10	LPUART0_TXD	I2S0_SD					
PD11	LPUART0_CTS	I2S0_WS					
PD12	LPUART0_RTS	UART2_RTS					
PD13	UART2_RXD	I2S0_SDIN					
PD14	UART2_TXD						
PD15	CRS_SYNC	UART2_CTS					
PE00	TIM1_CHA						
PE01	TIM2_CHA						
PE02	PCA_ECI						
PE03	PCA_CH0						
PE04	PCA_CH1						
PE05	PCA_CH2						
PE06	PCA_CH3						
PE07	TIM3_ETR						
PE08	TIM3_CH0B						

PxSEL							
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PE09	TIM3_CH0A						
PE10	TIM3_CH1B						
PE11	TIM3_CH1A						
PE12	TIM3_CH2B	SPI0_CS	UART3_CTS				
PE13	TIM3_CH2A	SPI0_SCK	UART3_RTS				
PE14	TIM3_CH0B	SPI0_MISO	UART3_RXD				
PE15	TIM3_BK	SPI0_MOSI	UART3_TXD				
PF00	I2C0_SDA	CRS_SYNC	UART1_TXD				
PF01	I2C0_SCL		UART1_RXD				
PF02							
PF03							
PF04							
PF05							
PF06	I2C1_SCL	LPUART1_CTS	UART0_CTS				
PF07	I2C1_SDA	LPUART1_RTS	UART0_RTS				
PF09	TIM0_CHA						
PF10	TIM0_CHB						
PF11							

3.3 Module signal description

Table 3-1 Module signal description

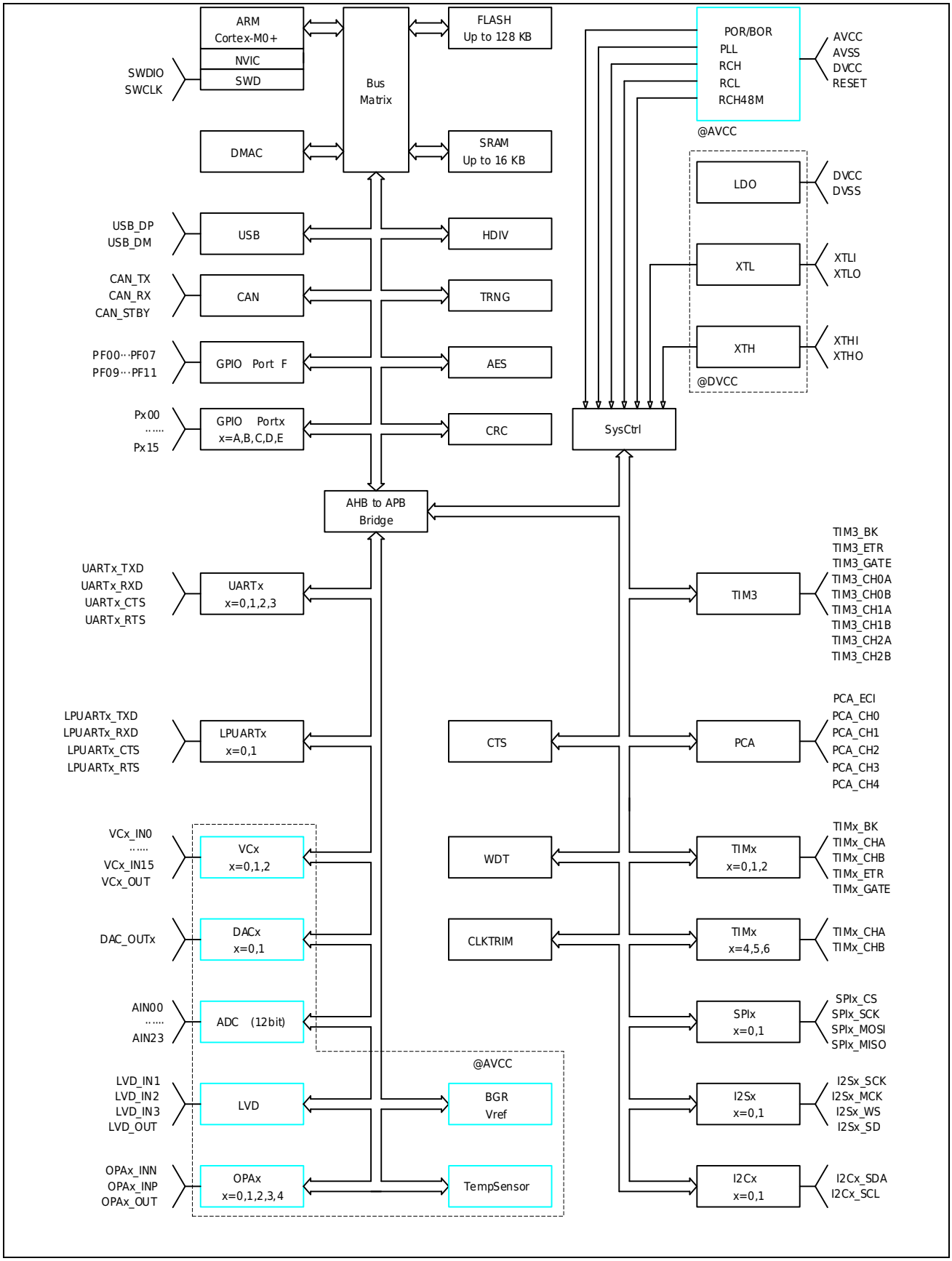
Modules	Pin name	Description
Power supply	DVCC	Digital power supply
	AVCC	Analog power
	DVSS	Digitally
	AVSS	Analog ground
	AVCC_USB	USB module power supply (not greater than 3.6V, see Electrical characteristics for details)
	AVSS_USB	USB module ground
	VCAP	LDO core power output (only for internal circuit use, external decoupling capacitor no less than 1uF is required)
ISP	BOOT0	When reset, the BOOT0 (PF11) pin is high, the chip works in ISP programming mode, and FLASH can be programmed using the ISP protocol; When reset, the BOOT0 (PF11) pin is low, the chip works in user mode, the chip executes the program code in the FLASH, and the Flash can be programmed through the SWD.
ADC	AIN0~AIN35	ADC input channel 0-35
	ADC_VREF	ADC external reference voltage
VC	VCIN0~VCIN15	VC input 0-15
	VC0_OUT	VC0 comparison output
	VC1_OUT	VC1 comparison output
	VC2_OUT	VC2 comparison output
LVD	LVDIN0	Voltage detection input 0
	LVDIN1	Voltage detection input 1
	LVDIN2	Voltage detection input 2
	LVD_OUT	Voltage detection output
OPA x=0,1,2,3,4	OPx_INN	OPA negative input
	OPx_INP	OPA positive input
	OPx_OUTy	OPA output
UART x=0,1,2,3	UARTx_TXD	UARTx data transmitter
	UARTx_RXD	UARTx data receiver
	UARTx_CTS	UARTx CTS
	UARTx_RTS	UARTx RTS
LPUART x=0,1	LPUARTx_TXD	LPUART data transmitter
	LPUARTx_RXD	LPUART data receiver
	LPUARTx_CTS	LPUART CTS
	LPUARTx_RTS	LPUART RTS
I2Sx x=0,1	I2Sx_CK	I2S module clock signal
	I2Sx_WS	I2S module word selection signal
	I2Sx_MCK	I2S module master mode clock output

Modules	Pin name	Description
	I2Sx_SD	I2S module data input and output
USB	USB_DP	USB signal
	USB_DM	USB signal
CAN	CAN_TX	CAN TX output signal
	CAN_RX	CAN RX input signal
	CAN_STBY	CAN STBY signal
CTS	CTS_SYNC	CTS external synchronization signal
SPI x=0,1	SPIx_MISO	SPI module host input and slave output data signal
	SPIx_MOSI	SPI module master output slave input data signal
	SPIx_SCK	SPI module clock signal
	SPIx_CS	SPI chip select
I2C x=0,1	I2Cx_SDA	I2C module data signal
	I2Cx_SCL	I2C module clock signal
Universal timer TIMx x=0,1,2	TIMx_CHA	Timer capture input compare output A
	TIMx_CHB	Timer's capture input compare output B
	TIMx_ETR	Timer's external count input signal
	TIMx_GATE	Timer gate signal
Universal timer TIM3 y=0,1,2	TIM3_CHyA	Timer capture input compare output A
	TIM3_CHyB	Timer's capture input compare output B
	TIM3_ETR	Timer's external count input signal
	TIM3_GATE	Timer gate signal
Programmable counting array PCA	PCA_ECI	External clock input signal
	PCA_CH0	Capture input/comparison output/PWM output 0
	PCA_CH1	Capture input/comparison output/PWM output 1
	PCA_CH2	Capture input/comparison output/PWM output 2
	PCA_CH3	Capture input/comparison output/PWM output 3
	PCA_CH4	Capture input/comparison output/PWM output 4
Advanced Timer	TIM4_CHA	Advanced Timer4 compare output/capture input A
	TIM4_CHB	Advanced Timer4 compare output/capture input B
	TIM5_CHA	Advanced Timer5 compare output/capture input A
	TIM5_CHB	Advanced Timer5 compare output/capture input B
	TIM6_CHA	Advanced Timer6 compare output/capture input A
	TIM6_CHB	Advanced Timer6 compare output/capture input B

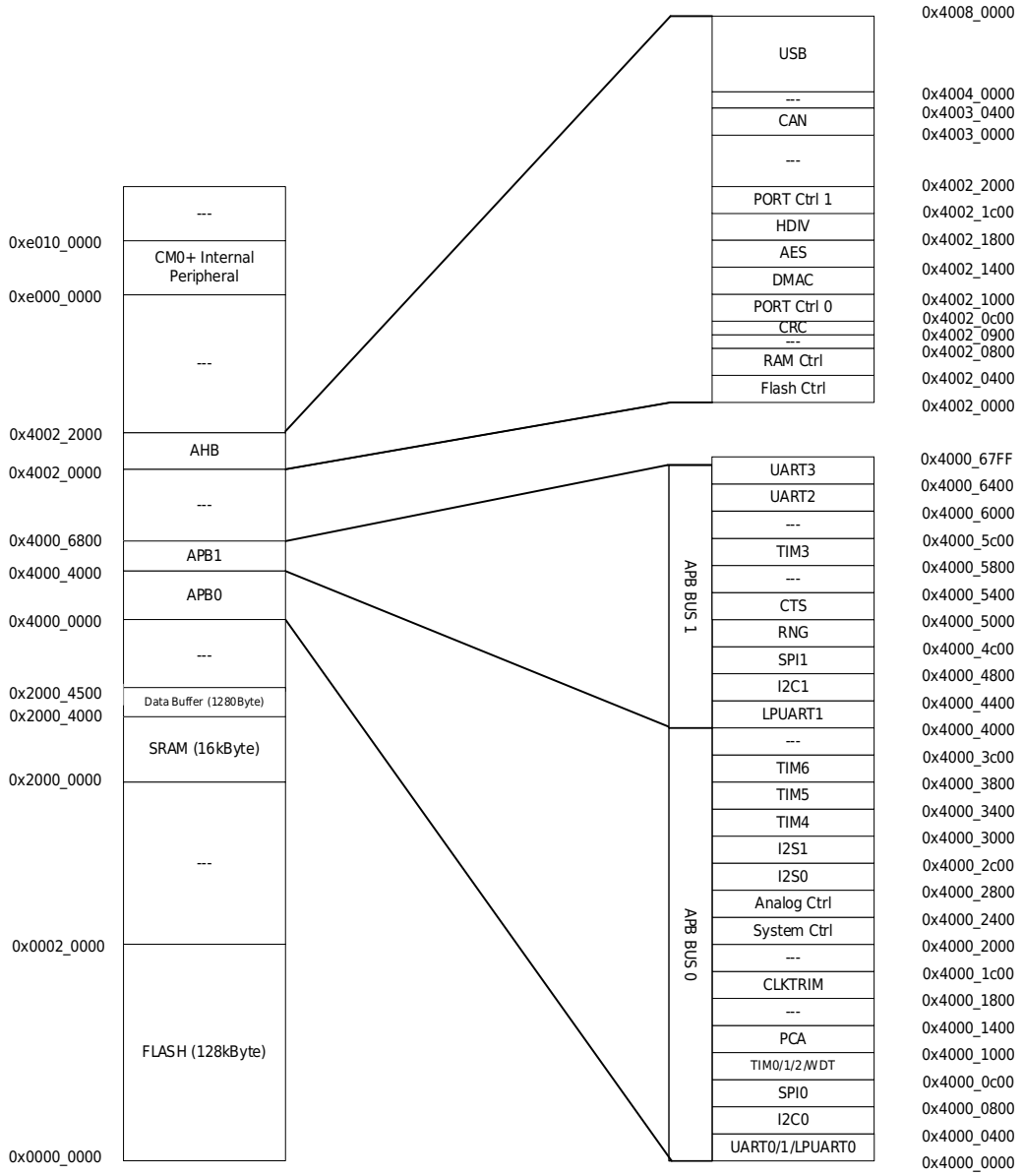
Note:

– The IO port is reset to the input high impedance state, and the sleep mode and deep sleep mode maintain the previous port state.

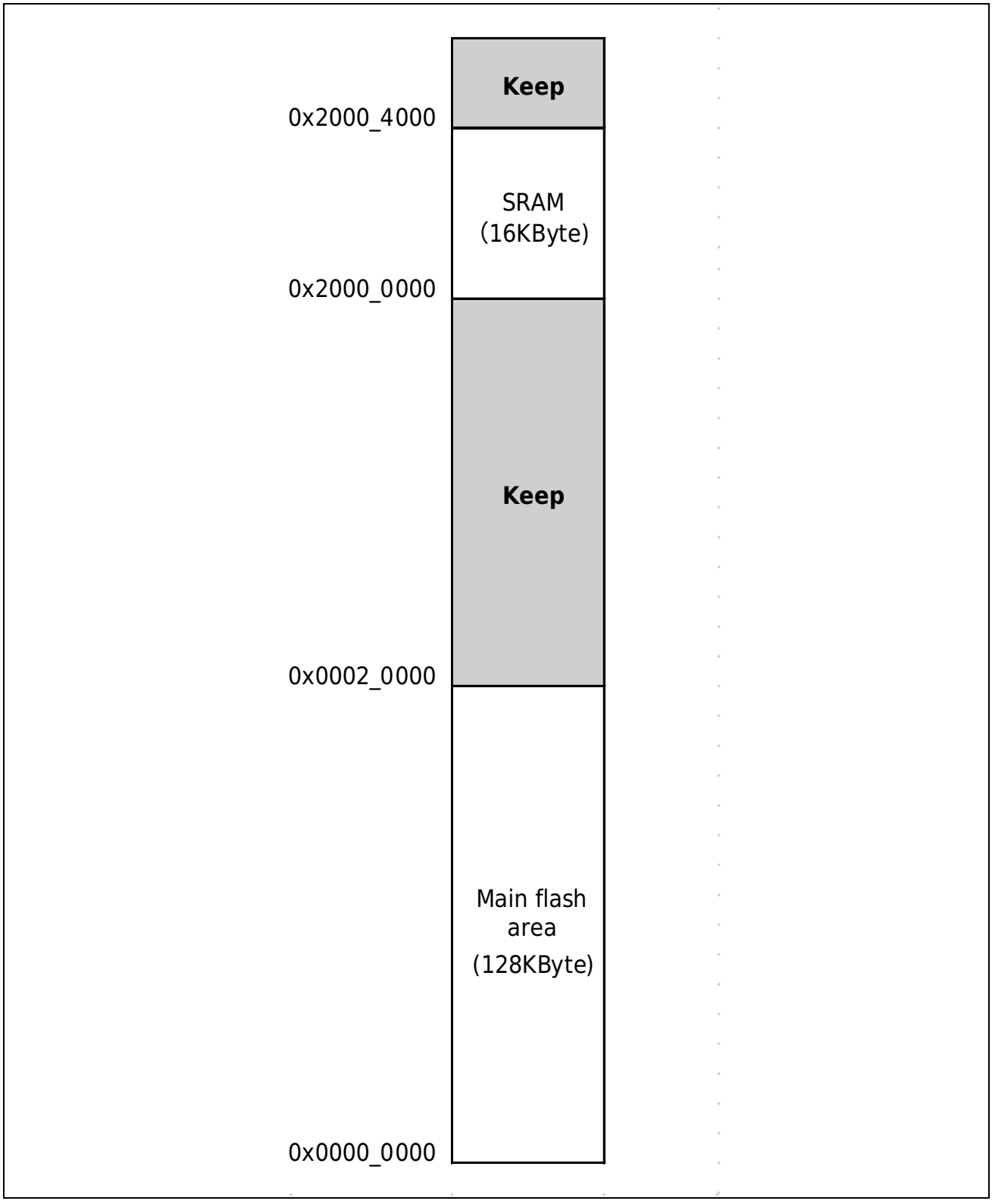
4 Functional block diagram



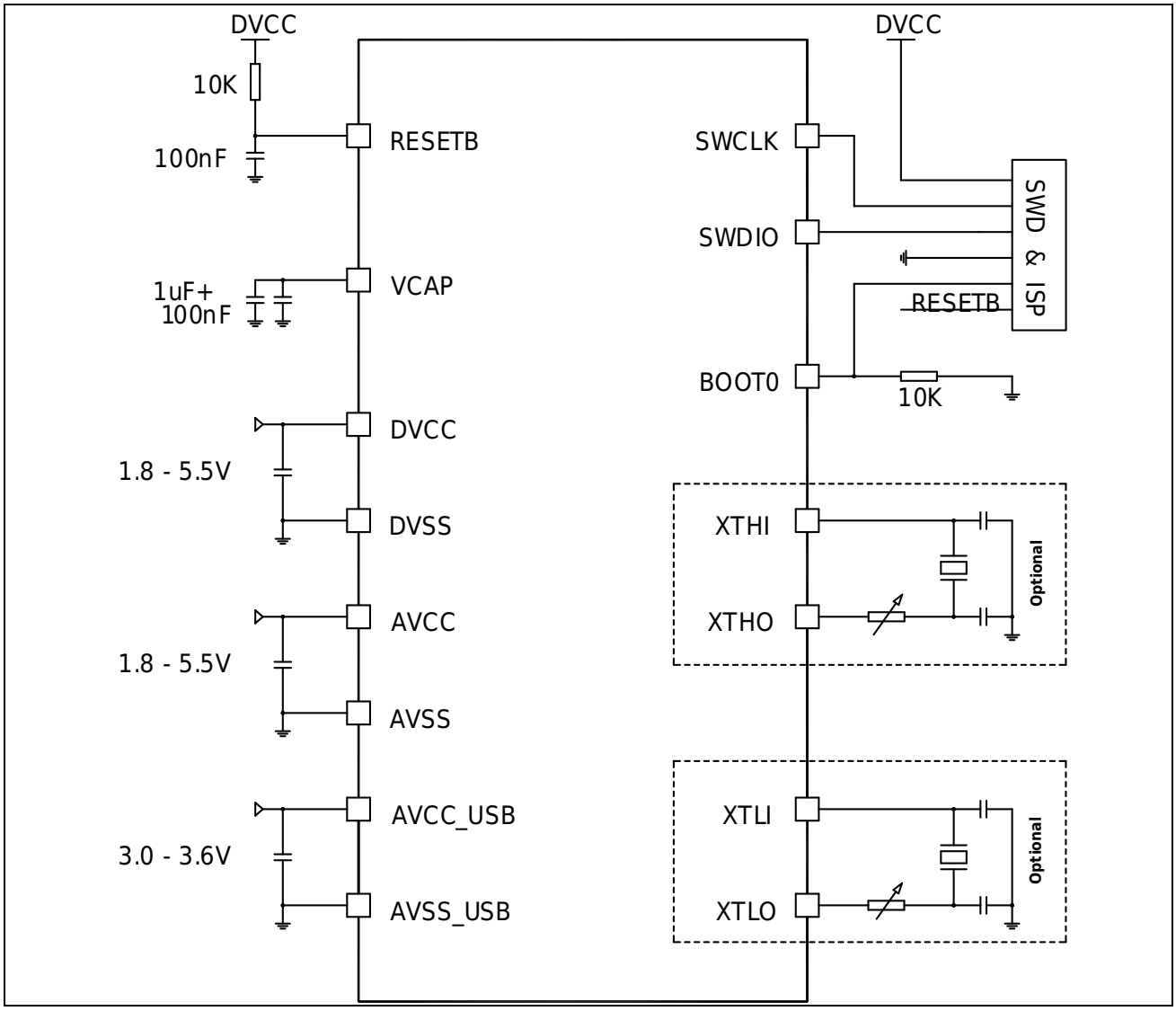
5 Storage area map



Note:
1.The port ctrl module is divided into two addresses.


Keep
0x2000_4000
SRAM
(16KByte)
0x2000_0000
Keep
0x0002_0000
Main flash
area
(128KByte)
0x0000_0000

6 Typical application circuit diagram



Note:

- AVCC and DVCC voltage must be the same.
- When supplying power to AVCC_USB, the voltage of AVCC and DVCC should not be less than AVCC_USB.
- When the USB function is not used, the AVCC_USB pin is recommended to be left floating or grounded.
- Each power supply needs a decoupling capacitor, which should be as close as possible to the corresponding power supply pin.

7 Electrical characteristics

7.1 Test Conditions

Unless otherwise specified, all voltages are based on VSS.

7.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be in the worst environment through the test performed on 100% of the products in the production line at ambient temperature T_A=25℃ and T_A=$T_A$max ($T_A$max matches the selected temperature range) Guaranteed over temperature, supply voltage, and clock frequency.

The notes at the bottom of each table indicate data obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line; on the basis of comprehensive evaluation, the minimum and maximum values are after sample testing. Take the average value and add or subtract three times the standard distribution (mean ± 3Σ).

7.1.2 Typical value

Unless otherwise specified, typical data is based on T_A=25℃ and VCC=3.3V (1.8V ≤ VCC ≤ 5.5V voltage range). These data are only used for design guidance and not tested.

The typical ADC accuracy value is obtained by sampling a standard batch and testing under all temperature ranges. The error of 95% of the products is less than or equal to the given value (average ± 2Σ).

7.2 Absolute maximum ratings

If the load on the device exceeds the value given in the "Absolute Maximum Ratings" list, it may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device under this condition is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 7-1 Voltage Characteristics

Symbol	Description	Minimum Value	Maximum Value	Unit
VCC - VSS	External main supply voltage (includes AVCC and DVCC)(1)	-0.3	5.5	V V
AVCC_USB	USB module supply voltage(2)	3.0	3.6	V
V_{IN}	Input voltage on other pins(3)	VSS-0.3	VCC + 0.3	V
| ΔVCCx |	Voltage difference between different power supply pins		50	mV
| VSSx - VSS |	Voltage difference between different ground pins		50	mV
V_{ESD}(HBM)	ESD electrostatic discharge voltage (human body model)	Refer to absolute maximum electrical parameters		V

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to the external power supply system within the allowable range.
2. AVCC_USB cannot be higher than AVCC/DVCC 0.3V.
3. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When V_{IN} >VCC, there is a forward injection current; when V_{IN} <VSS, there is a reverse injection current.

Table 7-2 Voltage Characteristics

Symbol	Description	Max (1)	Unit
IVCC	The total current (supply current) through the DVCC/AVCC power cord (1)	300	mA
IVSS	The total current through the VSS ground wire (outflow current) (1)	300	mA
IIO	Output sink current on any I/O and control pin	25	mA
	Output current on any I/O and control pin	-25	mA
IINJ(PIN)(2) (3)	Injection current of RESETB pin	+/-5	mA
	Injection current of XTHI pin of XTH and XTLI pin of XTL	+/-5	mA
	Injection current of other pins (4)	+/-5	mA
∑IINJ(PIN) (2)	Total injection current on all I/O and control pins (4)	+/-25	mA

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to the external power supply system within the allowable range.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When V_{IN} >VCC, there is a forward injection current; when V_{IN} <VSS, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute value of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 temperature characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-65 ~ + 150	℃
T_J	Maximum junction temperature	105	℃

7.3 Operating conditions

7.3.1 General working conditions

Table 7-4 General Operating Conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
f_{HCLK}	Internal AHB clock frequency		0	48	MHz
f_{PCLK0}	Internal APB0 clock frequency		0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	48	MHz
DVCC	Working voltage of digital part	AVCC_USB=0V	1.8	5.5	V
AVCC(1)	Analog part working voltage		1.8	5.5	V
DVCC	Working voltage of digital part	AVCC_USB>3.0V	AVCC_USB	5.5	V
AVCC(1)	Analog part working voltage		AVCC_USB	5.5	V
AVCC_USB	USB module supply voltage		3.0	3.6	V
P_D	Power dissipation T_A=85℃	LQFP100		476	mW
	Power dissipation T_A=85℃	LQFP64		455	mW
	Power dissipation T_A=85℃	LQFP48		364	mW
	Power dissipation T_A=85℃	QFN32		526	mW
T_A	Ambient temperature	Maximum power consumption	-40	85	℃
		Low power consumption (2)	-40	105	℃
T_J	Junction temperature range		-40	105	℃

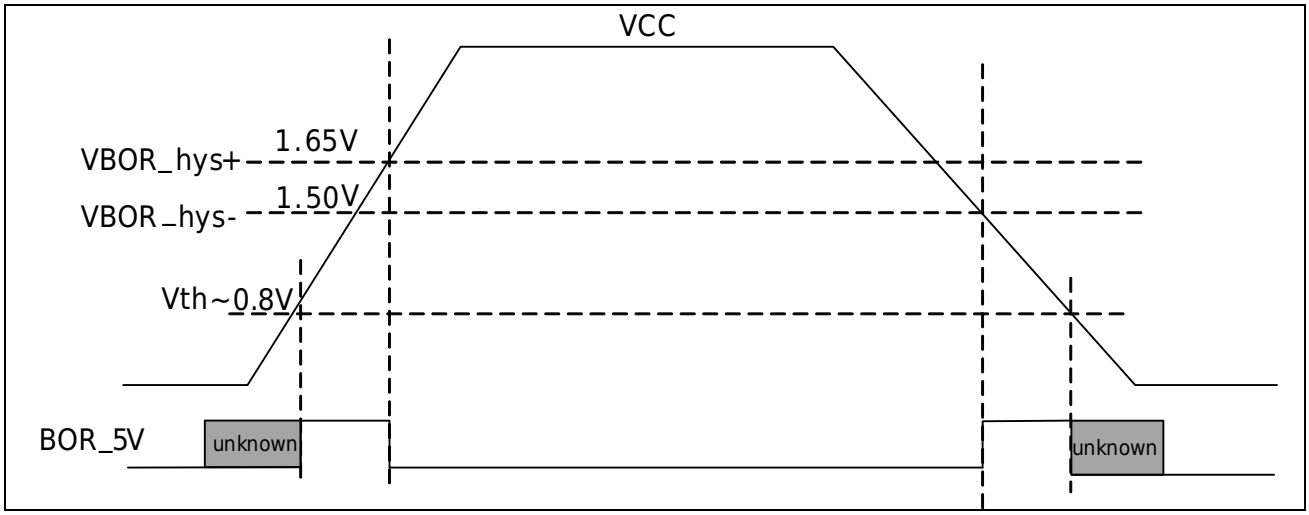
1. AVCC and DVCC voltage must be the same.
2. In a state of lower power dissipation, as long as T_J does not exceed T_{Jmax} , T_A can be extended to this range.

7.3.2 Working conditions at power-up and power-down

Table 7-5 Power-up and power-down operating conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{Vcc}	VCC rising rate		0	5	V/μs
t_{Vcc}	VCC falling rate		10	5	V/μs

7.3.3 Embedded reset and LVD module features



1. Guaranteed by design, not tested in production.

Figure 7-1 POR/Brown Out Diagram

Table 7-6 POR/Brown Out

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vpor	POR release voltage (power-on process) BOR detection voltage (power-down process)		1.45	1.50	1.65	V

Table 7-7 LVD module characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vex	External input voltage range		0		VCC	V
Vlevel	Detection threshold	LVD_CR.VTDS=0000 LVD_CR.VTDS =0001 LVD_CR.VTDS =0010 LVD_CR.VTDS =0011 LVD_CR.VTDS =0100 LVD_CR.VTDS=0101 LVD_CR.VTDS=0110 LVD_CR.VTDS=0111 LVD_CR.VTDS=1000 LVD_CR.VTDS=1001 LVD_CR.VTDS=1010 LVD_CR.VTDS=1011 LVD_CR.VTDS=1100 LVD_CR.VTDS=1101 LVD_CR.VTDS=1110 LVD_CR.VTDS=1111	1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2	1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3	1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3 3.4	V
Icomp	Power consumption			0.12		μA
Tresponse	Response time			80		μs
Tsetup	Establishment time			400		μs
Vhyste	Hysteresis voltage			40		mV
Tfilter	Filter time	LVD_debounce = 000 LVD_debounce = 001 LVD_debounce = 010 LVD_debounce = 011 LVD_debounce = 100 LVD_debounce = 101 LVD_debounce = 110 LVD_debounce = 111		7 14 28 112 450 1800 7200 28800		μs

7.3.4 Built-in reference voltage

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{REF25}	Internal 2.5V Reference Voltage	Room temperature 25°C 3.3V	2.475	2.5	2.525	V
V_{REF25}	Internal 2.5V Reference Voltage	-40 ~ 85°C 2.8 ~ 5.5V	2.463	2.5	2.525	V[1]
V_{REF15}	Internal 1.5V Reference Voltage	Room temperature 25°C 3.3V	1.485	1.5	1.515	V
V_{REF15}	Internal 1.5V Reference Voltage	-40 ~ 85°C 1.8 ~ 5.5V	1.477	1.5	1.519	V[1]
T_{Coeff}	Internal 2.5V 1.5V temperature coefficient	-40 - 85°C			120	ppm/°C

1. The data is based on the assessment results, not tested in production

7.3.5 Supply Current characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program in memory The location in and executed code, etc.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24MHz, 1 wait cycle for 24~48MHz).
- When the peripheral is turned on: $f_{PCLK0} = f_{HCLK}$, $f_{PCLK1} = f_{HCLK}$.

Table 7-8 Operating Current Characteristics

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
I_{DD} (AVCC_USB)		Active			4		mA
I_{DD} (Run in RAM)	All peripherals clock ON, Run while(1) in RAM	Vcap=1.5V V_{CC}=3.3V T_A=2xC	RCH clock source	4M	990		µA
				8M	1960		
				16M	3870		
				22.12M	5360		
				24M	5780		
			PLL RCH4M to xxM clock source	32M	7910		
				48M	11770		
	All peripherals clock OFF, Run while(1) in RAM	Vcap=1.5V V_{CC}=3.3V T_A=2xC	RCH clock source	4M	340		µA
				8M	650		
				16M	1240		
				22.12M	1700		
				24M	1840		

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
			PLL RCH4M to xxM clock source	32M	2690		
				48M	3950		
I_{DD} (Run CoreMark)	All peripherals clock OFF, Run CoreMark in Flash	Vcap=1.5V V_{CC}=3.3V T_A=2xC	RCH clock source	4M	820		µA
				8M	1550		
				16M	2980		
				22.12M	4000		
				24M	4320		
			PLL RCH4M to xxM	48M FlashWait=1	6810		
I_{DD} (Run mode)	All peripherals clock ON, Run while(1) in Flash	Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	RCH clock source	4M	1330	1800	µA
				8M	2490	3430	
				16M	4990	6570	
				22.12M	6760	8960	
				24M	7260	9680	
		Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH4M to xxM clock source	16M	5270	6550	µA
				24M	7390	9260	
				32M FlashWait=1	9200	10640	
				40M FlashWait=1	11350	13150	
				48M FlashWait=1	13470	15750	
		Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH8M to xxM clock source	16M	5350	6620	µA
				24M	7460	9390	
				32M FlashWait=1	9250	10740	
				40M FlashWait=1	11380	13290	
				48M FlashWait=1	13560	15850	
	All peripherals clock OFF, Run while(1) in Flash	Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	RCH clock source	4M	670	1080	µA
				8M	1190	1990	
				16M	2280	3580	
				22.12M	3070	4790	
				24M	3290	5120	
		Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH4M to xxM clock source	16M	2560	3530	µA
				24M	3450	4780	
				32M FlashWait=1	3950	4670	
				40M FlashWait=1	4800	5710	
				48M FlashWait=1	5680	6780	
		Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH8M to xxM clock source	16M	2620	3610	µA
				24M	3510	4860	
				32M FlashWait=1	4010	4730	
				40M FlashWait=1	4850	5760	

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
				48M FlashWait=1	5730	6850	
I_{DD} (Sleep mode)	All peripherals clock ON	Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	RCH clock source	4M	840	950	μA
				8M	1640	1880	
				16M	3240	3680	
				22.12M	4490	5120	
				24M	4850	5570	
		Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH4M to xxM clock source	16M	3550	4070	μA
				24M	5060	5770	
				32M FlashWait=1	6680	7640	
				40M FlashWait=1	8300	9510	
				48M FlashWait=1	9920	11370	
		Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH8M to xxM clock source	16M	3620	4120	μA
				24M	5120	5850	
				32M FlashWait=1	6740	7710	
				40M FlashWait=1	8340	9580	
				48M FlashWait=1	9980	11430	
	All peripherals clock OFF	Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	RCH clock source	4M	180	230	μA
				8M	330	390	
				16M	600	690	
				22.12M	820	930	
				24M	880	1000	
		Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH4M to xxM clock source	16M	900	1020	μA
				24M	1110	1260	
				32M FlashWait=1	1410	1610	
				40M FlashWait=1	1730	1970	
				48M FlashWait=1	2040	2330	
		Vcap=1.5V V_{CC}=1.8-5.5V T_A=N40C-85C	PLL RCH8M to xxM clock source	16M	960	1090	μA
				24M	1170	1330	
				32M FlashWait=1	1470	1670	
				40M FlashWait=1	1780	2030	
				48M FlashWait=1	2100	2390	
I_{DD} (LP Run)	All peripherals clock ON, Run while(1) in Flash	Vcap=1.5V V_{CC}=1.8-5.5V	XTL32K clock source Driver=0x0	T_A=N40-25C	17	22	μA
				T_A=50C	18	23	
				T_A=85C	24	31	
	All peripherals clock OFF, Run while(1) in Flash	Vcap=1.5V V_{CC}=1.8-5.5V	XTL32K clock source Driver=0x0	T_A=N40-25C	12	16	μA
				T_A=50C	13	17	
				T_A=85C	19	25	

Symbol	Parameter	Conditions			Typ(1)	Max(2)	Unit
I_{DD} (LP Sleep)	All peripherals clock ON	Vcap=1.5V V_{CC}=1.8-5.5V	XTL32K clock source Driver=0x0	T_A=N40-25C	12	13	μA
				T_A=50C	13	14	
				T_A=85C	19	21	
	All peripherals clock OFF	Vcap=1.5V V_{CC}=1.8-5.5V	XTL32K clock source Driver=0x0	T_A=N40-25C	7	7	μA
				T_A=50C	8	8	
				T_A=85C	14	16	
I_{DD} (DeepSleep mode)	XTL32K +DeepSleep	Vcap=1.5V V_{CC}=1.8-5.5V	XTL32K Driver=0x0	T_A=N40-25C	4580	5460	nA
				T_A=50C	5290	6390	
				T_A=85C	9750	12000	
	IRC32K +DeepSleep	Vcap=1.5V V_{CC}=1.8-5.5V		T_A=N40-25C	4570	5430	nA
				T_A=50C	5270	6350	
				T_A=85C	9750	12000	
	WDT +DeepSleep	Vcap=1.5V V_{CC}=1.8-5.5V		T_A=N40-25C	4300	5120	nA
				T_A=50C	4990	6030	
				T_A=85C	9410	11620	
	DeepSleep	Vcap=1.5V V_{CC}=1.8-5.5V		T_A=N40-25C	4190	5000	nA
				T_A=50C	4880	5910	
				T_A=85C	9330	11570	

1. If there are no other specified conditions, the value of this Typ is measured at 25℃& V_{CC} = 3.3V.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of V_{CC} = 1.8-5.5 & Temperature = N40-85°C.
3. The data is based on the assessment results and is not tested in production.

7.3.6 Time to wake up from low power mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- RCH oscillator when entering deep sleep

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
T_{wu}	Sleep mode wake-up time			1.8		μs
	Deep sleep wake-up time	F_{MCLK} = 4MHz		9.0		μs
		F_{MCLK} = 8MHz		6.0		μs
		F_{MCLK} = 16MHz		5.0		μs
		F_{MCLK} = 24MHz		4.0		μs

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

7.3.7 External timer characteristic

7.3.7.1 External input high-speed clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTH_ext}	User external clock frequency (1)		0	8	32	MHz
V_{XTHH}	Input pin high level voltage		0.7VCC		VCC	V
V_{XTHL}	Input pin low voltage		VSS		0.3VCC	V
$T_{r(XTH)}$	Rise time (1)				20	ns
$T_{f(XTH)}$	Falling time (1)				20	ns
$T_{w(XTH)}$	Enter high or low time (1)		16			ns
$C_{in(XTH)}$	Input capacitive reactance (1)			5		pF
Duty	Duty ratio		40		60	%
I_L	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

7.3.7.2 External input low-speed clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{XTL_ext}	User external clock frequency (1)		0	32.768	1000	kHz
V_{XTLH}	Input pin high level voltage		0.7VCC		VCC	V
V_{XTLL}	Input pin low voltage		VSS		0.3VCC	V
$T_{r(XTL)}$	Rise time (1)				50	ns
$T_{f(XTL)}$	Falling time (1)				50	ns
$T_{w(XTL)}$	Enter high or low time (1)		450			ns
$C_{in(XTL)}$	Input capacitive reactance (1)			5		pF
Duty	Duty ratio		30		70	%
I_L	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

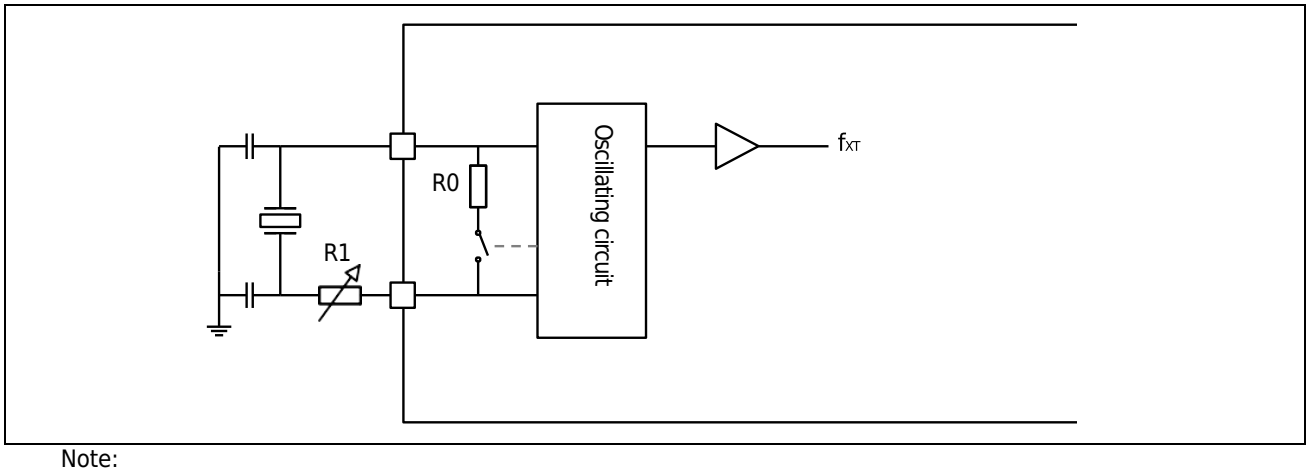
7.3.7.3 High-speed external clock XTH

The high-speed external clock (XTH) can be generated using a 8-32MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency	-	8	-	32	MHz
ESR_{CLK}	Supported crystal oscillator ESR range	32MHz	-	-	60	Ω
		24MHz	-	-	80	
		16MHz	-	-	100	
		8MHz	-	-	120	
C_{LX} (3)	Load capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
Duty	Duty ratio	-	40	50	60	%
I_{dd} (4)	Current	XTH_CR[3:0]=0b1111	-	1000	-	μA
		XTH_CR[3:0]=0b1110	-	600	-	
		XTH_CR[3:0]=0b1010	-	370	-	
		XTH_CR[3:0]=0b0110	-	300	-	
		XTH_CR[3:0]=0b0010	-	160	-	
g_m	transconductance	XTH_CR[3:0]=0b1111	-	11.75	-	mA/V
		XTH_CR[3:0]=0b1110（32MHz 24MHz Recommended value）	-	6.34	-	
		XTH_CR[3:0]=0b1101	-	4.38	-	
		XTH_CR[3:0]=0b1100	-	3.38	-	
		XTH_CR[3:0]=0b1011	-	7.41	-	
		XTH_CR[3:0]=0b1010（16MHz Recommended value）	-	4.01	-	
		XTH_CR[3:0]=0b1001	-	2.77	-	
		XTH_CR[3:0]=0b1000	-	2.14	-	
		XTH_CR[3:0]=0b0111	-	5.59	-	
		XTH_CR[3:0]=0b0110（12MHz Recommended value）	-	3.01	-	
		XTH_CR[3:0]=0b0101	-	2.08	-	
		XTH_CR[3:0]=0b0100	-	1.60	-	

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
		XTH_CR[3:0]=0b0011	-	2.50	-	
		XTH_CR[3:0]=0b0010（8MHz Recommended value）	-	1.30	-	
		XTH_CR[3:0]=0b0001	-	0.93	-	
		XTH_CR[3:0]=0b0000	-	0.72	-	
T_{start}(5)	Start time	32MHz, CL=16pF @ XTH_CR[3:0]=0b1110	-	500	-	μs
		8MHz, CL=16pF @ XTH_CR[3:0]=0b0010	-	2	-	ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Resulted from comprehensive evaluation, not tested in production.
3. C_{LX} refers to the load capacitors C_{L1} and C_{L2} of XTAL's two pins. For C_{L1} and C_{L2}, it is recommended to use a high quality ceramic capacitor designed for high frequency applications and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give load capacitance parameters in a serial combination of C_{L1} and C_{L2}. When selecting C_{L1} and C_{L2}, parameters such as crystal frequency and ESR should be taken into account, and the capacitive reactance of PCB and MCU pins should be taken into account.
4. The current varies with the choice of frequency and drive capability. The higher the frequency, the stronger the driving power, and the greater the current consumption.
5. Tstart is the start-up time, which is the time from the software enabling XTH to start measuring until a stable 32MHz/8MHz oscillation is obtained. This value is measured on a standard crystal resonator under the setting of XTH_CR[5:4] =0b10. It may vary greatly depending on the crystal manufacturer and model.



Note:

- The matching capacitor of the crystal **is recommended to** be configured in accordance with the requirements of the crystal manufacturer's technical manual.
  If the crystal manufacturer gives the ***value of the load capacitor***, the matching capacitor should be twice the value of the load capacitor given by the crystal manufacturer. If the crystal manufacturer gives the ***capacitance value of the matching capacitor***, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.
- The feedback resistor R0 has been integrated in the chip.

– Damping resistor R1 is optional. The value of the resistance depends on the crystal characteristics. The default value is 0Ω.

7.3.7.4 Low-speed external clock XTL

The low-speed external clock (XTL) can be generated using a 32.768kHz crystal/ceramic resonator oscillator. The information given in this section is based on typical external components and the results obtained through comprehensive characteristic evaluation. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency	-	-	32.768	-	kHz
ESR_{CLK}	Supported crystal oscillator ESR range	-	-	-	60	kΩ
C_{Lx} (2)	Load capacitance	Configure as required by the crystal manufacturer.	8	12	20	pF
DC_{ACLK}	Duty ratio	-	30	50	70	%
I_{dd}(3)	Current	XTL_CR[3:0]=0b1111	-	1330	-	nA
		XTL_CR[3:0]=0b1011	-	1230	-	
		XTL_CR[3:0]=0b0111	-	1140	-	
		XTL_CR[3:0]=0b0011	-	1050	-	
		XTL_CR[3:0]=0b1110	-	630	-	
		XTL_CR[3:0]=0b1010（Recommended value)	-	580	-	
		XTL_CR[3:0]=0b0110	-	530	-	
		XTL_CR[3:0]=0b0010	-	490	-	
g_m	transconductance	XTL_CR[3:0]=0b1111	-	14.64	-	μA/V
		XTL_CR[3:0]=0b1011	-	13.17	-	
		XTL_CR[3:0]=0b0111	-	11.67	-	
		XTL_CR[3:0]=0b0011	-	10.15	-	
		XTL_CR[3:0]=0b1110	-	7.37	-	
		XTL_CR[3:0]=0b1010（Recommended value)	-	6.62	-	
		XTL_CR[3:0]=0b0110	-	5.87	-	
		XTL_CR[3:0]=0b0010	-	5.10	-	
T_{start}(4)	Start time	ESR=30kΩ C_L=12pF XTL_CR[3:0]=0b1010	-	2000	-	ms

1. Resulted from comprehensive evaluation, not tested in production.
2. C_{LX} refers to the load capacitance of the two pins of XTAL. The user **must** select the capacitance value of this capacitor according to the requirements of the crystal manufacturer.

   If the crystal manufacturer gives the ***value of the load capacitor***, the matching capacitor should be twice

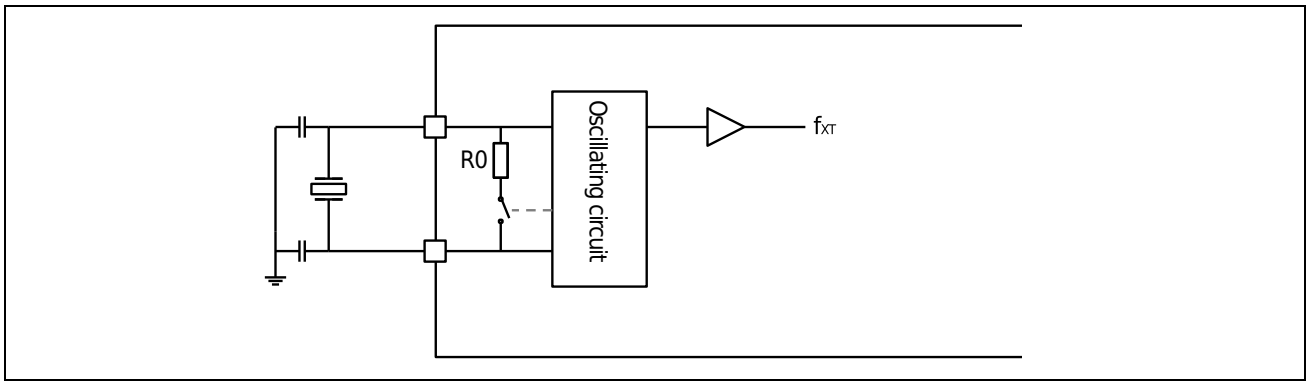
the value of the load capacitor given by the crystal manufacturer.

If the crystal manufacturer gives the ***capacitance value of the matching capacitor***, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.

Example: When the crystal manufacturer gives the ***load capacitance*** of the crystal as 8pF, the capacitance of the matching capacitor should be 16pF. Considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 15pF or 12pF.

The crystal manufacturer gives the ***matching capacitance*** of the crystal as 12pF, the matching capacitance should be 12pF. Considering the distributed capacitance between the PCB and MCU pins, it is recommended to choose a matching capacitor with a capacitance of 10pF or 8pF.

3. Select a high-quality oscillator with a small ESR value (such as MSIV-TIN32.768kHz), which can be adjusted by the XTL_CR[3:0] setting value to optimize current consumption. Current consumption is proportional to the transconductance (gm) provided by the circuit.
4. Tstart is the start-up time, which is the time from the software enabling XTL to start measuring until a stable 32768 oscillation is obtained. This value is measured on a standard crystal resonator under the settings of XTL_CR[3:0]=0b1010 and XTL_CR[5:4]=0b11. It may vary greatly depending on the crystal manufacturer and model.



Note:

- The matching capacitor of the crystal is recommended to be configured in accordance with the requirements of the crystal manufacturer's technical manual.

  If the crystal manufacturer gives the ***value of the load capacitor***, the matching capacitor should be twice the value of the load capacitor given by the crystal manufacturer. If the crystal manufacturer gives the ***capacitance value of the matching capacitor***, you can directly use the capacitance value of the matching capacitor given by the crystal manufacturer.
- The feedback resistor R0 has been integrated in the chip.

7.3.8 Internal timer characteristics

7.3.8.1 Internal RCH oscillator

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and T_A conditions		0.25		%
		VCC = 1.8 ~ 5.5V T_{AMB} = -40 ~ 85°C	-3.5		+3.5	%
		VCC = 1.8 ~ 5.5V T_{AMB} = -20 ~ 85°C	-2.5		+2.5	%
		VCC = 1.8 ~ 5.5V T_{AMB} = -20 ~ 50°C	-2.0		+2.0	%
F_{CLK}	Oscillation frequency		4.0	4.0 8.0 16.0 22.12 24.0	24.0	MHz
I_{CLK}	Power consumption	F_{MCLK} = 4MHz		80		µA
		F_{MCLK} = 8MHz		100		µA
		F_{MCLK} = 16MHz		120		µA
		F_{MCLK} = 24MHz		140		µA
DC_{CLK}	Duty Cycle (1)		45	50	55	%

1. Resulted from comprehensive evaluation, not tested in production.

7.3.8.2 Internal RCL oscillator

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and T_A conditions		0.5		%
		VCC = 1.8 ~ 5.5V T_{AMB} = -40 ~ 85°C TAMB = -40°C ~ 85°C	-5		+5	%
		VCC = 1.8 ~ 5.5V T_{AMB} = -20 ~ 50°C	-3		+3	%
F_{CLK}	Oscillation frequency			38.4 32.768		kHz
T_{CLK}	Start time			150		µs
DC_{CLK}	Duty Cycle (1)		25	50	75	%
I_{CLK}	Power consumption			0.35		µA

1. Resulted from comprehensive evaluation, not tested in production.

7.3.8.3 Internal low speed clock 10k oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V	Operation voltage	-	1.8		5.5	V
Dev	Oscillator accuracy(1)	VCC = 1.8 ~ 5.5V T_{AMB} = -20 ~ 50°C	-50	-	50	%
F_{CLK}	Oscillation frequency	VCC=3.3v T_{AMB} = 25°C		10		KHz

1. Resulted from comprehensive evaluation, not tested in production.

7.3.8.4 Internal USB dedicated RCH48M oscillator

Parameter	Description	Min	Typ	Max	Units	Condition
DVCC	Analog 5V Supply	1.8	3.3	5.5	V	
T	Junction Temperature	-40	27	105	deg C	
F_{RCH48M}	Frequency	-	48	-	MHz	-
TRIM	RCH48M user-trimming step	0.06(2)	0.12	0.2(2)	%	-
$DUCy_{RCH48M}$	Duty cycle	45(2)	-	55(2)	%	-
ACC_{RCH48M}	Accuracy of the RCH48M oscillator(factory calibrated)	6(3)	-	6(3)	%	T_A=-40 to 105 ºC
		TBD(3)	-	TBD(3)	%	T_A=-10 to 85 ºC
		TBD(3)	-	TBD(3)	%	T_A=0 to 70 ºC
		2(3)	-	2(3)	%	T_A=25 ºC
$t_{su(RCH48M)}$	RCH48M oscillator startup time	-	-	20(2)	µs	
$I_{DDA(RCH48M)}$	RCH48M oscillator power consumption	-	270	350(2)	µA	

1. AVCC=3.3V, T_A=-40 to 105 ºC unless otherwise specified.
2. Guatanteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

7.3.9 PLL Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Fin(1)	Input clock		4	4	24	MHz
	Input clock duty cycle		40		60	%
Fout	Output frequency		8	-	48	MHz
Duty(1)	Output duty cycle		48%	-	52%	
Tlock(1)	Lock time	Input frequency 4MHz	-	100	200	μs

1. Resulted from comprehensive evaluation, not tested in production.

7.3.10 Memory Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
EC_{FLASH}	Erase times	Regulator voltage=1.5V, T_{AMB} = 25℃	20			kcycles
RET_{FLASH}	Data retention period	T_{AMB} = 85℃, after 20 kcycles	20			Years
T_{b_prog}	Programming time (bytes)		22		30	μs
T_{w_prog}	Programming time (words)		40		52	μs
T_{p_erase}	Page erase time		4		5	ms
T_{m_erase}	Whole chip erase time		30		40	ms

7.3.11 EFT Characteristic

A chip reset can restore the system to normal operation.

Symbol	Level/Type
EFT to IO (IEC61000-4-4)	Class:4（A）
EFT to Power (IEC61000-4-4)	Class:4（A）

Software recommendations

The software process must include control to deal with program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc.)

During the EFT test, interference that exceeds the application requirements can be directly applied to the chip power supply or IO. When an unexpected action is detected, the software part is strengthened to prevent unrecoverable errors.

7.3.12 ESD Characteristic

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$VESD_{HBM}$	ESD @ Human Body Mode			4		kV
$VESD_{CDM}$	ESD @ Charge Device Mode			1		kV
$VESD_{MM}$	ESD @ machine Mode			200		V
Ilatchup	Latch up current			200		mA

7.3.13 I/O port characteristics

7.3.13.1 Output characteristics——ports

Table 7-9 Port output characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
V_{OH}	High level output voltage Source Current	Sourcing 4 mA, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 8 mA, VCC = 3.3 V (see Note 2)	VCC-0.6		V
V_{OL}	Low level output voltage Sink Current	Sinking 5 mA, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 14 mA, VCC = 3.3 V (see Note 2)		VSS+0.6	V
V_{OHD}	High level output voltage Double source Current	Sourcing 8 mA, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 18 mA, VCC = 3.3V (see Note 2)	VCC-0.6		V
V_{OLD}	Low level output voltage Double Sink Current	Sinking 8 mA, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 18 mA, VCC = 3.3 V (see Note 2)		VSS+0.6	V

NOTES: 1. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 40 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, I_{OH}(max) and I_{OL}(max), for all outputs combined, should not exceed 100 mA to satisfy the maximum specified voltage drop.

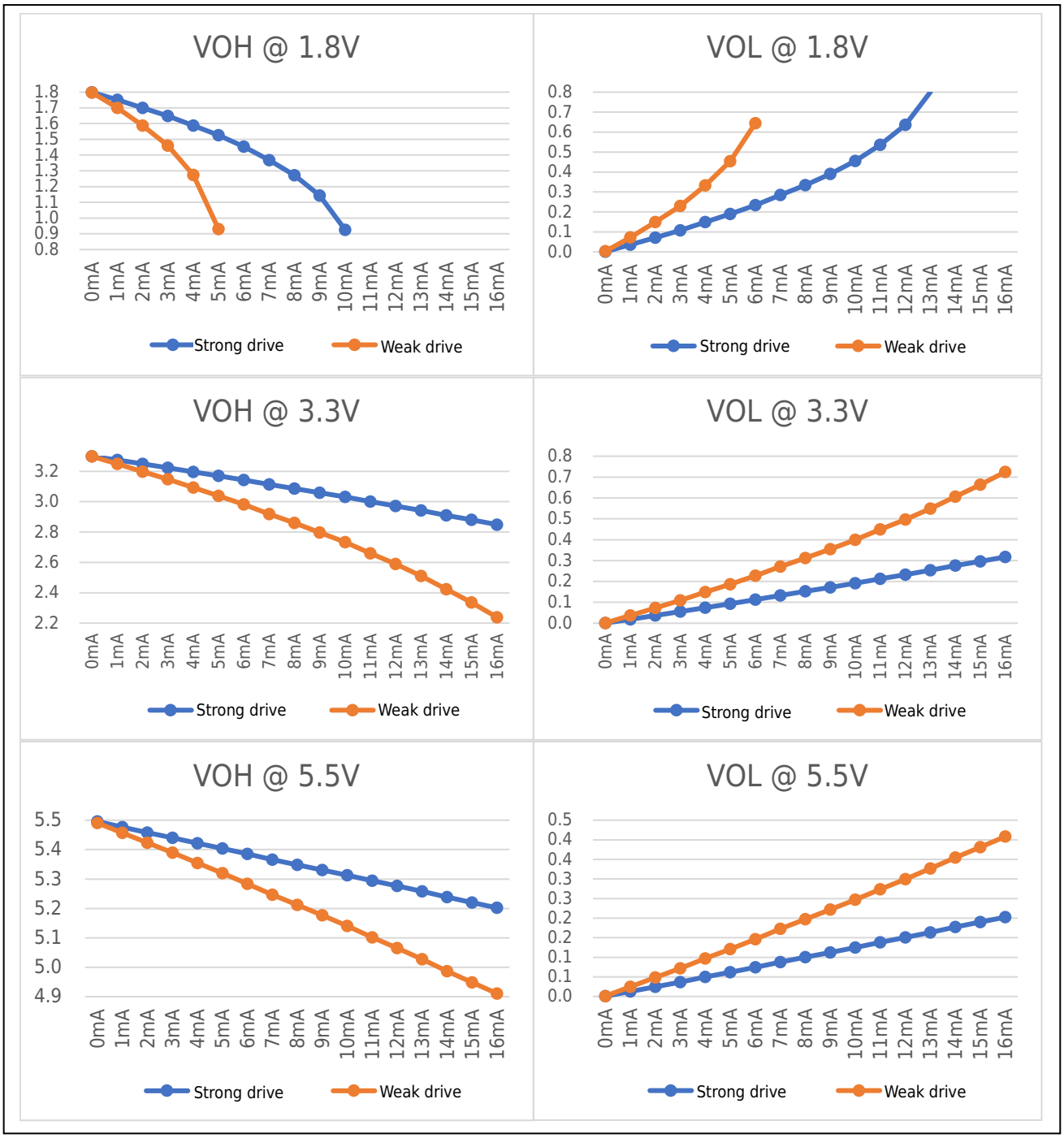


Figure 7-2 Output port VOH/VOL measured curve

7.3.13.2 Input characteristics——ports PA, PB, PC, PD, PE, PF

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IH}	Positive-going input threshold voltage	VCC=1.8V	0.7VCC			V
		VCC=3.3V	0.7VCC			V
		VCC=5.5V	0.7VCC			V
V_{IL}	Negative-going input threshold voltage	VCC=1.8V			0.3VCC	V
		VCC=3.3V			0.3VCC	V
		VCC=5.5V			0.3VCC	V
$V_{hys(1)}$	Input voltage hysteresis (V_{IH} - V_{IL})	VCC=1.8V		0.3		V
		VCC=3.3V		0.4		V
		VCC=5.5V		0.6		V
$R_{pullhigh}$ (GPIO)	Pullup resistor	Pullup enabled VCC=3.3V		80		kΩ
$R_{pulllow}$ (GPIO)	Pulldown resistor	Pulldown enabled VCC=3.3V		40		kΩ
C_{input}	Input capacitance			5		pf

1. Resulted from comprehensive evaluation, not tested in production.

7.3.13.3 Input characteristics——USB_DP, USB_DM

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IH}	Positive-going input threshold voltage	AVCC_USB = 3.0 ~ 3.6	0.7AVCC_USB			V
V_{IL}	Negative-going input threshold voltage				0.3AVCC_USB	V
$V_{hys(1)}$	Input voltage hysteresis (V_{IH} - V_{IL})			0.3		V
$R_{pullhigh}$	Pullup resistor	Transmitting	1425		3090	Ohm
		Idle	900		1575	
C_{input}	Input capacitance			5		pf

1. Resulted from comprehensive evaluation, not tested in production.

7.3.13.4 Port external input sampling requirements——Timer Gate/Timer Clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
t(int)	External interrupt timing	External trigger signal for the interrupt flag (see Note 1)	1.8V	30		ns
			3.3V	30		ns
			5.5V	30		ns
t(cap)	Timer capture timing	Timer4/5/6 capture pulse width Fsystem = 4MHz	1.8V	0.5		μs
			3.3V	0.5		μs
			5.5V	0.5		μs
t(clk)	Timer clock frequency applied to pin	Timer0/1/2/4/5/6 external clock input Fsystem = 4MHz	1.8V		PCLK/2	MHz
			3.3V		PCLK/2	MHz
			5.5V		PCLK/2	MHz
$t(pca)^{(2)}$	PCA clock frequency applied to pin	PCA external clock input Fsystem = 4MHz	1.8V		PCLK/8	MHz
			3.3V		PCLK/8	MHz
			5.5V		PCLK/8	MHz

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.
2. Resulted from comprehensive evaluation, not tested in production.

7.3.13.5 Port leakage characteristics——PA, PB, PC, PD , PE, PF

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$I_{lkg(Px.y)}$	Leakage current	$V_{(Px.y)}$ (see Note 1，2)		±50		nA

NOTES: 1. The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

7.3.14 RESETB pin characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

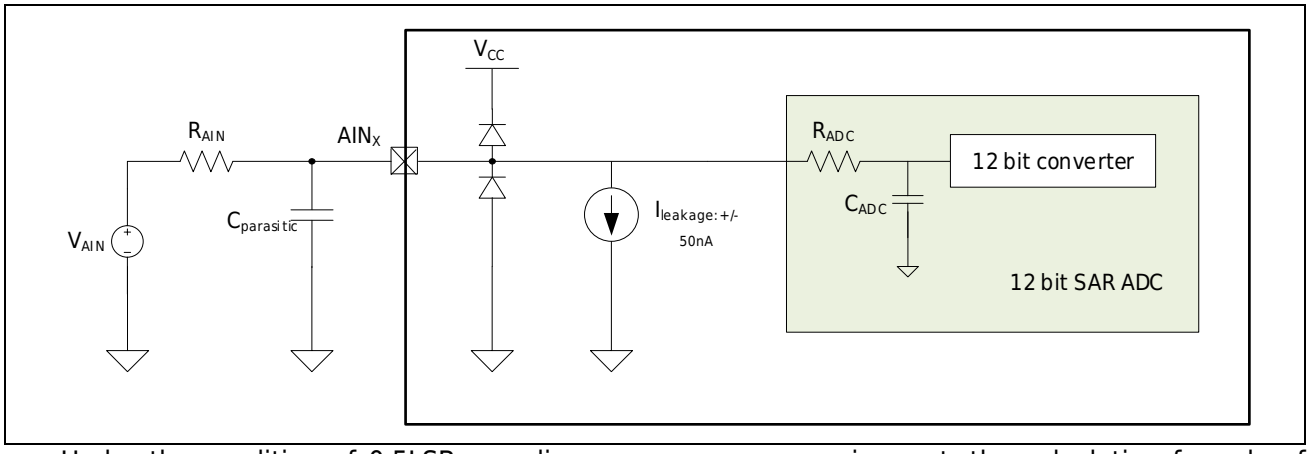
Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
VIL(RESETB) (1)	Input low level voltage		-0.3		0.3VCC	V
VIH(RESETB)	Input high level voltage		0.7VCC		VCC+0.3	V
Vhys(RESETB)	Schmitt trigger voltage hysteresis			200		mV
RPU	Weak pull-up equivalent resistance	VIN = VSS		80		KΩ
TF(RESETB) (1)	Input filter pulse				2	μs
TNF(RESETB) (1)	Input unfiltered pulse		10			μs

1. Guaranteed by design, not tested in production.

7.3.15 ADC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{ADCIN}	Input voltage range	Single ended	0		$V_{ADCREFIN}$	V
$V_{ADCREFIN}$	Input range of external reference voltage	Single ended	0		AVCC	V
$DEV_{AVCC/3}$	AVCC/3 accuracy			3		%
I_{ADC1}	Active current including reference generator and buffer	200Ksps		2		mA
I_{ADC2}	Active current without reference generator and buffer	1Msps		0.5		mA
C_{ADCIN}	ADC input capacitance			16	19.2	pF
R_{ADC}(1)	ADC sampling switch impedance			1.5		kΩ
R_{AIN}(1)	ADC external input resistor(2)				100	kΩ
F_{ADCCLK}	ADC clock Frequency				24M	Hz
$T_{ADCSTART}$	Startup time of reference generator and ADC core			30		μs
$T_{ADCCONV}$	Conversion time		20	24	28	cycles
ENOB	Effective Bits	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF		10.3		Bit
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC		10.3		Bit
		200Ksps@VCC>=1.8V REF=internal 1.5V		9.4		Bit
		200Ksps@VCC>=2.8V REF=internal 2.5V		9.4		Bit
SNR	Signal to Noise Ratio	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF		68.2		dB
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC		68.2		dB
		200Ksps@VCC>=1.8V REF=internal 1.5V		60		dB
		200Ksps@VCC>=2.8V REF=internal 2.5V		60		dB
DNL(1)	Differential non-linearity	200Ksps; VREF=EXREF/AVCC	-1		1	LSB
INL(1)	Integral non-linearity	200Ksps; VREF=EXREF/AVCC	-3		3	LSB
E_o	Offset error			0		LSB
E_g	Gain error			0		LSB

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} = \frac{M}{F_{ADC} * C_{ADC} * (N + 1) * \ln(2)} - R_{ADC}$$

among them F_{ADC} It is the ADC clock frequency. Register ADC_CR0<3:2> can set its relationship with PCLK, as shown in the following table.

The following table shows the ADC clock frequency F_{ADC} Relationship with PCLK frequency division ratio:

ADC_CR0<3:2>	**N**
00	1
01	2
10	4
11	8

M is the number of sampling periods, which is set by the register ADC_CR0<13:12>.

The following table shows the sampling time t_{sa} And ADC clock frequency F_{ADC} Relationship:

ADC_CR0<13:12>	**M**
00	4
01	6
10	8
11	12

The following table shows the ADC clock frequency F_{ADC} And external resistance R_{AIN} Relationship (M=12, under the condition of sampling error 0.5LSB):

R_{AIN} (kΩ)	F_{ADC}(kHz)
10	5600
30	2100
50	1300
80	820
100	660
120	550
150	450

For the above typical applications, you should pay attention to:

- Minimize the ADC input port AIN_X parasitic capacitance $C_{PARACITIC}$;
- In addition to considering R_{AIN} value, if the internal resistance of signal source V_{AIN}, it also needs to be considered.

7.3.16 VC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vin	Input voltage range		0		5.5	V
Vincom	Input common mode range		0		VCC-0.2	V
Voffset	Input offset	Normal temperature 25°C 3.3V	-10		+10	mV
Icomp	Comparator's current	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		0.3 1.2 10 20		μA
Tresponse	Comparator's response time when one input cross another	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2		μs
Tsetup	Comparator's setup time when ENABLE. Input signals unchanged.	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2		μs
Twarmup	From main bandgap enable to Temp sensor voltage, ADC internal 1.5V, 2.5V reference stable			20		μs
Tfilter	Digital filter time	VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111		7 14 28 112 450 1800 7200 28800		μs

7.3.17 OPA Characteristic

OPA: (AVCC=2.2 ~ 5.5 V, AVSS=0 V, Ta=- 40 ~ +85℃)

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vi	Input voltage		0	-	AVCC	V
Vo	Output voltage (1)		0.1	-	AVCC-0.2	V
Io	Output current (1)				2.2	mA
RL	Load resistance (1)		5K			Ohm
Tstart	Initialization time (2)				20	μs
Vio	Input offset voltage	Vic=AVCC/2, Vo=AVCC/2 RL=5kΩ, Rs=50 pF		±6		mV
PM	Phase margin (1)	Vic=AVCC/2, Vo=AVCC/2 RL=5kΩ, CL=50pF		80	-	deg
UGBW	Unity gain bandwidth (1)	Vic=AVCC/2, Vo=AVCC/2 RL=5kΩ, CL=50pF		9.3		MHz
SR	Slew rate (1)	RL=5kΩ, CL=50pF		8		V/μs

1. Guaranteed by design, not tested in production.
2. Need to set BGR_CR<0>=1 at the same time.

7.3.18 DAC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{DACOUT}	Output voltage range	AVCC voltage reference, single ended	0		Vcc	V
V_{DACCM}	Output common mode voltage range		0		Vcc	V
I_{DAC}	Active current	500KSamples/s		15		μA
SR_{DAC}	Sample rate				500	Ksps
$t_{DACCONV}$	Conversion time		2			μs
$t_{DACSETTLE}$	Setting time			5		μs
SNR_{DAC}	Signal to Noise Ratio			59		dB
$SNDR_{DAC}$	Signal to Noise and Distortion Ratio			57		dB
$SFDR_{DAC}$	Spurious Free Dynamic Range			56		dB
$V_{DACOFFSET}$	Offset voltage	w/o buffer		2		mV
DNL_{DAC}	Differential non-linearity			±1		LSB
INL_{DAC}	Integral non-linearity			±5		LSB

7.3.19 TIM timer features

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 7-10 Advanced Timer (ADVTIM) Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution			16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	μs
T_{MAX_COUNT}	Maximum possible count			67108864	t_{TIMCLK}
		f_{TIMCLK}=48MHz		1.4	s

1. Guaranteed by design, not tested in production.

Table 7-11 General Timer Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution			16	Bit
		Mode 0 free counting		32	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	μs
T_{MAX_COUNT}	Maximum possible count			16777216	t_{TIMCLK}
		f_{TIMCLK}=48MHz		349.5	ms

1. Guaranteed by design, not tested in production.

Table 7-12 PCA Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=48MHz	20.8		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=48MHz	0	24	MHz
Res_{Tim}	Timer resolution			16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}
		f_{TIMCLK}=48MHz	0.0208	1363	μs
T_{MAX_COUNT}	Maximum possible count			2097152	t_{TIMCLK}
		f_{TIMCLK}=48MHz		43.69	ms

1. Guaranteed by design, not tested in production.

Table 7-13 WDT Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	WDT overflow time	f_{WDTCLK}=10kHz	1.6	52000	ms

1. Guaranteed by design, not tested in production.

7.3.20 Communication Interface

7.3.20.1 I2C features

I2C interface characteristics are as follows:

Table 7-14 I2C Interface Characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	Minimum Value	Maximum Value	
t_{SCLL}	SCL clock low time	4.7		1.25		0.5		μs
t_{SCLH}	SCL clock high time	4.0		0.6		0.26		μs
$t_{SU.SDA}$	SDA establishment time	250		100		50		ns
$t_{HD.SDA}$	SDA hold time	0		0		0		μs
$t_{HD.STA}$	Start condition hold time	2.5		0.625		0.25		μs
$t_{SU.STA}$	Repeated start condition establishment time	2.5		0.6		0.25		μs
$t_{SU.STO}$	Stop condition establishment time	0.25		0.25		0.25		μs
t_{BUF}	Bus idle (stop condition to start condition)	4.7		1.3		0.5		μs

1. Guaranteed by design, not tested in production.

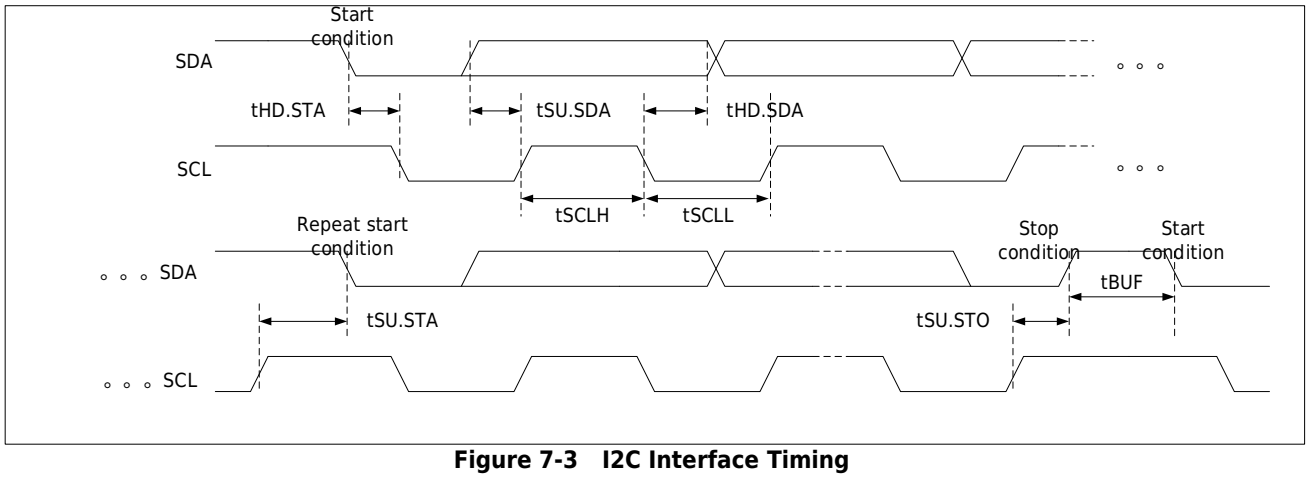


Figure 7-3 I2C Interface Timing

7.3.20.2 SPI features

Table 7-15 SPI Interface Features (1)(2)

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
$t_{c(SCK)}$	Serial clock period(3)	Host Transmission Mode f_{PCLK} = 32MHz	62.5	-	ns
		Host Receive Mode f_{PCLK} = 48MHz	160	-	ns
		Slave Transmission Mode f_{PCLK} = 48MHz	160	-	ns
		Slave Receive Mode f_{PCLK} = 48MHz	84	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Host mode	0.45 × $t_{c(SCK)}$	-	ns
		Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Host mode	0.45 × $t_{c(SCK)}$	-	ns
		Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{h(SSN)}$	Hold time selected by slave	Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of host data output	-	-	3	ns
$t_{h(MO)}$	Hold time of host data output	-	2	-	ns
$t_{v(SO)}$	Effective time of slave data output	-	-	20+1.5*T_{PCLK}	ns
$t_{h(SO)}$	Hold time of slave data output	-	10+0.5*T_{PCLK}	-	ns
$t_{su(MI)}$	Setup time of host data input	-	10	-	ns
$t_{h(MI)}$	Hold time of host data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	10	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	2	-	ns

1. Guaranteed by design, not tested in production.
2. Data is given based on the condition that VCC=3.0V.
3. The maximum frequency division coefficient of host mode is PCLK/2, and the maximum frequency division coefficient of slave mode is PCLK/4.

The waveform and timing parameters of the SPI interface signal are as follows:

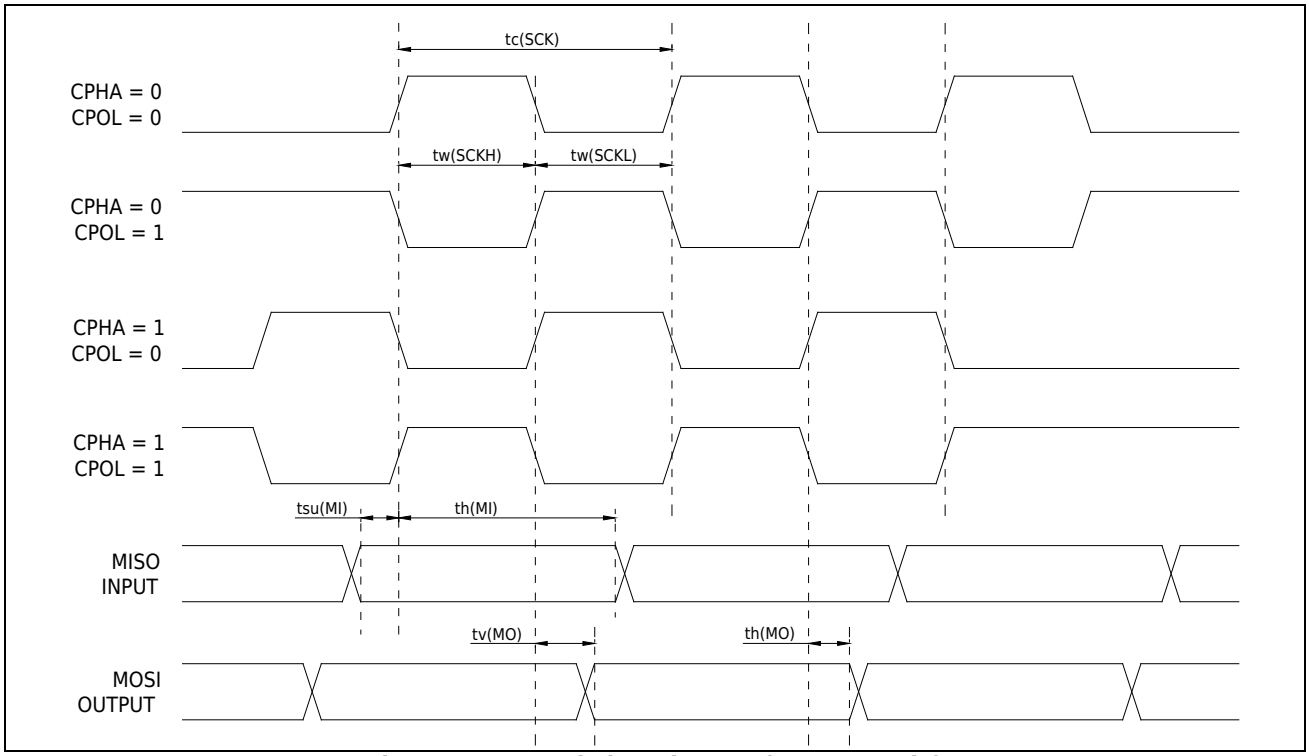


Figure 7-4 SPI Timing Diagram (Master mode)

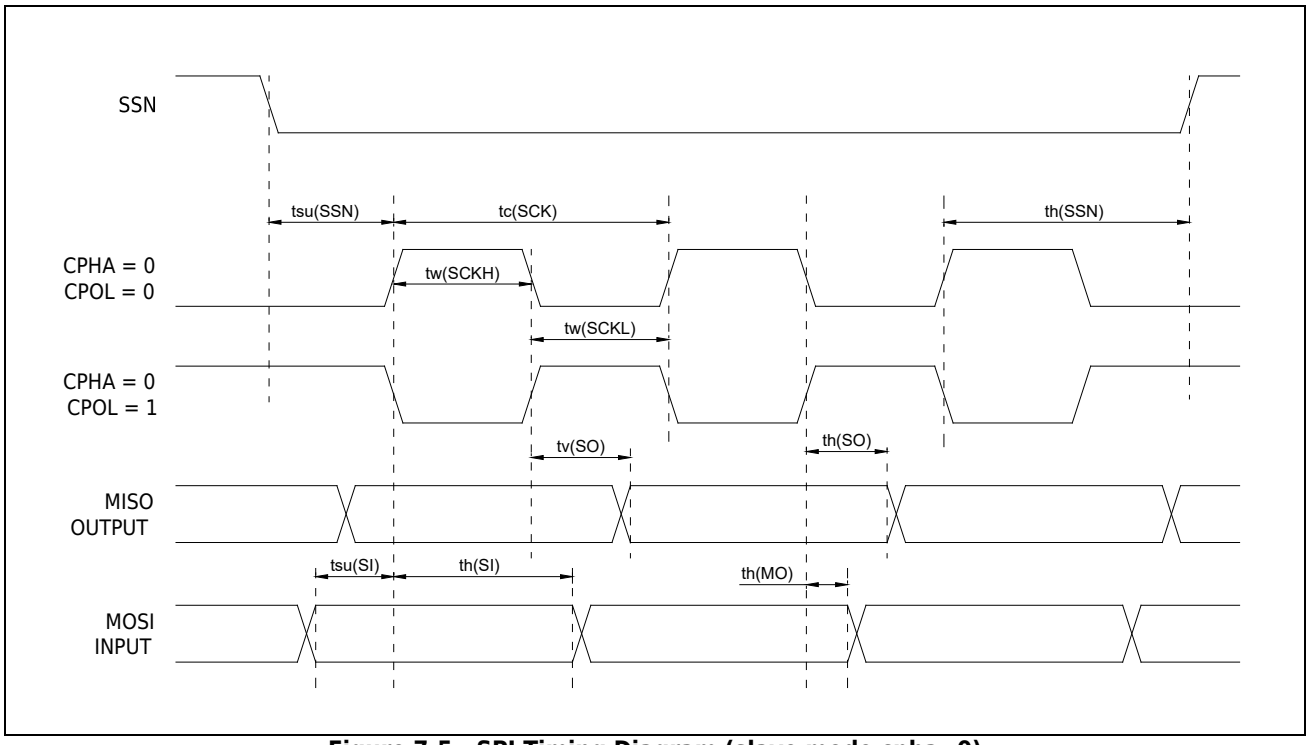


Figure 7-5 SPI Timing Diagram (slave mode cpha=0)

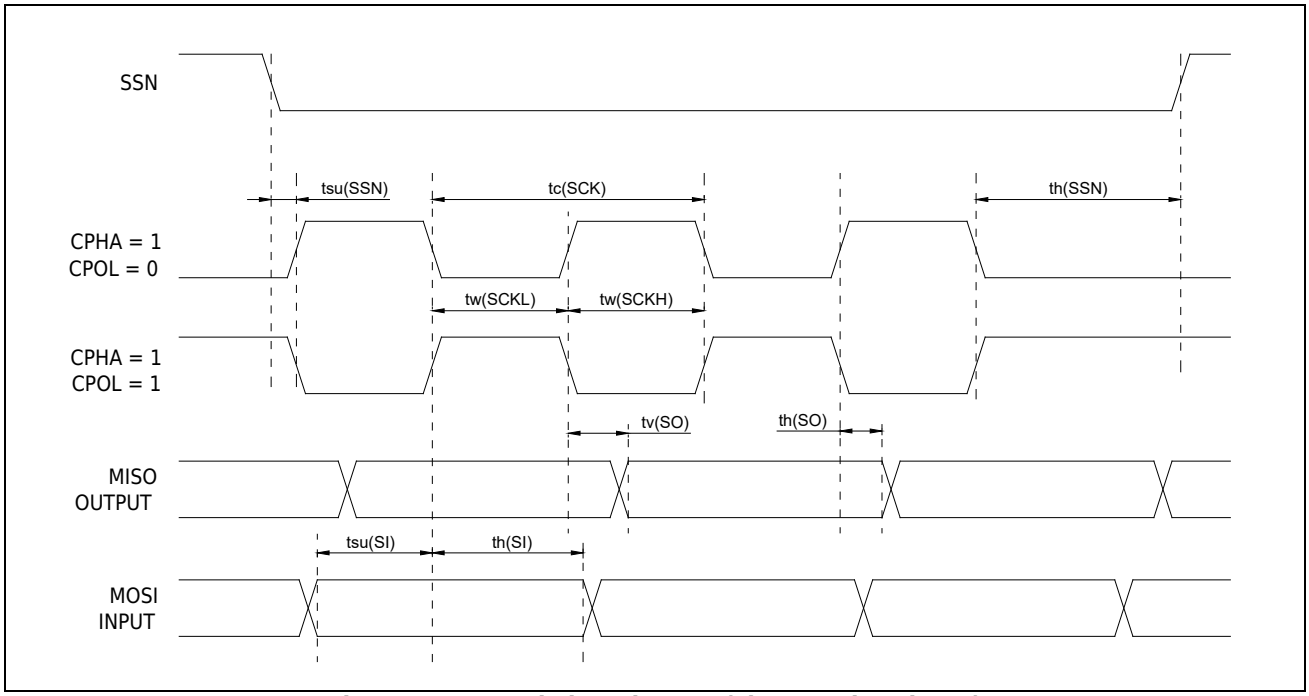
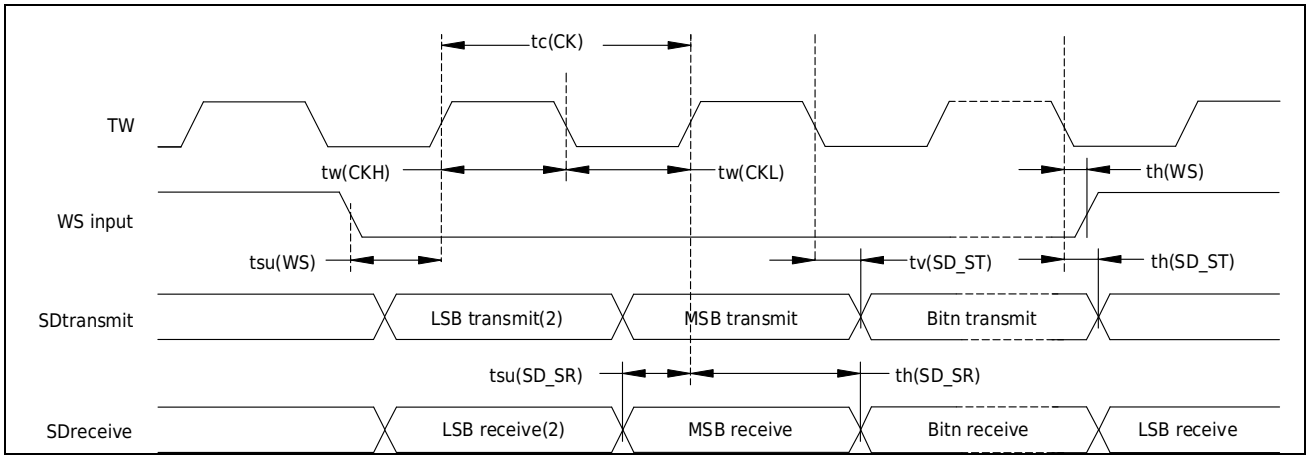


Figure 7-6 SPI Timing Diagram (slave mode cpha=1)

7.3.20.3 I2S features(1)

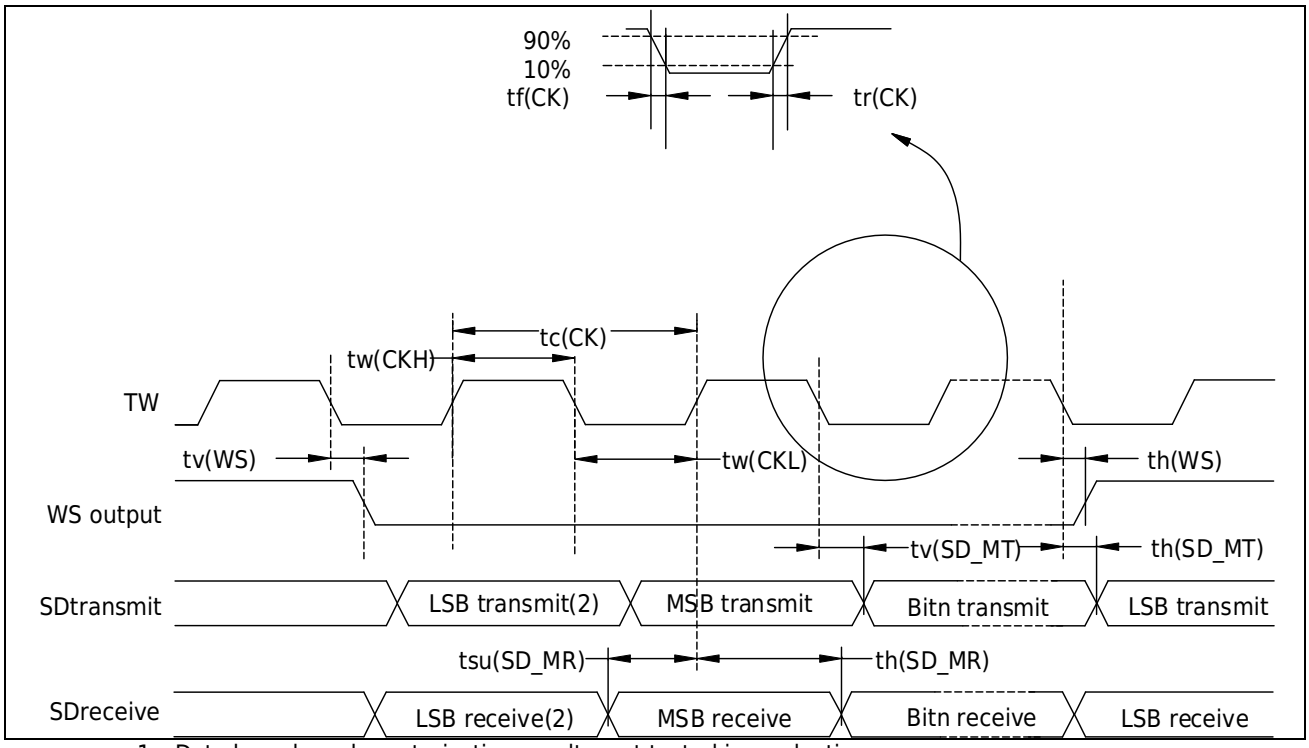
Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
f_{ck}	I2S clock frequency	Master mode (data:16bits,audio freq 48kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(ck)}$	I2S clock rise time	Capacitive load C_L=15pF	-	10	ns
$T_{f(ck)}$	I2S clock fall time		-	12	
$t_{w(ckh)}$	I2S clock high time	Master fpclk=16MHz, audio freq 48kHz	306	-	
$t_{w(ckl)}$	I2S clock low time		312	-	
$t_{v(ws)}$	WS effective time	Master mode	2	-	
$T_{h(ws)}$	WS hold time	Master mode	2	-	
$T_{su(ws)}$	WS establishment time	Slave mode	7	-	
$T_{h(ws)}$	WS hold time	Slave mode	0	-	
Duty(sck)	Slave mode clock duty cycle	Slave mode	25	75	%
$T_{su(SD\_MR)}$	SD input setup time	Master receiver	6	-	ns
$T_{su(SD\_SR)}$		Slave receiver	2	-	
$T_{h(SD\_MR)}$ (2)	SD input hold time	Master receiver	4	-	
$T_{h(SD\_SR)}$ (2)		Slave receiver	0.5	-	
$T_{v(SD\_MR)}$ (2)	SD output setup time	Master transmitter	-	4	
$T_{v(SD\_SR)}$(2)		Slave transmitter	-	20	
$T_{h(SD\_MR)}$	SD output hold time	Master transmitter	0	-	
$T_{h(SD\_SR)}$		Slave transmitter	13	-	

1. Guaranteed by design, not tested in production.
2. Related to F_{PCLK} , for example, F_{PCLK} =10M T_{PCLK} =1/F_{PCLK} =100ns.



1. Measurement points are done at CMOS levels：$0.3\times V_{DDIOx}$ and $0.7\times V_{DDIOx}$。
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 7-7　I2S slave timing diagram



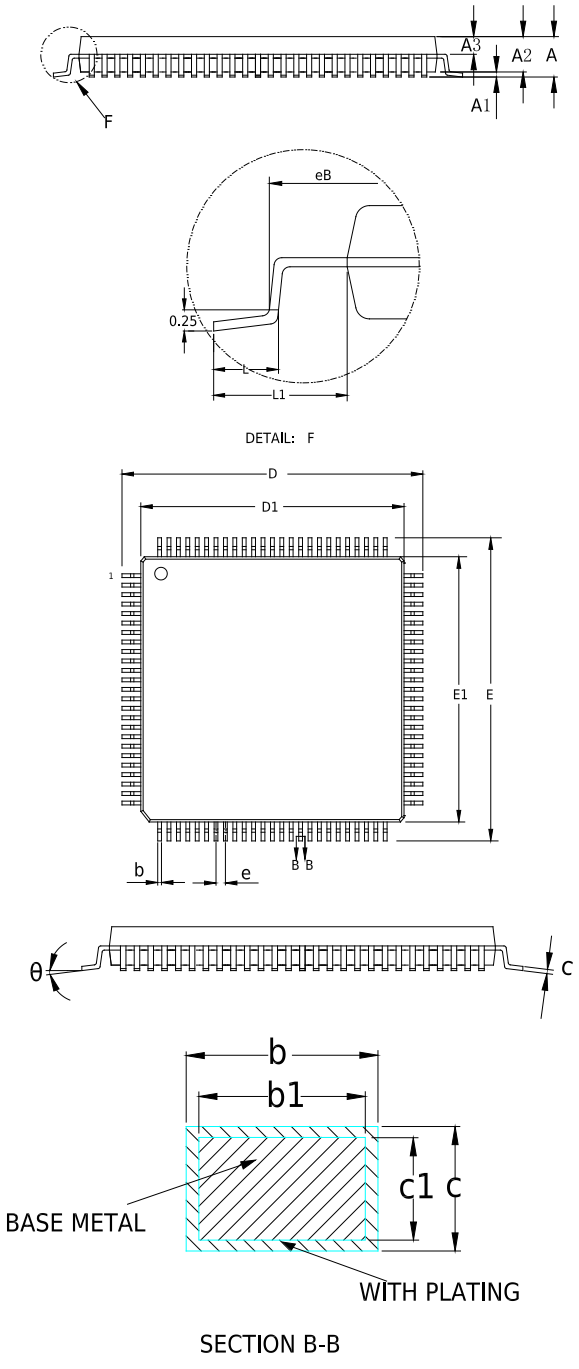
1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 7-8　I2S master timing diagram

8 Packaging Information

8.1 Packaging Size

LQFP100 packaging

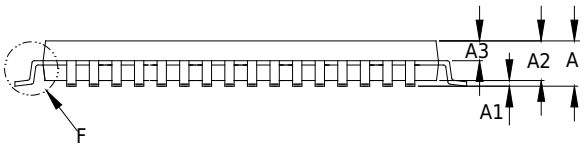


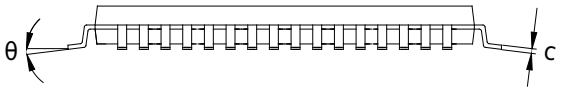
Symbol	14 x 14 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	--	15.35
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

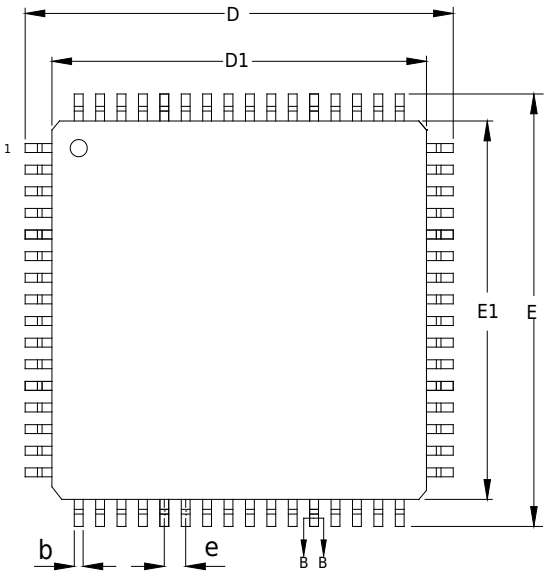
NOTE:

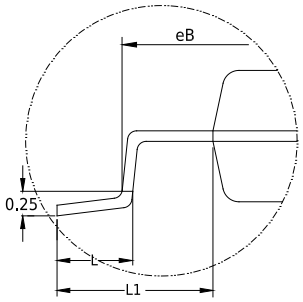
- **Dimensions "D1" and "E1" do not include mold flash.**

LQFP64 packaging

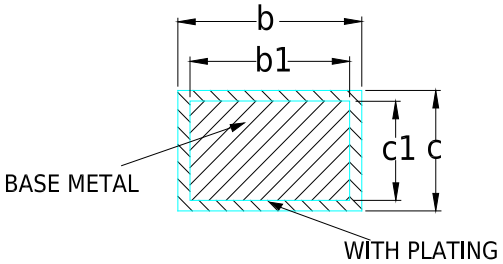








DETAIL: F



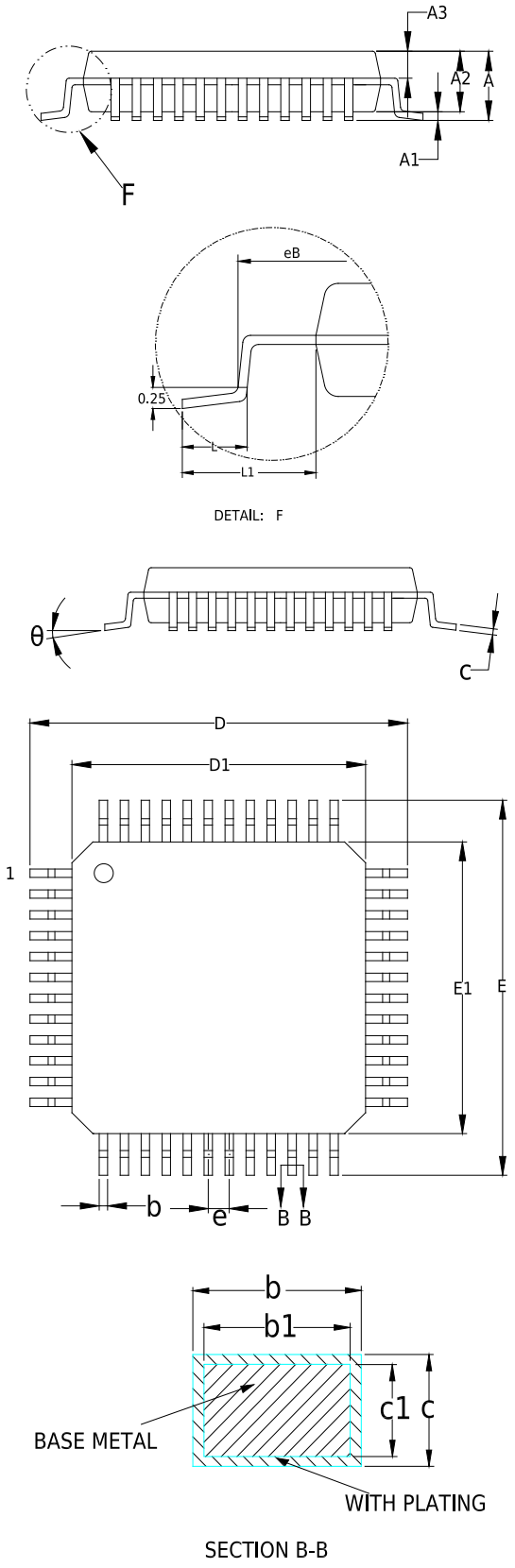
SECTION B-B

Symbol	10 x 10 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
eB	11.05	--	11.25
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0°	--	7°

NOTE:

– **Dimensions “D1” and “E1” do not include mold flash.**

LQFP48 packaging

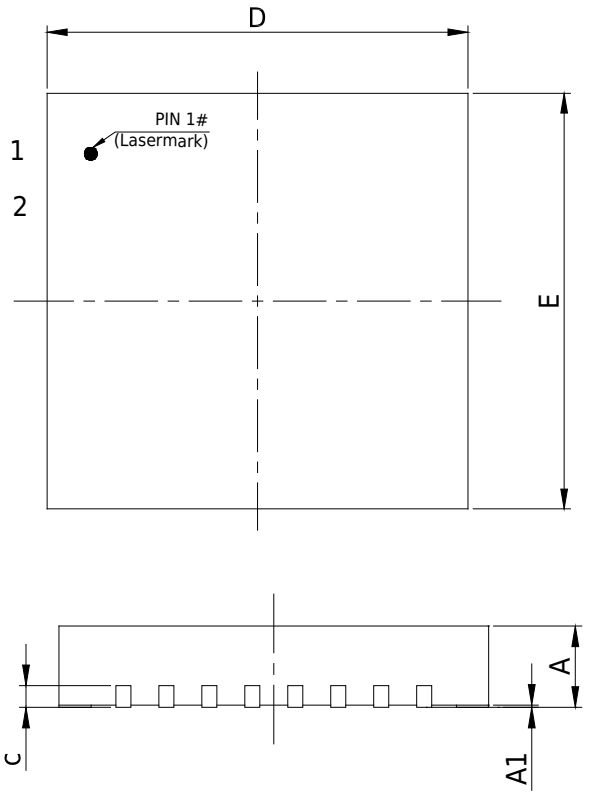


Symbol	7 x 7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	--	8.25
e	0.50BSC		
L	0.40	--	0.65
L1	1.00REF		
θ	0	--	7°

NOTE:

– **Dimensions "D1" and "E1" do not include mold flash.**

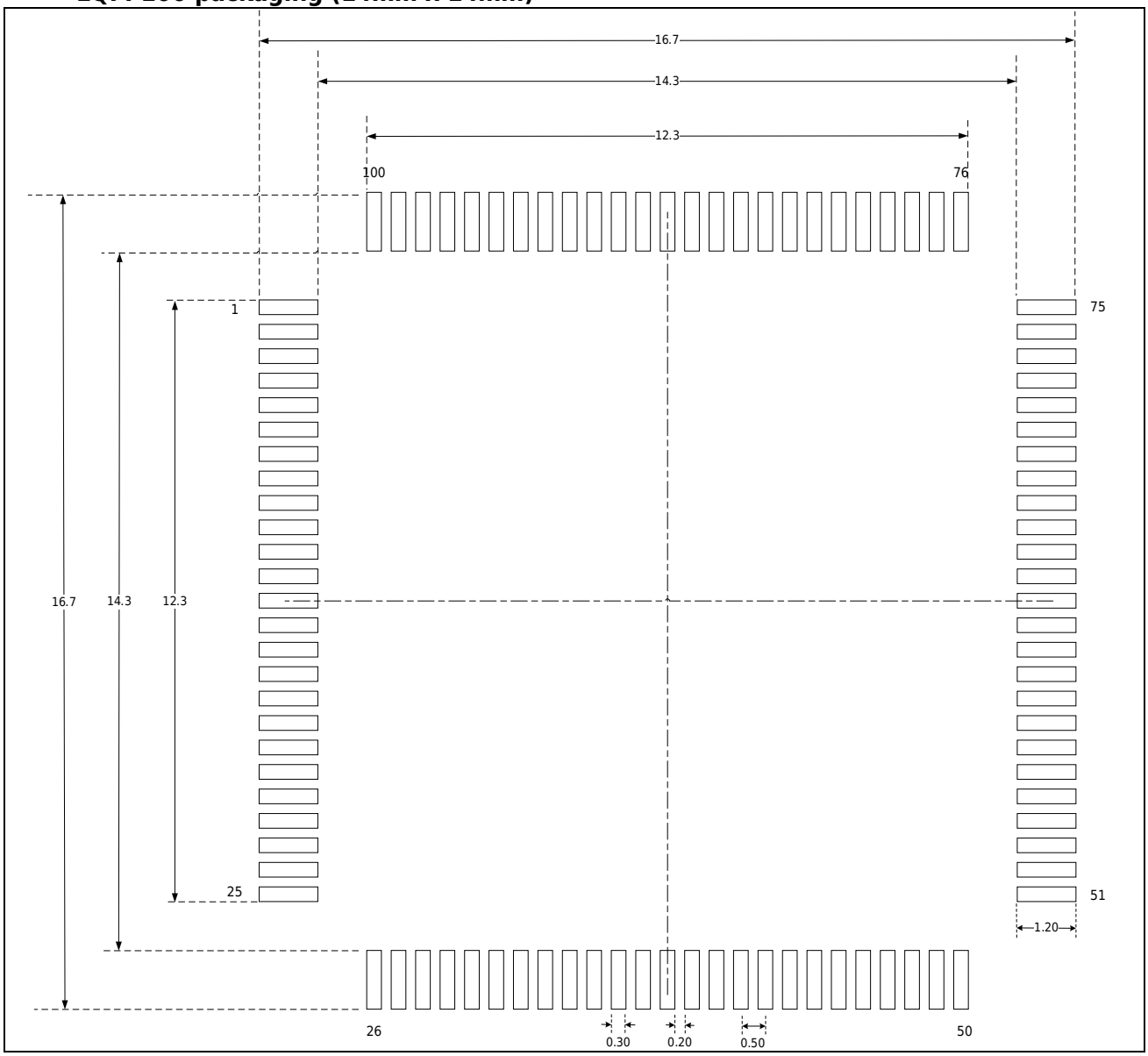
QFN32 packaging



Symbol	5 x 5 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1		0.16REF	
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.70	3.80	3.90
e		0.50BSC	
Ne		3.50BSC	
Nd		3.50BSC	
E	4.90	5.00	5.10
E2	3.70	3.80	3.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F carrier size		4.10 x 4.10	

8.2 Schematic diagram of pad

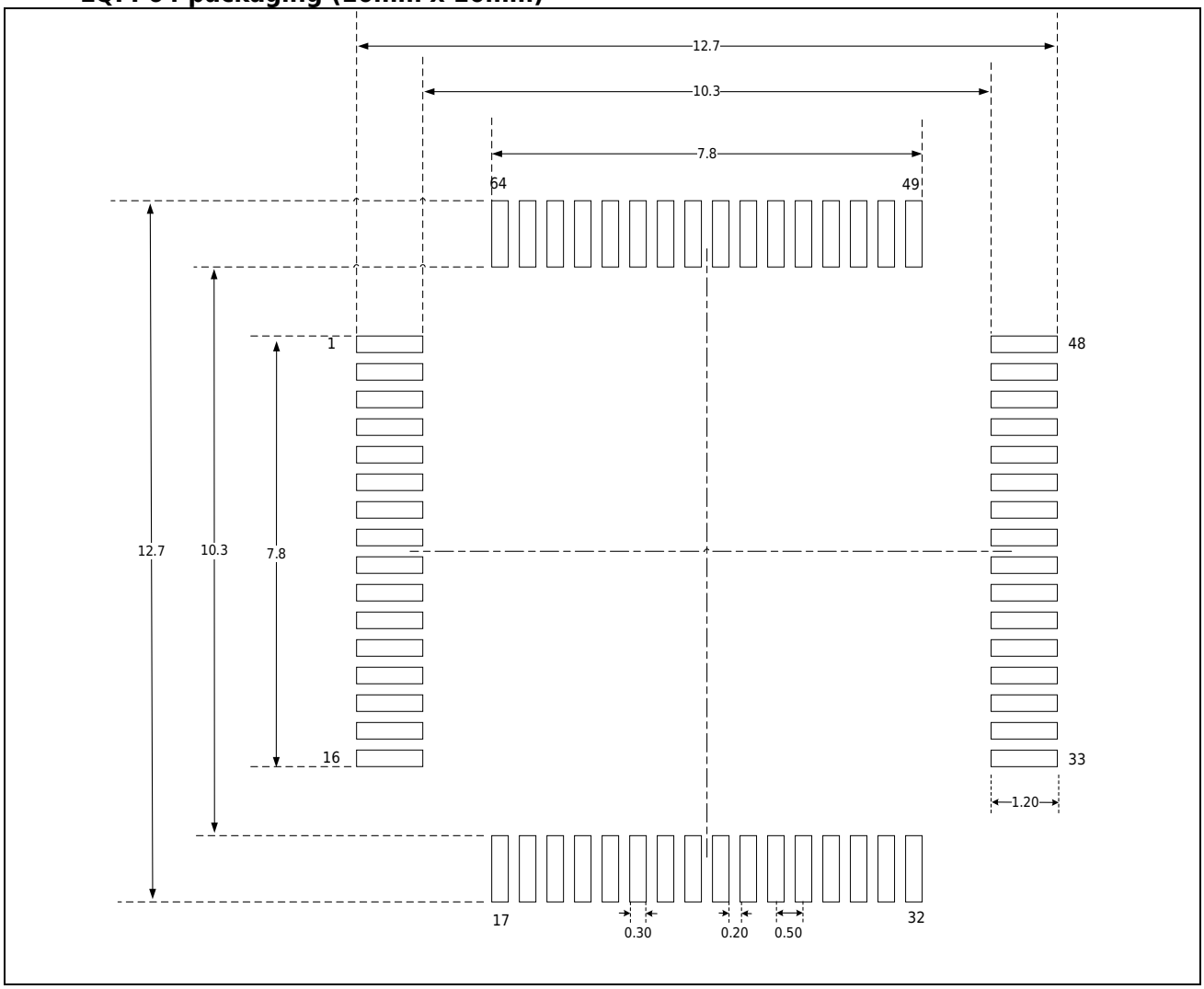
LQFP100 packaging (14mm x 14mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

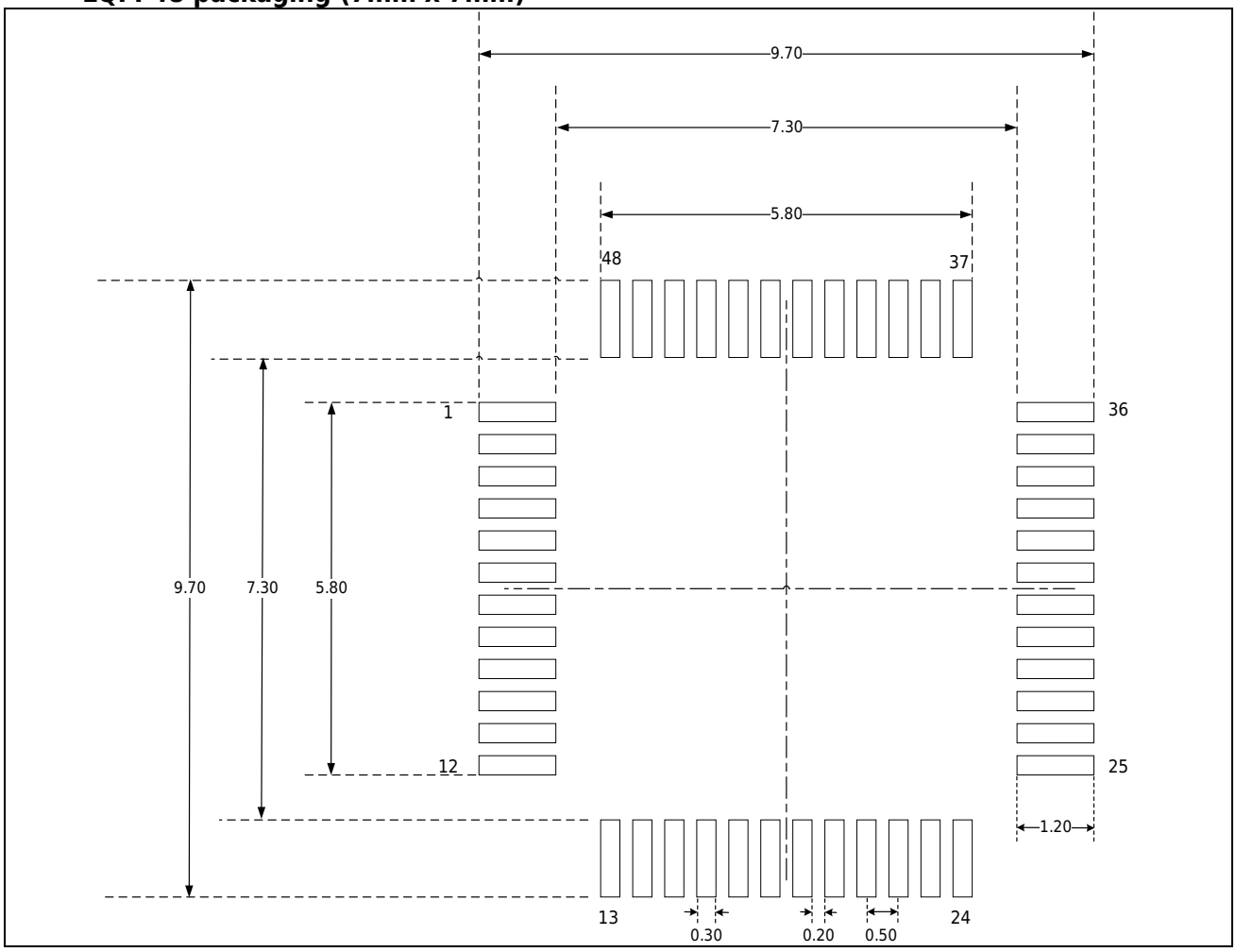
LQFP64 packaging (10mm x 10mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

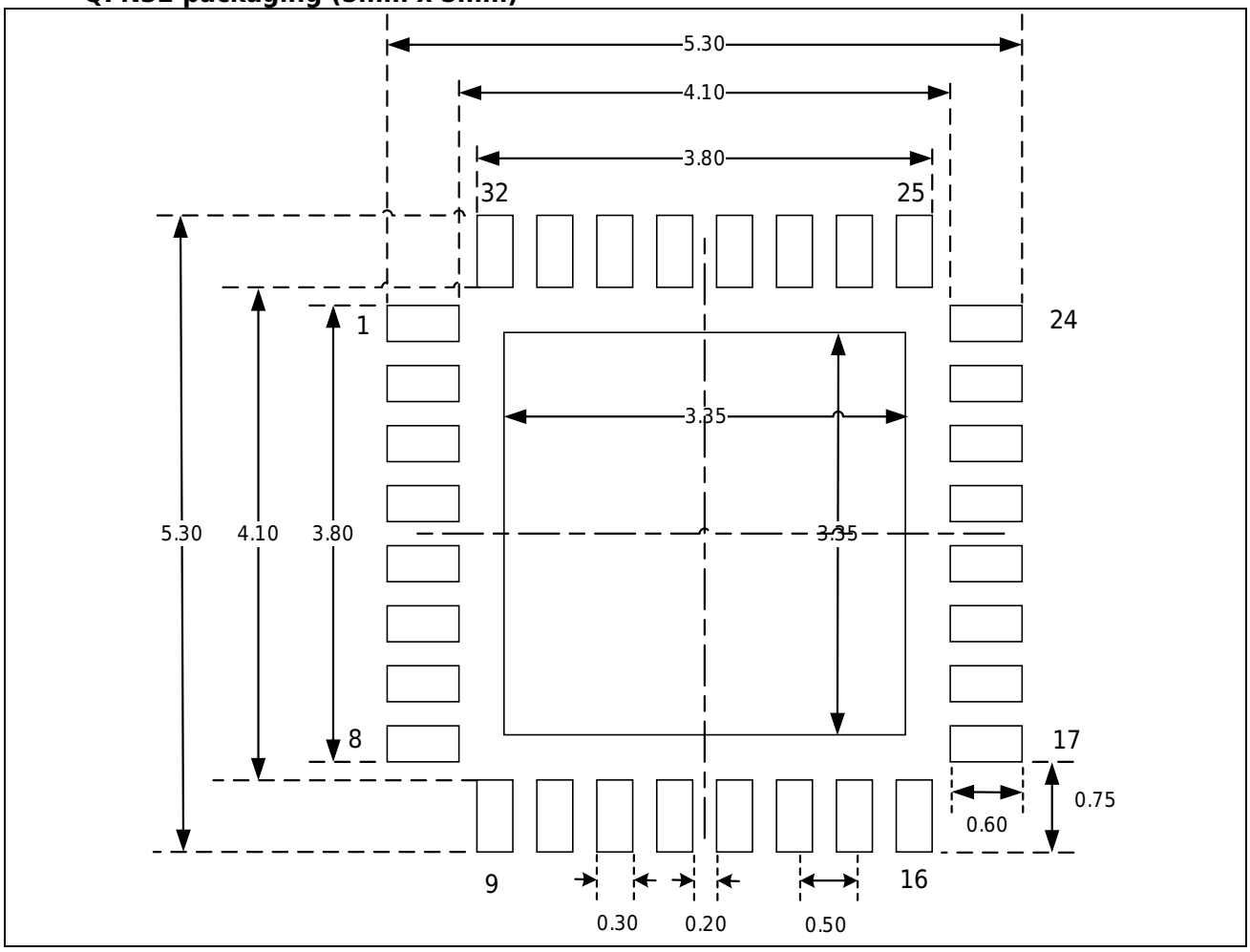
LQFP48 packaging (7mm x 7mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

QFN32 packaging (5mm x 5mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

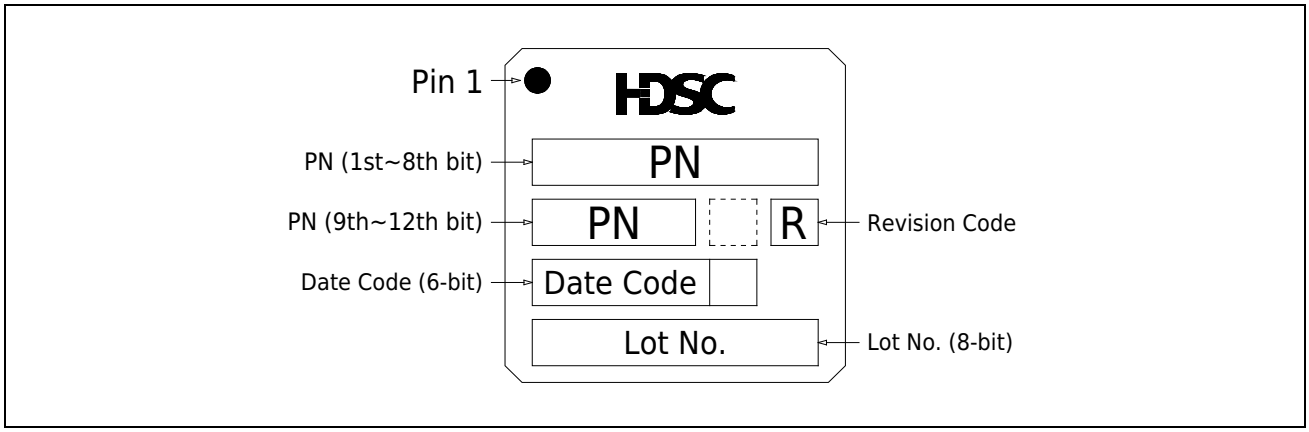
8.3 Silkscreen instructions

The position and information of Pin 1 printed on the front of each package are given below.

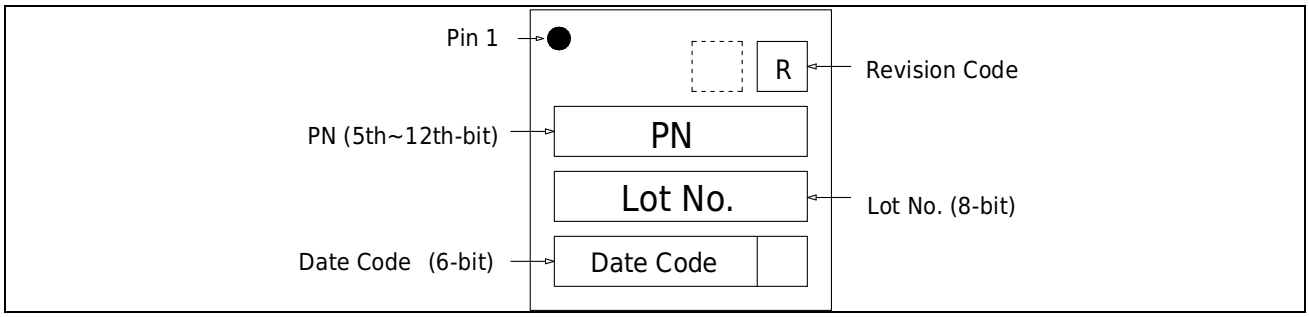
LQFP100 packaging (14mm x 14mm)

LQFP64 packaging (10mm x 10mm)

LQFP48 packaging (7mm x 7mm)



QFN32 packaging (5mm x 5mm)



Note:

– The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

8.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (℃) of the chip surface can be calculated according to the following formula:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's I_{DD} x V_{DD} . I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually this part of the value is very small and can be ignored.

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 8-1 Thermal resistance coefficient table for each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP100 14mm x 14mm / 0.5mm pitch	50 +/- 10%	℃/W
LQFP64 10mm x 10mm / 0.5mm pitch	65 +/- 10%	℃/W
LQFP48 7mm x 7mm / 0.5mm pitch	75 +/- 10%	℃/W
QFN32 5mm x 5mm / 0.5mm pitch	42 +/- 10%	℃/W

9 Ordering Information

Part Number		HC32F072PATA-LQFP100	HC32F072KATA-LQFP64	HC32F072JATA-LQ48	HC32F072FAUA-QN32TR
Memory	Flash	128K	128K	128K	128K
	RAM	16K	16K	16K	16K
I/O		86	50	36	25
TIMER	GTIMER	4	4	4	4
	ATIMER	3	3	3	3
Connectivity	UART	4	4	2	2
	LPUART	2	2	2	1
	I2C	2	2	2	1
	SPI	2	2	2	1
	USB	✓	✓	✓	✓
	CAN	✓	✓	✓	✓
	I2S	2	2	2	1
Analog	ADC*12bit	24ch	23ch	17ch	11ch
	DAC*12bit	2ch	2ch	2ch	2ch
	OP	5	5	3	1
	Comp	3	3	3	3
Secruty	AES	✓	✓	✓	✓
LVD		✓	✓	✓	✓
LVR		✓	✓	✓	✓
Votage	Vdd	1.8~5.5v	1.8~5.5v	1.8~5.5v	1.8~5.5v
Package		LQFP100(14*14)	LQFP64(10*10)	LQFP48(7*7)	QFN32(5*5)
Shipping Form		Plate	Plate	Plate	Tape
Product Thickness		1.6mm	1.6mm	1.6mm	0.75mm
Foot Spacing		0.5mm	0.5mm	0.5mm	0.5mm

Before ordering, please contact the sales window for the latest mass production information.

Version revision history

Version number	Revision Date	Modify the content
Rev1.00	2019/11/18	The first draft is released.
Rev1.10	2019/12/25	Update the following information: ①Add QFN32 package; ②Typical application circuit diagram; ③High-speed external clock XTH and low-speed external clock XTL with diagrams and precautions; ④Silk printing description; ⑤Description of general working conditions; ⑥Ordering information.
Rev1.20	2020/04/10	Update the following information: ①pin function description; ② add AVCC/3 precision in ADC features.
Rev1.30	2020/05/29	Update the following information: ① Correct typos in 7.3.7.2; ② RCL oscillator accuracy in 7.3.8.2.
Rev1.40	2020/06/30	Update the following information: ①Add I2S information in the pin function description; ②Unified pin function names.
Rev1.50	2020/07/31	Update the following information: ① Add 7.3.19, 7.3.20, 8.2 and 8.4; ②7.3.11 grade; ③ V_{IH} and V_{IL} values in 7.3.13.2.
Rev1.60	2020/09/30	Update the following information: ①Functional block diagram; ② Add SPI feature and I2S feature(1); ③1.4 description; ④ V_{IL} and V_{IH} in 7.3.14; ⑤ Add 7.3.13.3;⑥The OPA quantity of HC32F072FAUA is 1.
Rev1.70	2021/05/31	Update the following information: ① modify the statement; ② correct the ANALOG function of PB04 and port multiplexing table in the pin function description; ③ $t_{HD.STA}$ and $t_{SU.STO}$ parameters in the I2C feature; ④ data retention period in the memory feature; ⑤ increase the g_m parameter in the external clock source feature.
Rev1.80	2022/03/09	The company logo is updated.
Rev1.81	2022/08/13	Update the following information: ①3.2 Pin function description, delete the PF01 function mapping of TIM4_CHB; ②7.3.14 RESETB pin characteristics, modify the input filter pulse time.
Rev1.82	2023/06/21	Update the following information:① The address range of the storage map APB1 is incorrect.
Rev1.83	2024/06/25	Update the following information: ① The number of ADC and VC channels is modified and 1.2V related descriptions are deleted in 1.27 and 1.29, and 1.2V related descriptions are deleted in 7.3.16; ②The storage temperature range listed in Table 7-3 Temperature characteristics is changed. ③The section "7.3.8.3 Internal low speed clock 10k oscillator" is added.
Rev1.84	2024/12/12	Update the following information: ①The content of 7.3.7.3 High-speed external clock XTH and 7.3.7.4 Low-speed external clock XTL is updated.
Rev1.85	2025/03/28	Update the following information: ①Update the relevant parameters of the SPI interface features in Table 7-15; ②Modify the maximum value of the input filter pulse and the minimum value of the input non-filtered pulse in Section 7.3.14 RESETB pin characteristics.