XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

32-bit microcontrollers

How to improve ADC sampling accuracy

Application Notes

Rev1.0 November 2023

Target customers

Product range	Product Model
HC32A/F/L/M	All Models

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Table of contents

1 Overview

HC32A/F/L/M series products are MCUs launched by Xiaohua Semiconductor based on the ARM cortex core. Each MCU has 1~3 built-in

Sub-compare digital-to-analog converter (SAR ADC). Each unit can support 8~16 external pin input channels or specific internal voltage, temperature

The maximum precision is 12 bits, the maximum sampling conversion rate can reach 2.5 mbps, the internal channel is flexibly mapped, the sampling results can be read

through DMA, and it can be linked with the multi-function TIMER to achieve precise control of the sampling timing. It can meet absolute

Most consumer, home appliance and industrial products require ADC.

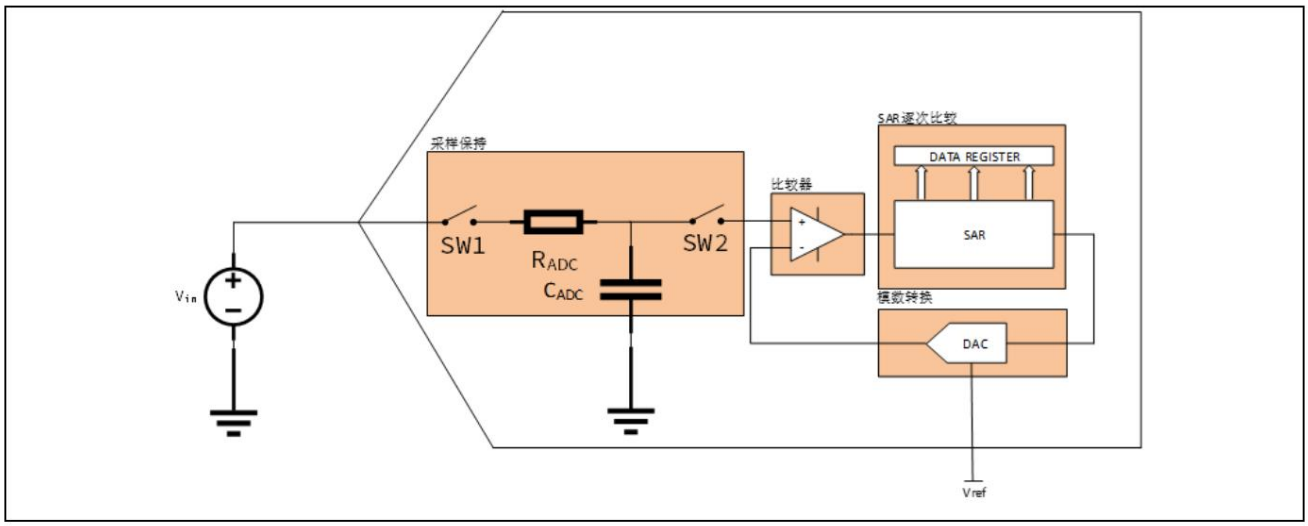
This article describes the principles and inherent errors of SAR ADC, the main factors affecting its sampling accuracy, and how to improve the sampling accuracy of ADC.

2 SAR ADC Introduction

2.1 SAR ADC Principle

Successive approximation ADC (SAR ADC), as the name implies, realizes analog signal conversion by comparing the input signal with the reference source voltage step by step.

The conversion process of SAR ADC is divided into two stages: sampling stage and conversion stage.



Sampling phase:

SW1 is closed, SW2 is open, and Vin charges the sampling capacitor CADC through the internal switch RADC. After the sampling period, the conversion phase begins.

Conversion phase:

SW1 is open, SW2 is closed, and the voltage on the sampling capacitor (ideally Vin) is equal to 1 $\frac{}{2}$ *VREF is compared, if Vin highest position $\frac{1}{2}$ * VREF, then 1, DAC inputs the next comparison value 3 $\frac{}{4}$ * VREF, Vin and 3 $\frac{}{4}$ *VREF comparison determines the value of the second highest bit. According to the comparison result Then output the DAC value, compare it, and finally get the conversion value.

2.2 SAR ADC Intrinsic Error

The SAR ADC has several inherent errors due to its principle and structure.

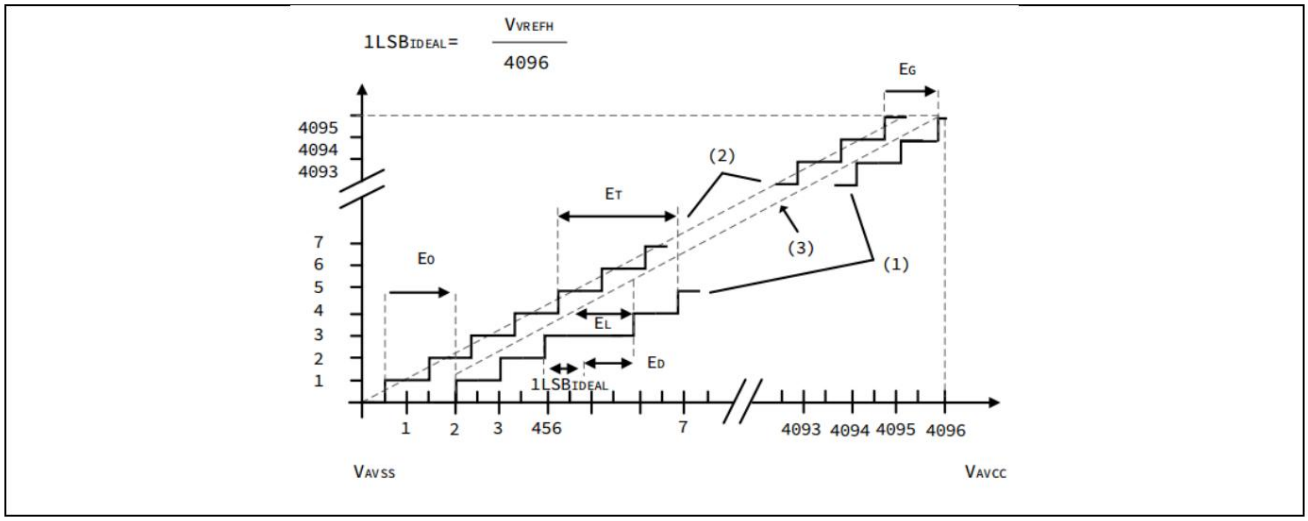


Figure 2-1 SAR ADC error

ÿ Offset error EO

The offset error refers to the difference between the actual input analog value and the theoretical input analog value when the conversion value is 1. The offset error can be positive or negative.

Can be negative.

ÿ Differential nonlinearity error ED

Differential nonlinearity error refers to the maximum difference between the actual analog value step and 1 LSB when the conversion value changes by 1.

ED = Actual Analog Change - 1 LSB

ÿ Integral nonlinearity error EL

Integral nonlinearity error refers to the maximum deviation between the actual analog quantity and the actual conversion curve.

ÿ Total unadjusted error ET

The total unadjusted error refers to the maximum error between the actual analog value and the ideal conversion curve.

ÿ Gain Error ED

Gain error refers to the error between the actual analog value and the theoretical analog value of the last conversion.

3 ADC external error sources and solutions

3.1 Reference Sources

The principle of SAR ADC is to obtain the conversion result by comparing the input signal with the reference voltage, that is:

$$CodeADC = \frac{Vin}{Vref} * 2N \quad (1)$$

From equation (1), it can be seen that Vref has a great influence on the accuracy of ADC, which is mainly manifested in the following aspects:

3.1.1 Reference source voltage range

The reference source voltage must meet the following requirements: 1. Be higher than the highest voltage of the input signal and lower than or equal to the ADC power supply voltage.

2. Try to get as close to the input signal range as possible.

ÿ The reference source voltage must be higher than the input signal voltage to accurately measure the extreme value of the input signal.

The reference voltage source causes current backflow to the ADC power supply.

ÿ The reference source voltage range is close to the input signal range to maximize theoretical accuracy. For example:

For a 12-bit ADC, the input signal range is 0~1.8V.

If the reference supply voltage is selected as 3.3 V, then 1 LSB = $\frac{3.3}{212} = \frac{3.3}{4096}$=0.81 mV. In this case, theoretically,

0.81 mV accuracy.

If the reference supply voltage is selected as 2.0 V, then 1 LSB = $\frac{2.0}{212} = \frac{2.0}{4096}$=0.49 mV. In this case, theoretically,

0.49 mV accuracy.

Optimization suggestions:

ÿ A reasonable reference source voltage range can significantly improve the theoretical sampling accuracy. The reference source is slightly larger than the maximum amplitude of the input signal.

In actual product applications, the reference source is not necessarily selected arbitrarily, and may be the power supply voltage.

The maximum amplitude of the reference source is close to the reference source range, which can also reduce the accuracy loss.

It is slightly larger than the input signal and also needs to meet the special requirements in the specification, such as the requirements of HC32F4A0 of Xiaohua Semiconductor.

conform to	name	Minimum	Typical Value	Maximum
Vref	Positive reference voltage	1.8 V	-	AVCC

0 ÿ Vref - AVCC ÿ 1.2 V

3.1.2 Reference source accuracy

It is not difficult to understand from equation (1) that the conversion value of ADC is the relative value of the input signal and the reference source. The reference source must have high accuracy to ensure that ADC

The accuracy of the reference source is affected by factors including temperature coefficient, linear regulation rate, load regulation rate, etc.

Need to pay attention, especially in high precision occasions.

If the 12-bit ADC input signal is 2.5 V and the reference voltage is 3.3 V, the converted value is:

$$\frac{2.5}{3.3} * 212 = 0xC1F$$

If the reference source accuracy is 1%, assuming 3.3*0.99 = 3.267 V, the converted value is:

$$\frac{2.5}{3.267} * 212 = 0xC3E$$

Codeÿ=0xC3E-0xC1F=31 LSB

Therefore, 1% accuracy is far from meeting the 1 LSB accuracy requirement and needs to be improved.

Optimization suggestions:

ÿ In high-precision applications, a high-precision voltage reference IC is often required to provide a reference source for the ADC.

3.1.3 Reference source noise

During the ADC conversion process, the switching and charging process of the ADC internal capacitors will cause input spike currents, which will cause the reference

The source voltage has a spike, which affects the sampling accuracy of the ADC. Especially when the input signal is large, the reference source noise has a more obvious impact.

It is critical to reduce the noise of the reference source voltage.

Optimization suggestions:

ÿ On the one hand, a low noise LDO or voltage reference can be selected as the ADC reference source.

ÿ On the other hand, Xiaohua Semiconductor also recommends that customers configure low-ESR ceramic capacitors near the chip reference source for noise suppression.

At the same time, it provides nearby energy storage for the reference source. Taking HC32F4A0 as an example, its data sheet requires the following configuration:

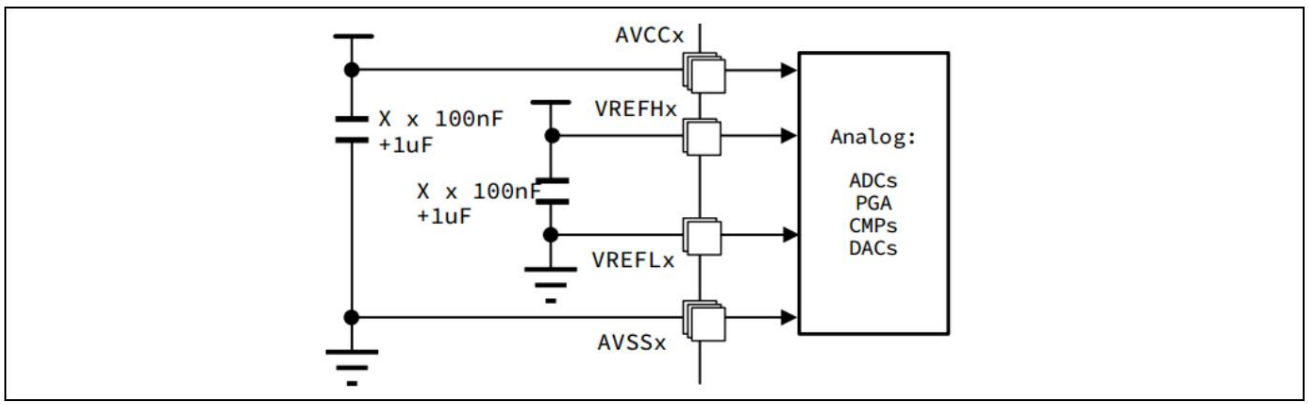


Figure 3-1 HC32F4A0 ADC reference source capacitance

ÿ When designing the PCB layout, ensure that the reference power supply loop is as small as possible and separate from the digital ground. Use single-point grounding and use the same grounding as the analog power supply.

The same ground plane. Energy storage and decoupling capacitors should be as close to the power pins as possible.

3.2 Power Supply Noise

We have discussed the influence of reference source noise on ADC accuracy. In fact, a “clean” ADC power supply is also crucial to ADC accuracy.

Power supply noise may affect the internal circuit of the ADC, and may also be transmitted to the reference source or input signal, resulting in sampling errors.

DC-DC power supply: DC-DC power supply transfers energy in the form of switches. There are high-frequency switching signals in its topology, accompanied by inductance, input

The switching signal may induce a spike pulse at the power output or ground plane, and the charging and discharging process of the inductor and output capacitor will

This causes the output voltage to have obvious ripples, which can be regarded as noise from the power supply.

Linear LDO: Linear LDO is based on linear loop control, has no switching signal, does not generate spike pulses, and has a small ripple.

Power supply rejection ratio (PSRR) and low noise LDO is an ideal analog power supply solution.

Optimization suggestions:

ÿ For the power supply for analog modules, it is best to use an LDO with high PSRR and low noise, and avoid using a switching power supply directly.

This introduces larger spike pulses and ripples into the power.

ÿ Similarly, Xiaohua Semiconductor MCU also requires low ESR ceramic capacitors to be configured near the analog power pins for decoupling and energy storage.

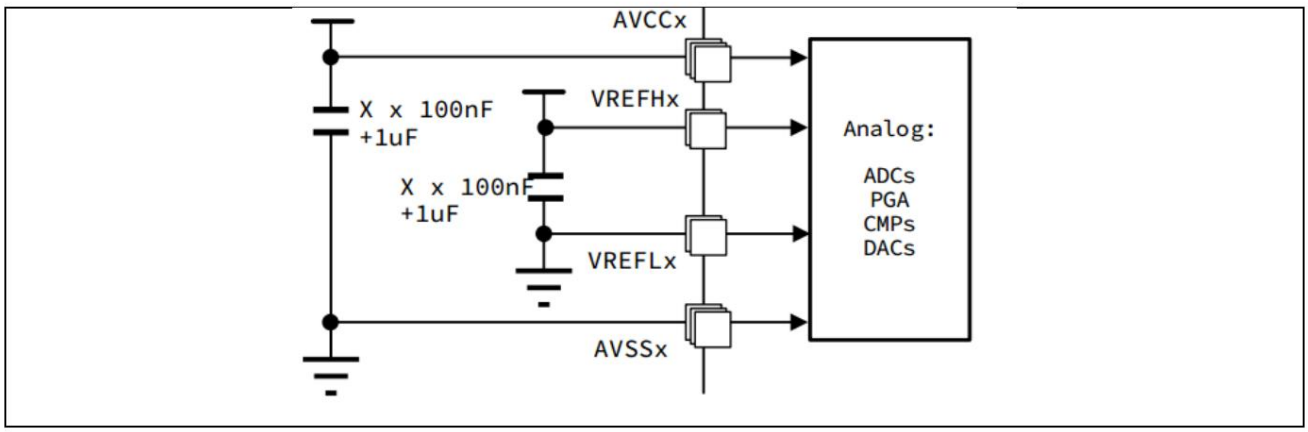


Figure 3-2 HC32F4A0 analog power capacitor

ÿ When designing PCB layout, ensure that the analog power loop is as small as possible and separate it from the digital ground, using single-point grounding.

quantity close to the power supply pins.

3.3 ADC Input Impedance and Sampling Time

In the ADC section of Xiaohua Semiconductor's MCU specification, the important parameters of the ADC model are generally listed, as shown in the following table:

表 3-51 ADC 特性

符号	参数	条件	最小值	典型值	最大值	单位
V_{AVCC}	电源	–	1.8	–	3.6	V
V_{REFH}(1)	正参考电压	–	1.8	–	V_{AVCC}	V
f_{ADC}	ADC 转换时钟频率	高速工作模式下 V_{AVCC}=2.4 ~3.6V	1	–	60	MHz
		低速工作模式下 V_{AVCC}=1.8 ~2.4V	1	–	30	
		超低速工作模式	1	–	8	
V_{AIN}	转换电压范围	–	V_{REFL}	–	V_{REFH}	V
R_{AIN}	外部输入阻抗	详见公式1	–	–	50	kΩ
R_{ADC}	采样开关电阻	–	–	3	6	kΩ
C_{ADC}	内部采样和保持电容	–	–	4	7	Pf
t_D	触发器转换延迟	f_{ADC} = 60 MHz	–	–	0.3	μs

The ADC sampling switch resistance RADC and the ADC internal sampling and holding capacitance CADC are indicated .

Maximum external input impedance. The formula mentioned here is:

$$RAIN\ddot{y} \frac{t}{CADC^* \ln 2N+1} - RADC$$

in:

t : sampling period

N : ADC bits

The sampling circuit of SAR ADC can be simplified as shown below:

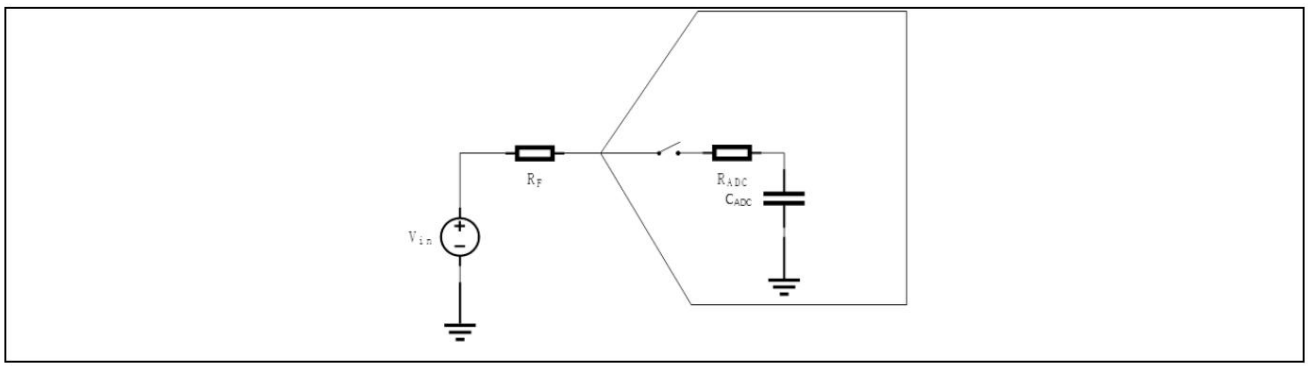


Figure 3-3 SAR ADC block diagram

When the internal channel of the ADC switches to an external pin, the signal voltage on the pin will charge Cs through RAIN and RADC.

The time constant is:

$$\ddot{y} = (RF+RADC)*CADC$$

Assuming the initial voltage of Cs is Vt0, the unit step response of the system is:

$$Vt=Vt0+(Vin-Vt0)*(1-e-ÿ)\ \frac{t}{}$$

After a fixed time (i.e., sampling time t), the voltage difference between the voltage across the CADC capacitor and the signal source is:

$$Verr= (Vin-Vt0)*e-\ \frac{t}{ÿ} \qquad (2)$$

When Vt0=0, that is, when the initial state is zero, the error is the largest. The larger Vin is, the larger the error is, and it is the largest when it is equal to VREF.

The charging curve is as follows:

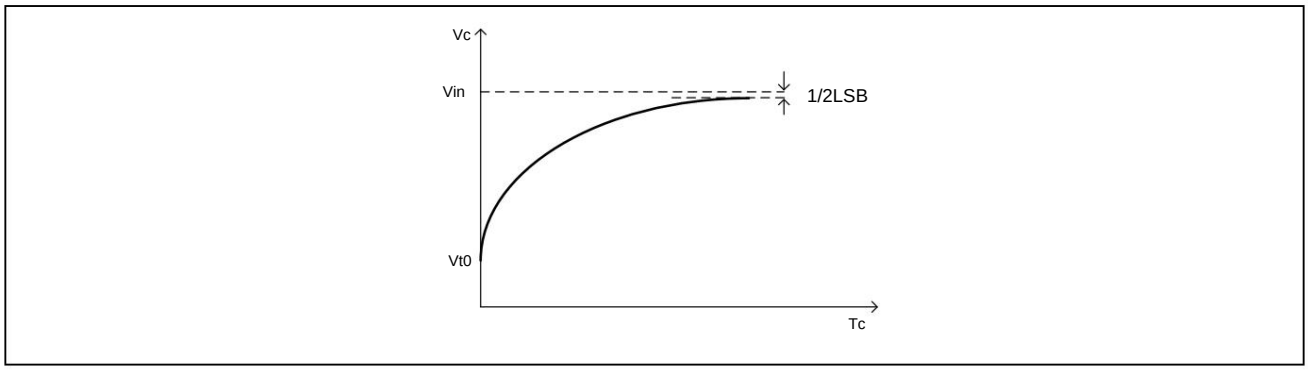


Figure 3-4 RC unit step response

If the sampling accuracy is required to reach 1/2 LSB, the error needs to meet the following requirements:

$$Vin*e-\ \frac{t}{(RF+RADC)*CADCÿ}\ \frac{1}{2} * \frac{Vref}{2N}$$

Simplifying, we can get:

$$RFÿ\ \frac{t}{CADC* \ln 2N+1}\text{-}RADC \qquad (3)$$

or

$$tÿ(RF + RADC) *CADC* \ln 2N+1 \qquad (4)$$

Therefore, to obtain a higher sampling rate, it is necessary to reduce the external input impedance. If the external impedance is large, it is necessary to consider increasing the drive

The dynamic stage performs impedance conversion or increases the sampling time.

In actual applications, the ADC input pin may be connected to an external RC filter circuit, as shown in Figure 3-5.

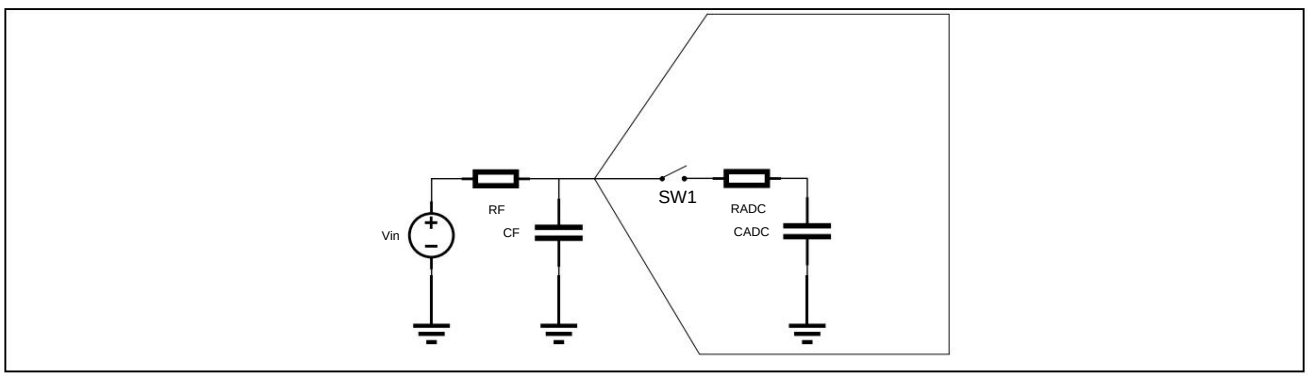


Figure 3-5 ADC external RC filter circuit diagram

In this case, charging is divided into 2 stages, and the process is shown in the figure below.

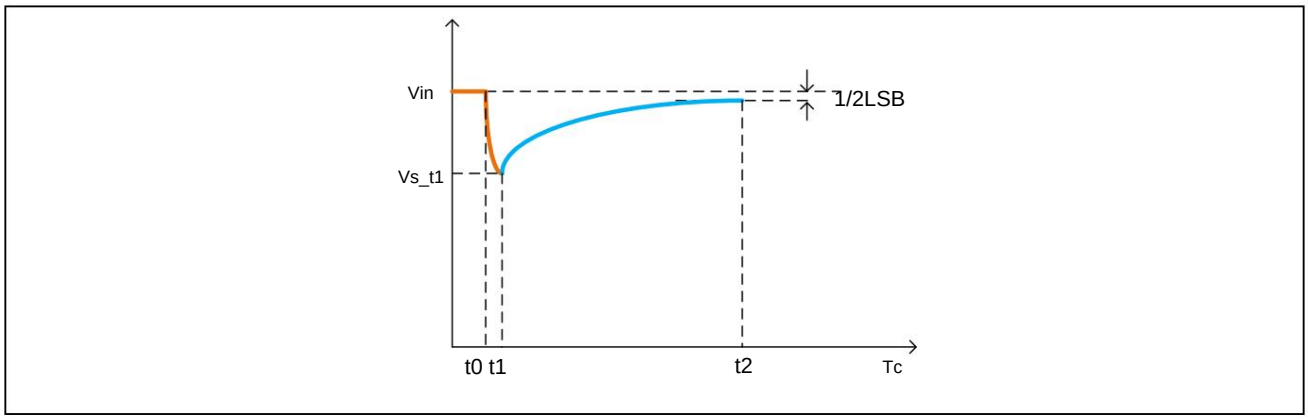


Figure 3-6 Capacitor balancing and charging process

Assume that the voltage across CF has reached the input signal amplitude Vin before the ADC channel switches to the external pin. After the internal switch is closed, CF and CADC

The charges are balanced and eventually the voltage is balanced.

The balanced voltage is:

$$Vs\_t1= \frac{Vin*CF}{CF+CADC} \quad (5)$$

At this balanced voltage, the input signal charges CF and CADC through RAIN + RADC , and the starting point of charging is the balanced voltage.

The time constant is:

$$ÿ= (RF+RADC)*(CF+CADC)$$

Substituting equation (5) into equation (2) yields:

$$Verr=ÿ \quad \frac{Vin*CADC}{CF+CADC}ÿ *(1-e- \frac{t}{ÿ})$$

If you want to achieve 1/2LSB accuracy, you must:

$$ÿ\frac{Vin*CADC}{CF+CADC}* ÿ1-e- \frac{t}{ÿRF+RADCÿ*(CF+CADC)} ÿ ÿ \frac{1}{2} * \frac{Vref}{2N}$$

After simplification, we can get

$$RFÿ \frac{t}{(CF+CADC)* \ln 2^{\frac{CADC}{CF+CADC}}} ^{N+1} -RADC \quad (6)$$

When CF = 0 , equation (6) is consistent with equation (3).

The values of RF and CF here also need to consider their bandwidth. Usually, in order to ensure that the input signal is not distorted after passing through the filter, it is necessary to meet

The following conditions:

$$ÿAIN ÿ 10* ÿFILT$$

Right now:

$$fFILT ÿ 10* fAIN \quad (7)$$

The 3dB bandwidth of the RC filter circuit is:

$$f3db = \frac{1}{2\ddot{y}} fFILT \quad (8)$$

In addition, in actual systems, the initial voltage of Cs is often the voltage of the previous channel, so if the input voltages of two consecutively sampled channels are

If the difference is large, the first channel may affect the sampling accuracy of the second channel.

Optimization suggestions:

ÿ Ensure sufficient sampling time.

ÿ Reduce the external input impedance. For high impedance input sources, it is necessary to increase the drive stage.

ÿ Add RC filtering to suppress input signal noise, and consider the RC bandwidth.

ÿ Avoid arranging two signals with large pressure difference to adjacent sampling channels as much as possible.

3.4 Input Signal

According to equation (1), it is not difficult to find that in addition to the reference source, another factor directly related to the conversion result is the input signal itself.

When the input signal is small, the input signal noise has a significant impact.

For DC input signals, you need to pay attention to whether the signal has spikes or ripples. You also need to pay attention to the output impedance of the signal source.

If the impedance is too large, resulting in insufficient output current capability, the sampling capacitor cannot be fully charged during the sampling period during high-speed sampling.

For AC signals, we also need to pay attention to whether the signal has spike pulses or ripples. If an amplifier or RC filter circuit is used at the front end of the ADC.

The bandwidth of the amplifier and the bandwidth of the RC are required to ensure that the input signal is not distorted.

Optimization suggestions:

ÿ Reduce the signal source impedance to provide sufficient charging current.

ÿ Add a suitable RC filter to reduce the input signal noise. The RC bandwidth can be roughly estimated according to equations (7) and (8), or

The exact calculation can be performed according to the following formula:

$$\ddot{y}FILT\_MAX = \frac{t}{\ln\left(\frac{2N+1*2\ddot{y}fAIN*Vpeak*tCONV*CADC}{VREF*(CF+CADC)}\right)}$$

The 3 dB bandwidth of the RC filter circuit is:

$$f3dB = \frac{1}{2\ddot{y}*\ddot{y}FILT\_MAX}$$

ÿ Add an amplifier for impedance conversion.

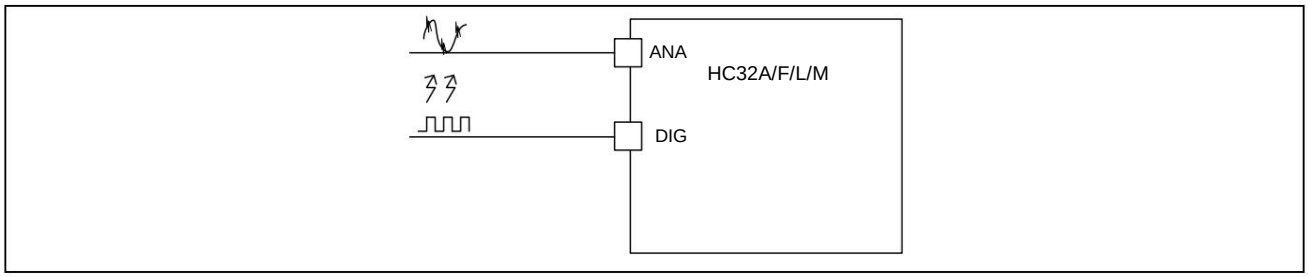
ÿ Trigger ADC sampling with accurate timing to avoid noise points of input signals.

3.5 IO Crosstalk

IO crosstalk may come from interference from adjacent lines on the circuit board, or from coupling inside the MCU port.

There are continuous high-speed square wave signals (communication signals, PWM signals, etc.) in close proximity to the wiring. This square wave signal will be coupled to the

The ADC circuit nearby will generate spikes, affecting the ADC sampling accuracy.

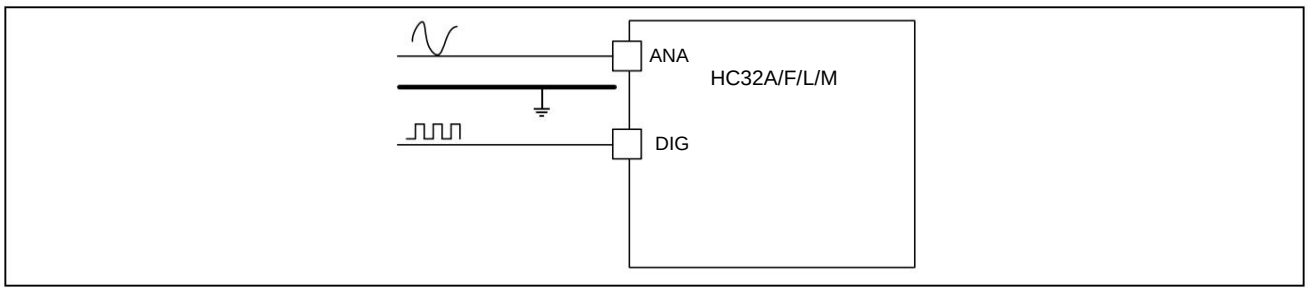


Optimization suggestions:

ÿ When arranging pin functions, try to avoid placing PWM, high-speed communication ports adjacent to ADC pins.

ÿ PCB layout, ADC input signal line is far away from PWM or high-speed communication line. ÿ Use ground wire to

isolate ADC input signal line from PWM or high-speed communication line.



3.6 Improving accuracy through software

Improving ADC sampling accuracy by optimizing power supply noise and external circuits is a fundamental method. However, in practical applications, the system electrical

The environment is very complex, hardware improvement will also increase the cost to a certain extent, and the inherent error and white noise of ADC cannot be eliminated by hardware.

Therefore, improving sampling accuracy through software is also an important means.

Optimization suggestions:

ÿ Software filtering: You can use appropriate software filtering methods based on noise characteristics, real-time performance, software overhead, etc., such as averaging

There are many filtering methods, such as value filtering, median filtering, first-order filtering, IIR filtering, etc.

ÿ Oversampling: Oversampling can effectively improve the SNR of ADC and increase the effective bits of ADC data. Applicable to real-time requirements

It is not high and the MCU storage resources are relatively abundant.

4 Conclusion

Successive approximation ADC (SAR ADC) has the advantages of fast speed, high accuracy and low cost, and is widely used in various MCUs.

The note briefly describes the working principle and inherent error of SAR ADC. It focuses on the factors that have a great impact on ADC sampling accuracy.

And how to optimize the design in practical applications. For example: reduce system noise, control input impedance, extend sampling time, etc.

In some applications, it is also common to properly use other peripherals to trigger ADC sampling to avoid noise.

In short, ADC, as the last link in the signal chain, is crucial to the stability, accuracy, and real-time performance of control.

Besides the relationship between the power supply and external circuit design, the ADC also needs to be matched.

At the same time, we also provide customers with strong technical support to reduce the burden on R&D personnel and shorten the time to market for products.

Version Revision History

Version Number	Revision Date	Revision Content
Rev1.0	2023/11/08	Initial version released.