Design of Three Stage CMOS Operational Amplifier in 180nm Technology

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***Abstract*—In this paper a CMOS based 3-stage operational amplifier is presented which operates at 1.8v power supply and at 180nm technology node. This op-amp provides a gain of 120db and a unity gain bandwidth of 110MZ for a load of 500fF.This op-amp had a CMRR 130db and output slew rate of 200 V/us and a output voltage swing 1.4v. The power consumption of oppamp is 300uW.**

***Index Terms*—Phase margin, Gain Bandwidth Product, CMRR, ICMR.**

I. Introduction

Operational Amplifier is one of the most useful parts in analogue and mixed-signal systems. It is widely used in high speed ADC/DACs, sampled data analogue filters, voltage references, instrumentation amplifiers, and many other applications. However, continued scaling in CMOS technology has caused many problems in OPAMP design. Scaling down of CMOS features enable yet faster speeds. However, it reduces the device reliability . As the minimum feature size of CMOS integrated circuits has been scaled down to nano-meter regime in recent years, the power supply voltage continues to scale down. However, the threshold voltage is not scaled down proportionally to the supply voltage due to the sub threshold leakage problem. Therefore, the design of analog circuits is becoming more difficult and challenging. The operational amplifier,which is an important analog building block, is a good example to demonstrate the challenges in design of analog circuit with the nano-meter CMOS process .

The trend towards low voltage low power silicon chip systems has been growing due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments including telecommunications, medical, computers and consumer electronics. The operational amplifier is undoubtedly one of the most useful devices in analog electronic circuitry. Op-amps are built with different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Operational Amplifiers, more commonly known as Op-amps, are among the most widely used building blocks in Analog Electronic Circuits.

Since, the conventional cascode structure of the high-gain OP amp requires multiple stacks of transistors between power supply and ground; it is difficult to design in low-voltage environment. As the solution to the design limits of cascode structure in low-voltage environment, the multistage amplifiers (cascade structure), which achieve the high gain by cascading multiple gain stages, have been researched. The multistage amplifier is more suitable to low-voltage applications, because the required number of stacks is less than cascode structure. However, since the multistage amplifier consists of multiple gain stages, it requires a complex frequency compensation scheme to ensure stability.

There are two representative frequency compensation techniques: Nested Miller Compensation (NMC) and Nested Gm-C Compensation (NGCC). In this paper we are using Nested Miller Compensation (NMC) with 3 stages.

II. analysis of 2-stage Nested Miller Frequency Compensation

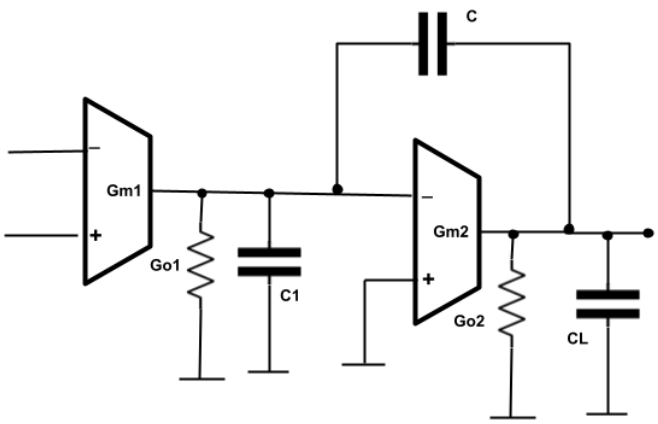


Fig. 1. 2-stage Miller Compensation oppamp

From Fig. 1 We can see that the 2 stage oppamp where we connected a miller capacitor for frequency compensation (..ie.,controlling thw two poles using the capacitor C). Here the oppamp has two differential inputs and one output stage. To analyze the poles and zeros for stability, below is the detailed transfer function of the 2 stage oppamp.

$$\frac{Vo}{Vin} = \frac{Gm1(Gm2 - SC)}{aS^2 + bS + c}$$

$$a = C1C + CCL + CLC1$$

$$b = C(Gm2 + Go1 + Go2) + C1Go2 + CLGo1$$

$$c = Go1Go2$$

By analysing the transfer function we can see that there are two poles P1 & P2 and a Zers Z. The poles and zeros of the system are:

$$P1 = \frac{-Go1Go2}{C(Gm2 + Go1 + Go2) + C1Go2 + CLGo1}$$

$$P2 = \frac{-(C(Gm2 + Go1 + Go2) + C1Go2 + CLGo1}{CC1 + C1CL + CLC)}$$

$$Z = \frac{Gm2}{C}$$

We can see the influence of the capacitor C on both poles, To analysis more simply we can approximate both the poles to following expressions,

$$P1 \approx \frac{-Go1}{C(\frac{Gm2}{Go2} + 1) + C1}$$

While for pole 2 we are assuming C $\gg C1$

$$P2 \approx \frac{-Gm2}{CL}$$

The gain bandwidth product of the oppamp,

$$GMW \approx \frac{Gm1}{C}$$

There the phase margin (PM) of the amplifier is ,

$$180 - (tan^{-1}(\frac{GMW}{P1}) + tan^{-1}(\frac{GMW}{P2}) + tan^{-1}(\frac{GMW}{Z}))$$

by making,.

$$tan^{-1}(\frac{GMW}{P1}) \approx 90$$

$$tan^{-1}(\frac{GMW}{Z}) \approx tan^{-1}(\frac{Gm1}{Gm2})$$

$$tan^{-1}(\frac{GMW}{P2}) \approx tan^{-1}(\frac{Gm1CL}{Gm2C})$$

The final phase margin(PM) we get as,.

$$PM = 90 - (tan^{-1}(\frac{Gm1}{Gm2}) + tan^{-1}(\frac{Gm1CL}{Gm2C})$$

III. Analysis of 3-stage Nested Miller Frequency Compensation

Fig. 2 represents 3 stage oppamp, by seeing it we can clearly say that it is simply cascading a differential amplifier with a 2 stage Miller Compensation Amplifier, By considering like that we can simply analyze the 3-stage with the help of the analysis from the 2-stage. Here our assumption is the 2 stage oppamp is a stable oppamp.

Using the above three stage anlysis, we can easily detect three poles and 2 zeros from the three stage oppamp, But there two dominant poles P1 & P2 and a Zero Z

$$P1 \approx \frac{-Go1}{Cc1(\frac{Gm2Gm3}{Go2Go3} + 1) + C1}$$

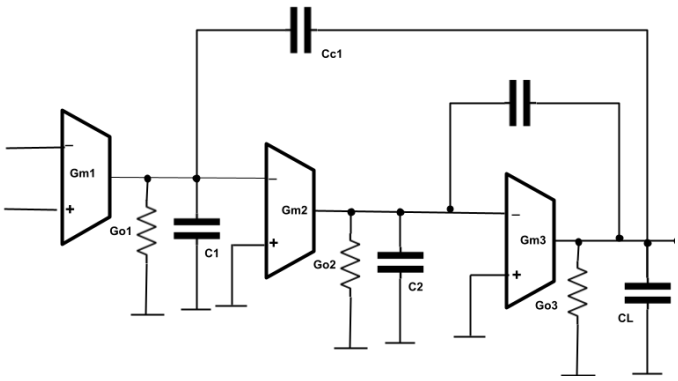


Fig. 2. 3-stage Miller Compensation oppamp

$$P2 \approx \frac{-Gm3}{CL}$$

$$Z = \frac{Gm2Gm3}{Cc1}$$

The gain bandwidth product of the 3-stage is same as 2-satge oppamp,

$$GMW \approx \frac{Gm1}{Cc1}$$

There the phase margin (PM) of the 3-stage amplifier is ,

$$180 - (tan^{-1}(\frac{GMW}{P1}) + tan^{-1}(\frac{GMW}{P2}) + tan^{-1}(\frac{GMW}{Z}))$$

by making,.

$$tan^{-1}(\frac{GMW}{P1}) \approx 90$$

Where Gm1 $\ll Gm2Gm3$

$$tan^{-1}(\frac{GMW}{Z}) = tan^{-1}(\frac{Gm1}{Gm2Gm3}) \approx 0$$

$$tan^{-1}(\frac{GMW}{P2}) \approx tan^{-1}(\frac{Gm1CL}{Gm2C})$$

The final phase margin(PM) we get for 3-stage oppamp as,.

$$PM = 90 - (tan^{-1}(\frac{Gm1CL}{Gm3Cc1})$$

Also, the 3-stage amplifier should meet the unity gain bandwidth condition,.

$$\frac{Gm1}{Cc1} < \frac{Gm2}{Cc2} < \frac{Gm3}{CL}$$

IV. Design of 3-stage oppamp

The Fig.3 shows the entire design of 3-stage oppamp which consists for a differential single ended Telescopic amplifier as first stage, where as single ended common source differential amplifier as Second stage, and finally a PMOS based common source amplifier is used as final stage . For designing the 3-stage oppamp we First Stabilize the 2-stage oppamp, for having a PM greaterthan 45 deg the, We are considering Gm3 = 2.7Gm2, and Cc2 = CL = 300fF, which brings us the phase margin 50deg

From 3 stage oppamp design, we should have Gm3Cc1 = 1.7Gm1CL for having a phase margin of 60deg, and also it

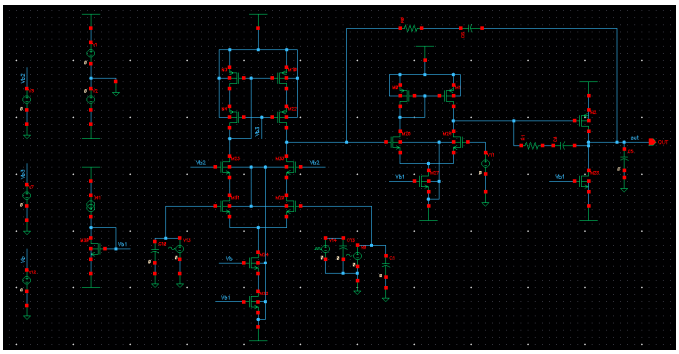


Fig. 3. 3-stage oppamp Design

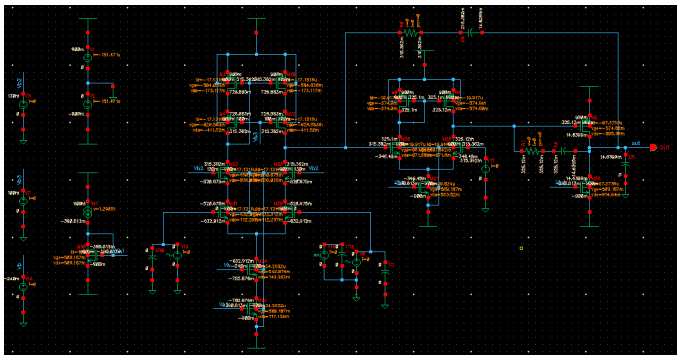
should satisfy the unity gain bandwidth condition. form there we consider Gm3 = 4Gm1, and CL = 2.35Cc1, there four Cc1 = 130fF. Our unity gain Band Width should be 110MHZ. We can consider the Gm1 = 250uS So, From this condition we can find Gm2 = 365uS and Gm3 = 1.017mS...
From the slew rate, I3/CL = 200V/us.. So I3 = 60uA..

By using the Gm Equation We can find the W/L for M2 mosfet Where (W/L)2 = 162, and considering a I2 = 20uA, We can have (W/L)26,25 mosfets as 32, and for the first stage the current flowing I1 = 17uA, So the (W/L)29,31 mosfets is 15

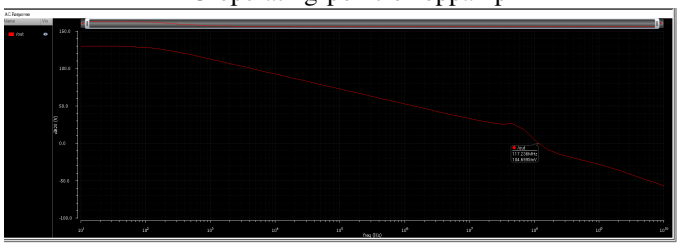
Mosfet Paremeters		
Device	Length(L)	Width(W)
M0	1u	50u
M1	1u	50u
M2	1u	162u
M3	1u	40u
M4	1u	40u
M10	1u	40u
M22	1u	40u
M23	500n	7.5u
M24	1u	30u
M25	500n	16u
M26	500n	16u
M27	500n	32u
M28	500n	50u
M29	500n	7.5u
M30	1u	8u
M31	500n	7.5u
M32	1u	30u
M33	500n	7.5u

V. (RESULTS)

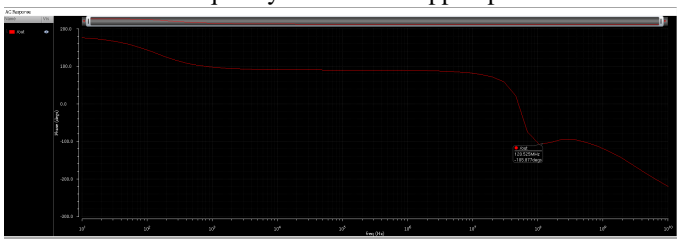
A. 3-stage Oppamp simulation results



DC operating point of oppamp

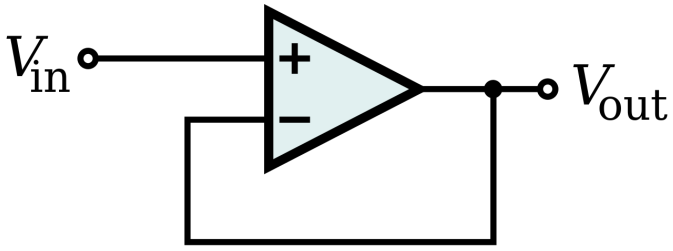


Frequency vs Gain of oppamp

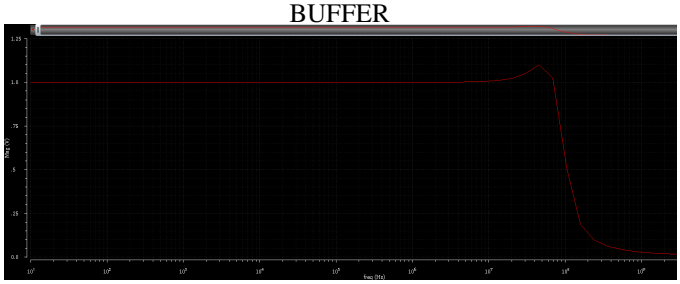


Frequency vs Phase of oppamp, where we can see the Phase margin of 60deg

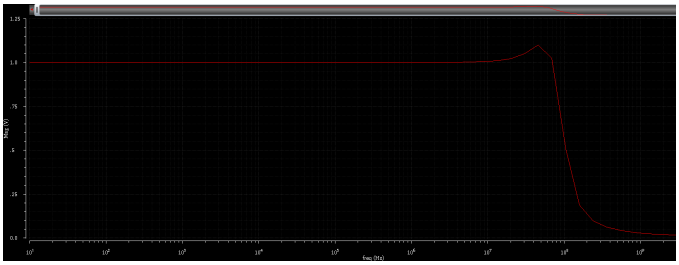
B. Using oppamp as a BUFFER



BUFFER

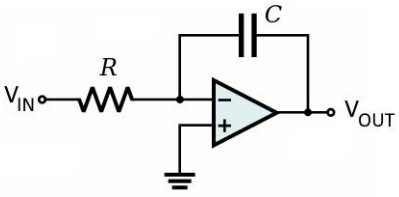


Gain of oppamp Buffer

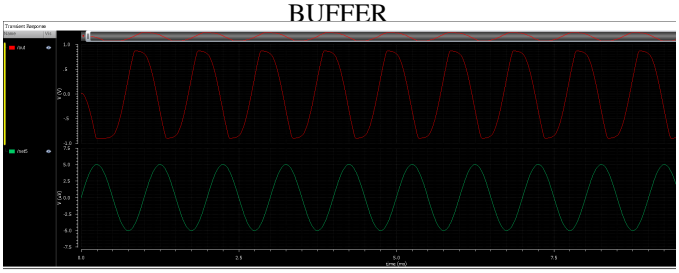


Transient analysis of oppamp buffer

C. Using oppamp as a Integrator



BUFFER



Transient analysis of oppamp integrator while providing a Sin wave as input

VI. (Conclusion)

In this design, we have satisfied all the parameters in the requirement and specially we achieved high Adm, slew rate and wide unity gain phase margin. By comparison we found that the simulation result is a little different from out theoretical design due to some omitting during our calculation. But after all, our calculation has represent the real situation and offered great help in the design of the device.