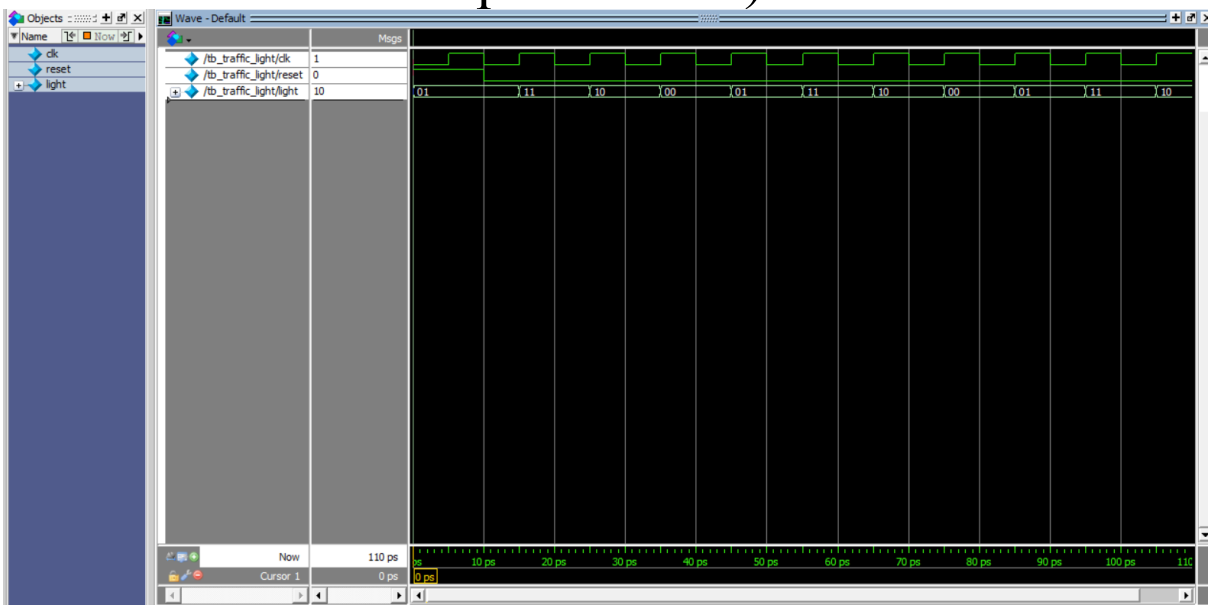
Simulation and Synthesis Report (Before optimization)



	Resource	Usage
1	Estimated Total logic elements	6
2		
3	Total combinational functions	4
4	▼ Logic element usage by number of LUT inputs	
1	-- 4 input functions	0
2	-- 3 input functions	0
3	-- <=2 input functions	4
5		
6	▼ Logic elements by mode	
1	-- normal mode	4
2	-- arithmetic mode	0
7		
8	▼ Total registers	4
1	-- Dedicated logic registers	4
2	-- I/O registers	0
9		
10	I/O pins	4
11		
12	Embedded Multiplier 9-bit elements	0
13		
14	Maximum fan-out node	clk~input