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In-situ Real-time Temperature Control of Baking Systems in Lithography

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ABSTRACT

We proposed an *in-situ* method to control the wafer spatial temperature uniformity during thermal cycling of silicon substrate in the lithography sequence. These thermal steps are usually conducted by the placement of the substrate on the heating plate for a given period of time. We have previously proposed an approach for controling the steady-state wafer temperature uniformity in steady-state. In this paper, we extend the approach by considering the dynamic properties of the system. A detailed physical model of the thermal system is first developed by considering energy balances on the system. Next, by monitoring the bake-plate temperature and fitting the data into the model, the temperature of the wafer can be estimated and controlled in real-time. This is useful as production wafers usually do not have temperature sensors embedded on it, these bake-plates are usually calibrated based on test wafers with embedded sensors. However, as processes are subjected to process drifts, disturbances, and wafer warpages, real-time correction of the bake-plate temperatures to achieve uniform wafer temperature is not possible in current baking systems. Any correction is done based on run-to-run control techniques which depends on the sampling frequency of the wafers. Our approach is real-time and can correct for any variations in the desired wafer temperature performance during both transient and steady state. Experimental results demonstrate the feasibility of the approach.

Keywords: Thermal processing, real-time control, temperature control

1. INTRODUCTION

Thermal processing of semiconductor substrate is common and critical to photoresist processing in the lithography sequence. Temperature uniformity control is an important issue in photoresist processing with stringent specifications and has a significant impact on the linewidth or critical dimension (CD). The most temperature sensitive step in the lithography sequence is the post-exposure bake (PEB) step. A number of recent investigations also showed the importance of proper bake-plate operation, both in steady-state and transient, on CD control,[1].[2]

Thermal processing of semiconductor wafers is commonly performed by placement of the substrate on a heated bake-plate for a given period of time. The heated bake-plate is usually of large thermal mass and is held at a constant temperature by a feedback controller that adjusts the heater power in response to a temperature sensor embedded in the bake-plate near the surface. The wafers are usually placed on proximity pins. When a wafer at room temperature is placed on the bake-plate, the temperature of the bake-plate drops at first but recovers gradually because of closed-loop control. Different air gap sizes will result in different temperature drops in the bake-plate due to the difference in the air gap thermal resistance between the substrates and the bake-plate. A warped wafer will thus affect the various baking processes in the lithography sequence. In this paper we present an in-situ approach to real-time control of both the transient and the steady-state wafer temperature uniformity during the baking steps in the lithography process. Our objective is to control the wafer to its desired value and minimize the spatial temperature non-uniformity across the wafer during the thermal cycle.

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We have demonstrated previously that information of the average air gap between the wafer and the bake-plate can be obtained with the use of system theory tools.[3] The relationship between the wafer and plate temperature at steady-state can be derived from physical modeling of the baking process. By monitoring the maximum plate temperature drop, the average air gap in each zone can be estimated, and we are able to calculate the new bake-plate temperature set point to achieve desirable wafer steady-state temperature.[4] One of the major drawbacks of the mentioned approach is that it does not take into account the dynamic performance of the wafer temperature. It has been reported that even though the steady-state temperature ranges was minimized, the resulting gains in CD uniformity cannot be realized attributed to the temperature distribution while rising to the PEB temperature.[5]

In this work, we proposed a real-time wafer temperature control method to minimize temperature non-uniformity in the whole heating process and improve the dynamic performance of the wafer temperature. By adopting a detailed simulation model based on first principle heat transfer of the system, we are able to extract the average air gap thickness between the bake-plate and wafer in each of the heating zones and consequently the wafer temperature online. Experimental result shows that the estimated wafer temperature is accurate, with which we can decrease the root mean square (RMS) of temperature non-uniformity in the whole process by more than 70%.

2. THERMAL MODELING OF THE SYSTEM

The distributed thermal processing system used in this work is shown in Figure 2. The bake plate is discretized into two zones and separated with a small air gap of approximately 1mm for thermal insulation. The fact that the zones are spatially disjoint ensures no direct thermal coupling between the zones, enhancing controllability. In the baking process, the bake plate is heated up by the cartridge heater attached to it. Resistive heating elements are embedded in each of the heater. Each heating zone is configured with its own temperature sensor and electronics embedded in the cartridge for feedback control. Depending on application, the number of zones of the bake-plate can be easily configured. In this section, we will only present the system dynamics for a two-zone system shown in Figure 2.

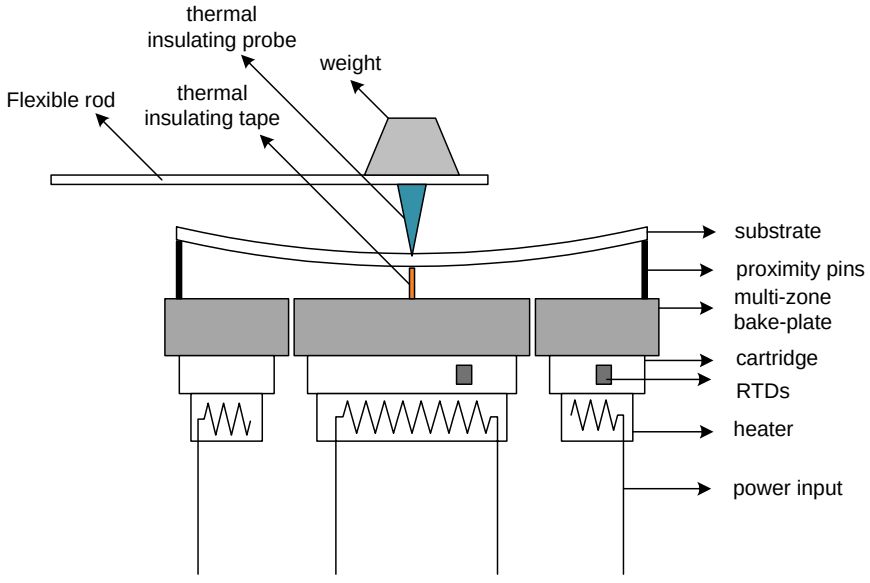

Figure 1. Schematic diagram of the thermal processing system.

Energy balances on the elements in the system can then be carried out to obtain a thermal model as follows:

$$\begin{aligned} C_w\dot{T}_w &= q_w^{in} + q_w^{out} + q_w^{top} + q_w^{bottom} \\ C_{ag}\dot{T}_{ag} &= q_{ag}^{in} + q_{ag}^{out} + q_{ag}^{top} + q_{ag}^{bottom} \\ C_p\dot{T}_p &= q_p^{in} + q_p^{out} + q_p^{top} + q_p^{bottom} \\ C_c\dot{T}_c &= q_c^{in} + q_c^{out} + q_c^{top} + q_c^{bottom} \\ C_h\dot{T}_h &= q_h^{in} + q_h^{out} + q_h^{top} + q_h^{bottom} + q^{input} \end{aligned}$$

where T is the temperature above the ambient, C the thermal capacitance, q^{in}, q^{out}, q^{top}, and q^{bottom} the heat flow into the element from inner zone, outer zone, top surface and bottom surface respectively, q^{input} the heater input power and the subscribe w, ag, p, c, and h represent the wafer, the air gap, the bake plate, the cartridge and the heater respectively.

The wafer top surface is exposed to the surroundings and so we have

$$q_w^{top} = h_w \cdot A_w^{top} \cdot (-T_w)$$

where h_w is the convection coefficient over the wafer top area A_w^{top}.

The air gap between the wafer and TEDs is about $210\mu m$. Since it is much less than $5.8mm$, and their temperature difference is considerably smaller than $200°C$,[6] the heat transfer mechanism is essentially conductive and given by

$$q_w^{bottom} = -k_{ag}A_{ag}\frac{\partial T_{ag}}{\partial z_{ag}}\bigg|_{boundary}$$

where k is thermal conductivity, and z the thickness.

Since the governing thermal transport between the elements in the system is conductive, at the boundary layer of two adjacent elements, we have

$$-k_\alpha A_\alpha \frac{\partial T_\alpha}{\partial z_\alpha}|_{boundary} = -k_\beta A_\beta \frac{\partial T_\beta}{\partial z_\beta}\bigg|_{boundary}$$

where the subscript α and β represent the two adjacent elements.

At the bottom layer of the system, the heater is exposed to the ambient, and we have

$$q_h^{bottom} = h_h \cdot A_h^{bottom} \cdot (-T_h)$$

where h_h is the convection coefficient over the heater bottom area A_h^{bottom}.

Most thermophysical properties are temperature dependent. However, for the temperature range of interest from $15°C$ to $150°C$, it is reasonable to assume that they remain fairly constant and can be obtained from handbooks,[7,8] as tabulated in Table I.

To assess the quality of the proposed system model, we perform conventional baking process experiment and compare the simulation with the experimental results. Our objective is to demonstrate that the proposed model succeeds in predicting the experimental wafer temperatures using bake-plate temperature drop and the input signal without resorting to the use of any fitting parameter and is therefore useful for scaling up.

In the experiment, a room temperature flat wafer is dropped on the baking system with proximity pin height of $140\mu m$. This causes the bake-plate temperature drop at first but recovers gradually because of closed-loop control. Two proportional-integral (PI) controllers are used to control the two zones of the bake-plate. Figure 2 shows the comparison result of the simulation and experimental bake-plate and wafer temperature when the air gap thickness is $140\mu m$.

It can be seen that the fit between of the wafer temperature from simulation and experimental results are very closed, which verify the effectiveness of the proposed thermal model. With the confidence of the system modeling, we will next fulfill real-time control experiment with the system model.

	Property	Value
Wafer (silicon)	Density, ρ	$2330 kgm^{-3}$
	Specific heat capacity, c_v	$750 JK^{-1}kg^{-1}$
	Thermal conductivity, k	$99 Wm^{-1}K^{-1}$
	Convection coefficient, h	$3.3824 Wm^{-2}K^{-1}$
	Thickness, z	$0.675 mm$
Air	Density, ρ	$1.1 kgm^{-3}$
	Specific heat capacity, c_v	$1000 JK^{-1}kg^{-1}$
	Thermal conductivity, k	$0.03 Wm^{-1}K^{-1}$
Bake-plate (aluminum)	Density, ρ	$2700 kgm^{-3}$
	Specific heat capacity, c_v	$917 JK^{-1}kg^{-1}$
	Thermal conductivity, k	$250 Wm^{-1}K^{-1}$
	Convection coefficient, h	$7.271 Wm^{-2}K^{-1}$
	Thickness, z	$6.8 mm$
Cartridge (aluminum)	Density, ρ	$2700 kgm^{-3}$
	Specific heat capacity, c_v	$917 JK^{-1}kg^{-1}$
	Thermal conductivity, k	$250 Wm^{-1}K^{-1}$
	Convection coefficient, h	$4.86 Wm^{-2}K^{-1}$
	Thickness, z	$4.4 mm$
Heater (aluminum)	Density, ρ	$2700 kgm^{-3}$
	Specific heat capacity, c_v	$917 JK^{-1}kg^{-1}$
	Thermal conductivity, k	$250 Wm^{-1}K^{-1}$
	Convection coefficient, h	$5.7828 Wm^{-2}K^{-1}$
	Thickness, z	$5.4 mm$

Table 1. Physical parameters of the thermal processing system,[7].[8]

3. EXPERIMENTAL RESULT

3.1. Experimental Setup

Most of the experimental conditions are similar to.[3] The experimental setup for the baking of 200 mm wafer is shown in Figure 2. Resistance temperature detectors (RTDs) are attached to the wafer,[9][10] for temperature measurement. The wafer is dropped onto the chuck by aligning the major flat surface of the wafer with the proximity pins. A control-system software was developed using the National Instruments LabView programming environment[11] to create a multivariable PI control framework and a dynamic temperature control system.

3.2. Control Structure

The proposed approach required detailed information of the system in order to identify the average air gap during subsequent processing. For the two-zone system, we have got accurate state-space model in section 2. Based on the model, we can develop a grey-box state-space model with the air gap thickness of the two zones as unknowns. In the experiment, the bake-plate temperature readings and input control signals are collected and fitted into the model to extract the air gap thickness and wafer temperature.

Figure 3.2 shows the control systems framework, the bake-plate temperatures, T_{p1} and T_{p2}, and the control signal, u_1 and u_2, in the two zones system are measured and sent to the estimator. The grey-box-model-based estimator will then estimate the air gap thickness and the wafer temperature of the two zones. The estimated

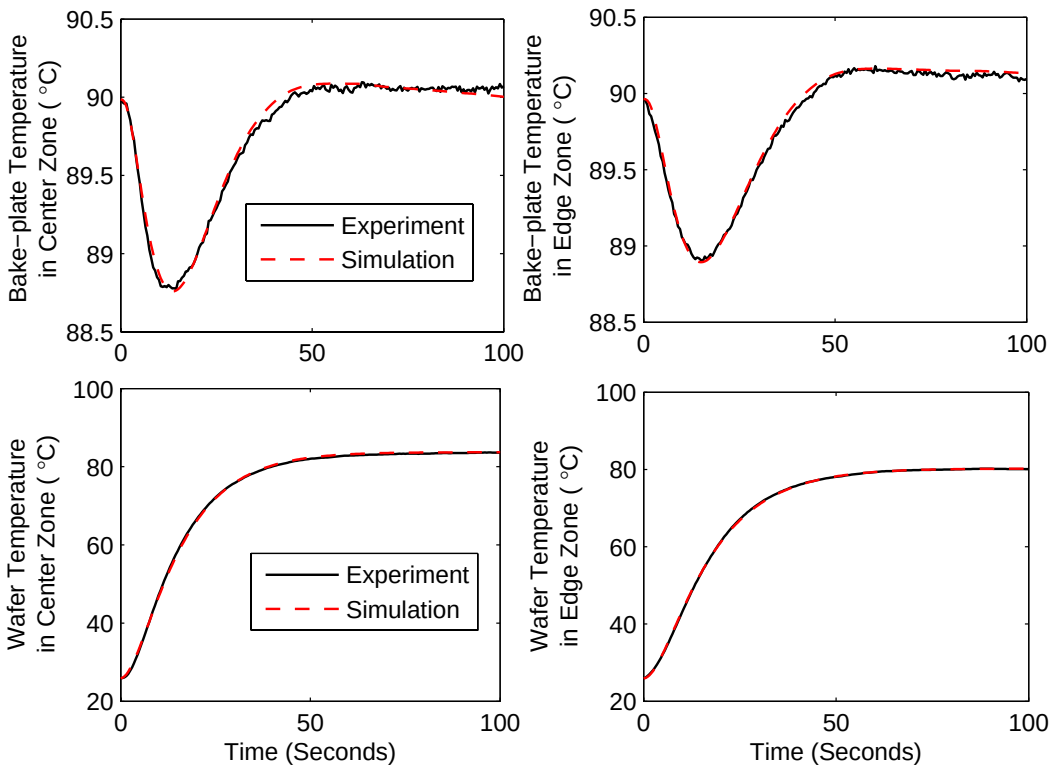

Figure 2. Bake-plate and wafer temperature in simulation and experiment with air gap thickness of $140\mu m$ using the calculated model.

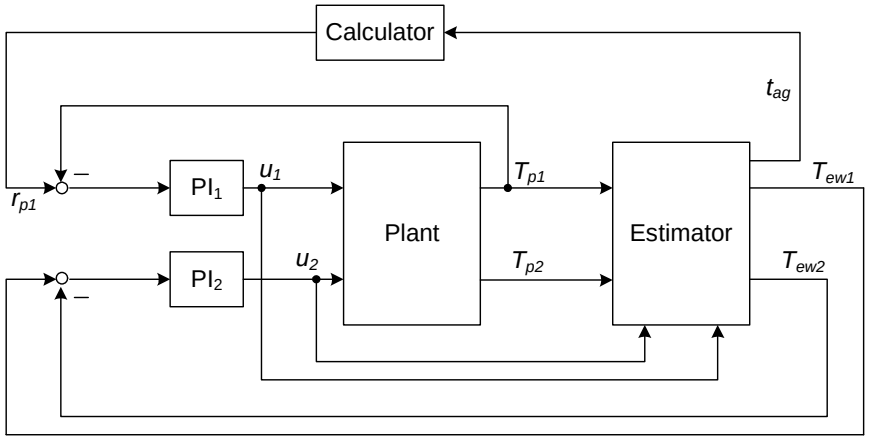

Figure 3. Block diagram of control structure.

air gap thickness t_{ag} is then used to determine the set-point r_{p1} of the bake plate and the estimated wafer temperatures T_{ew1} and T_{ew2} are used to control the wafer temperature uniformity in the process.

Using this method, we can real-time estimate the air gap thickness and wafer temperature and consequently regulate the control signal on-line to achieve desired wafer temperature and minimize temperature non-uniformity in the whole process.

3.3. Experimental Result

To demonstrate our approach, a flat wafer is firstly dropped on the bake-plate with a proximity pin height of $210\mu m$. Figure 3.3 shows the bake-plate and wafer temperature profiles using the steady-state temperature control method[4] and the proposed real-time control method. To validate our results, two temperature sensors (in this case RTDs) are embedded on the wafer surface corresponding to the center of each zone to monitor the wafer temperature.

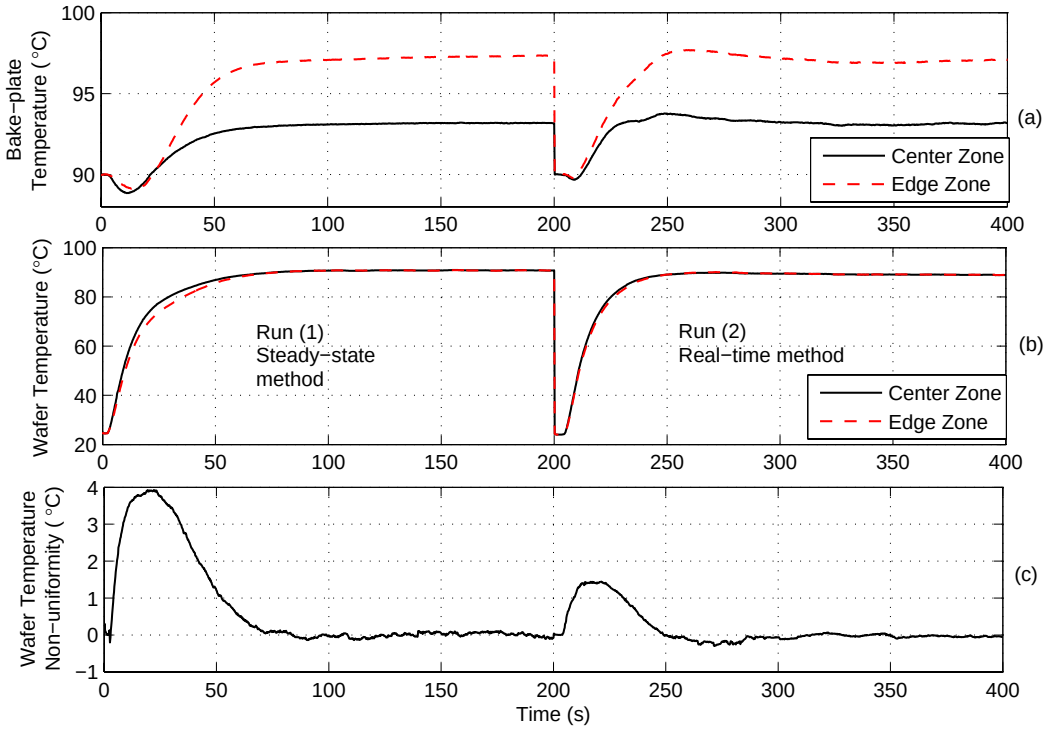

Figure 4. Temperature profile of bake-plate and wafer when a flat wafer is dropped on bake-plate with proximity pin height of $210\mu m$. The bake-plate temperatures, wafer temperatures and wafer temperature non-uniformity during the baking process are shown in subplots (a), (b) and (c) respectively.

Figure 3.3 consists of two experimental runs, (1) and (2). Run (1) corresponds to the steady-state control approach when the wafer is dropped on the bake-plate. The air gaps are first estimated based on the maximum bake-plate temperature drops. Then the new bake-plate temperature are set based on the estimated air gap thickness as shown in Figure 3.3(a). Notice that the wafer temperature is controlled to $90°C$ with a steady-state temperature nonuniformity of about $0.1°C$ as shown in Figure 3.3(b) and (c). However, since the new bake-plate temperature set-points are implemented about 20 seconds after the wafer is dropped to allow the maximum temperature drop point to occur as well as for computational delay of the corresponding air gap, the wafer can only reach steady state after about 80 seconds as shown in Figure 3.3(b). Furthermore, the wafer has a temperature nonuniformity of about $4°C$ in transient period as shown in Figure 3.3(c) since the temperature non-uniformity cannot be controlled before the air gap thickness estimation.

Next, real-time control of the wafer temperature is implemented. Figure 3.3(b) and (c) of run (2) shows that the wafer temperature reached $90°C$ in 50 seconds with the maximum temperature nonuniformity less than $1.5°C$ during the transient and steady state temperature nonuniformity less than $0.1°C$. The corresponding maximum temperature nonuniformity and root mean square error (RMS) during the thermal processing for experimental runs (1) and (2) are also shown in Table 2. It can be seen that the temperature nonuniformity RMS in the heating process is decreased form $1.48°C$ to $0.49°C$, an improvement of over 70%.

The feasibility of the approach is further demonstrated by heating a wafer with center-to-edge warpage of

$140\mu m$ on the same bake-plate with the proximity pin height of $210\mu m$. Wafer warpage is created mechanically as described in[3] and shown in Figure 2. The corresponding results are tabulated in Table 2 and shown in Figure 3.3, experimental run(3) and run(4). As expected, using the real-time control method, the warped wafer can also reach the steady-state temperature within 50 seconds, with much better temperature uniformity than steady-state control method. We note that both approaches described are superior to existing practice in the industries where any compensation is done in a run-to-run control approach.

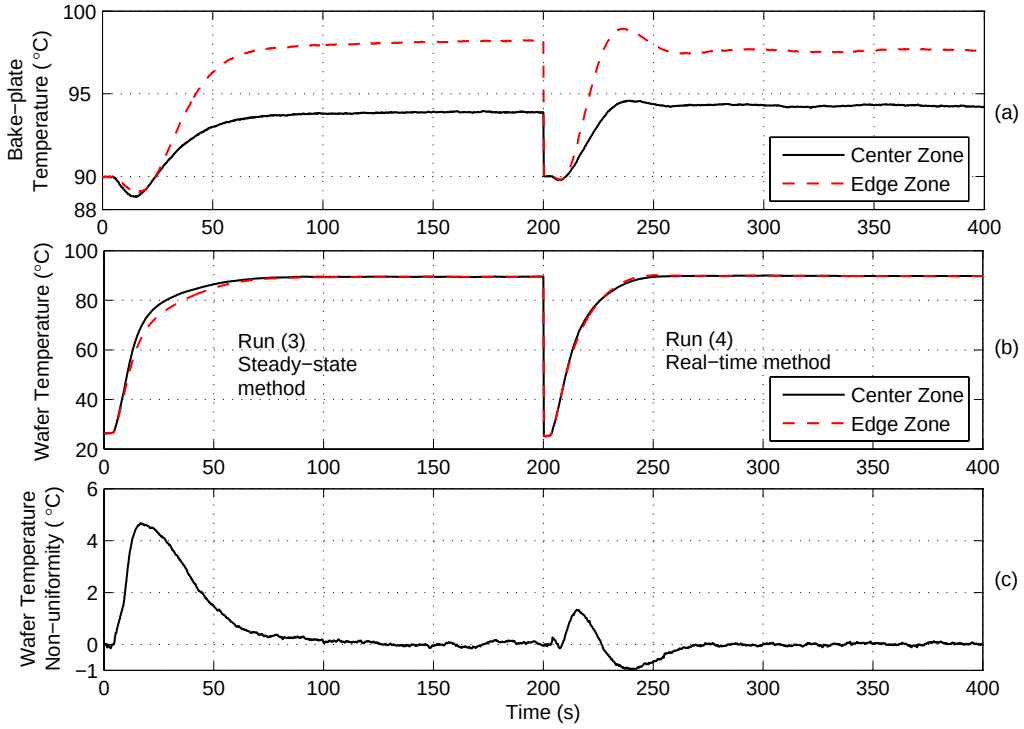

Figure 5. Temperature profile of bake-plate and wafer when a wafer with center-to-edge warpage of $140\mu m$ is dropped on bake-plate with proximity pin height of $210\mu m$. The bake-plate temperatures, wafer temperatures and wafer temperature non-uniformity during the baking process are shown in subplots (a), (b) and (c) respectively.

Run	Maximum nonuniformity ($°C$)	Nonuniformity RMS ($°C$)
(1)	3.93	1.48
(2)	1.45	0.49
(3)	4.68	1.62
(4)	1.33	0.39

Table 2. Performance comparison of the steady-state wafer temperature control method and the proposed real-time control method.

4. CONCLUSION

The lithography manufacturing process will continue to be a critical area in semiconductor manufacturing that limits the performance of microelectronics. Enabling advancements by computational, control, and signal processing methods are effective in reducing the enormous costs and complexities associated with the lithography sequence. In this paper, we have demonstrated an *in situ* approach to real-time control of the wafer temperature uniformity in heating process. Wafer temperature uniformity in transient period has been improved greatly

compared to the previous steady-state method. With the proposed approach, the root mean square of the wafer temperature nonuniformity across the wafer in the whole heating process has been improved more than 70%. The proposed approach can also be scaled up for larger wafers by increasing the number of sensors, actuators, and controllers.

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