RESEARCH ARTICLE | JULY 11 2005

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Rev Sci Instrum 76, 075111 (2005)
https://doi.org/10.1063/1.1979468

Estimation of wafer warpage profile during thermal processing in microlithography

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(Received 10 December 2004; accepted 29 May 2005; published online 11 July 2005)

Wafer warpage is common in microelectronics processing. Warped wafers can affect device performance, reliability, and linewidth control in various processing steps. Early detection will minimize cost and processing time. We propose in this article an *in situ* approach for estimating wafer warpage profile during the thermal processing steps in the microlithography process. The average air gap between wafer and bake-plate at multiple locations of a multizone bake-plate can be estimated and a profile can be obtained by joining these points. Experimental results demonstrate the feasibility and repeatability of the approach. This is a major improvement over our previously developed approach, in which only the average warpage could be obtained. The proposed approach requires no extra processing steps and time, as compared to conventional off-line methods. © *2005 American Institute of Physics.* [DOI: 10.1063/1.1979468]

I. INTRODUCTION

Wafer warpage can affect device performance, reliability, and linewidth or critical dimension (CD) control in various microelectronic manufacturing processes. The drive toward smaller device geometries has placed much tighter control limits on the various semiconductor manufacturing processes. Hence, any knowledge of the wafer warpage profile could be a source of active compensation during the subsequent processing steps. In cases of serious warpage, the wafer could be discarded, thereby saving cost and time in future processing. Current techniques for measuring wafer warpage include capacitive measurement probe,[1] shadow Moire technique,[2] and pneumatic-electromechanical technique.[3] These are off-line methods in which the wafer has to be removed from the processing equipment and placed in the metrology tool, resulting in increased processing steps, time, and cost. In this work, we describe an *in situ* approach to detect and estimate the profile of a warped wafer during thermal processing steps in microlithography.

The baking of a semiconductor substrate is common and critical to photoresist processing[4] in the microlithography sequence. Temperature uniformity control is an important issue in photoresist processing with stringent specifications.[5] The most temperature-sensitive step is the postexposure bake step. Requirements call for temperature to be controlled within 0.1 °C at temperatures between 70°C and 150°C. For commercially available deep ultraviolet resist, a representative postexposure bake latitude for CD variation is about 5 nm/°C.[6] A number of recent investigations also showed the importance of proper bake-plate operation on CD control.[7–12] Warpage can result in a nonuniform wafer temperature distribution across the wafer. Results show that warpage of less than 50 μm can lead to a temperature variation of 1 °C across the wafer during baking.[13] This can lead to substantial spatial variation in CD. Warpage becomes more problematic for larger wafers and the maximum allowable warpage for a 300 mm wafer is 100 μm from center to edge.[14]

Thermal processing of semiconductor wafers is commonly performed by placement of the substrate on a heated bake-plate for a given period of time. The heated bake-plate is usually of large thermal mass[13] and is held at a constant temperature by a feedback controller that adjusts the heater power in response to a temperature sensor embedded in the bake-plate near the surface. The wafers are usually placed on proximity pins of the order of 100-200 μm to create an air gap so as to minimize contamination. When a wafer at room temperature is placed on the bake-plate, the temperature of the bake-plate drops at first but recovers gradually because of closed-loop control, as shown in Fig. 1. Figure 1 also shows the bake-plate temperature when a flat wafer and a warped wafer with center-to-edge warpage of 110 μm is dropped on the plate. It is clear that different air-gap sizes will result in different temperature drops in the bake-plate due to the difference in the air-gap/thermal resistance between the substrates and the bake-plate. Warped wafers will thus affect the various baking steps in the microlithography sequence[7] due to a different air gap across the wafer. The bake-plate temperature can provide useful information of the wafer warpage.

We have previously demonstrated that by monitoring the temperature profile of a conventional bake-plate during the thermal processing steps in microlithography, we are able to detect wafer warpages.[15] For a conventional thermal processing system, the proposed approach will provide the user with information on the degree of warpage; information on the profile of the warpage is not possible due to the fact that the

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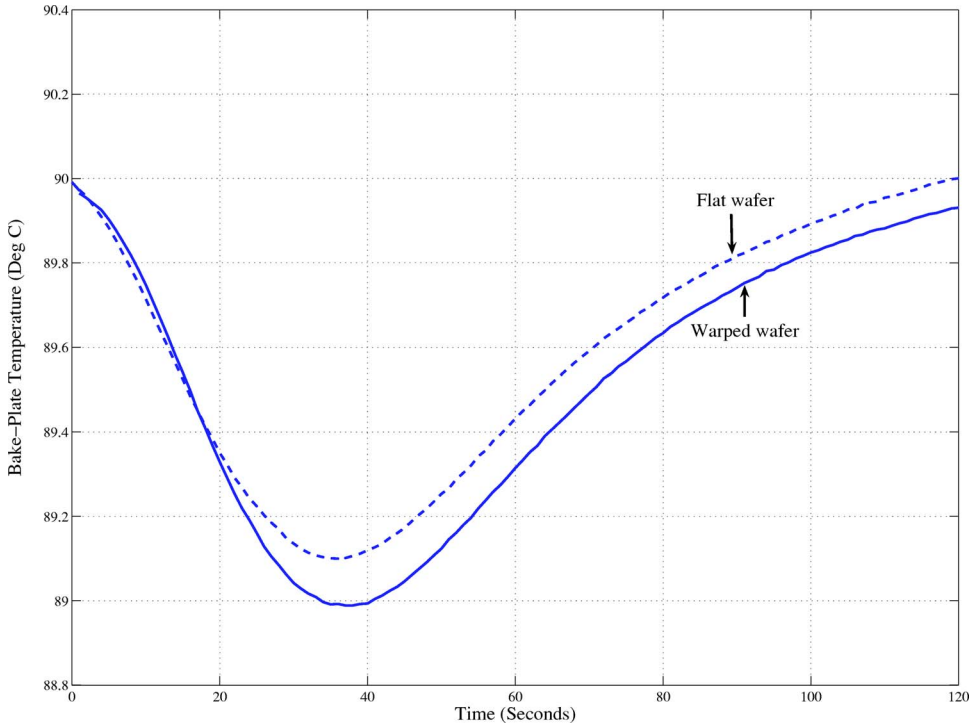

FIG. 1. (Color online) The bake-plate temperature when a warped and flat wafer is dropped on the bake-plate. The solid and dashed lines represent the case of a warped and flat wafer, respectively. The warped wafer has a warpage of 110 μm center to edge.

bake-plate is of a single zone. In this article, we extend the approach to estimating the profile of the warped wafer. To estimate the profile of the wafer, multiple temperature measurements of the bake-plate are required; this is only possible with a multizone bake-plate with integrated temperature sensing within each zone. A distributed thermal processing system is developed consisting of an array of heating zones. Resistive heating elements are embedded within each of the heating zones. Each heating zone is configured with its own temperature sensor and electronics for feedback control. Each heating zone is separated with a small air gap of approximately 1 mm for thermal insulation. The fact that the zones are spatially disjoint ensures no direct thermal coupling between the zones, enhancing controllability. Its small thermal mass allows for fast dynamic manipulation of temperature profile. Depending on application, the number of zones of the bake-plate can be easily configured.

By monitoring the plate temperature profiles within each of the zones, coupled with first-principles thermal modeling and system identification techniques, an estimate of the profile of the warped wafer can be obtained. The proposed approach is also robust to modeling errors compared to our previous method[15] in which only a single point (the maximum temperature drop point of the bake-plate) on the plate temperature profile is used for warpage detection. The profile of the warped wafer can be estimated as follows. A detailed thermal model of the system is first developed and formulated in state-space form.[16] The variables of interest which are the air gaps in the various zones are the unknowns in the state matrices. Next, the plate temperatures during the baking process are monitored and collected. The collected data are then fitted into the model using subspace identification techniques. The various air gaps can then be extracted from the state-space model to estimate the profile of the wafer. We would also like to point out that the proposed technique requires no extra processing steps and is an *in situ* approach. The proposed approach can also serve as a fault-detection technique to determine if a wafer warps.

II. THERMAL MODELING OF THE BAKING PROCESS

Analysis of the thermal processing system can be done with a model considering the radial as well as the axial effects of heat transfer in the module. Consider the setup of Fig. 2, which deals with the plate/air gap/wafer system of a simplified two-radial-zone system (the model for N-radial zone can be extended easily). The bake-plate is a multizone bake-plate with a small proximity air gap between each zone. The system is discretized spatially into N radial elements, where N corresponds to the number of zones in the bake-plate. Spatial distributions of temperature and other quanti-

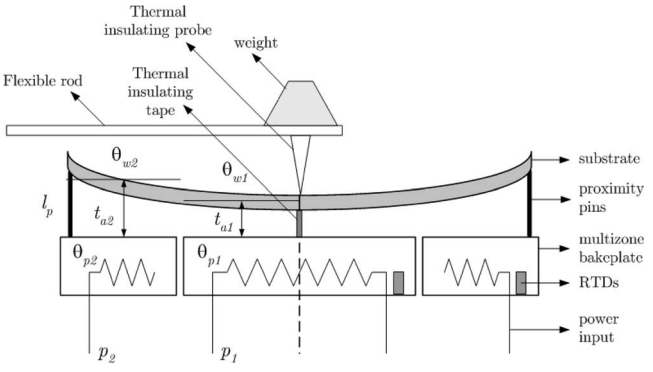

FIG. 2. Schematic of warpage setup and thermal modeling of a two-zone thermal processing system.

TABLE I. Thermophysical properties of the thermal processing system.

	Property	Value
Wafer (silicon)	Density, ρ_w	2330 kg/m^3
	Specific-heat capacity, c_w	0.750 kJ/kgK
	Thermal conductivity of silicon, k_w	99 W/mK
	Diameter, D	200 mm
	Thickness, t_w	750 μm
Bake-plate (aluminum)	Density, ρ_p	2700 kg/m^3
	Specific-heat capacity, c_p	0.917 kJ/kg K
	Thickness, t_p	0.0107 m
	Element width, Δ_r	50 mm
Air	Thermal conductivity, k_a	0.03 W/mK
	Convective heat transfer coefficient, h	3 W/m^2 K

TABLE II. Thermal capacitances and resistances of the baking system.

Thermal capacitances and resistances	Value
C_{w1}	0.0103 kJ/K
C_{w2}	0.0309 kJ/K
R_{wz1}	42.1941 K/W
R_{wz2}	14.065 K/W
R_{w1}	2.3549 K/W
R_{w2}	707.36 K/W
R_{p1}	544.70 K/W
R_{p2}	49.581 K/W

ties in a silicon wafer are most naturally expressed in a cylindrical coordinate system. We will assume that the substrate used for baking is a silicon wafer and the bake-plate is cylindrical in shape with the same diameter as the wafer. Energy balances on the wafer and bake-plate can then be carried out to obtain a two-dimensional model as follows:

$$C_{p1}\dot{\theta}_{p1} = -\frac{\theta_{p1}-\theta_{p2}}{R_{p1}} - \frac{\theta_{p1}-\theta_{w1}}{R_{a1}} + q_1, \tag{1}$$

$$C_{pi}\dot{\theta}_{pi} = \frac{\theta_{p(i-1)}-\theta_{pi}}{R_{p(i-1)}} - \frac{\theta_{pi}-\theta_{p(i+1)}}{R_{pi}} - \frac{\theta_{pi}-\theta_{wi}}{R_{ai}} + q_i, \quad 2 \leqslant i \leqslant N-1, \tag{2}$$

$$C_{pN}\dot{\theta}_{pN} = \frac{\theta_{p(N-1)}-\theta_{pN}}{R_{p(N-1)}} - \frac{\theta_{pN}}{R_{pN}} - \frac{\theta_{pN}-\theta_{wN}}{R_{aN}} + q_N, \tag{3}$$

$$C_{w1}\dot{\theta}_{w1} = \frac{\theta_{p1}-\theta_{w1}}{R_{a1}} - \frac{\theta_{w1}-\theta_{w2}}{R_{w1}} - \frac{\theta_{w1}}{R_{wz1}}, \tag{4}$$

$$C_{wi}\dot{\theta}_{wi} = \frac{\theta_{w(i-1)}-\theta_{wi}}{R_{w(i-1)}} + \frac{\theta_{pi}-\theta_{wi}}{R_{ai}} - \frac{\theta_{wi}-\theta_{w(i+1)}}{R_{wi}} - \frac{\theta_{wi}}{R_{wzi}}, \quad 2 \leqslant i \leqslant N-1, \tag{5}$$

$$C_{wN}\dot{\theta}_{wN} = \frac{\theta_{w(N-1)}-\theta_{wN}}{R_{w(N-1)}} + \frac{\theta_{pN}-\theta_{wN}}{R_{aN}} - \frac{\theta_{wN}}{R_{wN}} - \frac{\theta_{wN}}{R_{wzN}}, \tag{6}$$

where $\theta_{pi}=T_{pi}-T_\infty$ is the ith plate element temperature above ambient; $\theta_{wi}=T_{wi}-T_\infty$ is the ith wafer element temperature above ambient; T_∞ is the ambient temperature; C_{pi} is the thermal capacitance of the ith plate element; C_{wi} is the ther-

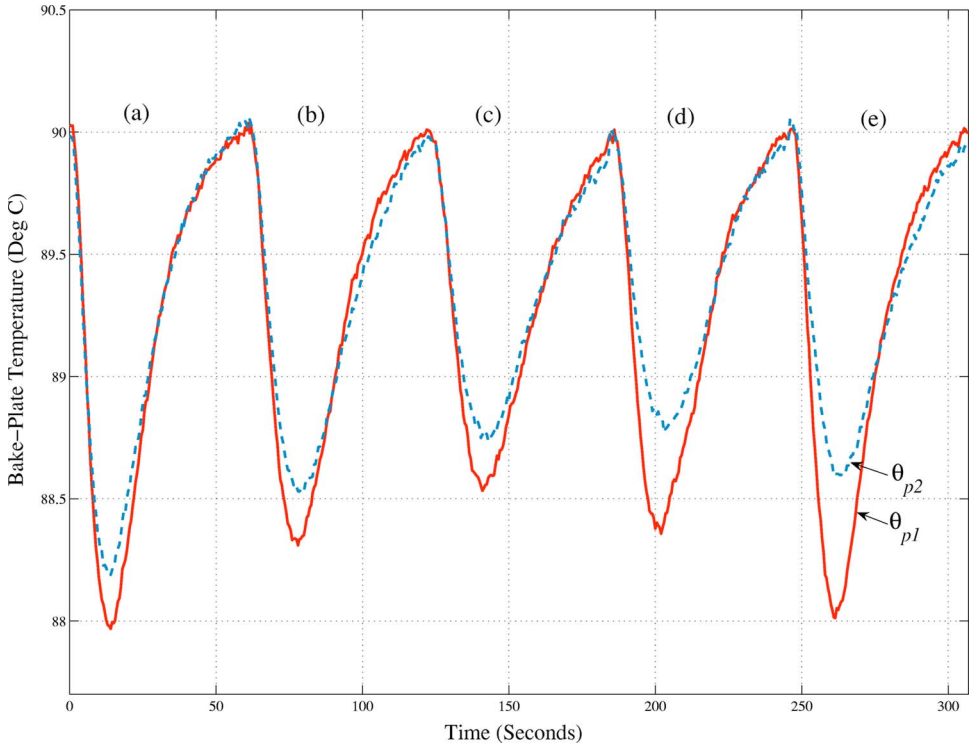

FIG. 3. (Color online) Results for five experimental runs to demonstrate that different air-gap sizes cause different magnitudes of bake-plate temperature drops before recovery for a two-zone baking system. Experimental runs (a)-(e) represent different experimental conditions outlined in Section III C. The solid and dashed curves represent the bake-plate temperature in the center (θ_{p1}) and the edge zone (θ_{p2}), respectively.

TABLE III. Estimation of air gap.

Expt. run	Proximity pin height $l_p(\mu m)$	Estimated air gap: Center zone t_{a1} (μm)	Estimated air gap: Edge zone t_{a2} (μm)	Deviation from flat wafer: Center zone $\delta_1=t_{a1}-l_p$ (μm)	Deviation from flat wafer: Edge zone $\delta_2=t_{a2}-l_p$ (μm)
(b)	110.0	109.0	107.8	−1.0	−2.2
(c)	165.0	162.1	163.7	−2.9	−1.3
(d)	220.0	125.5	174.0	−94.5	−46.0
(e)	165.0	69.1	123.8	−95.9	−41.2

mal capacitance of the ith wafer element; R_{pi} is the thermal conduction resistance between the ith and $(i+1)$th plate element; R_{wi} is the thermal conduction resistance between the ith and $(i+1)$th wafer element; R_{wzi} is the thermal convection loss of the ith wafer element; R_{ai} is the thermal conduction resistance between the ith plate and ith wafer element; and q_i is the power into the i_{th} plate element.

The various thermal resistances and capacitances are given by

$$R_{pi} = \frac{\ln\left(\frac{i+1/2}{i-1/2}\right)}{2\pi k_a t_p}\ (\mathrm{K/W}), \quad 1 \leqslant i \leqslant N-1,$$

$$R_{pN} = \frac{1}{h(\pi D t_p)}\ (\mathrm{K/W}),$$

$$R_{wi} = \frac{\ln\left(\frac{i+1/2}{i-1/2}\right)}{2\pi k_w t_w}\ (\mathrm{K/W}), \quad 1 \leqslant i \leqslant N-1,$$

$$R_{wN} = \frac{1}{h(\pi D t_w)}\ (\mathrm{K/W}),$$

$$R_{wzi} = \frac{1}{hA_{zi}}\ (\mathrm{K/W}),$$

$$R_{ai} = \frac{t_{ai}}{k_a A_{zi}}\ (\mathrm{K/W}),$$

$$C_{pi} = \rho_p c_p (t_p A_{zi})\ (\mathrm{J/K}), \quad 1 \leqslant i \leqslant N,$$

$$C_{wi} = \rho_w c_w (t_w A_{zi})\ (\mathrm{J/K}), \quad 1 \leqslant i \leqslant N,$$

$$A_{zi} = \pi \Delta_r^2 [i^2 - (i-1)^2]\ (\mathrm{m}^2), \quad 1 \leqslant i \leqslant N,$$

where A_{zi} is the cross-sectional area of element i normal to the axial heat flow. t_p and t_w are the bake-plate thickness and wafer thickness, respectively, and t_{ai} is the air gap between the ith wafer and bake-plate elements. k_a and k_w are the thermal conductivity of air and wafer, respectively. h is the

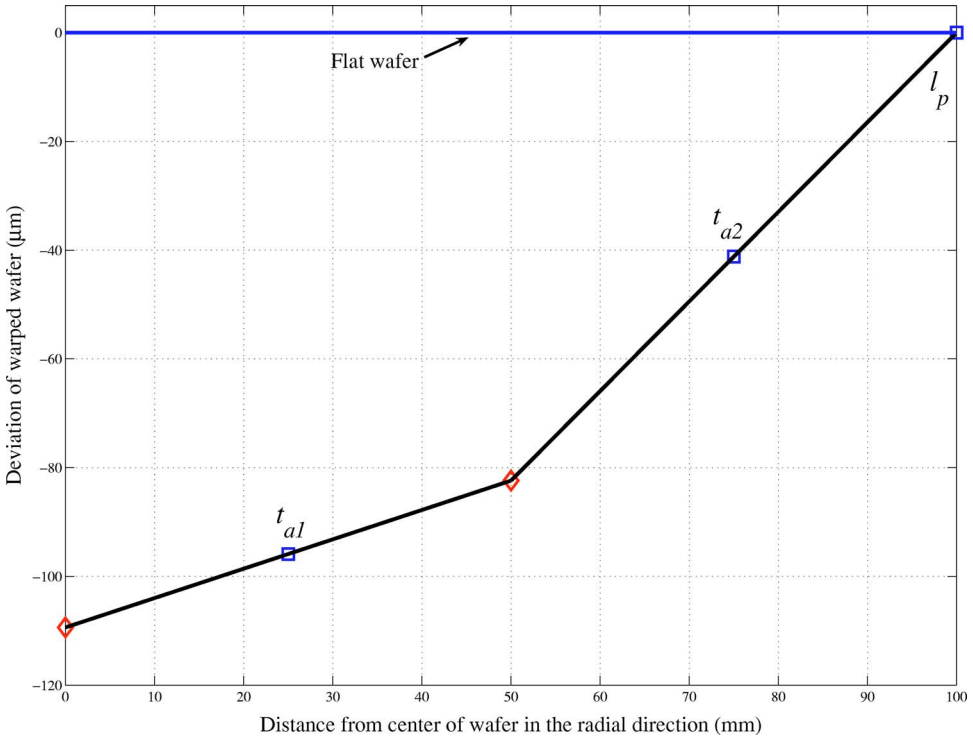

FIG. 4. (Color online) Estimated profile of the warped wafer based on experimental run (e).

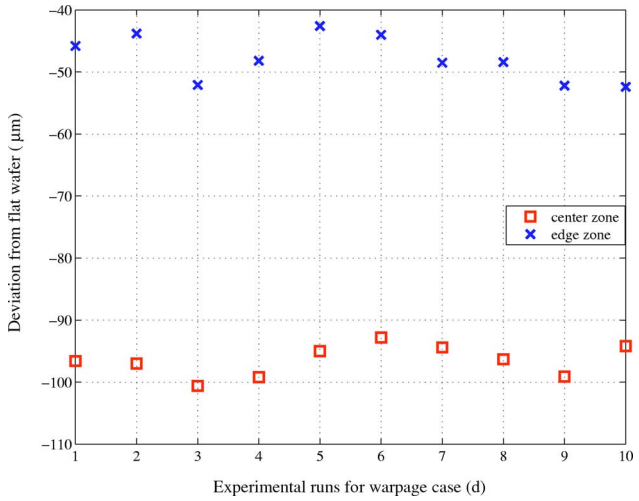

FIG. 5. (Color online) Experimental runs for the warped wafer based on experimental run (d).

convective heat transfer coefficient. ρ_p and ρ_w are the density of the bake-plate and wafer, respectively. c_p and c_w are the specific-heat capacity of the bake-plate and wafer, respectively. The width of each element is given by $\Delta_r = D/(2N)$.

Equations (1)–(6) can be rearranged into a state-space format,

$$\dot{\theta} = \begin{bmatrix} \dot{\theta}_p \\ \dot{\theta}_w \end{bmatrix} = \begin{bmatrix} \mathbf{F_{pp}} & \mathbf{F_{pw}} \\ \mathbf{F_{wp}} & \mathbf{F_{ww}} \end{bmatrix} \begin{bmatrix} \theta_p \\ \theta_w \end{bmatrix} + \begin{bmatrix} \mathbf{G_{pp}} \\ \mathbf{0_N} \end{bmatrix} \mathbf{q} = \mathbf{F}\boldsymbol{\theta} + \mathbf{G}\mathbf{q}, \tag{7}$$

where θ_p and θ_w are vectors containing the n-plate and wafer temperatures, respectively. The state matrices **F** and **G** can be found in the Appendix. In the next section, we will demonstrate that by monitoring the bake-plate temperatures, θ_{pi}, and making use of system-identification techniques,[17] we are able to extract the air-gap information, t_{ai}, between the ith wafer and bake-plate elements from the state matrix, **F**. Coupled with the information of the proximity pins, an estimate of the warped wafer profile can be obtained. We demonstrate experimentally the approach on a two-zone thermal processing system.

III. EXPERIMENTAL RESULTS

Although most of the parameters in the model developed in the previous section can be obtained from handbooks, to obtain a more accurate and realistic model of the actual system, actual input-output data are used to estimate the various parameters in Eq. (7). In this section, we will first outline the experimental setup used to estimate the warped wafer profile and the experiments performed to demonstrate the feasibility and repeatability of the proposed approach.

A. Experimental setup

The experimental setup for the baking of 200 mm wafer is shown in Fig. 2. As discussed previously, the programmable thermal system can be configured up to 25 zones. Without loss of generality, we will demonstrate our proposed approach on a two-radial-zone system. A control software system was developed using the National Instruments Labview programming environment to create a multivariable proportional-integral (PI) control framework and a dynamic temperature control system. Two PI controllers of the following form are used to control the two zones of the bake-plate:

$$u(t) = K_{ci}\left(e(t) + \frac{1}{T_{Ii}}\int e(t)dt\right),$$

where $u(t)$ and $e(t)$ are the control signal to the bake-plate and the error between the desired and actual bake-plate temperatures. The PI parameters for the center and edge zones are given by $K_{c1}=14.0$, $T_{I1}=300$ and $K_{c2}=45.0$, $T_{I2}=300$, respectively. The experiments were conducted at a temperature set point of 90 °C with a sampling and control interval of 0.5 s. This temperature corresponds to a soft-bake condition for photoresist processing.[18] Most thermophysical properties are temperature-dependent. However, for the temperature range of interest from 15 to 150 °C, it is reasonable to assume that they remain fairly constant and can be obtained from handbooks[19] as tabulated in Table I.

Wafer warpage is a function of temperature. Even at the 25–120 °C range, changes of the order of up to1 μm/10 °C are possible. Our proposed approach makes use of available temperature signals and does not require extra instrumentation. Only the average air gap can be detected in each zone and hence the method may not be sensitive enough to detect possible warpage of up to10 μm (assuming1 μm/10 °C change) induced thermally.

For experimental verification, warpage must be known. Wafer warpage is created mechanically as shown in Fig. 2. We ensure minimal warpage during the baking experiment by mechanically pressing the center of the wafer against a thermal insulating tape of known thickness. The center-to-edge warpage is given by the difference between height of proximity pin and thermal tape thickness.

B. Initialization phase

The proposed approach required detailed information of the system in order to identify the air gap during each subsequent processing. Parameters that do not vary during subsequent processing can be estimated via system identification techniques during the initialization phase. For the two-zone system, the various elements of the state-space representation of Eq. (7) are given in the Appendix. The various thermal capacitances and resistances are tabulated in Table II. For a given bake-plate, the bake-plate element thermal capacitances (C_{p1} and C_{p2}) are expected to be fixed and hence can be determined during the initialization phase of the experiment. Run (a) in Fig. 3 was used to determine the plate element thermal capacitances (C_{p1} and C_{p2}) in the state-space matrices. The experiment was conducted by dropping a flat wafer on the bake-plate with a known air gap of $t_a = 55$ μm. Since the respective air gaps are known (i.e., t_{a1} and t_{a2}), the air-gap resistances R_{a1} and R_{a2} can be computed as

$$R_{a1} = \frac{t_{a1}}{k_a A_{z1}} = 0.2321 \text{ K/W}$$

and

$$R_{a2} = \frac{t_{a1}}{k_a A_{z2}} = 0.0774 \text{ K/W}.$$

Next, to determine the unknown parameters C_{p1} and C_{p2} in the structured state-space model in Eq. (7), standard state-space identification algorithms[17] can be used. The bake-plate temperature profile of the two-zone system is then fitted using the structured state-space model. The estimated C_{p1} and C_{p2} are 0.208 and 0.738 kJ/K, respectively.

C. Warpage profile estimation

Once the various wafer, bake-plate, and PI controller parameters are known, the average air gap (t_{a1} and t_{a2}) in each zone can be estimated via state-space identification using available bake-plate temperature measurements (θ_{p1} and θ_{p2}). The feasibility and repeatability of the approach are demonstrated via a series of experiments.

Experimental runs (b) and (c) in Fig. 3 show the case when a flat wafer is dropped on the bake-plate with different proximity pins (i.e., different air gaps). The proximity pin heights l_p for runs (b) and (c) are 110 μm and 165 μm, respectively. The estimated air gaps for the two runs are tabulated in Table III. A good measure of the extent of warpage is to measure the deviation of the average air gap from the proximity pin height. For experimental runs (b) and (c), since the wafer is flat, δ_1 and δ_2 are closed to zero as expected.

Experimental runs (d) and (e) in Fig. 3 show the case of a wafer with center-to-edge warpage of 110 μm dropped on the bake-plate with different proximity pin heights. The proximity pin heights l_p for runs (d) and (e) are 220 μm and 165 μm, respectively. The estimated air gaps for the two runs are also tabulated in Table III. δ_1 and δ_2 in experimental runs (d) and (e) are approximately the same. Based on the estimated δ_1 and δ_2 together with the proximity pin height, the profile of the wafer can be obtained by extrapolation as shown in Fig. 4 [based on experimental run (e)]. An estimated warpage of 109.4 μm from center to edge for the warped wafer is obtained which is close to the known warpage of 110 μm.

These two sets of experimental runs [(b),(c) and (d),(e)] demonstrate the feasibility of the approach in that a different bake system might have different proximity pin gaps, however the degree of warpage should be the same for the same wafer. Next, the repeatability of the proposed approach is demonstrated in Fig. 5, where the experimental condition (d) in Table III was repeated 10 times. For each run, the data are fitted to the state-space model in Eq. (7). In this article, we have demonstrated that it is possible to estimate the profile of a wafer. We expect the profile accuracy to increase as the number of zones is increased. The proposed approach can also act as a fault-detection technique. A standard approach to fault detection is to define a threshold based on manufacturing requirements so that any violation of the threshold is considered a fault.

APPENDIX: DETAILED REPRESENTATION OF THE THERMAL MODEL IN STATE-SPACE FORMAT

The energy balance equations in Eqs. (1)–(6) can be rearranged into state-space format

$$\dot{\theta} = \begin{bmatrix} \dot{\theta}_p \\ \dot{\theta}_w \end{bmatrix} = \begin{bmatrix} \mathbf{F_{pp}} & \mathbf{F_{pw}} \\ \mathbf{F_{wp}} & \mathbf{F_{ww}} \end{bmatrix} \begin{bmatrix} \theta_p \\ \theta_w \end{bmatrix} + \begin{bmatrix} \mathbf{G_{pp}} \\ \mathbf{0_N} \end{bmatrix} \mathbf{q} = \mathbf{F}\boldsymbol{\theta} + \mathbf{G}\mathbf{q},$$

where

$$\mathbf{F_{pp}}(1,1) = -\frac{(1/R_{p1} + 1/R_{a1})}{C_{p1}},$$

$$\mathbf{F_{pp}}(i,i) = -\frac{(1/R_{p(i-1)} + 1/R_{pi} + 1/R_{ai})}{C_{pi}}, \quad 2 \leqslant i \leqslant N,$$

$$\mathbf{F_{pp}}(i,i+1) = \frac{1/R_{pi}}{C_{pi}}, \quad 1 \leqslant i \leqslant N-1,$$

$$\mathbf{F_{pp}}(i,i-1) = \frac{1/R_{p(i-1)}}{C_{pi}}, \quad 2 \leqslant i \leqslant N,$$

$$\mathbf{F_{ww}}(1,1) = -\frac{(1/R_{w1} + 1/R_{a1} + 1/R_{wz1})}{C_{w1}},$$

$$\mathbf{F_{ww}}(i,i) = -\frac{(1/R_{w(i-1)} + 1/R_{wi} + 1/R_{ai} + 1/R_{wzi})}{Cwi}, \quad 2 \leqslant i \leqslant N,$$

$$\mathbf{F_{ww}}(i,i+1) = \frac{1/R_{wri}}{C_{wi}}, \quad 1 \leqslant i \leqslant N-1,$$

$$\mathbf{F_{ww}}(i,i-1) = \frac{1/R_{wr(i-1)}}{C_{wi}}, \quad 2 \leqslant i \leqslant N.$$

In addition, $\mathbf{F_{pw}}$ and $\mathbf{F_{wp}}$ are diagonal matrices given by

$$\mathbf{F_{pw}} = \begin{bmatrix} \frac{1}{R_{a1}C_{p1}} & 0 & \cdots & \\ 0 & \frac{1}{R_{a2}C_{p2}} & 0 & \\ & \ddots & & \\ & & & \frac{1}{R_{aN}C_{pN}} \end{bmatrix}$$

and

$$\mathbf{F_{wp}} = \begin{bmatrix} \frac{1}{R_{a1}C_{w1}} & 0 & \cdots & \\ 0 & \frac{1}{R_{a2}C_{w2}} & 0 & \\ & \ddots & & \\ & & & \frac{1}{R_{aN}C_{wN}} \end{bmatrix}.$$

The excitation term $\mathbf{G_{pp}}$ is given by

$$\mathbf{G_{pp}} = \begin{bmatrix} \frac{1}{C_{p1}} & 0 & \cdots & \\ 0 & \frac{1}{C_{p2}} & 0 & \\ & \ddots & & \\ & & & \frac{1}{C_{pN}} \end{bmatrix}.$$

For the two-zone system, the state matrices $\mathbf{F}$ and $\mathbf{G}$ can be further expressed as follows:

$$\mathbf{F_{pp}} = \begin{bmatrix} -\frac{1}{C_{p1}}\left(\frac{1}{R_{p1}} + \frac{1}{R_{a1}}\right) & \frac{1}{C_{p1}}\frac{1}{R_{p1}} \\ \frac{1}{C_{p2}}\frac{1}{R_{p1}} & -\frac{1}{C_{p2}}\left(\frac{1}{R_{p1}} + \frac{1}{R_{a2}} + \frac{1}{R_{p2}}\right) \end{bmatrix},$$

$$\mathbf{F_{pw}} = \begin{bmatrix} \frac{1}{C_{p1}}\frac{1}{R_{a1}} & 0 \\ 0 & \frac{1}{C_{p2}}\frac{1}{R_{a2}} \end{bmatrix},$$

$$\mathbf{F_{wp}} = \begin{bmatrix} \frac{1}{C_{w1}}\frac{1}{R_{a1}} & 0 \\ 0 & \frac{1}{C_{w2}}\frac{1}{R_{a2}} \end{bmatrix},$$

$$\mathbf{F_{ww}} = \begin{bmatrix} -\frac{1}{C_{w1}}\left(\frac{1}{R_{w1}} + \frac{1}{R_{wz1}} + \frac{1}{R_{a1}}\right) & \frac{1}{C_{w1}}\frac{1}{R_{w1}} \\ \frac{1}{C_{w2}}\frac{1}{R_{w1}} & -\frac{1}{C_{w2}}\left(\frac{1}{R_{w1}} + \frac{1}{R_{a2}} + \frac{1}{R_{w2}} + \frac{1}{R_{wz2}}\right) \end{bmatrix},$$

$$\mathbf{G_{pp}} = \begin{bmatrix} \frac{1}{C_{p1}} & 0 \\ 0 & \frac{1}{C_{p2}} \end{bmatrix}.$$

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