

# EE5110/EE6110: Selected Topics in Automation and Control

# Control in Semiconductor Manufacturing

Arthur Tay

# Contact Information

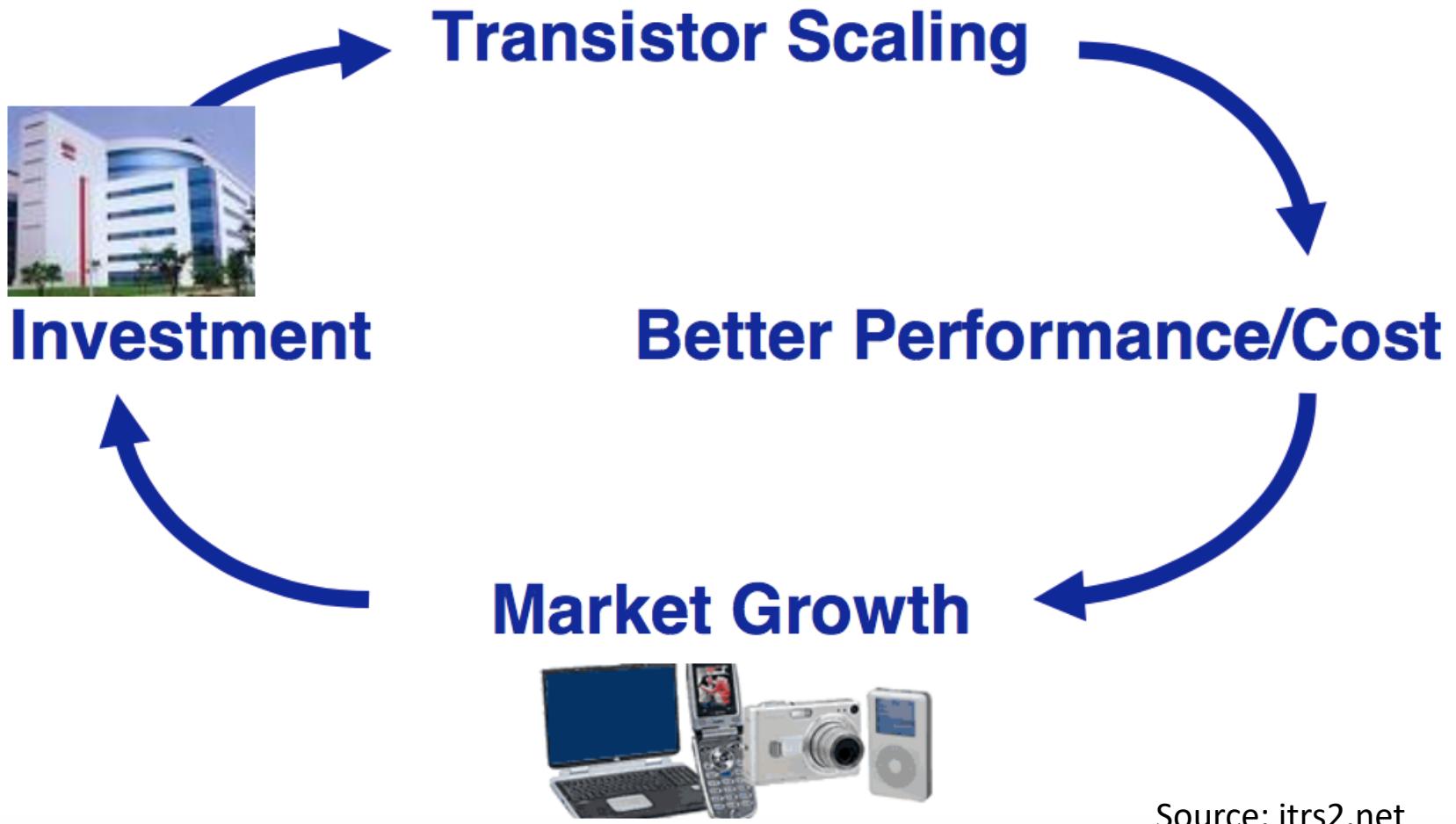
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# Outline

- Introduction to Semiconductor Manufacturing
  - Key steps
  - Current Trends
- Case study 1: RTP – Historical development
- Case study 2: Lithography
- State-Space Modeling & Estimation

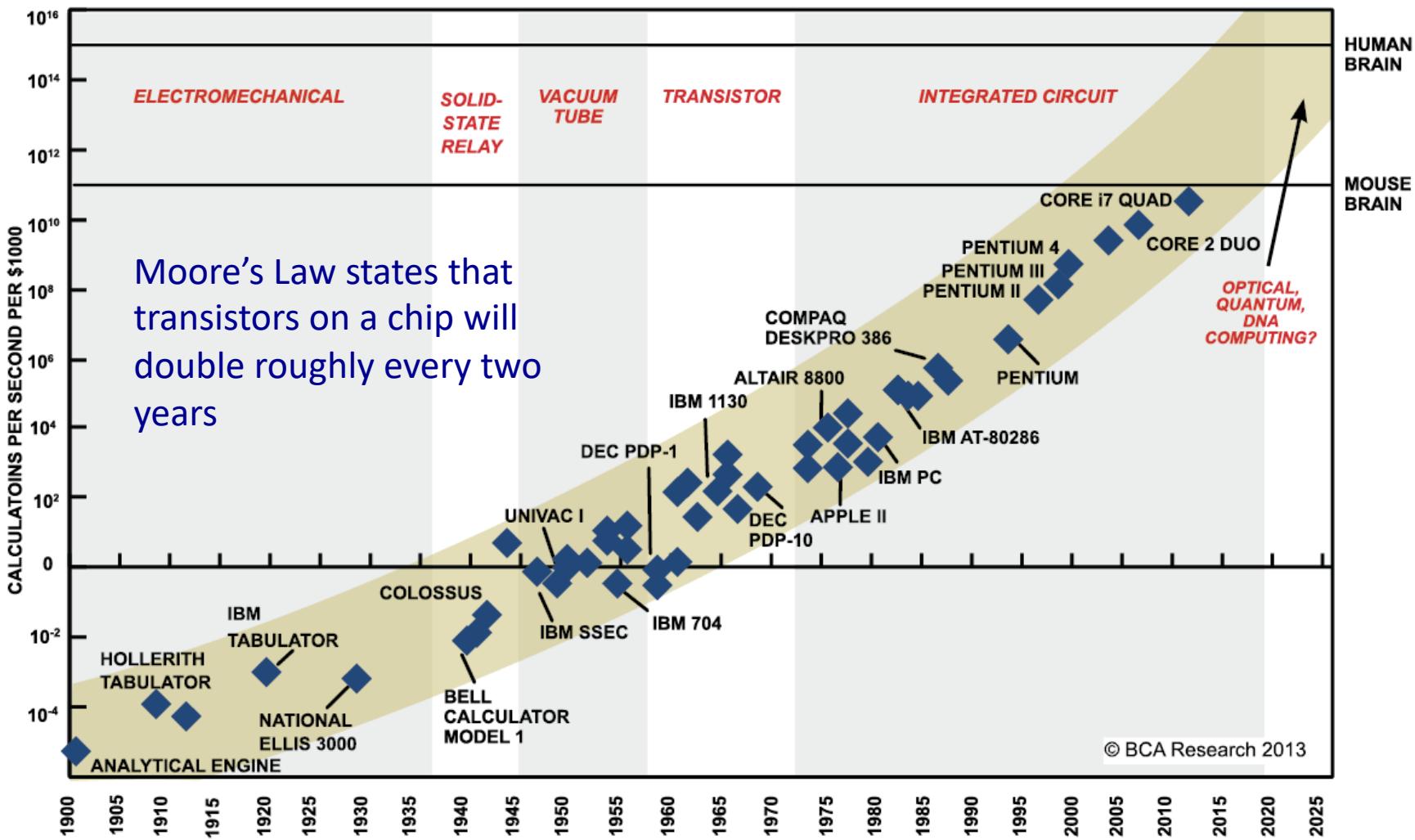
# **INTRODUCTION TO SEMICONDUCTOR MANUFACTURING**

# The Virtuous Cycle of the Semiconductor Industry



Source: itrs2.net

# Moore's Law



SOURCE: RAY KURZWEIL, "THE SINGULARITY IS NEAR: WHEN HUMANS TRANSCEND BIOLOGY", P.67, THE VIKING PRESS, 2006. DATAPOINTS BETWEEN 2000 AND 2012 REPRESENT BCA ESTIMATES.

# Mobile Devices

## Sensors

Accelerometer
Magnetometer
Gyroscope
Ambient Light
Pressure
Touch
Haptic
Fingerprint
Health
Environmental
UV & RGB
Humidity
Microphone



## Applications

Motion Characterization
Contextual Awareness
Health & Fitness
Smart TV Remote
Gestures
Navigation
Biometrics Unlock
Heart Rate
Blood Sugar
CO and Pollutants
Multimedia
Haptic Feedback
Building Floor

# Wearables

## Devices

Accelerometer
Gyroscope
Magnetometer
Pressure
Microphone
Temperature
Conductivity
Camera/Optical Sensor
Micro Speakers
eNose
pH
Humidity
Galvanic Skin Response



## Applications

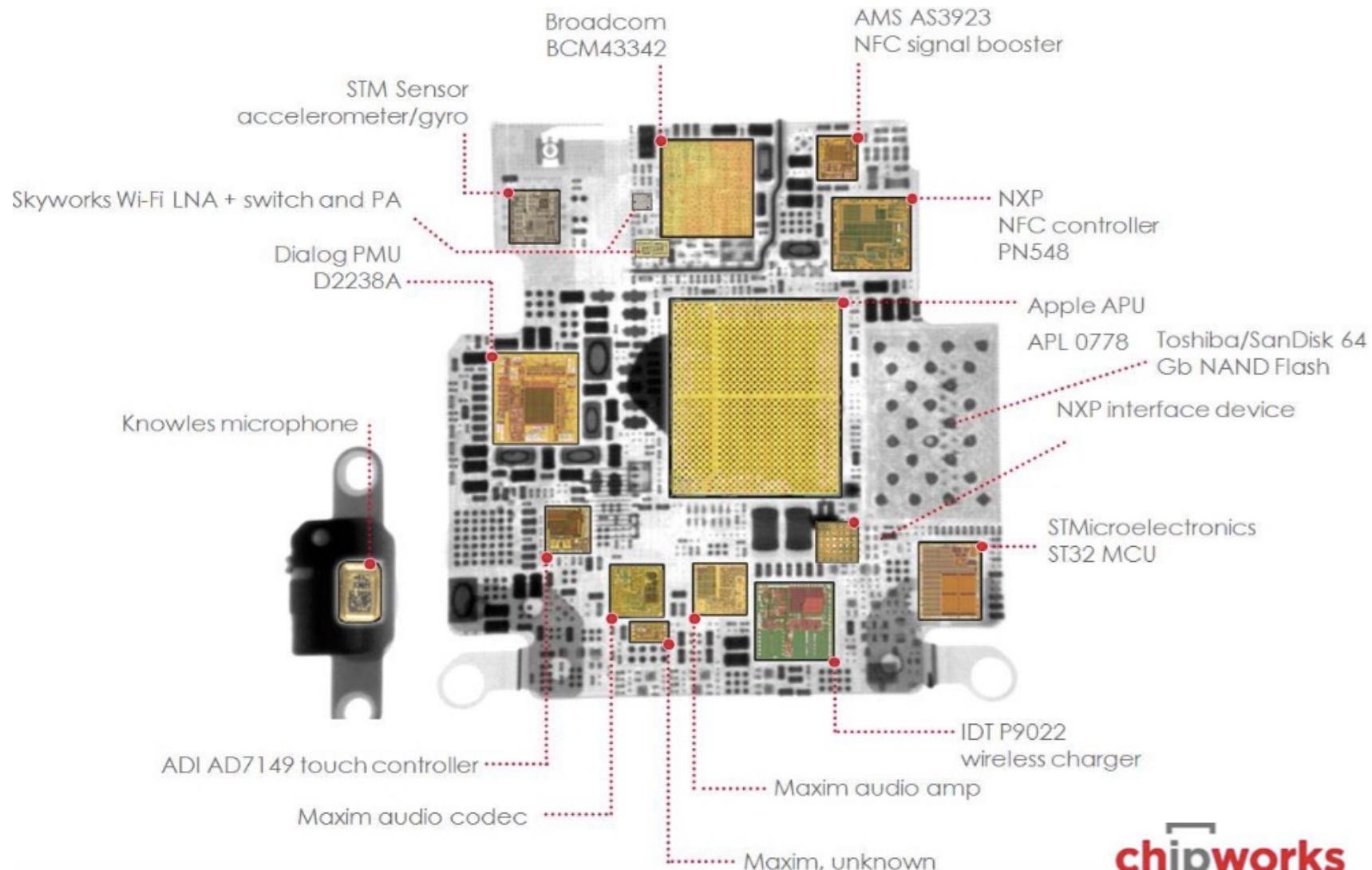
Caloric Consumption
Exercise Intensity
Exercise Safety
Sleep Patterns
Heart Rate
Blood Pressure
Walking Directions
Gas Monitor
Altitude
Motion
Shock
Messaging
Emergency Response

Sources: [itrs2.net](http://itrs2.net)

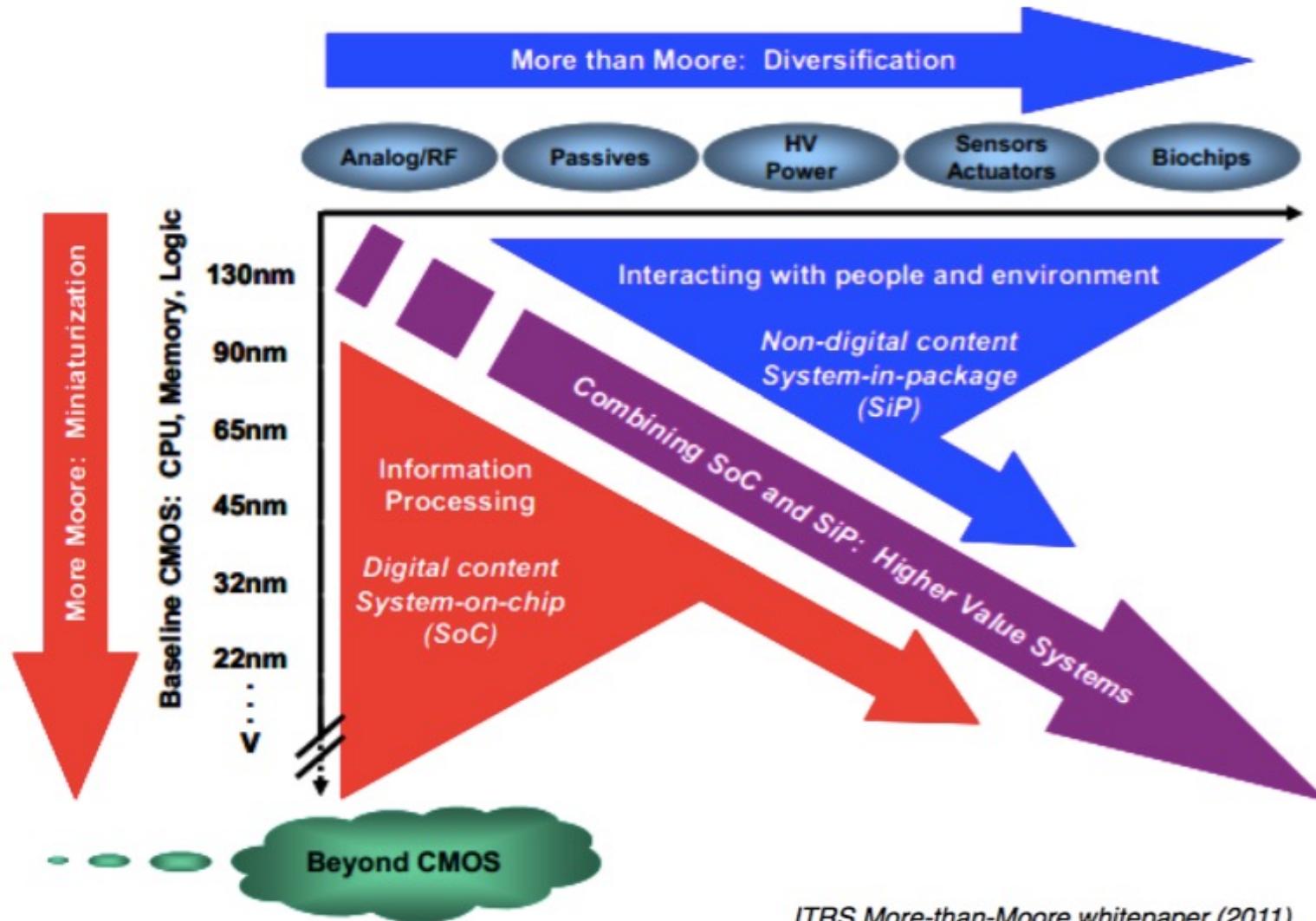
# Key Attributes for Devices differs for Applications

	<b>Automotive</b>	<b>Smart Phone</b>	<b>Wearable</b>	<b>Medical</b>
Inertial Sensors (accelerometers, gyroscopes and IMUs)	Crash Sensors, Inertial Positioning: reliability, accuracy, large ambient temperature range	Tilt, Movement, Inertial Positioning: low cost, low power.	Movement sensor, heart rate – low cost, low power.	Movement, tilt – reliability, low power, FDA approval
Microphones	Hands free communications	Voice, noise cancellation, ultrasonic communications	Voice, heart rate, ultrasonic communications – low cost, low power	Voice, heart rate - reliability, low power, FDA approval
Pressure Sensors	Tire, manifold, altitude, vapor pressure	Altitude, barometric pressure	Blood pressure – low cost, low power	Blood pressure – reliability, low power, FDA approval
Micro Speakers		Sound reproduction – small size, low power	Sound reproduction – small size, low power	
Conductivity			Perspiration	
Humidity			Ambient environmental conditions	
eNose		Environmental and Health monitoring	Environmental and Health monitoring	

# Apple Watch SiP

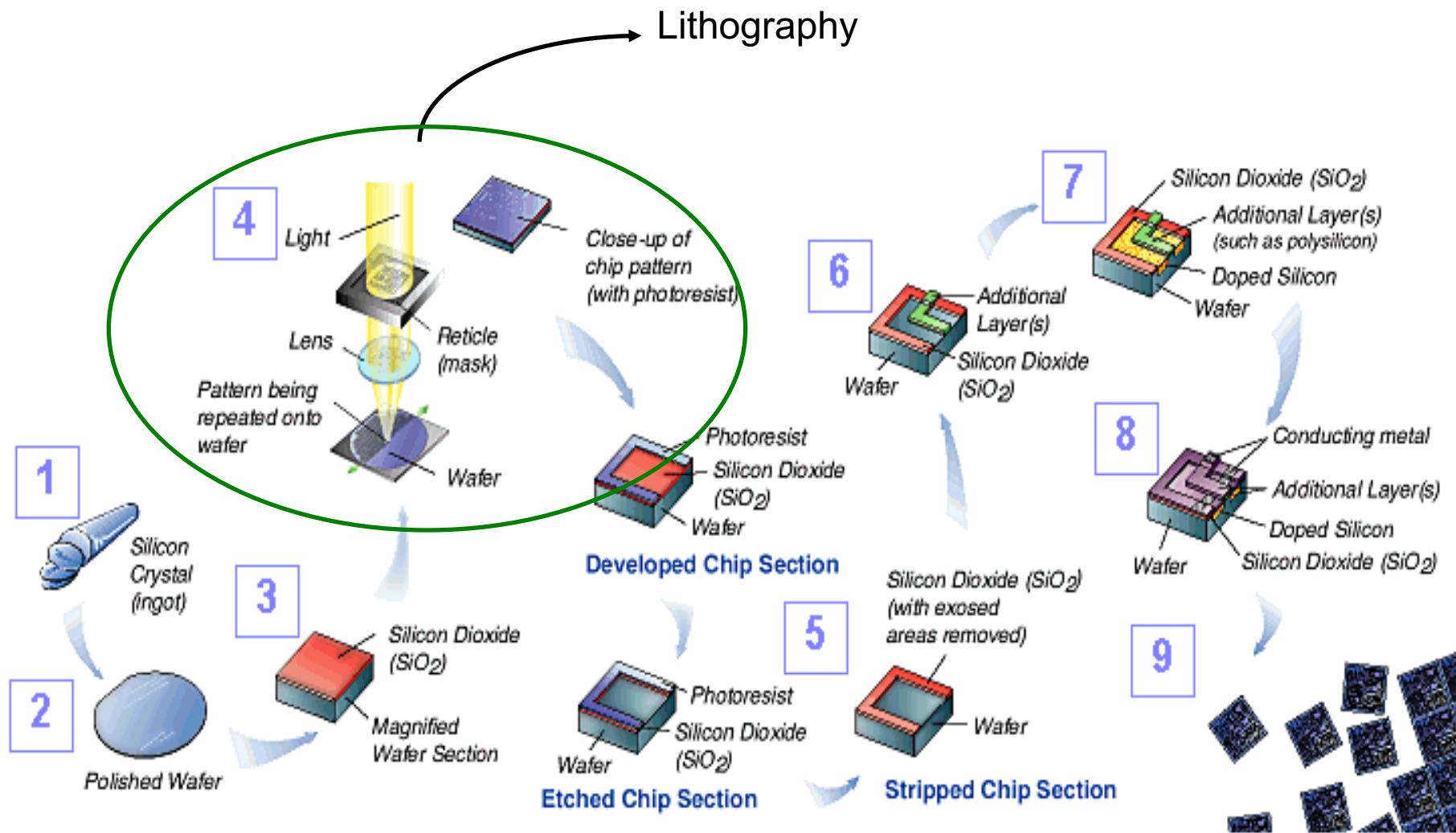


# More than Moore: Functional Diversification



ITRS More-than-Moore whitepaper (2011)

# Semiconductor Manufacturing



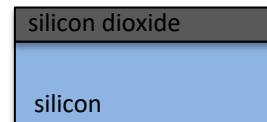
# Key Steps in Semiconductor Manufacturing

- The multiple steps in semiconductor manufacturing all serve to build components with the necessary electrical structure to rapidly switch and transfer signals for computational purposes.
- In addition to the switching transistors and the metal traces that conduct electrical signals between various regions of the chips, insulating materials separate conducting areas of the device.
- These processing steps are further divided into
  - Front-end processes: processes that deal with producing the integrated circuit (IC) on the wafer.
  - Back-end processes: processes deal with wire bonding and packaging the IC.

# Key Steps in Semiconductor Manufacturing

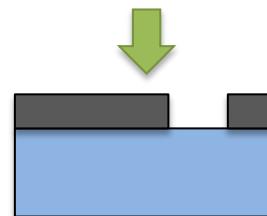
In order to alter the characteristics of the semiconductor, the following steps are undertaken in various sequences depending on the complexity and functionality of the device.

- **Deposition** is the process by which an insulating layer is grown on the silicon substrate.
- Photolithography is critical, it helps patterned areas of the chip with an image for that particular layer of the device. In photolithography, a very precise “mask” is used to expose photoresist that has been applied across the wafer, much like emulsion on film. This pattern hardens into an exact representation of the mask when it is developed.
- Etching then removes selective areas of the pattern using a plasma that reacts to the material not covered by the hardened photoresist.



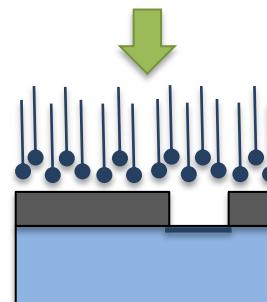
Oxide Deposition

Oxidation at high temperature or thermal CVD, PECVD, etc.



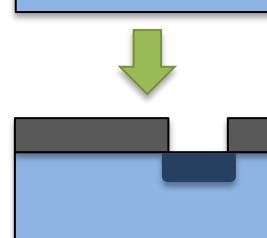
Pattern/Etch

Complicated step, involves photoresist spin-on, photolithography, photoresist development, dielectric etch (plasma), and photoresist removal.



Implant

Uniform deposition of dopant (e.g. As, P, B etc.) using ion implantation. Embeds atoms in thin surface layer of exposed Si.



Diffusion

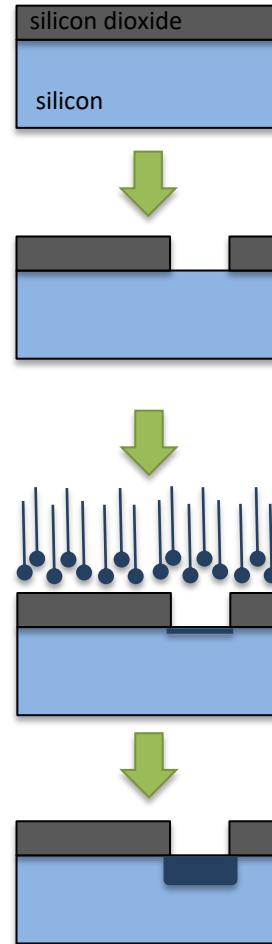
Implant anneal and dopant diffusion. Thermal process (e.g. RTP)

# Key Steps in Semiconductor Manufacturing

- Diffusion bakes impurities into areas of the wafer to alter its electrical characteristics.
- Ion implantation is another process for infusing the silicon with various dopants to change its electrical characteristics.
- Chemical Mechanical Polishing (CMP) is used to produce a planar wafer surface for subsequent processing.



- In a typical IC, there can be hundreds of these processing steps.



## Oxide Deposition

Oxidation at high temperature or thermal CVD, PECVD, etc.

## Pattern/Etch

Complicated step, involves photoresist spin-on, photolithography, photoresist development, dielectric etch (plasma), and photoresist removal.

## Implant

Uniform deposition of dopant (e.g. As, P, B etc.) using ion implantation. Embeds atoms in thin surface layer of exposed Si.

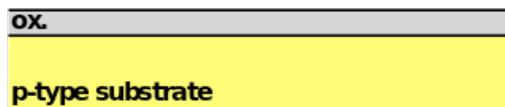
## Diffusion

Implant anneal and dopant diffusion. Thermal process (e.g. RTP)

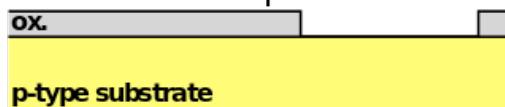
*For a more detailed descriptions of these processing steps, refer to any Silicon Processing Technology book.*

# Simplified CMOS Fabrication Steps

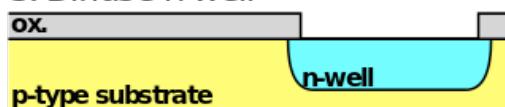
1. Grow field oxide



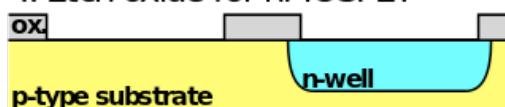
2. Etch oxide for pMOSFET



3. Diffuse n-well



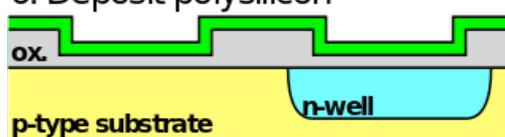
4. Etch oxide for nMOSFET



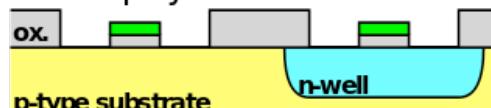
5. Grow gate oxide



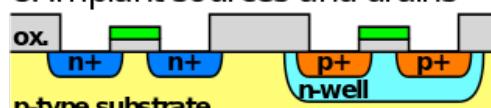
6. Deposit polysilicon



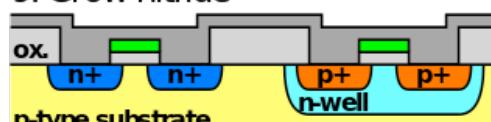
7. Etch polysilicon and oxide



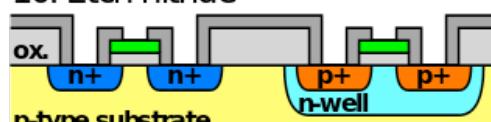
8. Implant sources and drains



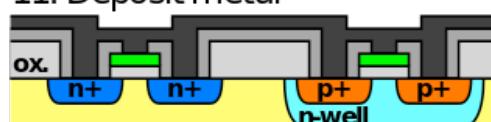
9. Grow nitride



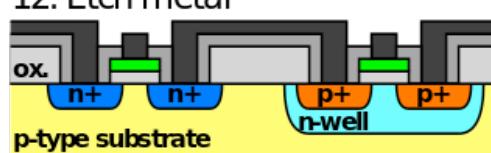
10. Etch nitride



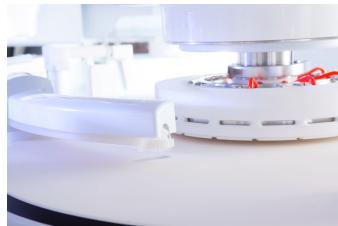
11. Deposit metal



12. Etch metal



# The Key Industrial Players



TOKYO ELECTRON



**ASML**



# Control of Semiconductor Manufacturing

- Control is ubiquitous in semiconductor manufacturing, for examples:
  - Silicon making: control of melt temperature, rotation speed and pull rate
  - Silicon slicing: control of thickness and removal rate
  - Deposition: control of plasma, pressure, flow, composition and thickness
  - Lithography: control of wafer stage with nm accuracy; control of temperature, thickness, uniformity
  - Ion Implantation: control of plasma
  - CMP: control of film thickness, uniformity and removal rate
- Robotics (wafer handling) and Automation is omnipresent in the fab

# Typical Process Metrics and Input Settings

Table: Typical process metrics, input settings, and intermediate process variables for semiconductor fabrication process

	Process Metrics	Intermediate Variables	Input Settings
Etching (Plasma and RIE)	etch rate etch anisotropy etch uniformity etch selectivity	dc bias gas species concentration pressure temperature	rf power throttle position gas flow
PECVD	Deposition rate Film stress Film uniformity Film purity	dc bias gas species concentration pressure temperature	rf power throttle position gas flow
Photolithography - Spin coat and bake step - Exposure step - Develop step	photoresist thickness photoactive concentration (PAC) exposed PAC pattern line width		spinning speed baking temperature exposure dose
Chemical Mechanical Polishing (CMP)	Removal rate uniformity		spinning speed pressure force

# History of Semiconductor Manufacturing

- Much attention has been focused on coordinating the schedules of different unit operations, controlling the purity of the required reactants, and monitoring the transfer of wafers between machines.
- Relatively less effort has been devoted to improving the control of individual unit operations.
- Traditionally, the approaches to meeting such demands is heavily based on empirical and heuristic techniques with relatively little understanding of the underlying physics and chemistry; based on a combination of ingenuity and experience.
- As processing specifications become tighter and higher performance is demanded from the equipment, this lack of understanding becomes a significant problem.
- These systems consists mainly of PI (proportional, integral) controllers executing fixed process recipes without feedback of important process outputs.
- The main control strategy is [Statistical Process Control \(SPC\)](#) where the process output is monitored (usually ex-situ) in order to detect an “out-of-control” process.

# Metrology in Semiconductor Manufacturing

**300 mm wafer**

**10 nm** →



**Scatter 100 coins**

**Find in 1 hour**



## Optical Inspection

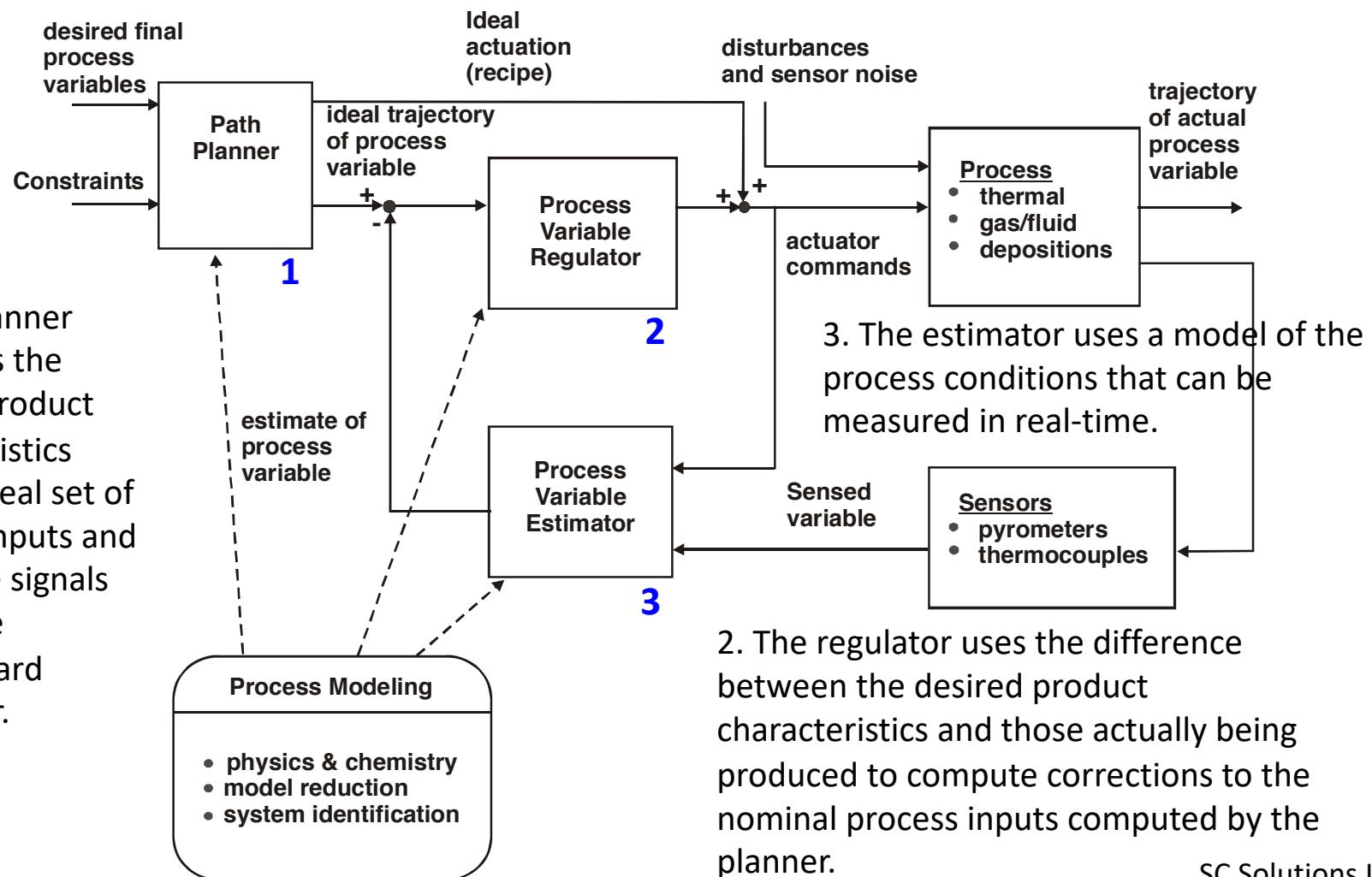
Samples all ~17 trillion pixels in this area and finds the coins in about an hour

Source: **KLA Tencor**

# Limitations in Metrology

- While SPC has been adopted in most wafer fabrication facilities, automatic process control has not been implemented on a large scale, due to the following reasons (Edgar et al.):
  - In-situ measurements of important process variables are rarely available.
  - Process understanding is so poor that it is often difficult to determine which variables should be included in a control scheme.
  - Post-process measurements are seldom used to automatically adjust process recipes.
  - Product specifications are extremely tight, pushing the limits of measurement technology.
  - Processing mistakes cannot be blended away; a processing error can destroy an entire batch of wafers with no hope of recovering the product through further processing.
  - Equipment software is inflexible and does not permit user-specified control strategies.

# General Control Structure for Semiconductor Manufacturing

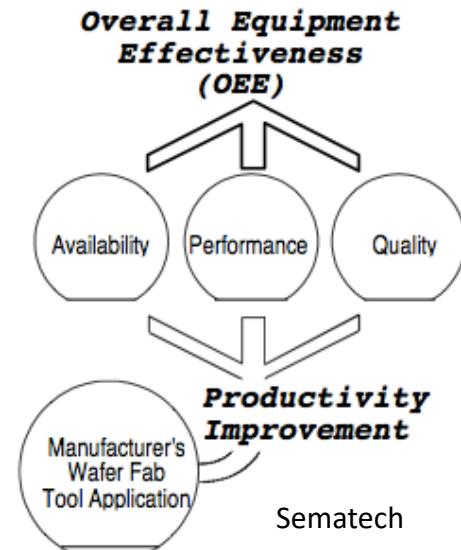


# Control Strategies

- **Feedforward control:** determine appropriate inputs to move a system from one operating point to another.
- **End-point control:** uses an in-situ sensor to detect the end-point of the process.
- **Real-time control:** feedback control with real-time sensors. Focus mainly on the equipment, real-time control of process is limited.
- **Run-to-run control:** a form of discrete process control in which a product recipe is modified using in-line or ex-situ metrology between “runs” to minimize or eliminate process drifts, and variability. It is a supervisory controller for the setpoints and settings for the regulatory controller. This supervisory controller is usually a fab level controller, part of the computer-integrated manufacturing (CIM) system.

# Process Monitoring, Fault Detection and Diagnosis

- Motivations:
  - Overall equipment effectiveness (OEE): < 50% in a wafer fab.
  - Scrap costs of \$0.5 - \$1.5 million/month in an average fab, and typical downtime costs of \$10,000 - \$100,000/instance.
  - Important to understand the effects of ageing, cleaning, and maintenance cycles on process tool performance.
- Emerging equipment monitoring and fault detection technologies: provide fabs to track key signals critical to each process step.
- Process monitoring: data are processed to extract control limits, mean, variance and plotted on SPC charts.
- Typical techniques for fault detection/diagnosis includes: neural networks, principal component analysis, expert systems, etc.

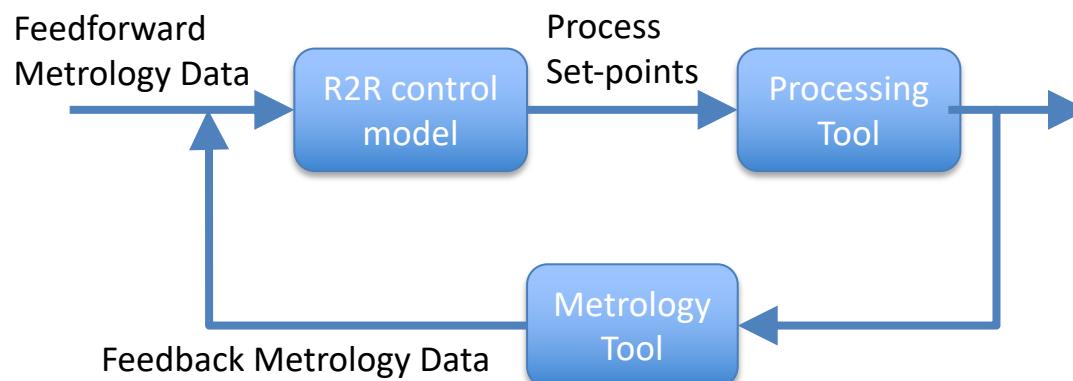


# Run-to-run control

- Monitoring and control of critical wafer parameters was performed outside the processing chamber in a non real-time fashion because
  - Poor process understanding
  - Lack of appropriate sensors and measurement techniques
- Once the critical wafer parameters are measured, it is used to update the parameters of a model (typically static), which relates a set of input variables (or recipes) to the critical wafer parameters.
- The updated model is then used to generate a suitable recipe correction, corresponding to the desired wafer parameters.
- This static model is usually obtained via a Design-of-Experiments (DoE) to determine the appropriate process variables, those that have the largest influence on the system outputs.

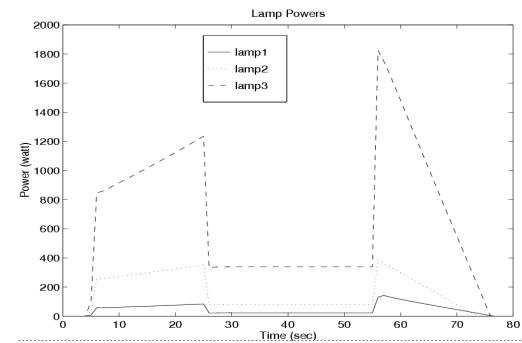
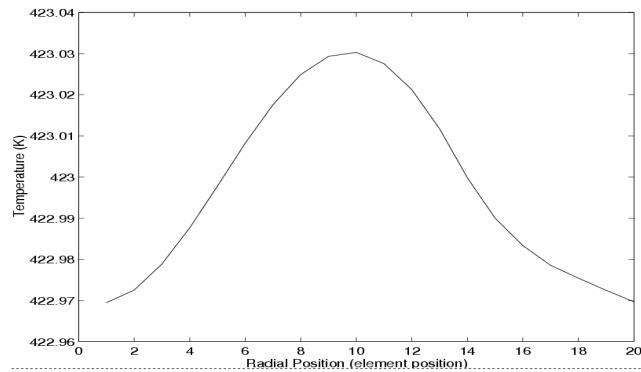
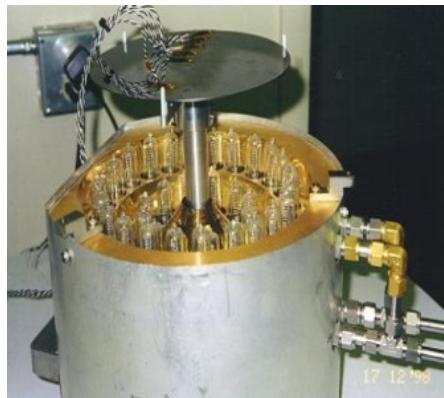
# Run-to-run control

- Automatic change in the process recipe for a given run based on feedback data from post-process metrology and feedforward data from previous operations.
- A Linear Regression model:  $y = Ax + c$ 
  - $x$  and  $y$  are the input and output vectors,
  - $A$  is a matrix containing the model parameters. Occasional shifts due to material variations and scheduled maintenance operations can be captured by  $A$
  - $c$  is a constant term (used to model slow process drift). Exponentially weighted moving average (EWMA) adaptation can be used to adjust  $c$



# Real-time Equipment Control: Main Issues

- What are the processes involved (physics)?
- What are the **actuators** (inputs)?
- What **sensors** are available (outputs)?
- What are the performance metrics?
- What are the disturbances and uncertainties?



# Journals & Conferences

## Key Journals

- IEEE Trans. on Semiconductor Manufacturing
- SPIE Journal on Micro/Nanolithography, MEMS, and MOEMS

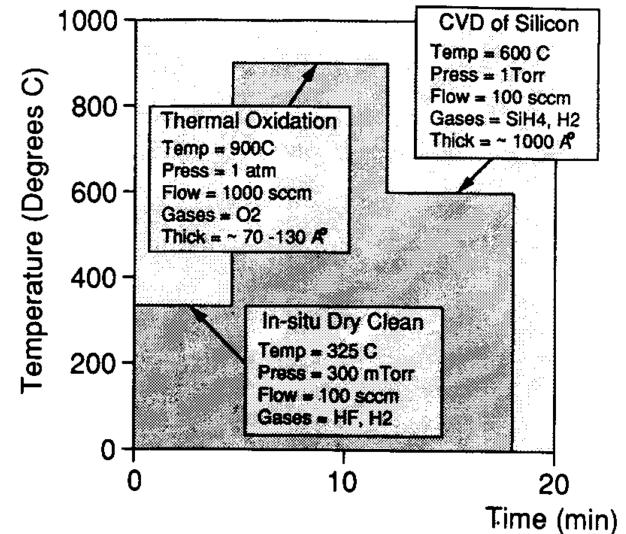
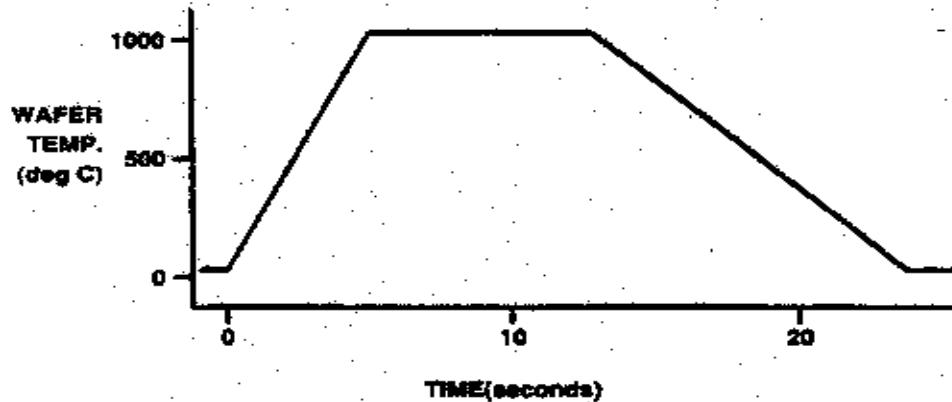
## Key Conferences

- Annual Advanced Process Control & Manufacturing conferences (EU, USA and Asia)
- International Symposium on Semiconductor Manufacturing
- SPIE Advanced Lithography & related SPIE conferences
- AIChE Annual meetings

# **CASE STUDY: RAPID THERMAL PROCESSING**

# The RTP Temperature Control Problem

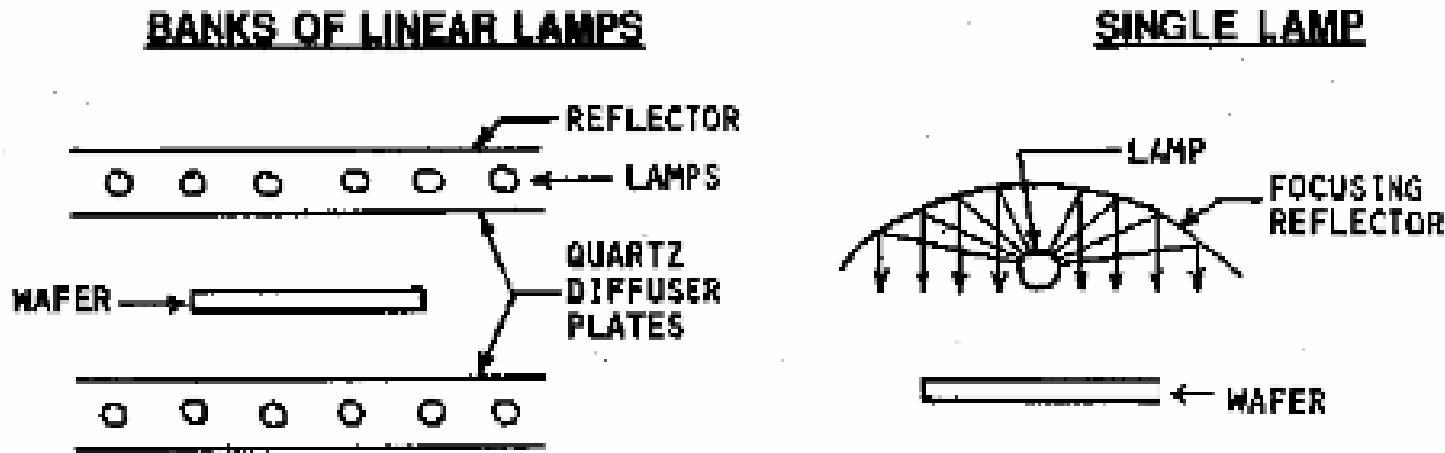
- A Typical RTP Temperature Trajectory



- Requirements:
  - Fast ramp-up and cool-down
    - High throughput
    - Minimal dopant diffusion
  - Precise trajectory following for process repeatability
  - Near-uniform temperature across wafer at all times
    - Uniform processing
    - No damage from thermal stress

# Historical Development

- Commonly used lamp in RTP



- Back to early 90's
  - Several small companies produced systems, each using different heat-lamp configurations and SISO control algorithms to try to achieve what the **conventional wisdom decreed – uniform heat flux over the wafer, over the entire thermal cycle.**
  - The approach was **largely empirical**, based on trial and error to tweak the control parameters. **It was not untypical of the industry at the time.**

# Historical Development

- The MMST project:
  - \$150M over 4 years from the Air Force to Texas Instruments to validate the feasibility of a new paradigm for semiconductor manufacturing
  - Final demonstration (May, 1993): 1000 wafer marathon run of two 0.35 micron CMOS process technologies in a 100% single wafer processing factory

(1/90 – 8/90)

**Modeling of heat transfer for RTP  
Optimization and simulation of performance limits  
Comparison of multizone lamp configurations**

(9/90 – 5/91)

**Development and simulation of controllers**

(6/91 – 3/92)

**Experimental demonstration on Stanford RTM**

(4/92 – 12/92)

**Transfer and customization on 8 RTPs,  
13 different processes at TI**

(1/93 – 5/93)

**Usage for 1,000 wafer MMST marathon demo**

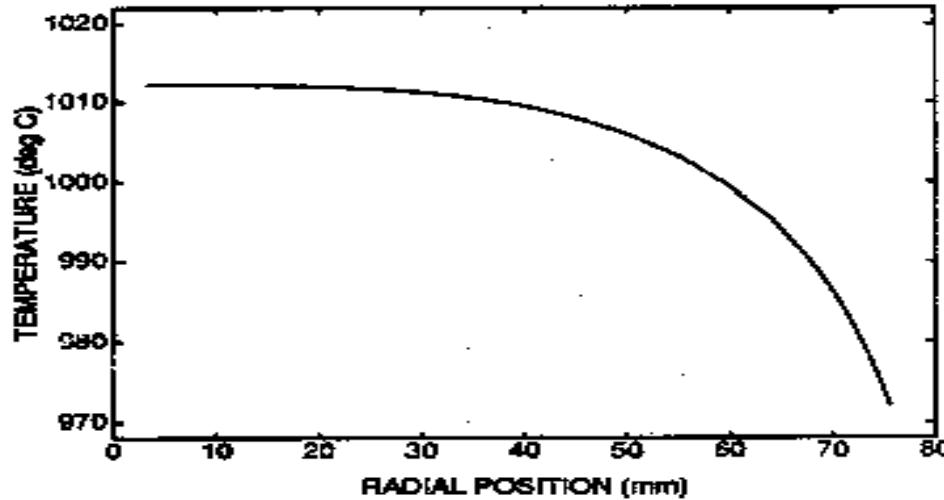
# The Systems Approach

- The first step is to abstract and simplify a real-world problem so that one can make a mathematical model for the problem: in automatic tracking and control, VLSI design, diverse problems in semiconductor manufacturing, and many others.
- Secondly, one uses, and sometimes develops *ab initio*, a variety of often surprisingly advanced mathematical tools to solve the idealized problems.
- The final step is to gain a sufficiently physical and intuitive understanding of the mathematical solution that one can translate it into a “practical” solution of the original physical problem. The word “practical” of course has many aspects, from technical feasibility to economic viability.

The first step was to conclude from analysis of simple models that the **conventional wisdom was wrong**. We need **non-uniform** heat flux over the wafer. Moreover **multivariable** control is essential.

# Uniform Illumination for Uniform Temperature?

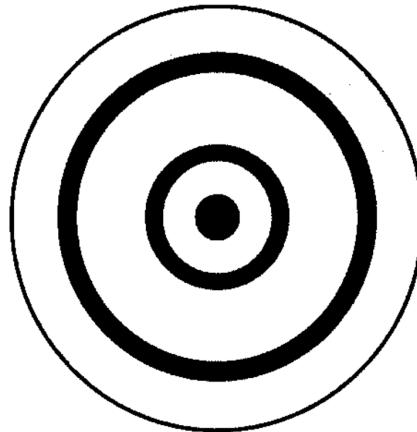
- Early RTP lamp designs attempted to ensure uniform illumination of the top surface of the wafer.
- Typical temperature profile at steady-state:



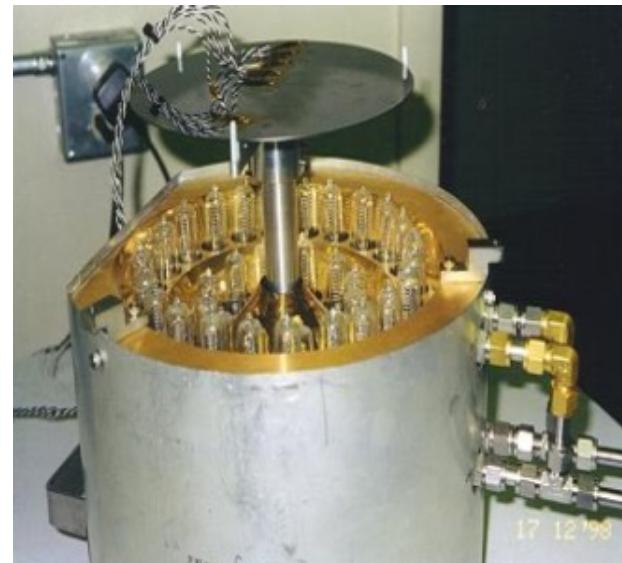
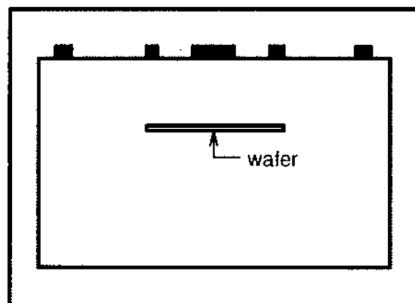
- Temperature is nonuniform because:
  - Radiative and convective losses at the edge setup a temperature gradient;
  - Convective loss coefficients tend to be higher nearer the wafer edge

# The new Lamp design

CHAMBER CEILING  
(VIEW FROM WAFER,  
LAMP ZONES IN BLACK):



CHAMBER CROSS-SECTION:



# The Control Problem

- The model based on energy balance:

$$q = Cm\dot{T} = -\mathbf{A}_{\text{rad}}T^4 - \mathbf{A}_{\text{conv}}(T - T_a) - \mathbf{A}_{\text{cond}}T + \mathbf{B}P$$

- Consider the problem of designing the lamp power settings,  $\mathbf{P}(t)$ , so that the entire wafer closely tracks a reference trajectory  $T^{\text{ref}}(t)$  over the entire thermal cycle.

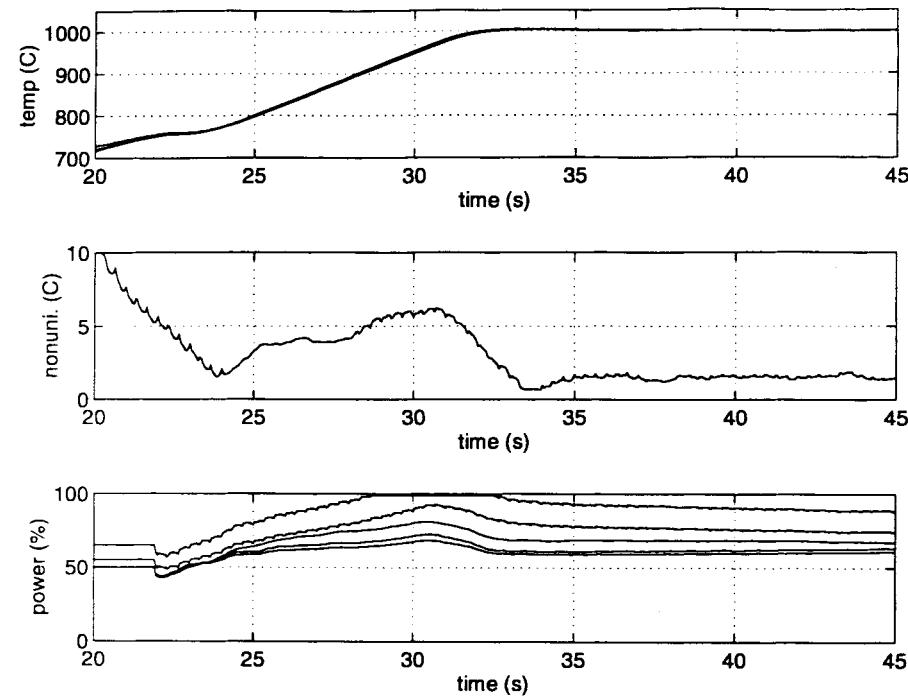
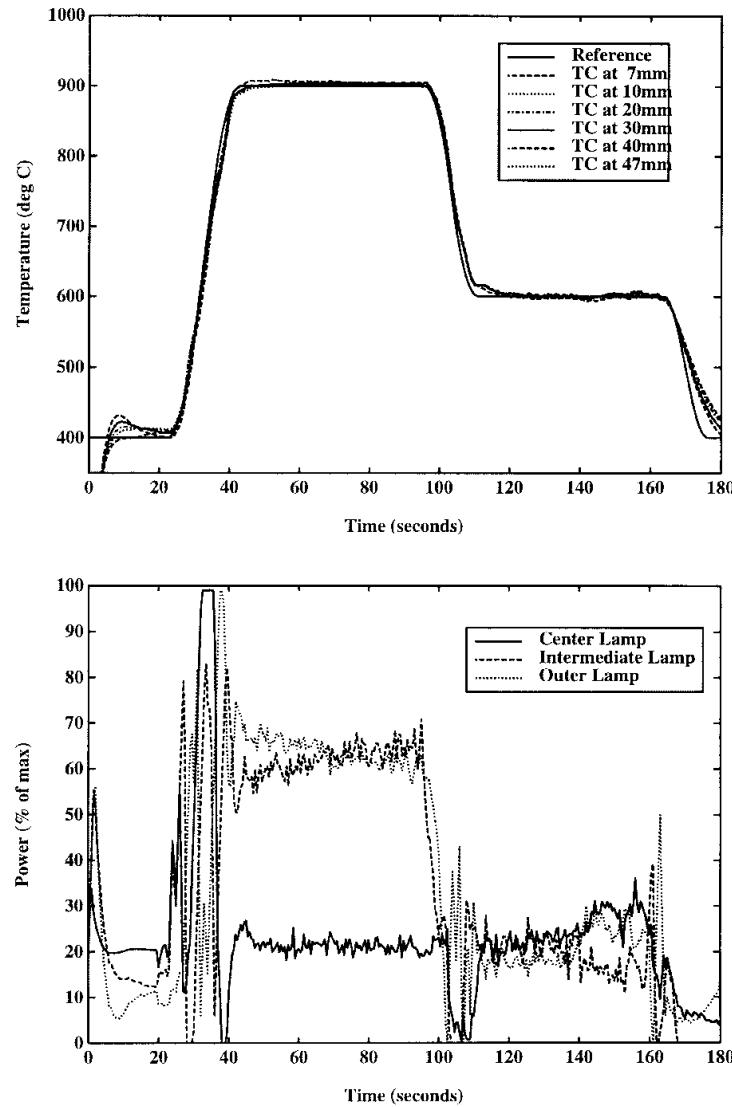
Given  $T_0$ , find  $\mathbf{P}_0, \mathbf{P}_1, \dots, \mathbf{P}_{N-1}$  to minimize

$$\max_{n=1, 2, \dots, N} \|\mathbf{T}_n - \mathbf{T}_n^{\text{ref}}\|_\infty$$

subject to, for  $n = 0, 1, \dots, N - 1$ ,

$$\mathbf{P}^{\min} \leq \mathbf{P}_n \leq \mathbf{P}^{\max}.$$

# Typical closed-loop control Temperature Profiles



# Current State-of-Art Systems

- Applied Materials VANTAGE system.
  - honeycomb lamp source,
  - seven-point temperature measurement,
  - 100 Hz closed-loop control, and
  - 240 rpm wafer rotation.

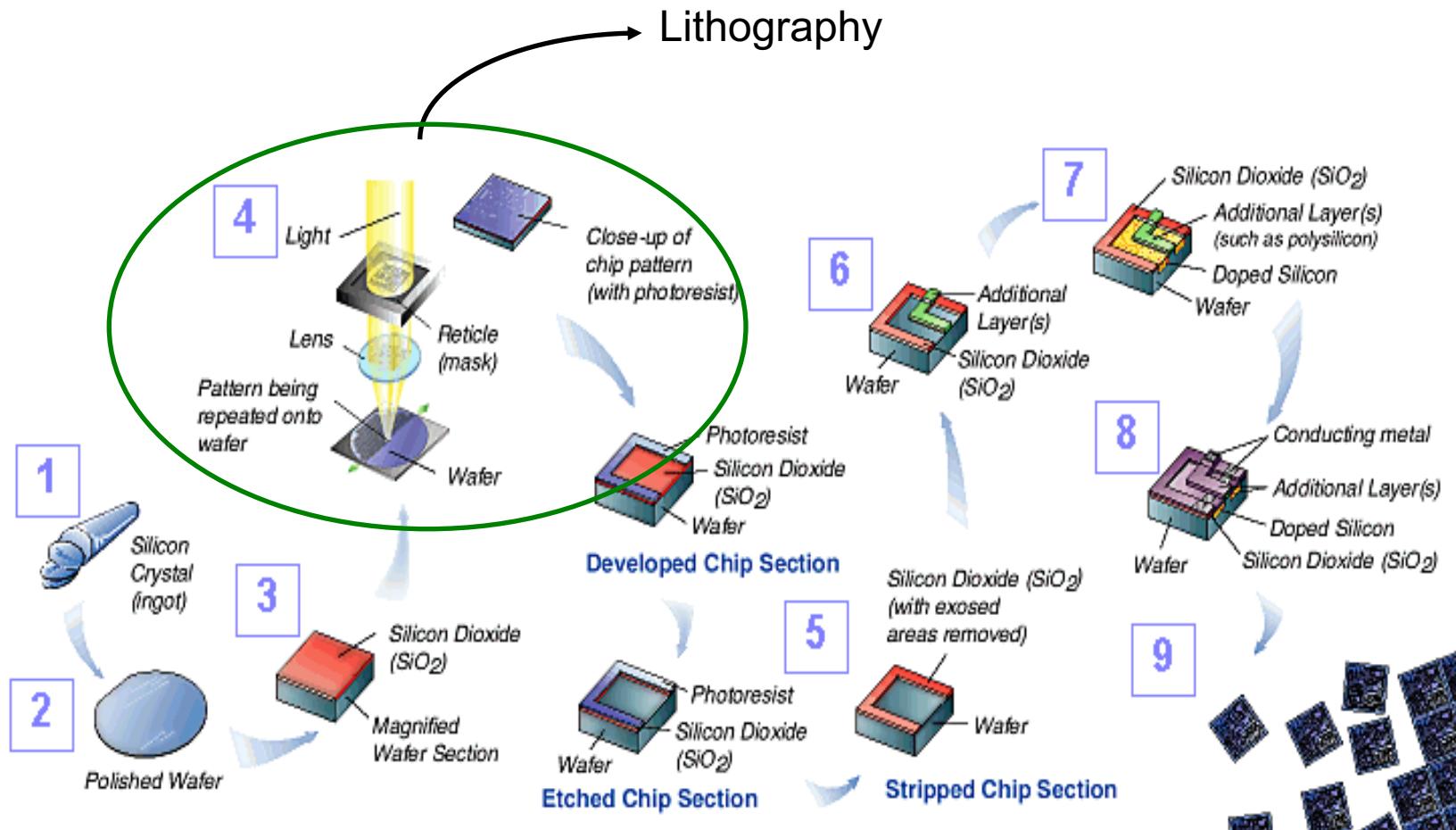


# **CASE STUDY: LITHOGRAPHY**

# What is Lithography?

- A manufacturing process for producing highly accurate, microscopic, two-dimensional patterns in a photosensitive resist material.
- These patterns are replicas of a master pattern on a durable photomask, typically made of a thin patterned layer of chromium on a transparent glass plate (reticle).
- The most common variation is by optically imaging a mask onto the wafer surface using a resist that is a radiation sensitive polymer. The resist is then developed to bring out the latent image of the mask – optical lithography.
- Largest capital investment and largest operating cost component of leading edge semiconductor fabs accounting for about 35% of the manufacturing cost. Estimated that Lithography equipment will cost about 27M euros for a 300mm 22nm Immersion system.

# Semiconductor Manufacturing Process



Source: Sematech, Inc.

# Optical Lithography

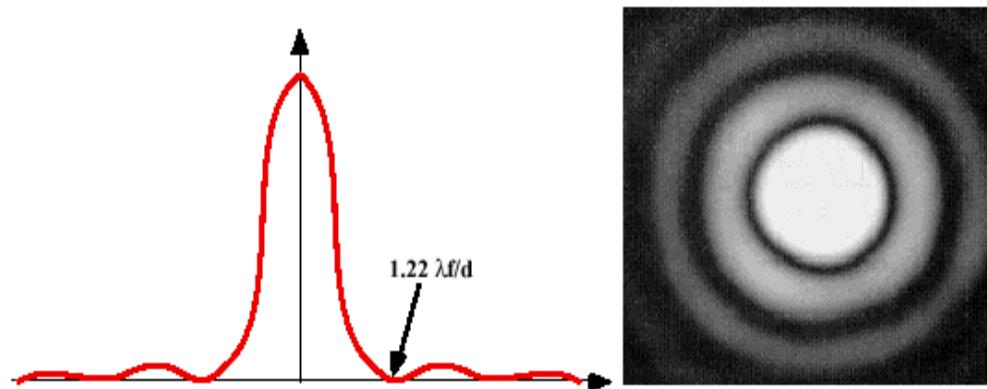
## Wafer Exposure Systems

- A basic understanding of optics is important in the study of modern wafer exposure system. The interested reader is referred to the following standard texts for more detailed treatment:
  1. Goodman, “Introduction to Fourier Optics”, QC355 Goo
  2. Born & Wolf, “Principles of Optics”, QC355.2 Bor
- Light travels as an electromagnetic wave through space. Two basic concepts: Geometrical optics and Fourier Optics.
- Geometrical optics:
  1. treats light as non-interacting particles, so ray-tracing may be used to determine the operation of the optical system,
  2. provides valuable information about imaging,
  3. true only when all of the dimensions of interest of the optical system are very large compared to the wavelength of light (e.g. light source and lens); when the dimensions of interest is comparable to the wavelength of light (e.g. features on mask), the wave nature of light has to be considered.

# Optical Lithography

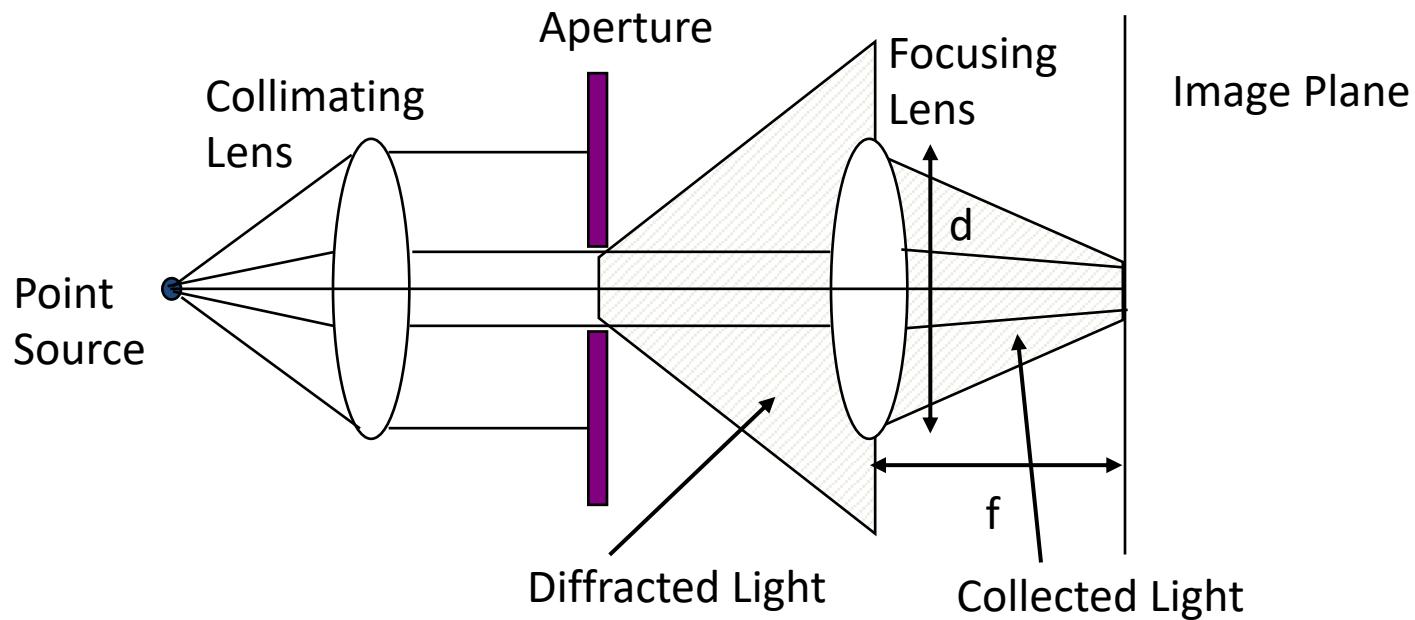
## Wafer Exposure Systems

- Fourier optics allow a more complete study of imaging, in which effects such as diffraction and interference can be studied.
- *Diffraction* can be thought of simply as the “bending” of light when it passes through an aperture. It is responsible for image creation in all optical situations.
- Classical example: Airy’s disk, as the image plane is move further away from the obstacle, there is a region in which the geometrical shadow is still recognizable. Beyond this region, far from the obstacle, the intensity pattern no longer resembles the geometrical shadow but contains regions of dark and light fringes.



# Optical Lithography

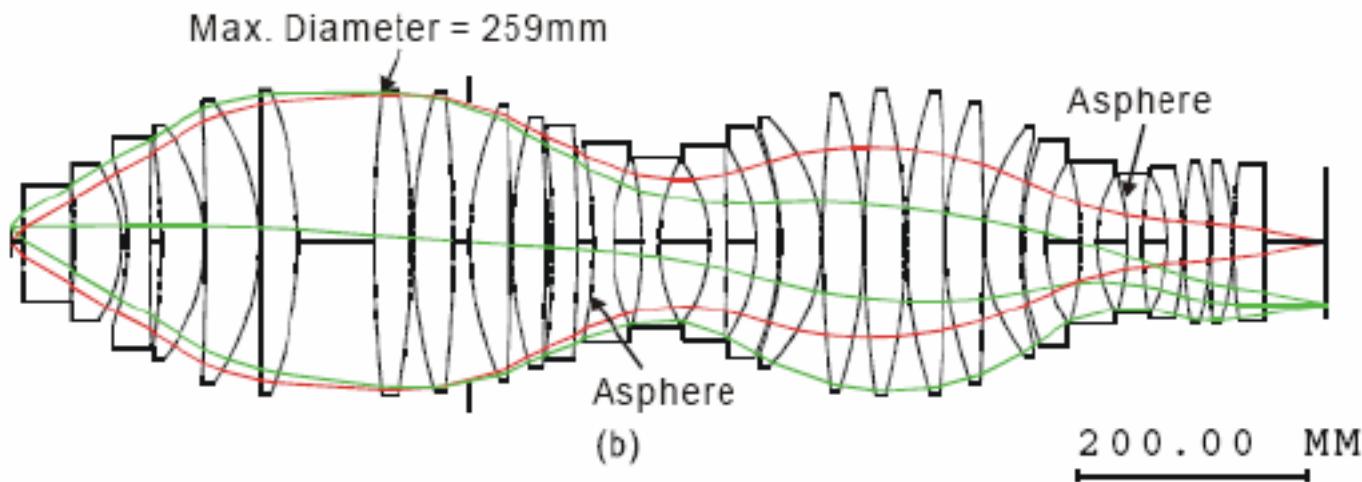
- Problem: Due to finite size, the focusing lens collects only part of the total diffracted pattern associated with the light passing through the aperture. The finer details of the aperture are diffracted at a larger angle and hence not captured by the focusing lens.
- Two limiting cases of diffraction: *Fresnel* diffraction (Near-field), *Fraunhofer* diffraction (Far-field).



# Optical Lithography

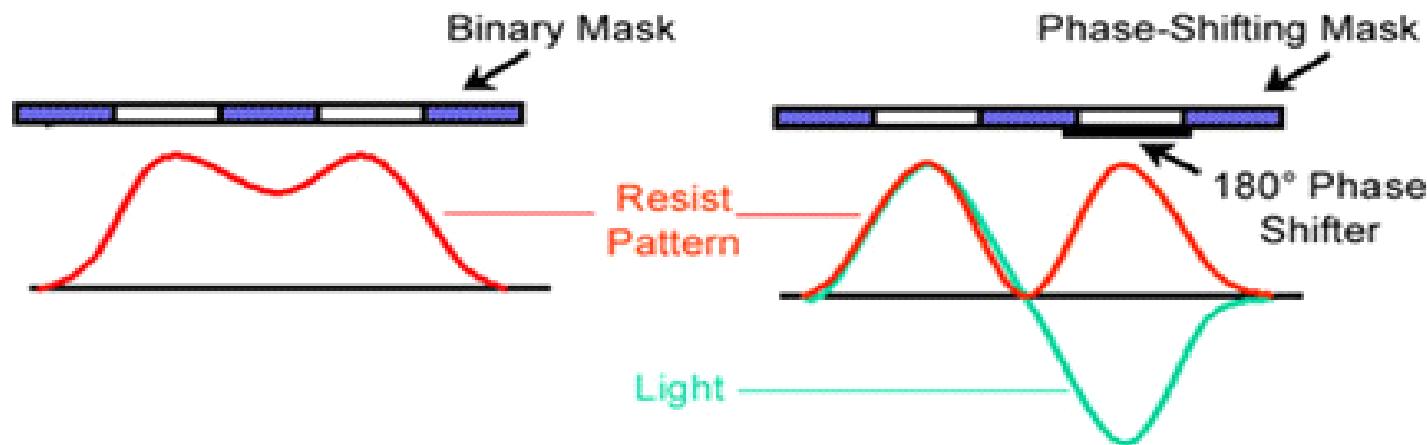
- Feature size limited by diffraction effects
- Rayleigh limits:

$$\text{Resolution, } R = k_1 \frac{\lambda}{NA}$$



# Resolution Enhancement Techniques

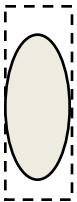
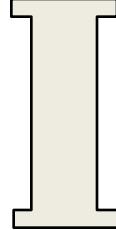
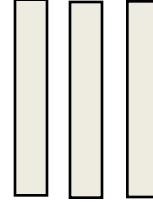
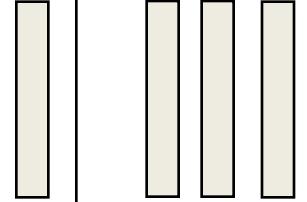
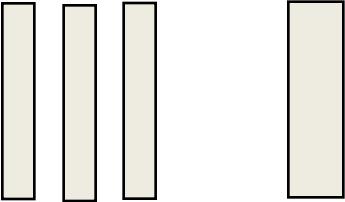
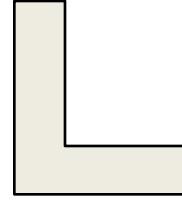
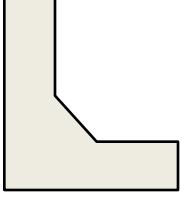
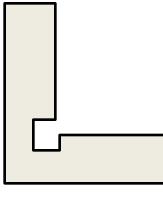
## Phase Shifting Mask



NASDAQ listed startup company: Numerical Technologies, later acquired by Synopsis

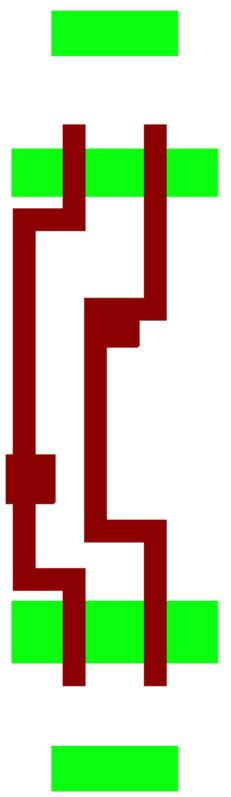
# Resolution Enhancement Techniques

## Optical Proximity Correction

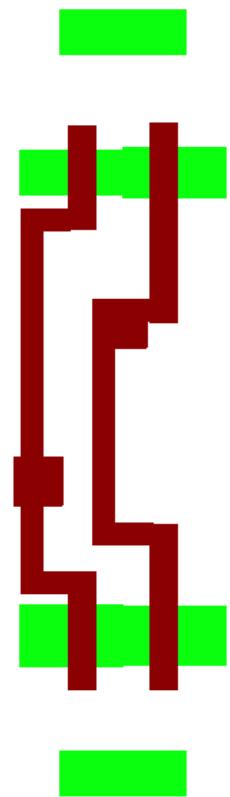
	Mask	Wafer	OPC corrected mask
Line end shortening			
Nested/iso bias			
Corner rounding			

# Optical Proximity Correction

- NAND gate



■ Design layout

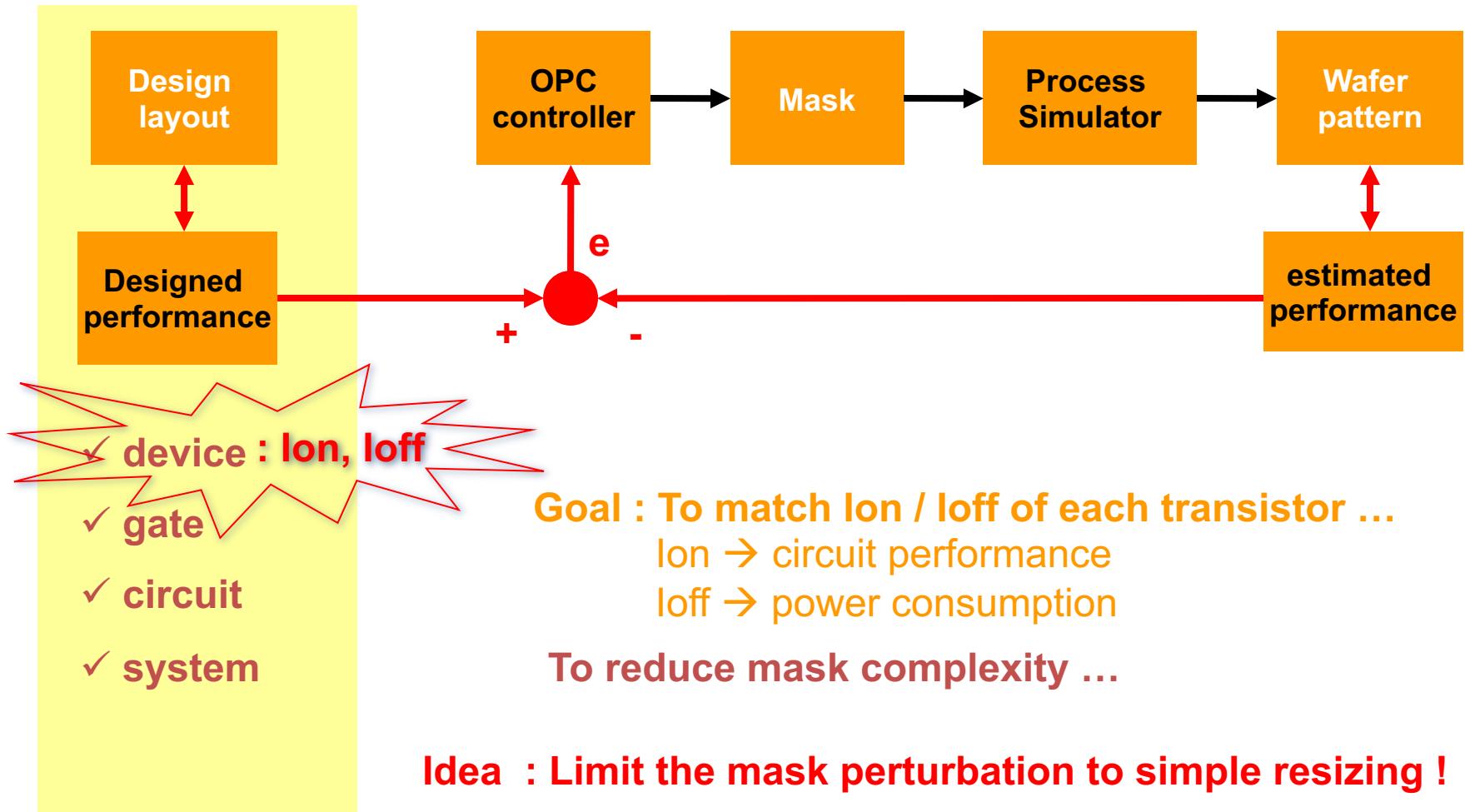


■ DPB-OPC mask



■ EPE-OPC mask

# Feedback Control Approach



# Simulation Results

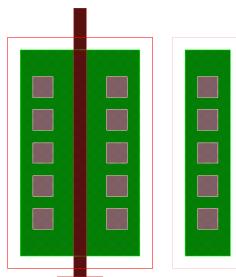
## ■ Single N-channel MOS transistor

Controlled output	Mask	Performance deviation error (%)				MEBES size for 1000 by 1000 array of single NMOS (Bytes)		OPC runtime (s)
		$I_{on}$	$I_{off}$	$L_{eq,Ion}$	$L_{eq,Off}$	Poly mask	Diff mask	
$I_{on}$	EPE-OPC	-0.05	29.24	0.05	-1.81	13740032	26632192	4.44
	DPB-OPC	0.02	-1.04	-0.02	0.08	10127360	13957120	54.09
	Improvement $ DPB / EPE -1$ (%)	-56.0	-96.4	-60.0	-95.6	-26.3	-47.6	1118.2

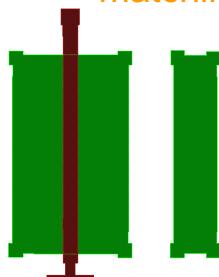
> 50 %      > 26%

✓ Closer performance matching to design value

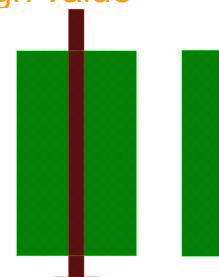
- ✓ Simpler mask
- ✓ Simpler fabrication process
- ✓ Shorter mask writing / inspection time



(a) Design layout



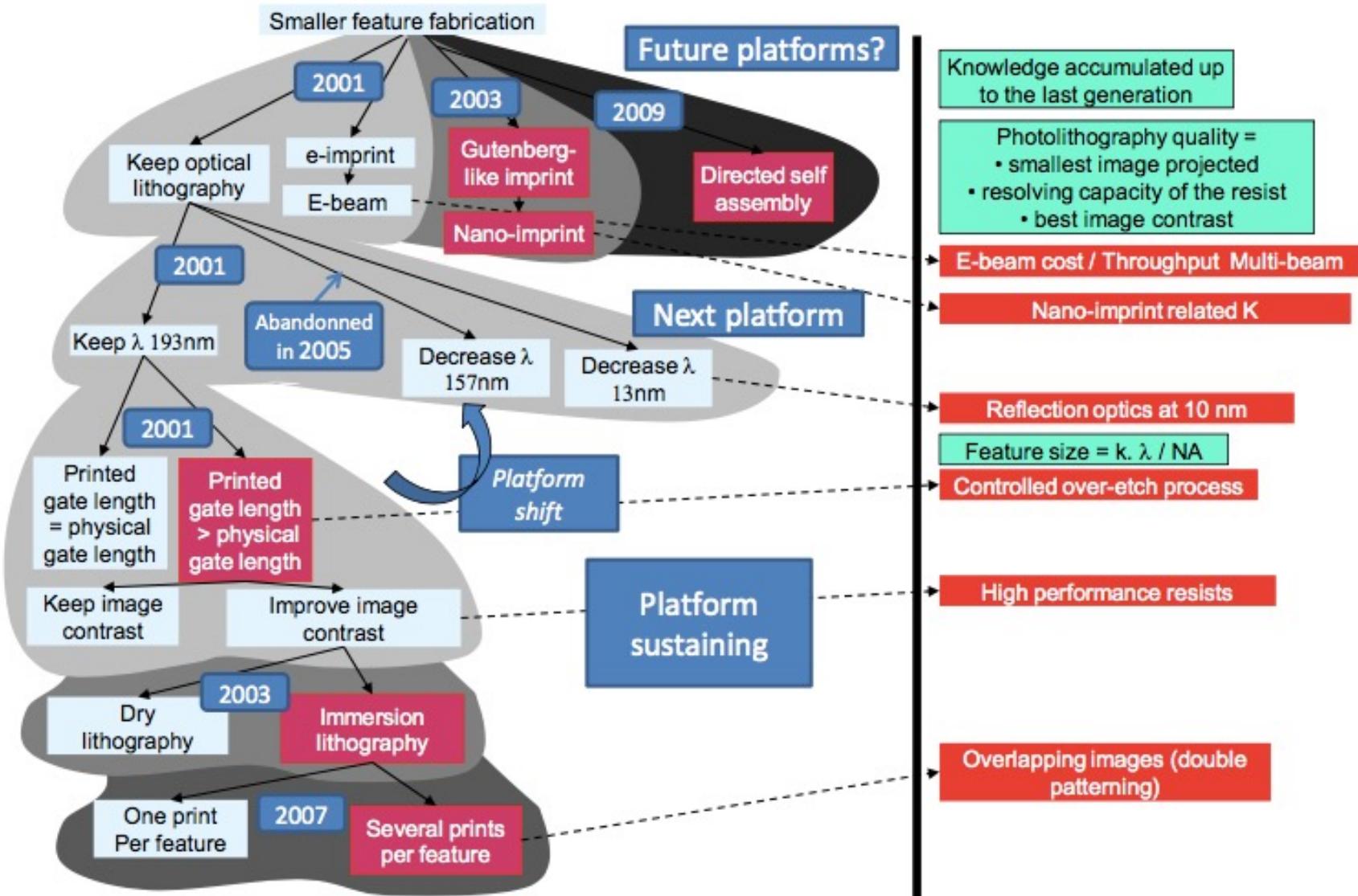
(b) Calibre OPCpro's mask



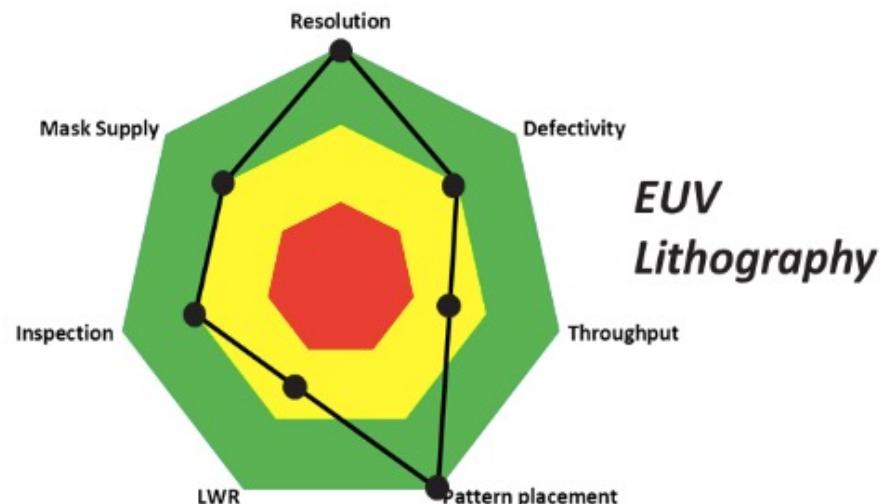
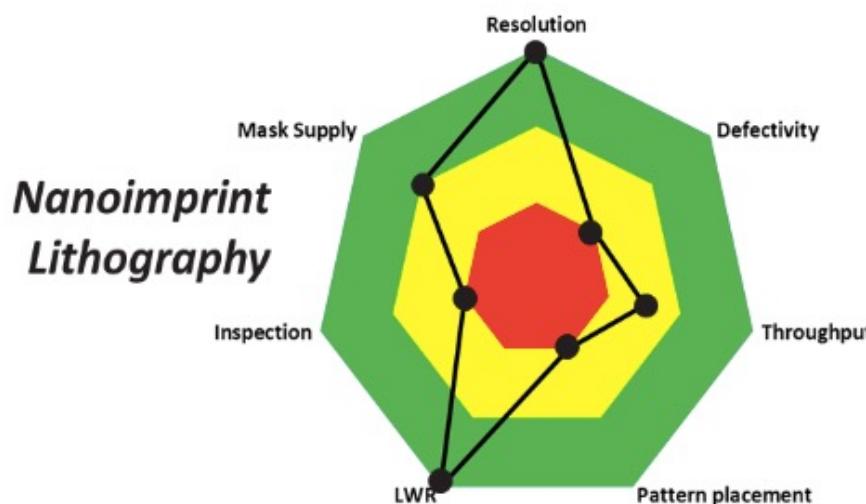
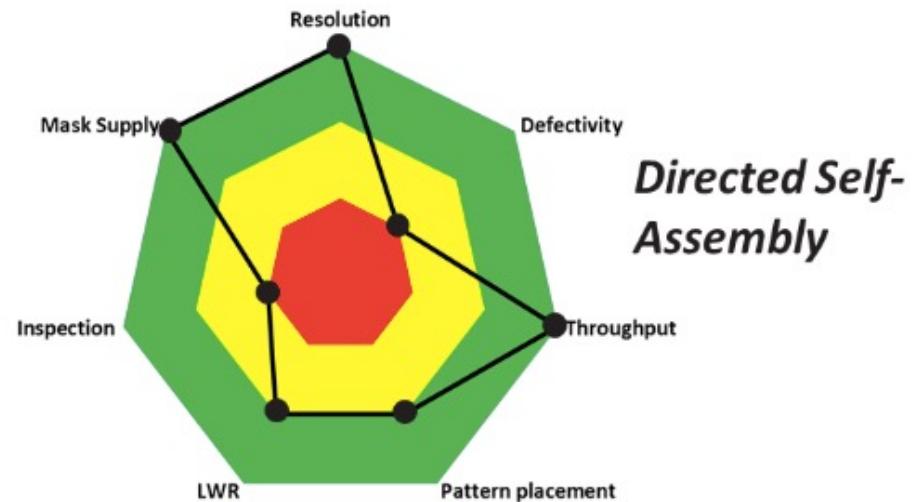
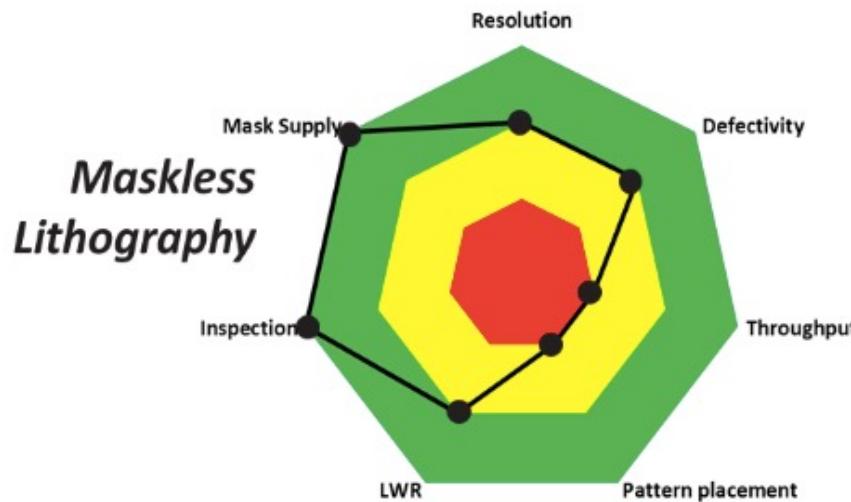
(c) Our DPB-OPC mask

Teh et al., IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, 29(1), pp 51, 2010

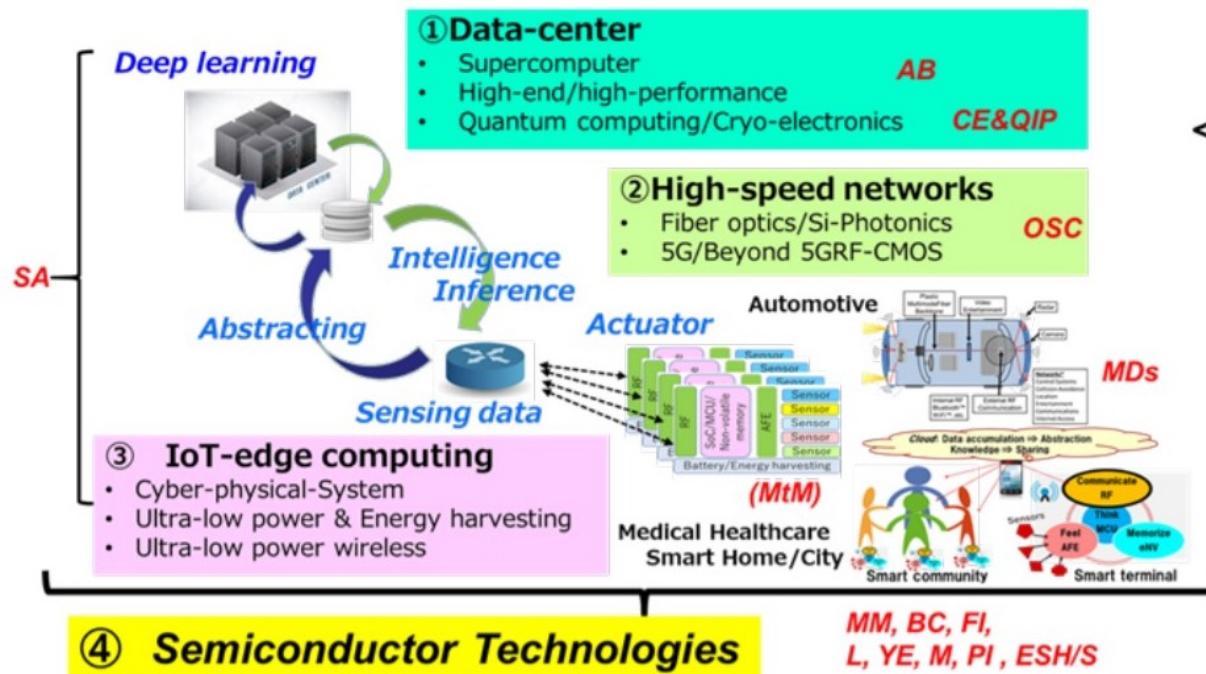
# From Mainstream technology to Wildest concepts



# Strength & Weakness of Patterning Approaches



# Drivers and Current Technologies



<International Collaboration>

International  
Roadmap Committee  
(IRC@2020.6)

- IEEE IRDS™
- SDRJ/JSAP\*1
- SINANO\*2 institute

**AB:** Applications Benchmarking, **SA:** Systems and Architecture, **OSC:** Outside system Connectivity, **MM:** More Moore, **BC:** Beyond CMOS, **CE&QIP:** Cryogenics Electronics and Quantum Information Processing, **PI:** Packaging Integration, **FI:** Factory Integration, **L:** Lithography, **YE:** Yield Enhancement, **M:** Metrology, **ESH/S:** Environment, Safety, Health, and Sustainability, **MtM:** More than Moore, **MDs:** Market drivers (automobile, medical devices).

\*1: The System Device Roadmap Committee of Japan/The Japan Society of Applied Physics

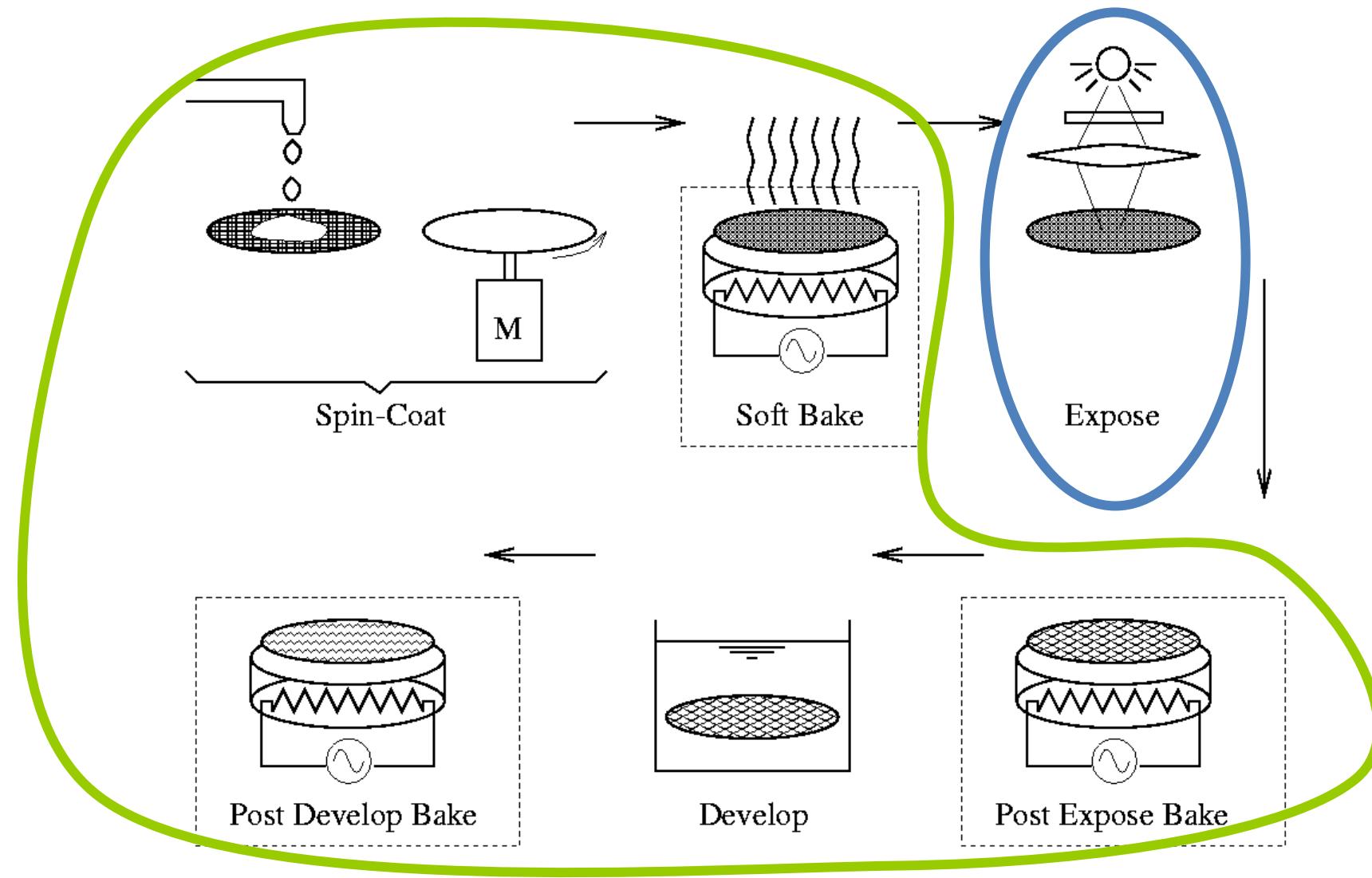
\*2: The European Academic and Scientific Association for Nanoelectronics

YEAR OF PRODUCTION	2020	2022	2025	2028	2031	2034
	G48M36	G45M24	G42M20	G40M16	G38M16T2	G38M16T4
Logic industry “Node Range” labeling (nm)	“5”	“3”	“2.1”	“1.5”	“1.0 eq”	“0.7 eq”
IDM-Foundry node labeling	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	FinFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Mainstream device for logic	FinFET	FinFET	LGAA	LGAA	LGAA-3D	LGAA-3D
LOGIC TECHNOLOGY ANCHORS						
Patterning technology inflection for Mx interconnect	193i, EUV DP	193i, EUV DP	193i, EUV DP	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV

Source: IRDS

# Photoresist Processing in Advanced Lithography Systems

# The Lithography Sequence



# Lithography Equipment



Stepper



Track

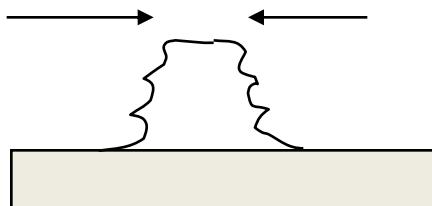
# Motivations

- International Panel on Future Directions in Control, Dynamics and Systems:
  - ...use of **control** is critical to future progress in the semiconductor sector. Modeling plays a crucial role and control techniques must make use of more **in-situ measurements** to control at a variety of temporal and spatial scales.

# Motivations

- International Technology Roadmap for Semiconductors (<http://www.itrs2.net/>):
  - Grand Challenges (Metrology):  
Real time *in situ*, integrated, and in-line metrology is required for manufacturing complicated devices.
  - process control for linewidth/critical dimension (CD) represents a major challenge.
- CD – smallest (critical) feature printed on the wafer.

What is the linewidth of this feature?



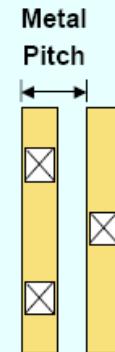
Tools to measure CD: AFM,  
SEM, Scatterometry

# International Technology Roadmap for Semiconductors (ITRS)

*Table LITH-1 Lithography Technology Requirements*

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
<b>DRAM</b>							
DRAM minimum $\frac{1}{2}$ pitch (nm)	18	17.5	17	14	11	8.4	7.7
Key DRAM Patterning Challenges							
CD control (3 sigma) (nm) [B]	1.8	1.8	1.7	1.4	1.1	0.84	0.8
Mininum contact/via after etch (nm) [H]	18	17.5	17	14.0	11	8.4	7.7
Minimum contact/via pitch(nm)[H]	54	53	51	42	33	25.2	23
Overlay (3 sigma) (nm) [A]	3.6	3.5	3.4	2.8	2.2	1.7	1.5
<b>MPU / Logic</b>							
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"		
Key MPU/Logic Patterning Challenges							
MPU/ASIC Minimum Metal $\frac{1}{2}$ pitch (nm)	18	15	12	10	8		
Metal LWR (nm) [C]	2.7	2.3	1.8	1.5	1.2		
Metal CD control (3 sigma) (nm) [B]	2.7	2.3	1.8	1.5	1.2		
Contacted poly half pitch (nm)	27.0	24.0	22.5	21.0	20.0		
Physical Gate Length for HP Logic (nm)	20	18	16	14	12		
Gate LER (nm) [C]	0.8	0.7	0.6	0.5	0.4		
Gate CD control (3 sigma) (nm) [B]	1.1	1.0	0.9	0.7	0.6		
Overlay (3 sigma) (nm) [A]	3.6	3.0	2.4	2.0	1.6		
MPU/ASIC finFET fin minimum 1/2 pitch (nm)	16.0	14.0	12.0				
FinFET Fin width (nm)	8.0	7.0	6.0				
Fin CD control (3 sigma) (nm) [B]	0.80	0.70	0.60				
FIN LER (nm) [C]	0.80	0.49	0.42				

DRAM  $\frac{1}{2}$  Pitch  
= DRAM Metal Pitch/2



Typical DRAM Metal Bit Line

The demand for faster circuits is the *main reason* for the acceleration of the roadmap towards smaller features.

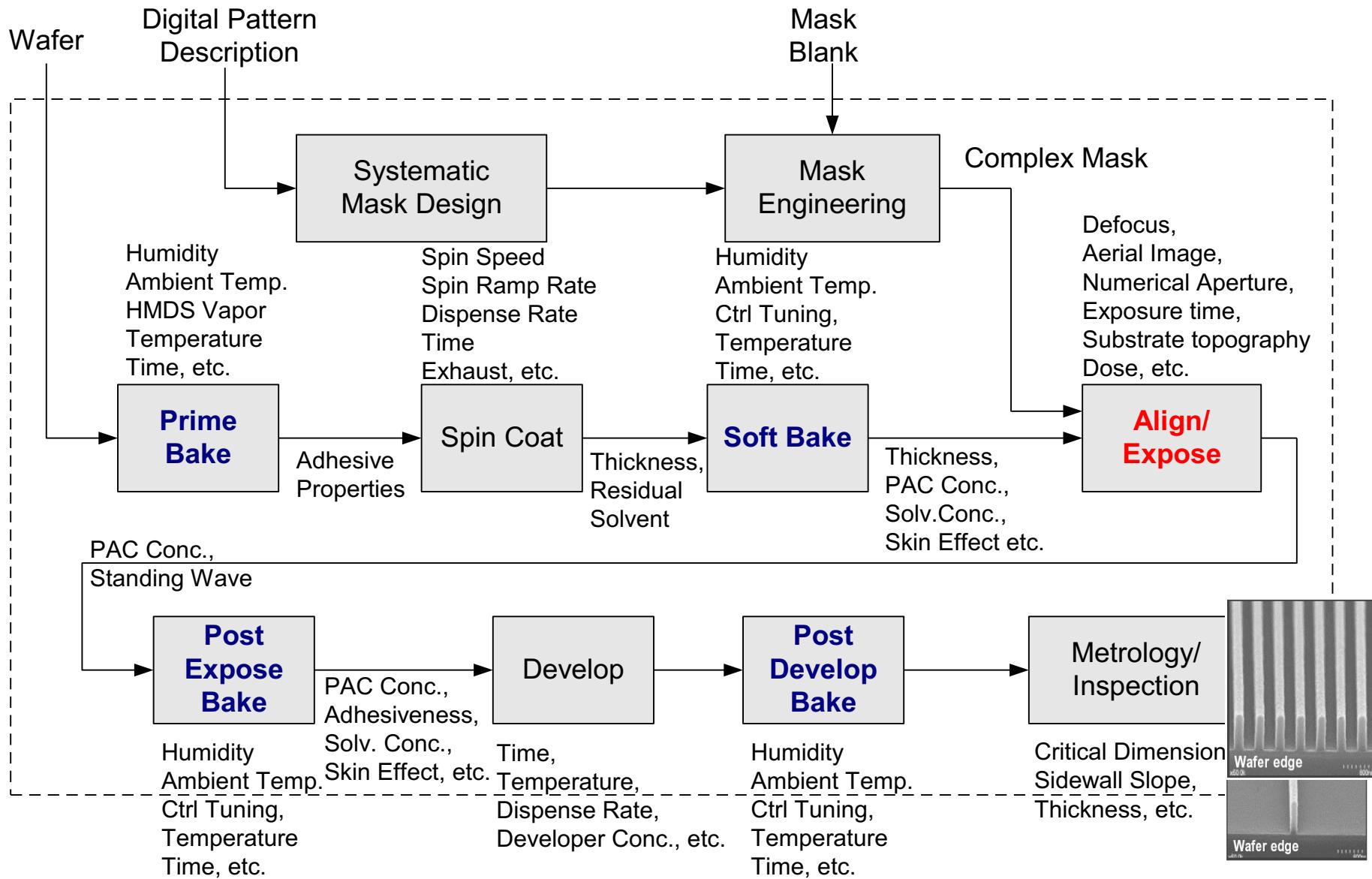
Source: IRDS roadmap

# ITRS roadmap Lithography Challenges

*Table LITH-3 2021 Lithography Difficult Challenges*

Next Generation Technology	First Possible Use in HVM	Feature Type	Device Type	Key Challenges	Required Date for Decision making
EUV Multiple Patterning	2022	12nm hp LS	"3nm" Logic Node	<ul style="list-style-type: none"> <li>Process control (EPE, overlay, CDU, LER/LWR)</li> <li>Cost/throughput</li> </ul>	2021
EUV high NA	2025	10.5nm hp LS	"2.1nm" Logic Node	<ul style="list-style-type: none"> <li>Resist capability (sensitivity, LER/LWR, resolution , defects)</li> <li>Stitching of two mask patterns</li> <li>Improved masks for high NA</li> <li>Cost/Throughput</li> </ul>	2024
NanoImprint	2021	20 nm lines and spaces 20 to 30nm contact holes	3D Flash Memory	<ul style="list-style-type: none"> <li>Defectivity</li> <li>Overlay</li> <li>Master Template fabrication and inspection &lt;20nm</li> <li>Defect repair</li> <li>Mass-production capacity</li> </ul>	Product Evaluation Underway
DSA (for pitch multiplication)	2022	Contact holes/cut levels for logic Possibly nanowire patterning	"3nm" Logic Node	<ul style="list-style-type: none"> <li>Defectivity and defect inspection</li> <li>Pattern Placement</li> <li>Design</li> <li>3D Metrology</li> </ul>	2021

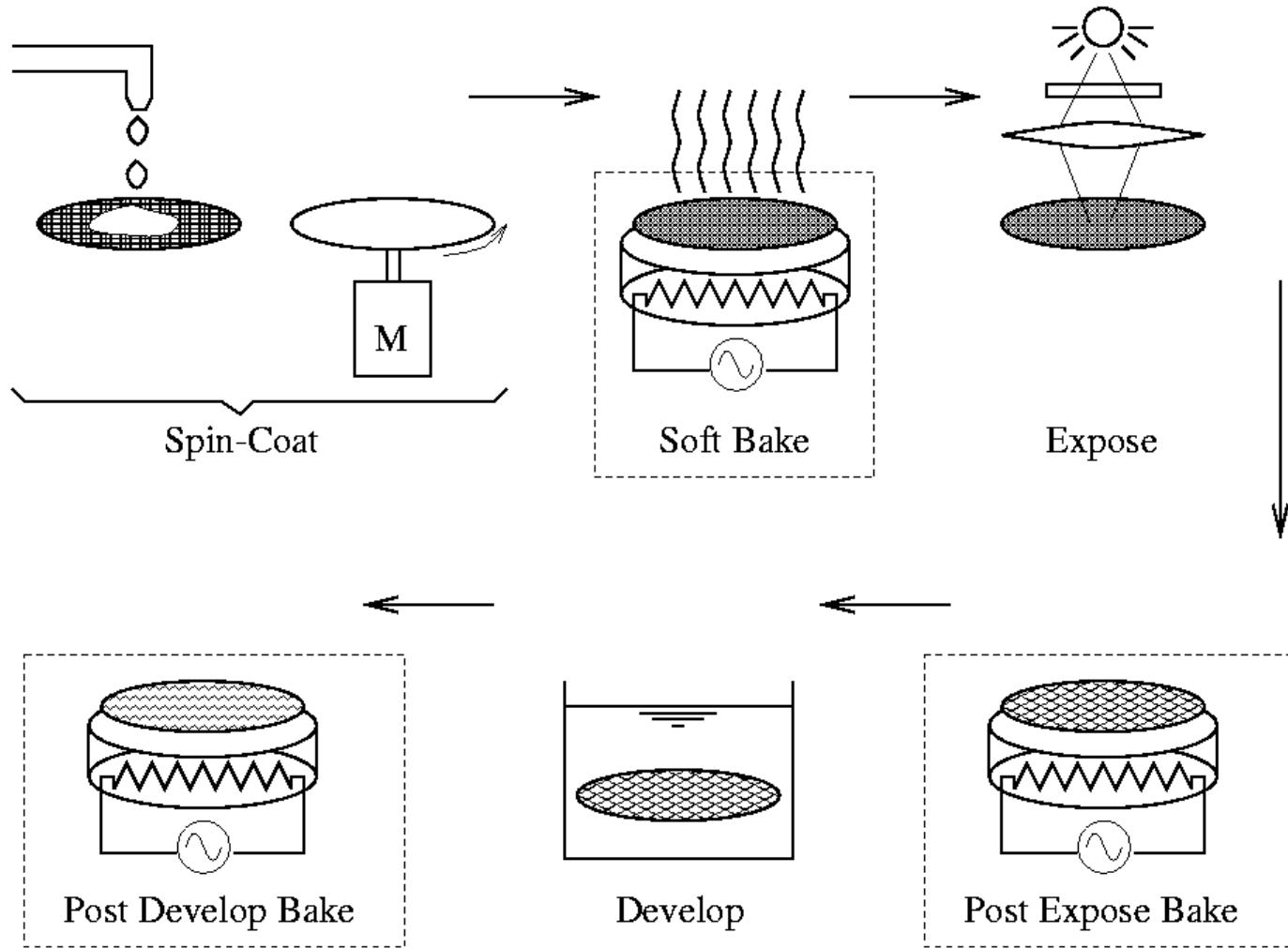
# The Lithography Sequence



## Our Approach:

To apply mathematical systems sciences tools including control, signal processing, optimization, simulation and modeling to the fabrication of integrated circuits.

# Thermal Processing is Critical



# Temperature Specifications

Thermal Step	Purpose	Approximate temperature range	Precision required
HMDS vapor prime bake	Promote Adhesion	70 <sup>0</sup> C – 150 <sup>0</sup> C	±5 <sup>0</sup> C
ARC bake	Cure ARC	90 <sup>0</sup> C – 180 <sup>0</sup> C	±1 <sup>0</sup> C – 2 <sup>0</sup> C
Post-apply bake (PAB or soft bake)	Drive off solvent, densify resist, stabilize thickness	90 <sup>0</sup> C – 140 <sup>0</sup> C	±1 <sup>0</sup> C
Post-exposure bake (PEB)	I-line; smooth standing waves	90 <sup>0</sup> C – 180 <sup>0</sup> C	±0.5 <sup>0</sup> C – 1 <sup>0</sup> C
PEB	DUV; deblock exposed resist	90 <sup>0</sup> C – 150 <sup>0</sup> C	<b>±0.12<sup>0</sup>C – 0.5<sup>0</sup>C</b>
Post-develop bake (PDB)	Harden coating, improve etch stability	120 <sup>0</sup> C – 180 <sup>0</sup> C	±1 <sup>0</sup> C

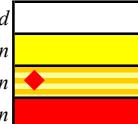
Ref: J. Parker and W. Renken, "Temperature metrology for CD control in DUV lithography", *Semiconductor International*, 20(10), p.111-6.

# ITRS – Photoresist requirements

Table LITH3 Resist Requirements

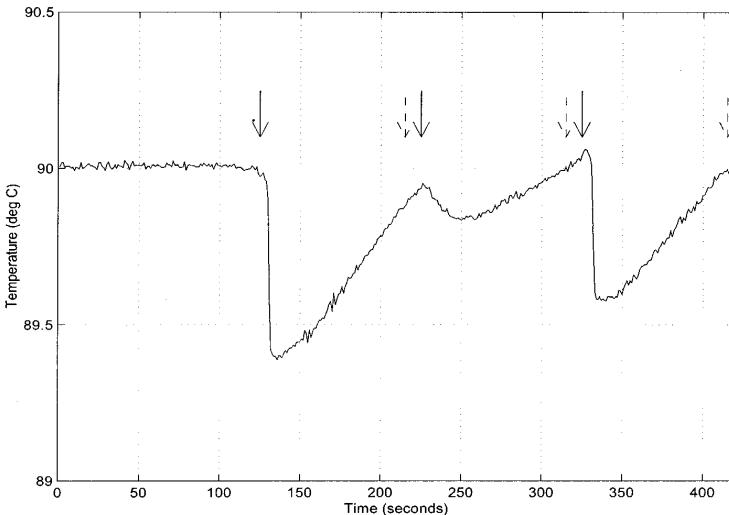
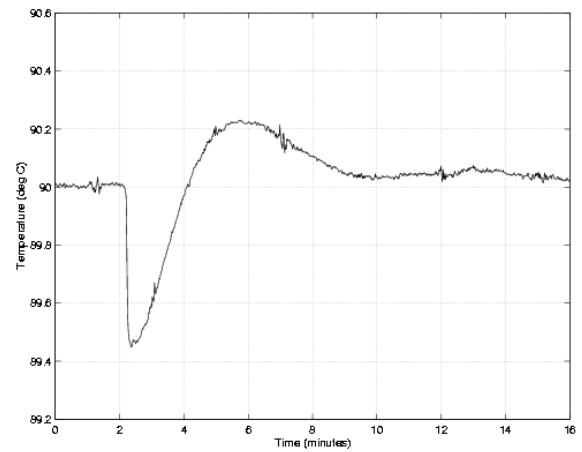
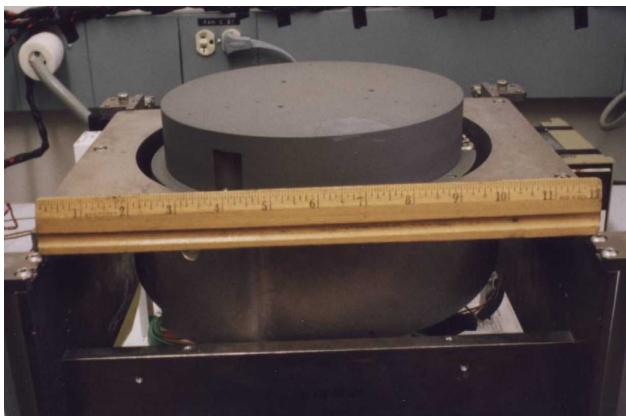
Year of Production	2013	2014	2015	2016	2017	2018	2019	2020
DRAM ½ pitch (nm) (contacted)	28	26	24	22	20	18	17	15
Flash ½ pitch (nm) (un-contacted poly)	18	17	15	14	13	12	12	11.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	40	32	32	28	25	23	20	18
MPU physical gate length (nm) [after etch]	20	18	17	15	14	13	12	11
MPU gate in resist length (nm)	28	25	22	20	18	16	14	12
Resist Characteristics								
Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) **†	2.0	1.8	1.7	1.5	1.4	1.3	1.2	1.1
Minimum resist thickness	42	37	33	30	26	24	21	19
Maximum resist thickness	80	64	64	57	51	45	40	36
Resist thickness (nm, single layer) ***	42-80	37-64	33-64	30-57	26-51	24-45	21-40	19-36
PEB temperature sensitivity (nm/C)	0.8	0.7	0.7	0.6	0.6	0.5	0.5	0.4
Backside particle density (particles/cm <sup>2</sup> )	0.28	0.28	0.28	0.28	0.28	0.28	0.28	0.28
Back surface particle diameter: lithography and measurement tools (nm)	75	75	75	50	50	50	50	50
Defects in spin-coated resist films (#/cm <sup>2</sup> ) †	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
Minimum defect size in spin-coated resist films (nm)	20	20	10	10	10	10	10	10
Defects in patterned resist films, gates, contacts, etc. (#/cm <sup>2</sup> )	0.02	0.02	0.01	0.01	0.01	0.01	0.01	0.01
Minimum defect size in patterned resist (nm) [J]	20	20	10	10	10	10	10	10
Low frequency line width roughness of physical gate: (nm, 3 sigma) <12% of CD *****	2.4	2.2	2.0	1.8	1.7	1.5	1.4	1.3
Correlation Length (nm) *****	19.6	18.6	17.0	15.5	12.6	12.8	11.5	10.2
Defects in spin-coated resist films for double patterning (#/cm <sup>2</sup> )	0.005	0.005	0.005	0.005	0.005	0.005	0.005	0.005
Backside particle density for double patterning (#/cm <sup>2</sup> )	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14

Manufacturable solutions exist, and are being optimized  
 Manufacturable solutions are known  
 Interim solutions are known  
 Manufacturable solutions are NOT known



# Feedforward Control: application to conventional thermal system

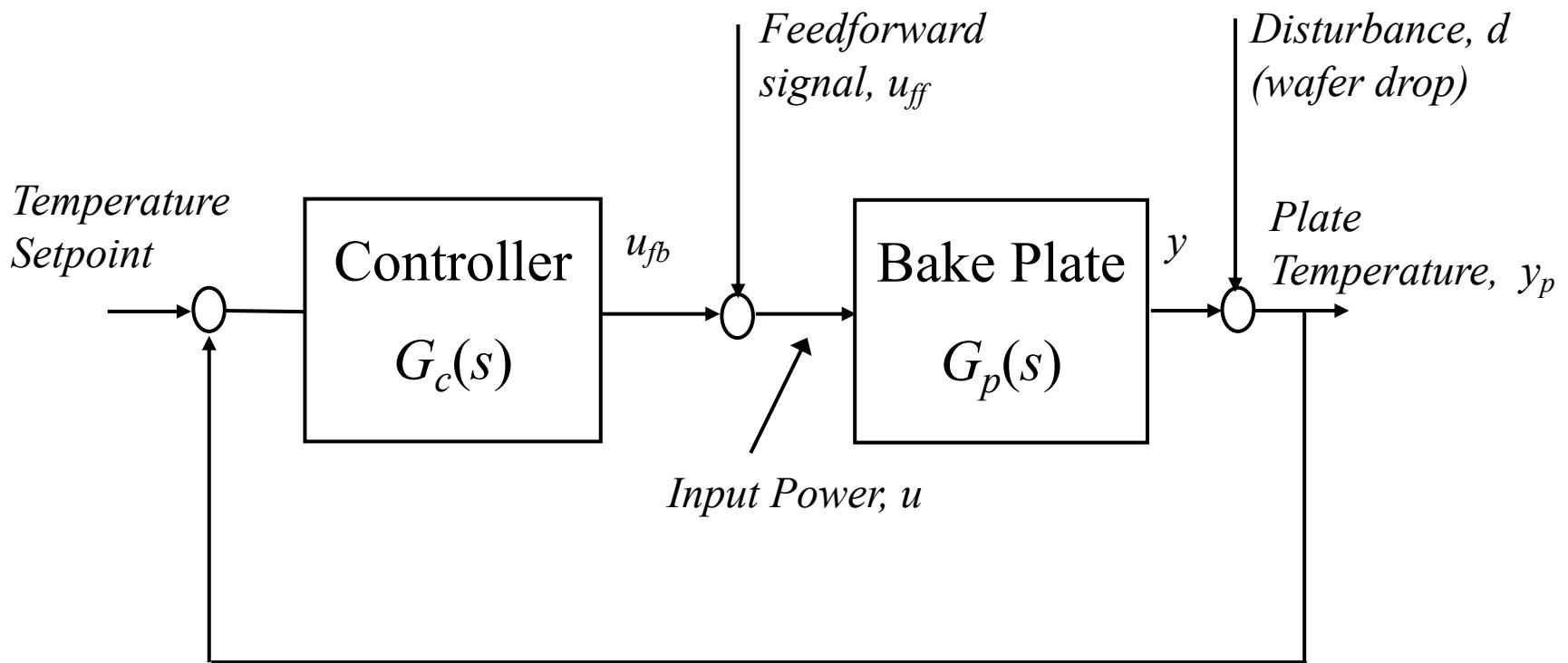
# Conventional bake-plate



## Problems

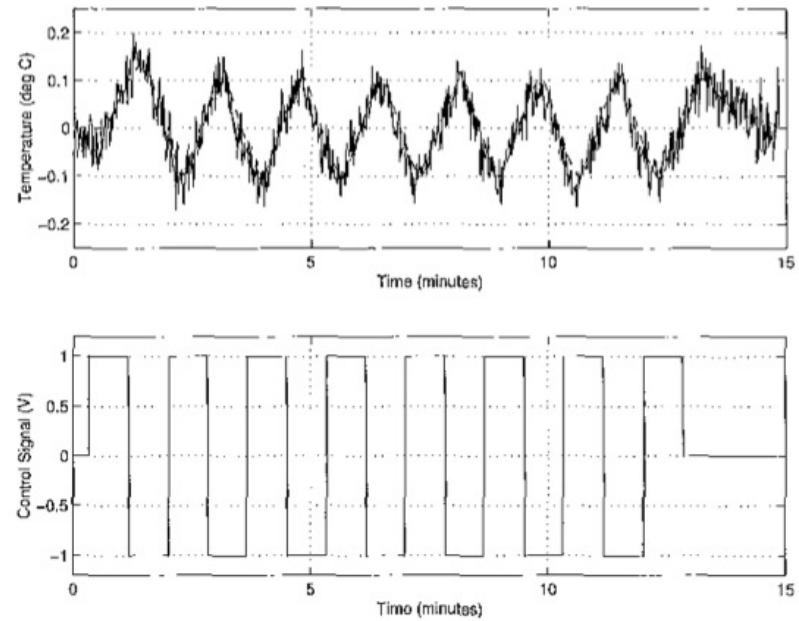
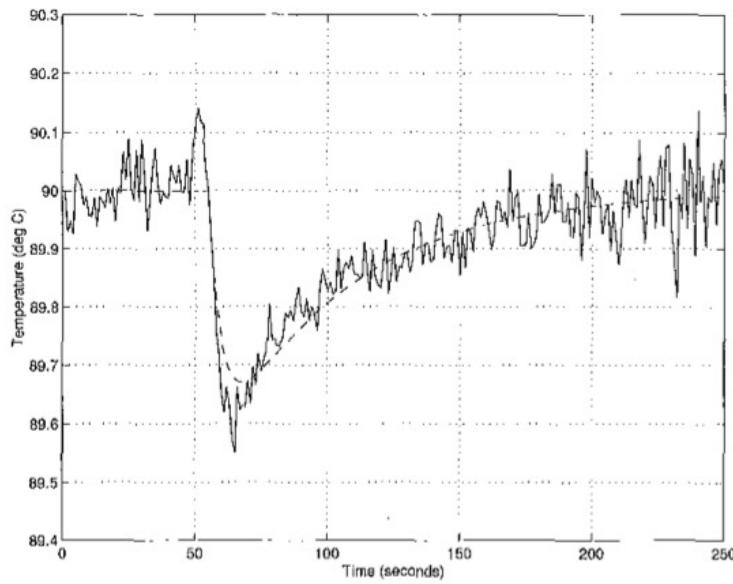
- Repeatability, if process time is shorter than the recovery time.
- System may never truly be at steady-state conditions.

# Feedforward/feedback Strategy



# Plant Modeling

- From modeling:  $G(s) = \frac{(s+0.526)(s+0.186)}{(s+0.191)(s+0.778)(s+0.00018)}$
- What are the time constants for this system?



# Optimal Predictive Control

- Effect of disturbance can be eliminated, if

$$y = -d$$

- Feedforward controller

$$u_{ff} = G_p^{-1} d$$

- Due to bounds placed on the achievable input power  $u \in [0, U^{\max}]$ ,

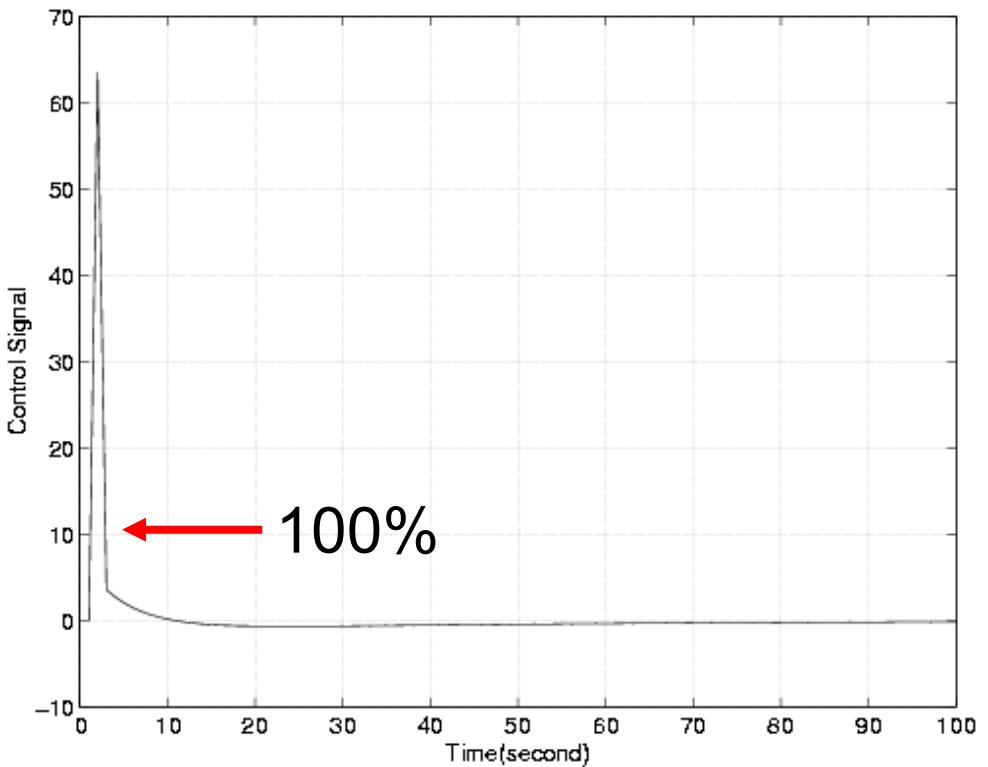
$$y \neq -d$$

- Objective function

$$\min_{u(k) \in [0, U^{\max}]} \max_{k \in \{0, 1, \dots, N\}} |y(k) + d(k)|$$

# Unconstrained Feedforward Control Signal

- Model Inversion
  - Effect of disturbance can be eliminated, if
$$y = -d$$
  - Feedforward controller
$$u_{ff} = G_p^{-1} d$$



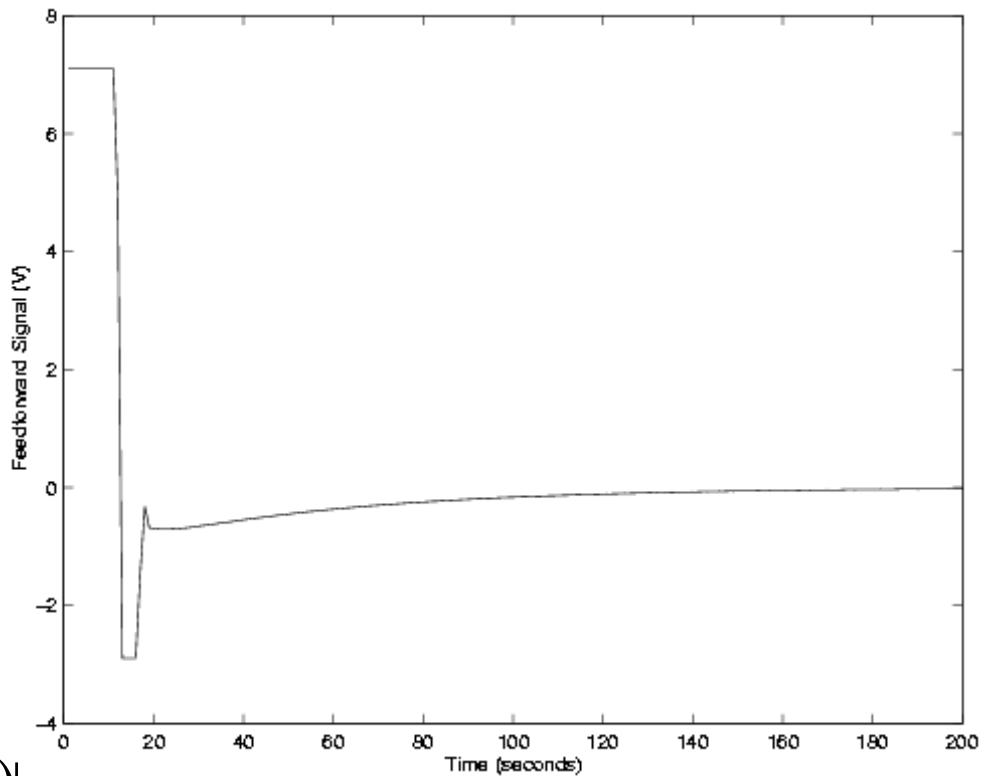
# Optimal Feedforward Control Signal

- Optimal Predictive Control
  - Due to bounds placed on the achievable input power  $u \in [0, U^{\max}]$ ,

$$y \neq -d$$

- Objective function

$$\min_{u(k) \in [0, U^{\max}]} \max_{k \in \{0, 1, \dots, N\}} |y(k) + d(k)|$$



# Optimal Predictive Control

- Equivalent linear programming problem:

Minimize

$$\begin{bmatrix} 0 & \dots & 0 & 1 \end{bmatrix} \begin{bmatrix} U \\ e \end{bmatrix}$$

objective function

subject to

$$\begin{bmatrix} \Psi & -1_I \\ -\Psi & -1_I \end{bmatrix} \begin{bmatrix} U \\ e \end{bmatrix} \leq \begin{bmatrix} -D \\ D \end{bmatrix}$$

dynamic model

$$U \leq U^{\max}$$

upper control signal saturation

$$U \geq 0$$

lower control signal saturation

$$y(k) + d(k) = 0$$

$$k \in [n_f, \dots, N]$$

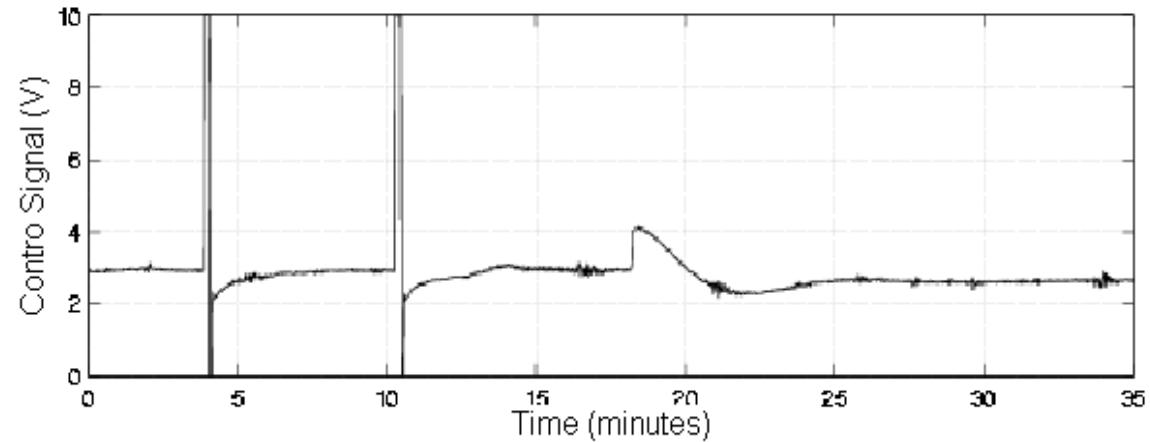
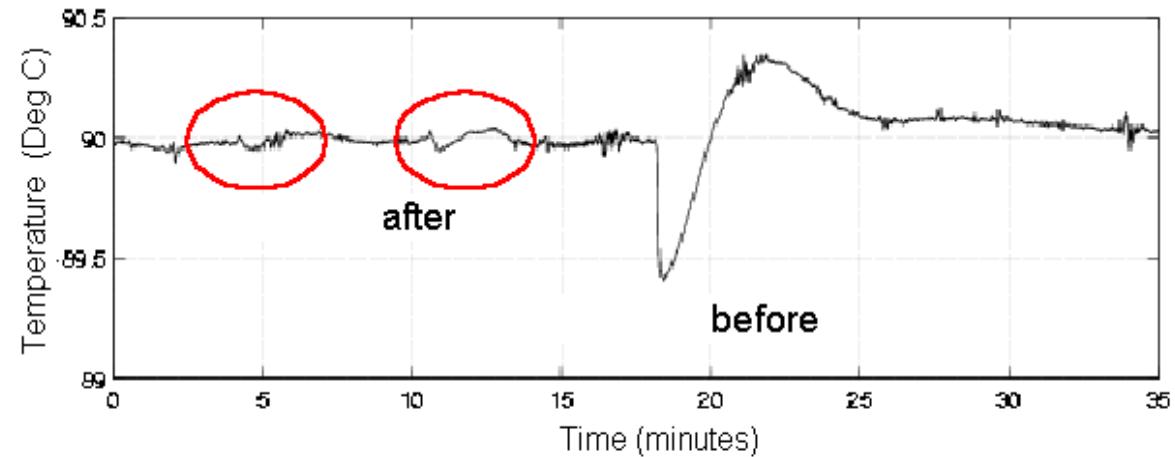
disturbance to be eliminated from  $n_f$  to  $N$

# Main Results: wafer processing

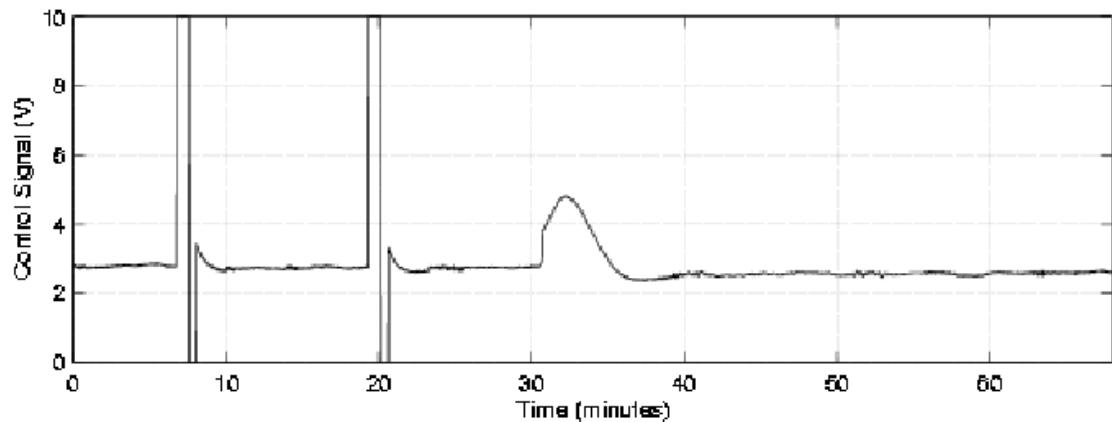
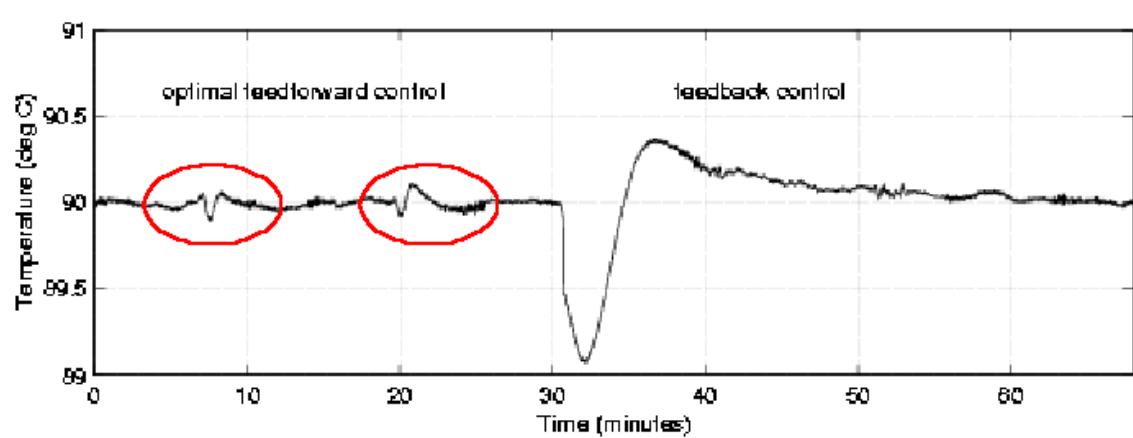
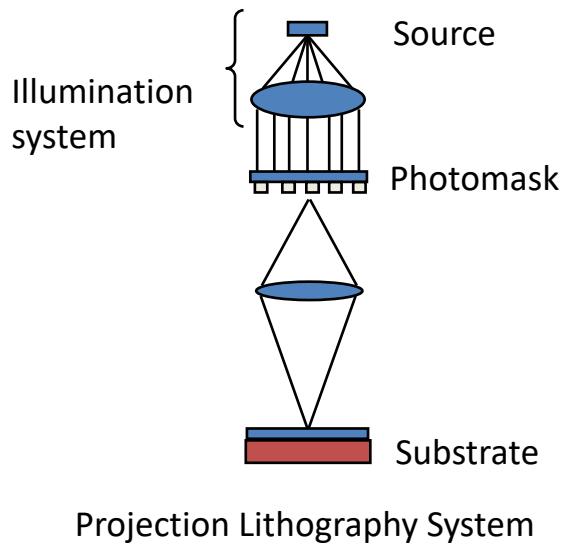
For wafer  
processing

Significant  
improvement in

- Integrated Square Error – 200×
- Settling time – 6×

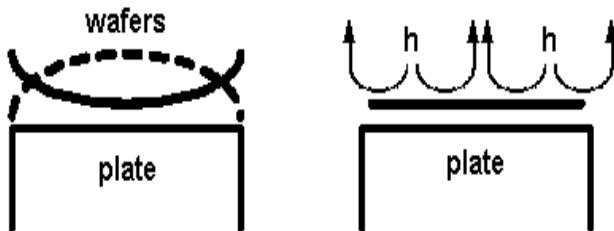
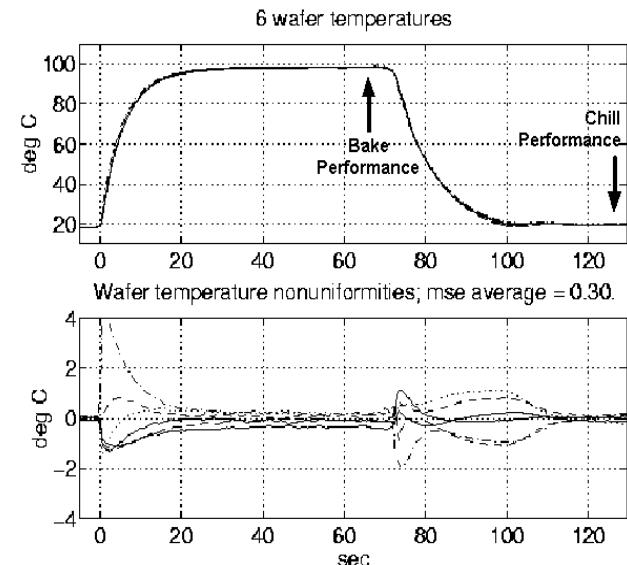
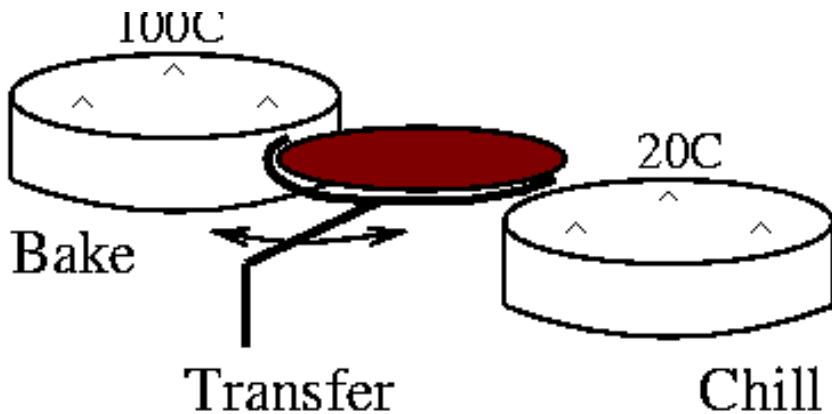


# Photomask processing

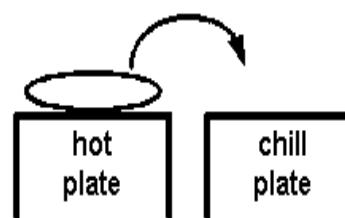


# Programmable Thermal Processing System

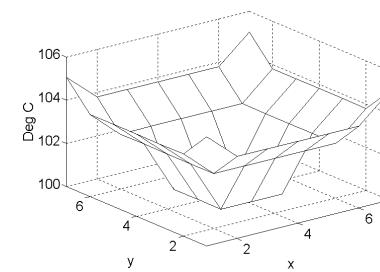
# Limitations of Conventional Bake-plates



Wafer warpage    Natural convection variations



Hot wafer transfer

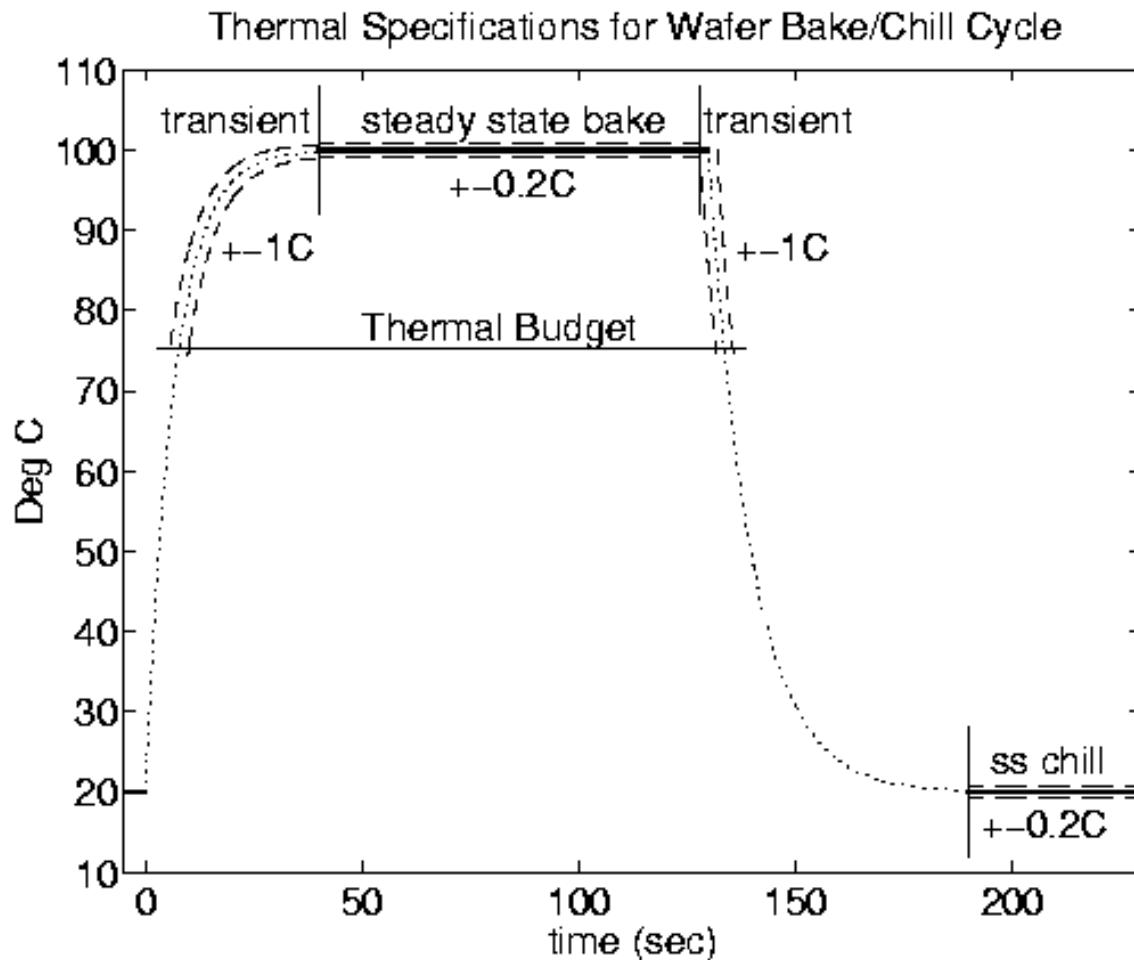


Optimal plate temp.

- Warpage, convection variations and other disturbances suggest the need for better spatial control.
- Uncontrolled transfer of hot wafers suggests the need to integrate the bake and chill in a single unit.

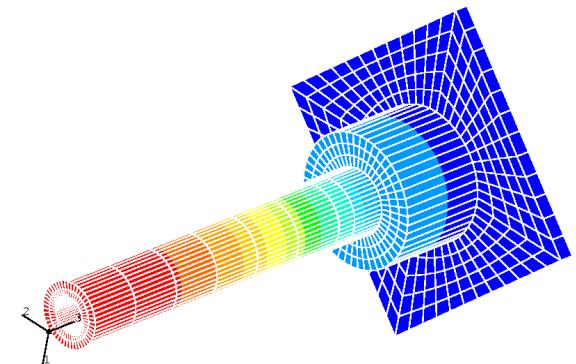
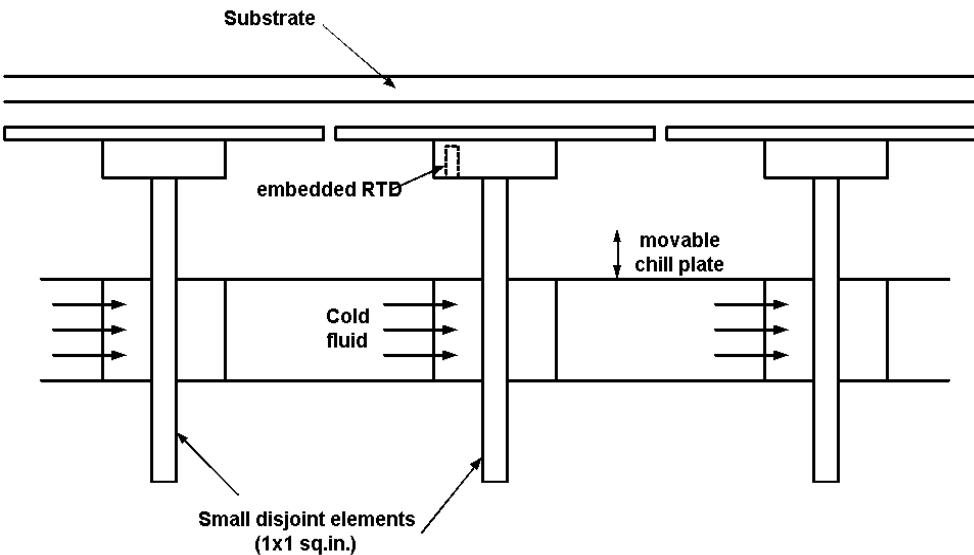
# Thermal Budget

- Reactions are typically activated before steady state is reached.
- Should define relevant bounds on the whole trajectory.
- Also, if one could choose the shape of the transient, what would it be?

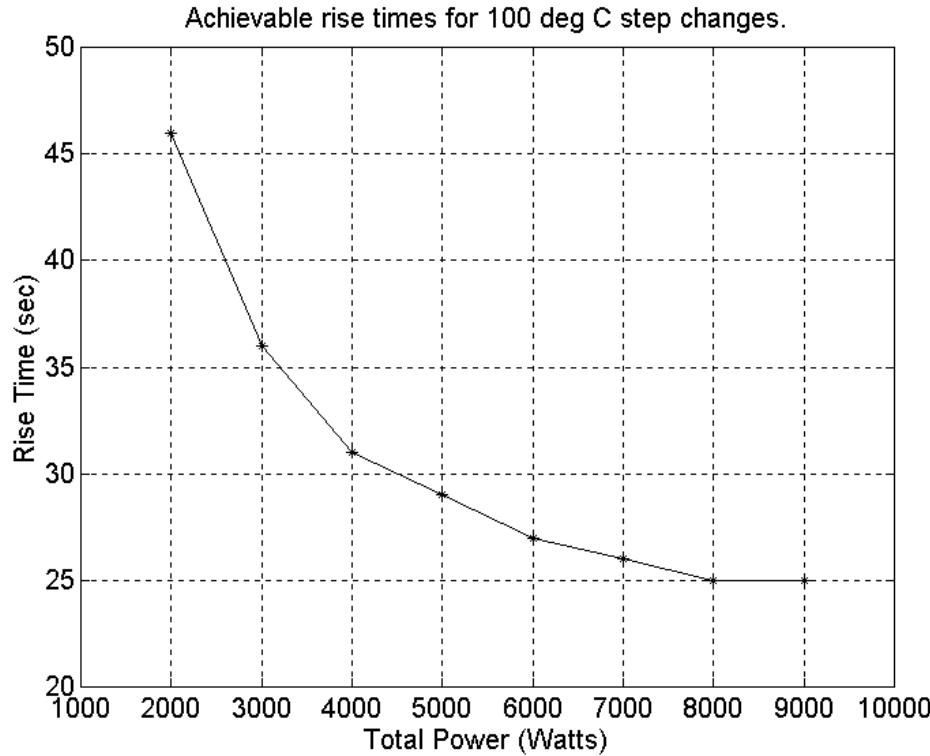


# New Thermal System Design

- Features
  - Integrated bake/chill module – thermal cycling
  - Distributed actuation – control of temperature uniformity
  - In-situ temperature measurement
  - Low thermal mass – faster response time
  - Each zones with its own set of electronics and data acquisition



# Optimization Problem



min  
rise time  
s.t.

wafer non-uniformity  $\|T_{\text{wafer}}(t) - \bar{T}_{\text{wafer}}(t)\|_\infty$

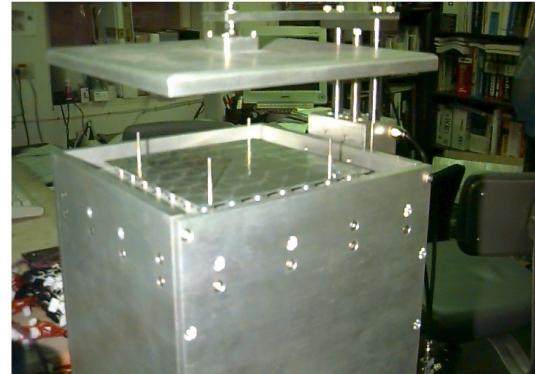
System dynamics  $\dot{T} = AT + Bu$

Power limitations  $0 \leq \text{Total Power} \leq P_{\max}$

Final Temperature  $T_{\text{wafer}}|_{final} = 100^\circ C$

# Prototype Integrated Bake/Chill System

## Photomask processing

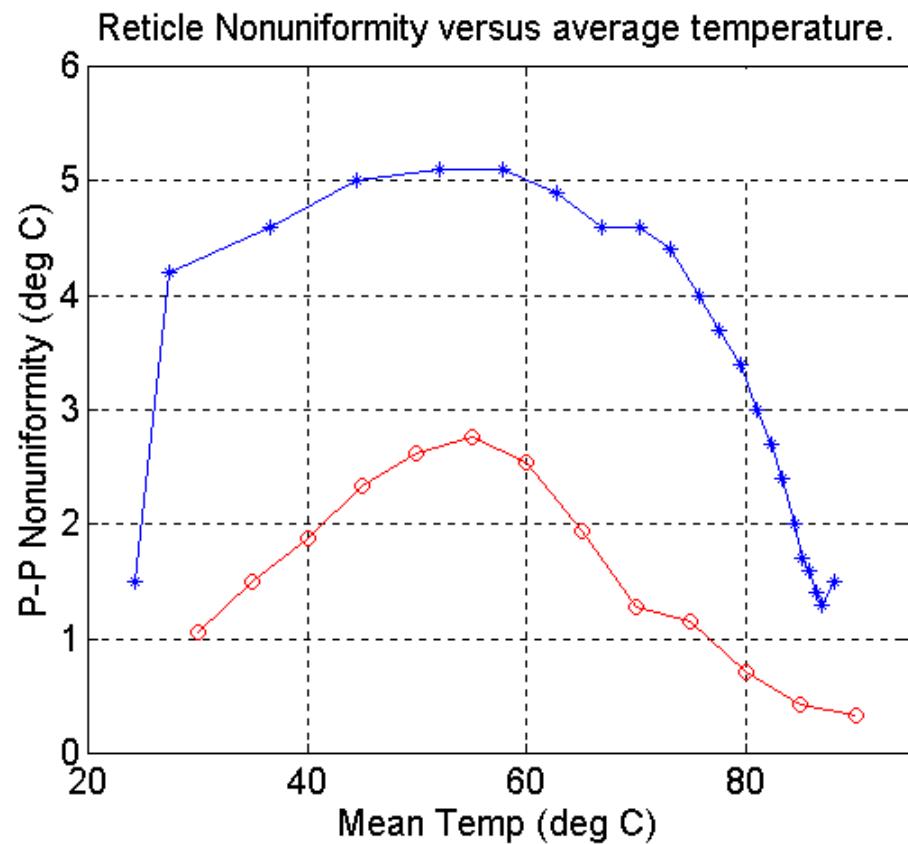
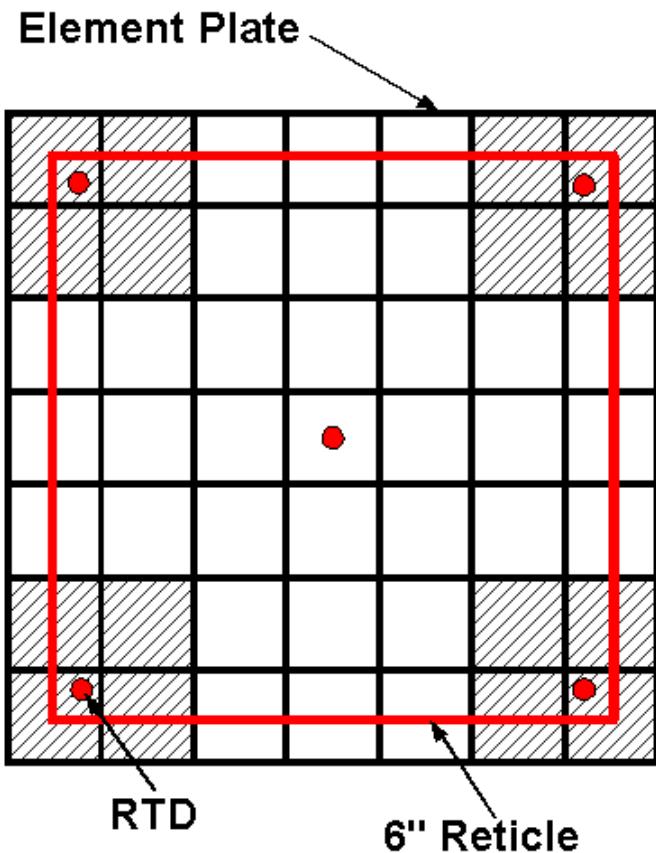


Pin lift, Lid lift engaged  
Chill plate disengaged



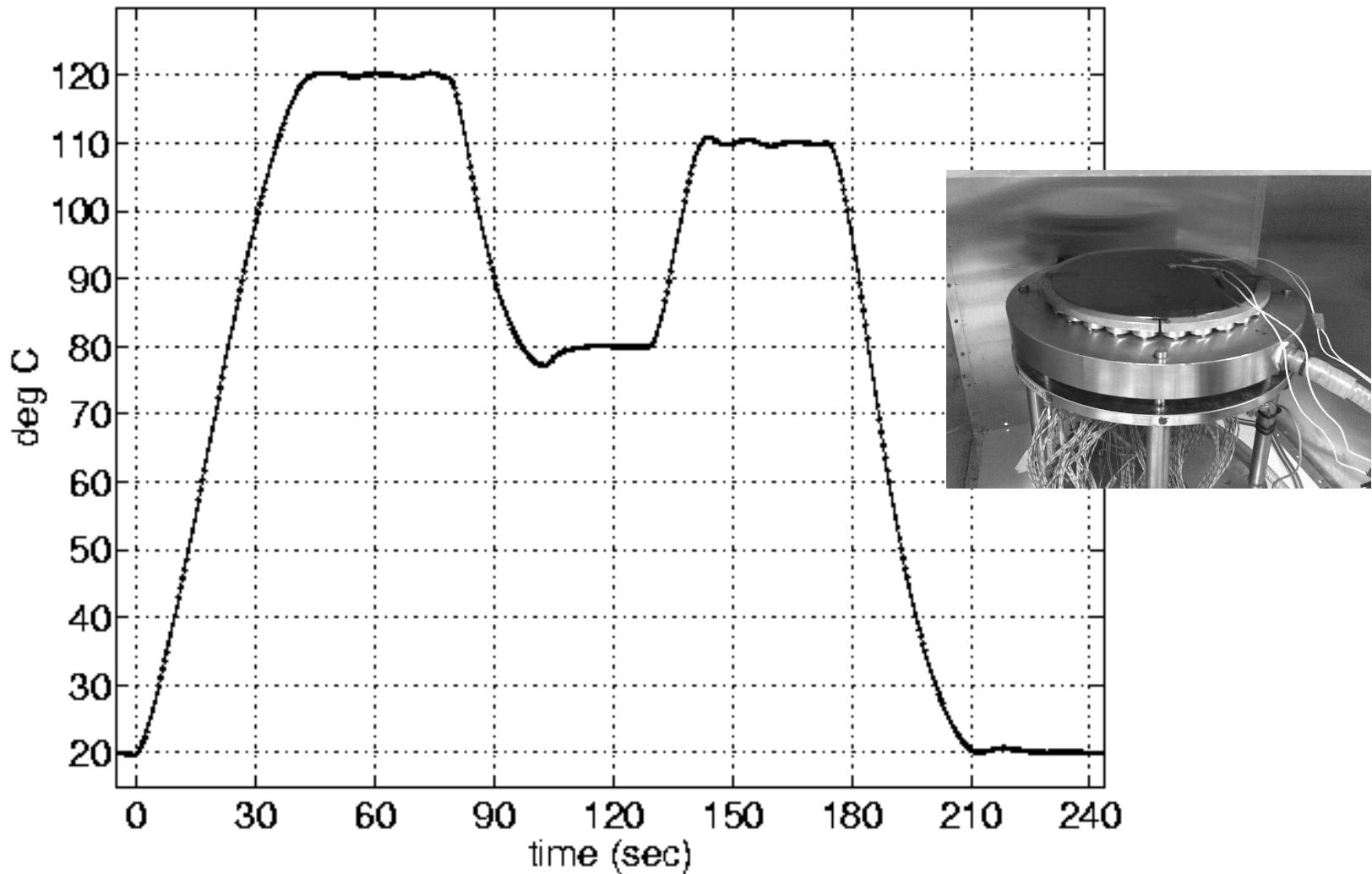
Robot transferring photomask

# Performance Comparison with commercial system



# Arbitrary Temperature Profiles

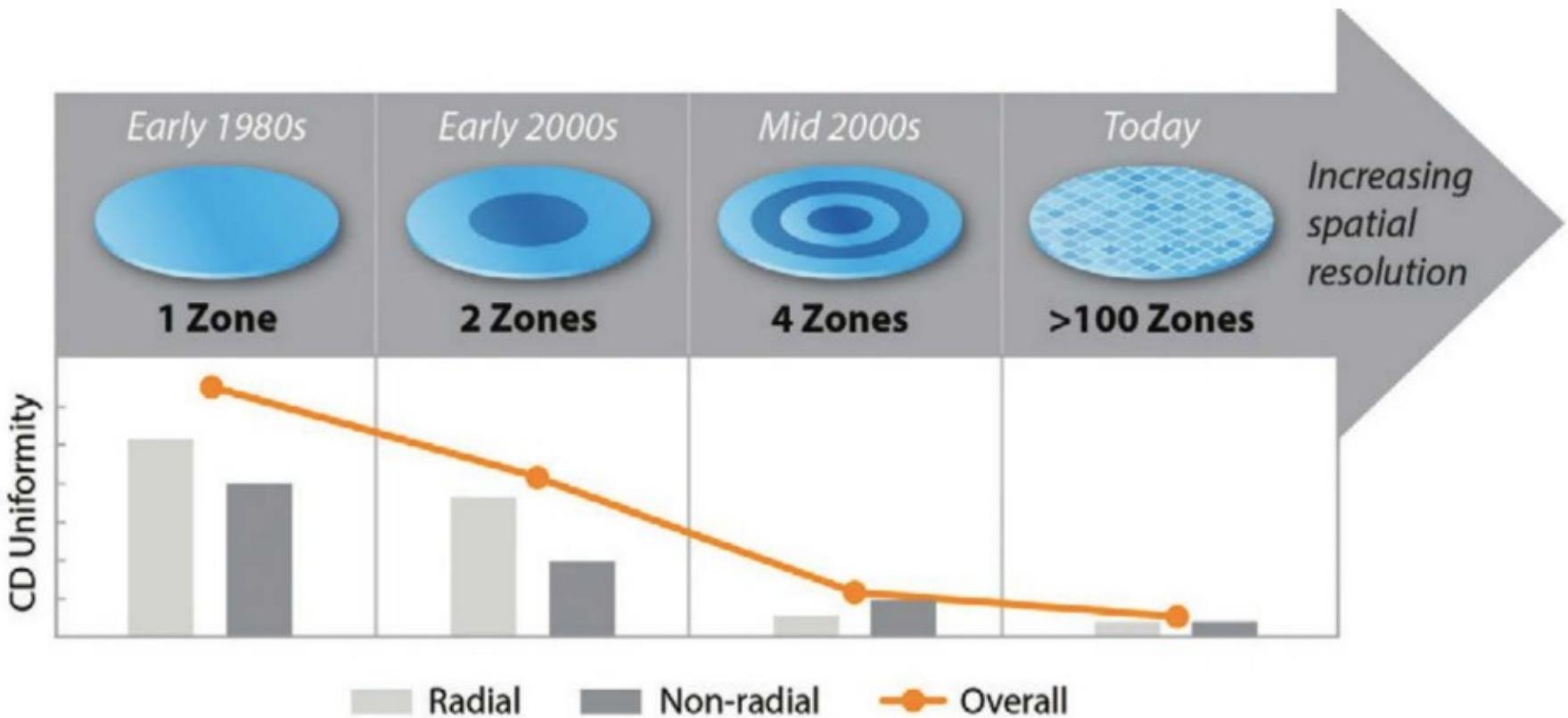
An example of a possible wafer bake profile.



# Advanced Applications

- CD uniformity control
  - Better temperature control throughout
  - Narrow the CD distribution
- Product yield enhancement
  - Feedback post-process spatial nonuniformities and adjust spatial temperature distribution to compensate
- Throughput improvement
  - Rapid response time allows multiple product runs without waiting for bake temperature stabilization
- Characterize temperature sensitivity
  - Utilize single wafer with spatial temperature distribution to analyze thermal effects on CD
- Photoresist film properties control
  - Uniform photoresist thickness, extinction coefficient etc. within wafer – reduce swing curve effect

# Evolution of Multizone Heating Plates

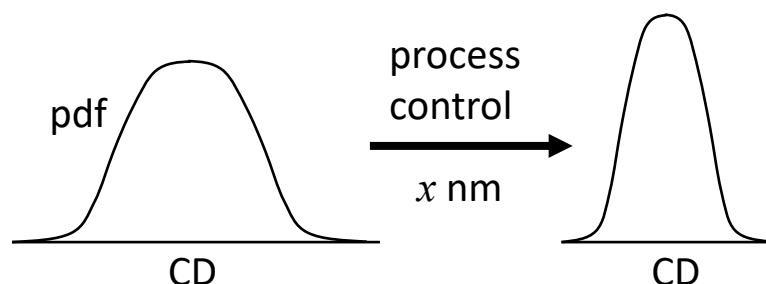


Source: Solid State Technology, July 2016, Vol. 59, No. 5

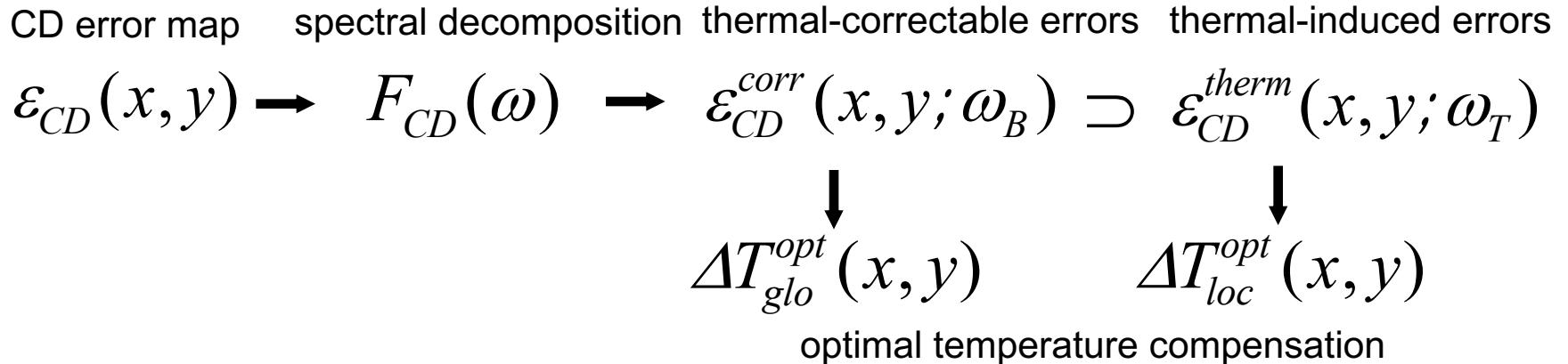
Run-to-run CD control via PEB

# Objectives/Motivations

- Reticle CD non-uniformity is a results of both exposure tool and process errors.
- Goal is to optimize process to reduce spatial CD error on mask.
- Determine CD – temperature sensitivity. Acid catalyzed resists exhibit more sensitivity to temperature errors at PEB than other resists and bake steps (less than  $\pm 0.1^{\circ}\text{C}$ )
- Requires good temperature control during both ramp and hold.

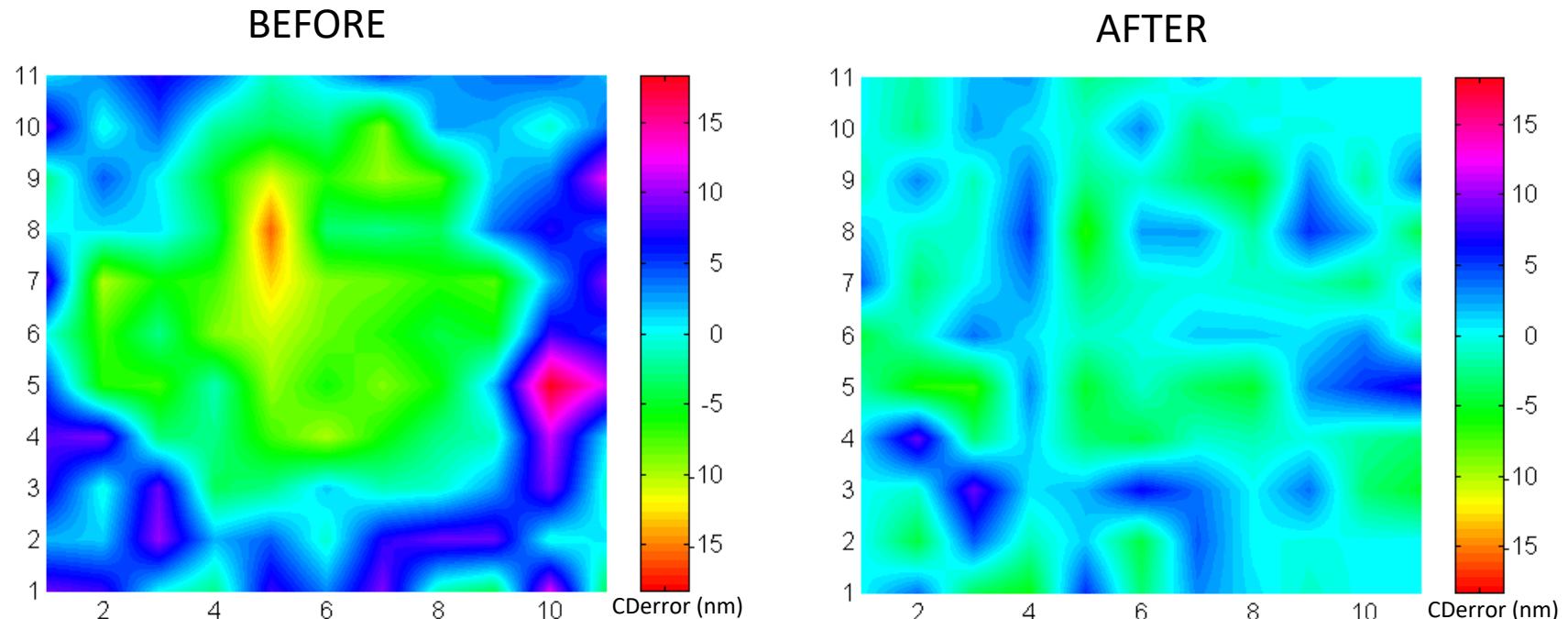


# Spectral Optimization for CD Uniformity



- *Nominal approach*: determine (spatial) thermal-induced errors and optimize temperature profile
  - *Aggressive approach*: determine all CD errors that are correctable by programmable multizone temperature array
  - $\omega_B \sim Z$ , Number of zones

# Low Spatial Frequency Compensation

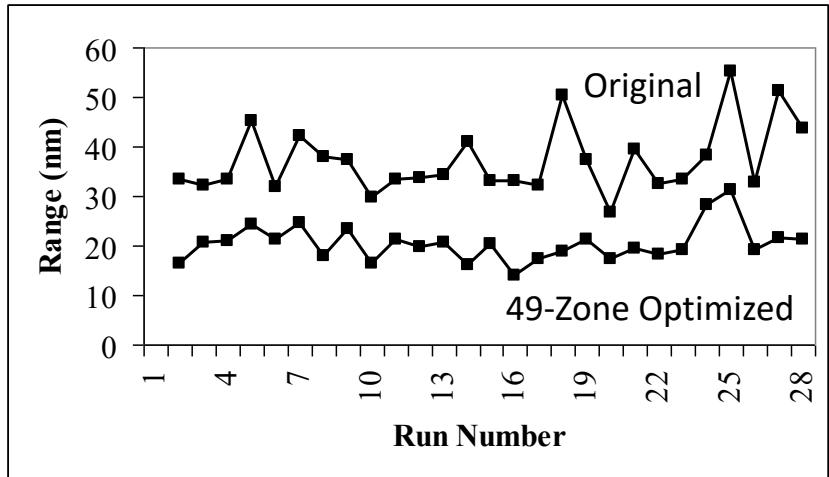
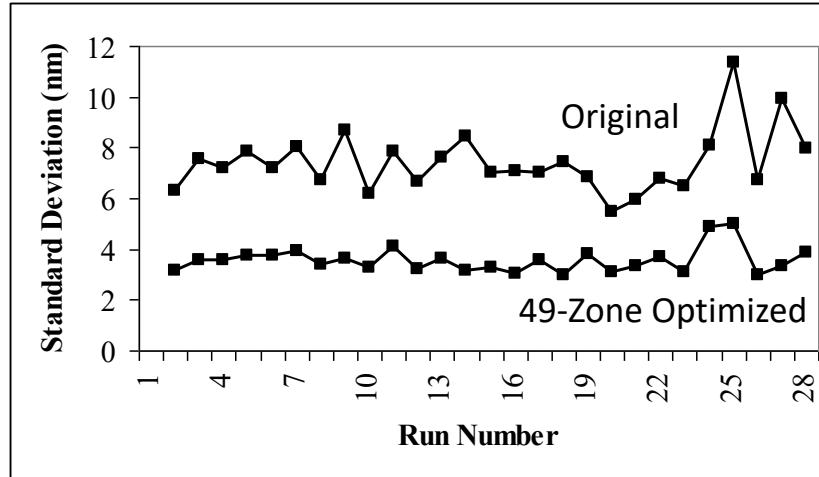
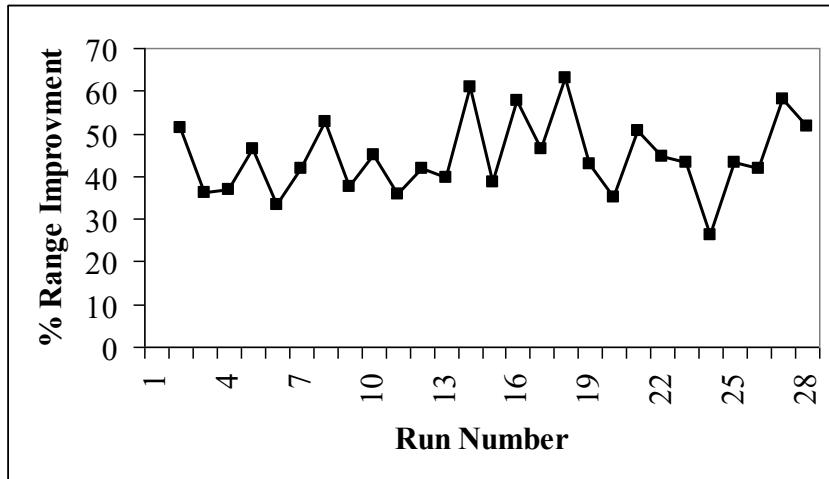
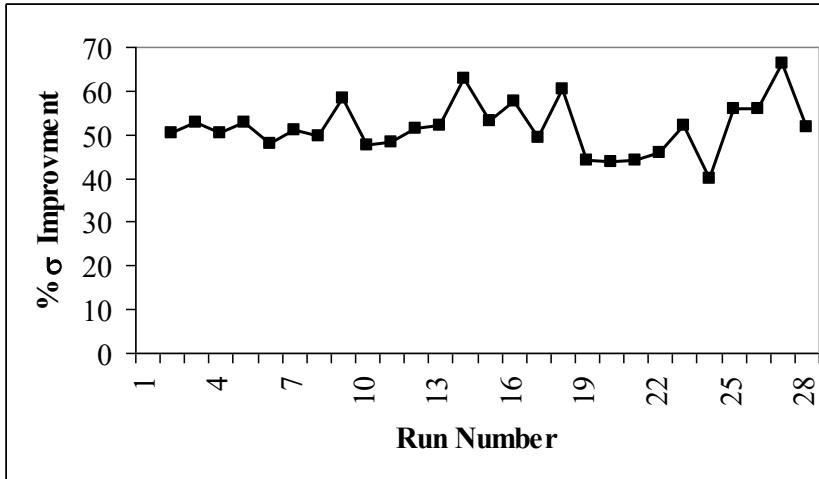


- *Predicted* improvement in CD distribution using 49-Zone low frequency compensation
- *Run ID4283 predictions:* Range 33 nm → 16 nm; Standard Deviation 6.3 nm → 3.1 nm
- Experimental verification performed with existing 49-zone control software

# Spectral Optimization for Each Data Set

- Average Improvement in  $\sigma = 3.9$  nm
- Corresponds to 51% improvement

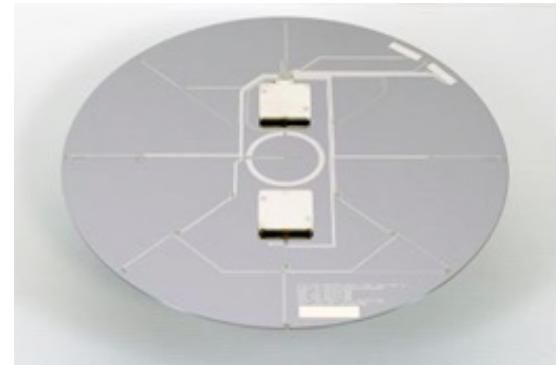
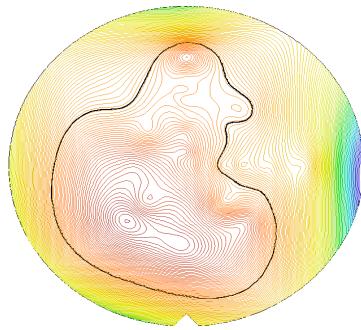
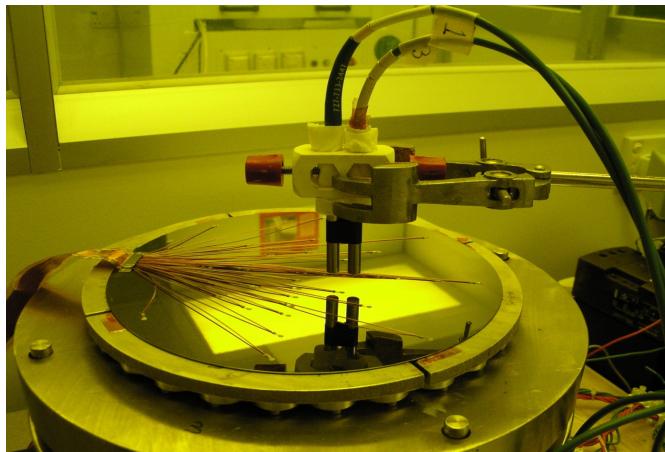
- Average Improvement in Range = 17 nm
- Corresponds to 44% improvement



# Real-time Temperature Control

# Motivations

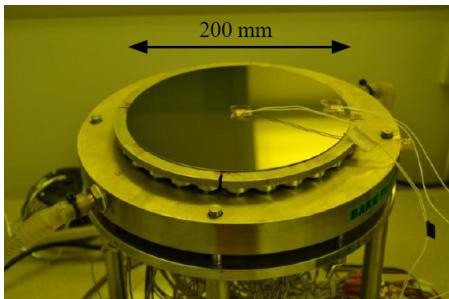
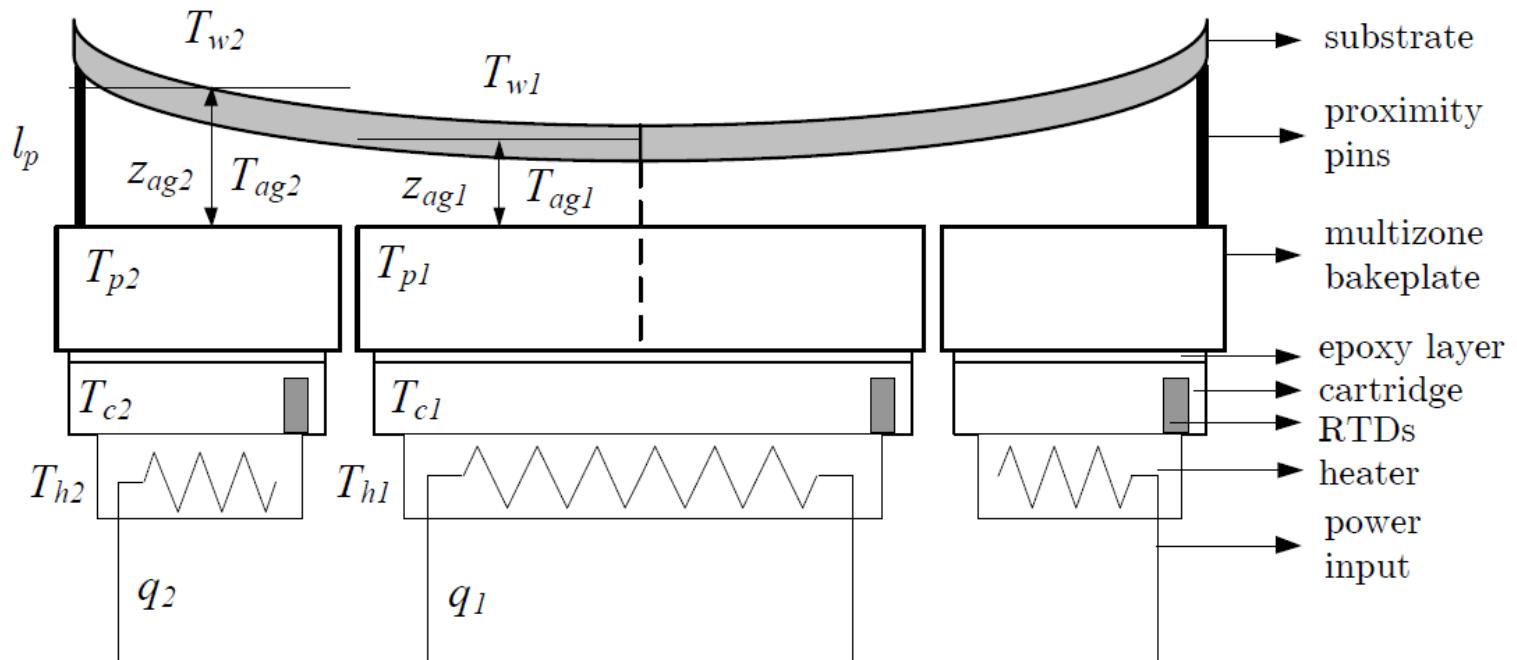
- Temperature control is critical in the processing of photoresist in lithography, currently it is an open-loop process, any correction is based on R2R.
- Real-time Temperature control not possible unless with an instrumented wafer; however production wafers are not instrumented.



Source: KLA Tencor

# Thermal Modeling

- Distributed Parameter Model (2-zone system):



*Ind. Eng. Chem. Res., 2013, 52 (13), pp 4805–4814*

# Thermal Modeling

- Energy balance equations:

$$C_w \dot{T}_w = q_w^{\text{in}} + q_w^{\text{out}} + q_w^{\text{top}} + q_w^{\text{bottom}}$$

$$C_{\text{ag}} \dot{T}_{\text{ag}} = q_{\text{ag}}^{\text{in}} + q_{\text{ag}}^{\text{out}} + q_{\text{ag}}^{\text{top}} + q_{\text{ag}}^{\text{bottom}}$$

$$C_p \dot{T}_p = q_p^{\text{in}} + q_p^{\text{out}} + q_p^{\text{top}} + q_p^{\text{bottom}}$$

$$C_c \dot{T}_c = q_c^{\text{in}} + q_c^{\text{out}} + q_c^{\text{top}} + q_c^{\text{bottom}}$$

$$C_h \dot{T}_h = q_h^{\text{in}} + q_h^{\text{out}} + q_h^{\text{top}} + q_h^{\text{bottom}} + q^{\text{input}}$$

where  $T$  is the temperature above the ambient,  $C$  the thermal capacitance,  $q^{\text{in}}$ ,  $q^{\text{out}}$ ,  $q^{\text{top}}$ , and  $q^{\text{bottom}}$  the heat flows into the element from inner zone, outer zone, top surface, and bottom surface, respectively,  $q^{\text{input}}$  the heater power and the subscripts w, ag, p, c, and h represent the wafer, the air gap, the bake plate, the cartridge, and the heater, respectively.

In the system, the wafer and the bake plate can be discretized into  $N$  zones to simulate their temperature response. For each discrete element, heat will be transferred from the adjacent inner and outer elements. We have

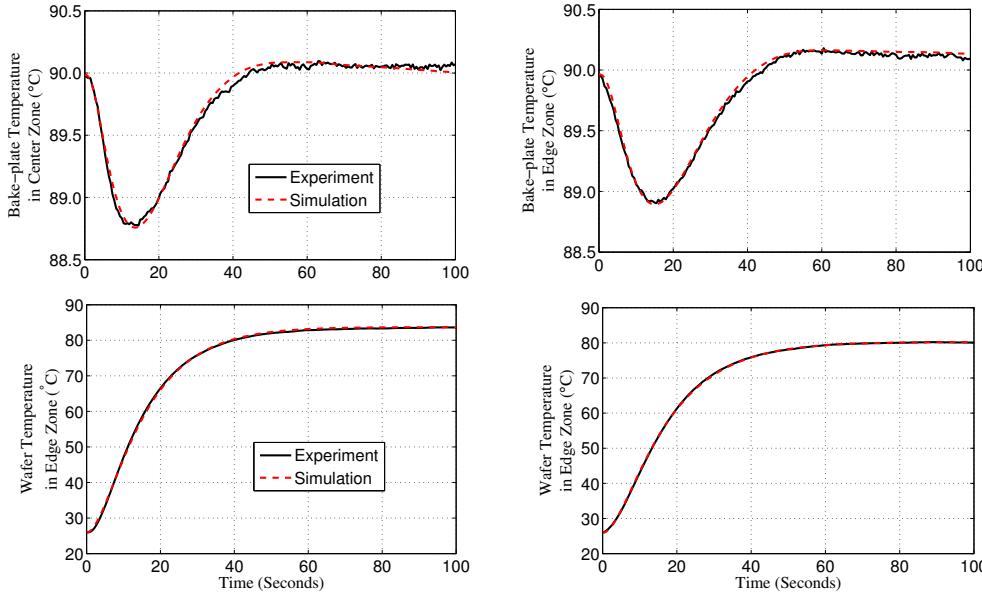
$$q_i^{\text{in}} = k A_i^{\text{side}} \frac{T_{i-1} - T_i}{r_{i-1}} \quad q_i^{\text{out}} = k A_{i+1}^{\text{side}} \frac{T_{i+1} - T_i}{r_i} \quad q_n^{\text{out}} = h_{\text{lm}} \cdot A_{\text{lm}}^{\text{side}} (-T_a)$$

$$q_n^{\text{top}} = h^{\text{top}} \cdot A_w^{\text{top}} (-T_w) \quad q_w^{\text{bottom}} = -k_{\text{ag}} A_{\text{ag}} \left. \frac{\partial T_{\text{ag}}}{\partial z_{\text{ag}}} \right|_{\text{boundary}} \quad q_n^{\text{bottom}} = h_{\text{bottom}} \cdot A_h^{\text{bottom}} \cdot (-T_h)$$

# Thermal Modeling

- State-space Model:

$$\dot{T} = \begin{bmatrix} F_{ww} & F_{wag} & 0_{NN} & 0_{NN} & 0_{NN} \\ F_{agw} & F_{agag} & F_{agp} & 0_{NN} & 0_{NN} \\ 0_{NN} & F_{pag} & F_{pp} & F_{pc} & 0_{NN} \\ 0_{NN} & 0_{NN} & F_{cp} & F_{cc} & F_{ch} \\ 0_{NN} & 0_{NN} & 0_{NN} & F_{hc} & F_{hh} \end{bmatrix} \cdot \begin{bmatrix} T_w \\ T_{ag} \\ T_p \\ T_c \\ T_h \end{bmatrix} + \begin{bmatrix} 0_N \\ 0_N \\ 0_N \\ 0_N \\ G_{hh} \end{bmatrix} \cdot q^{\text{input}}$$

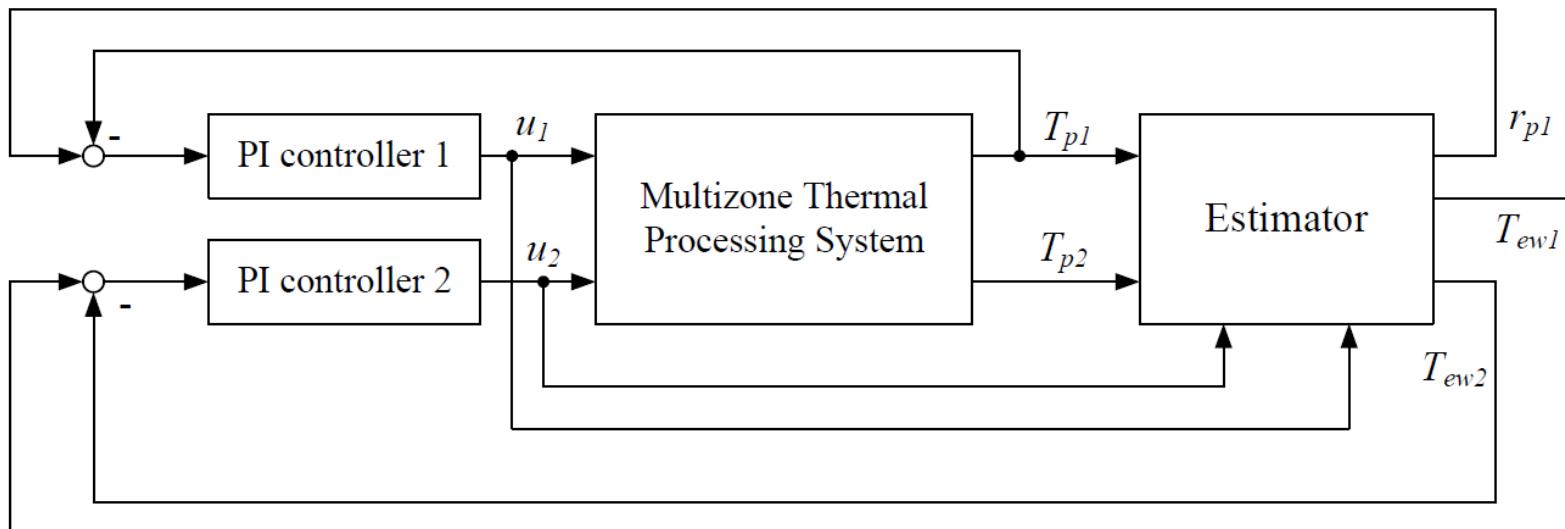


**Table 1. Physical Parameters of the Thermal Processing System<sup>16</sup>**

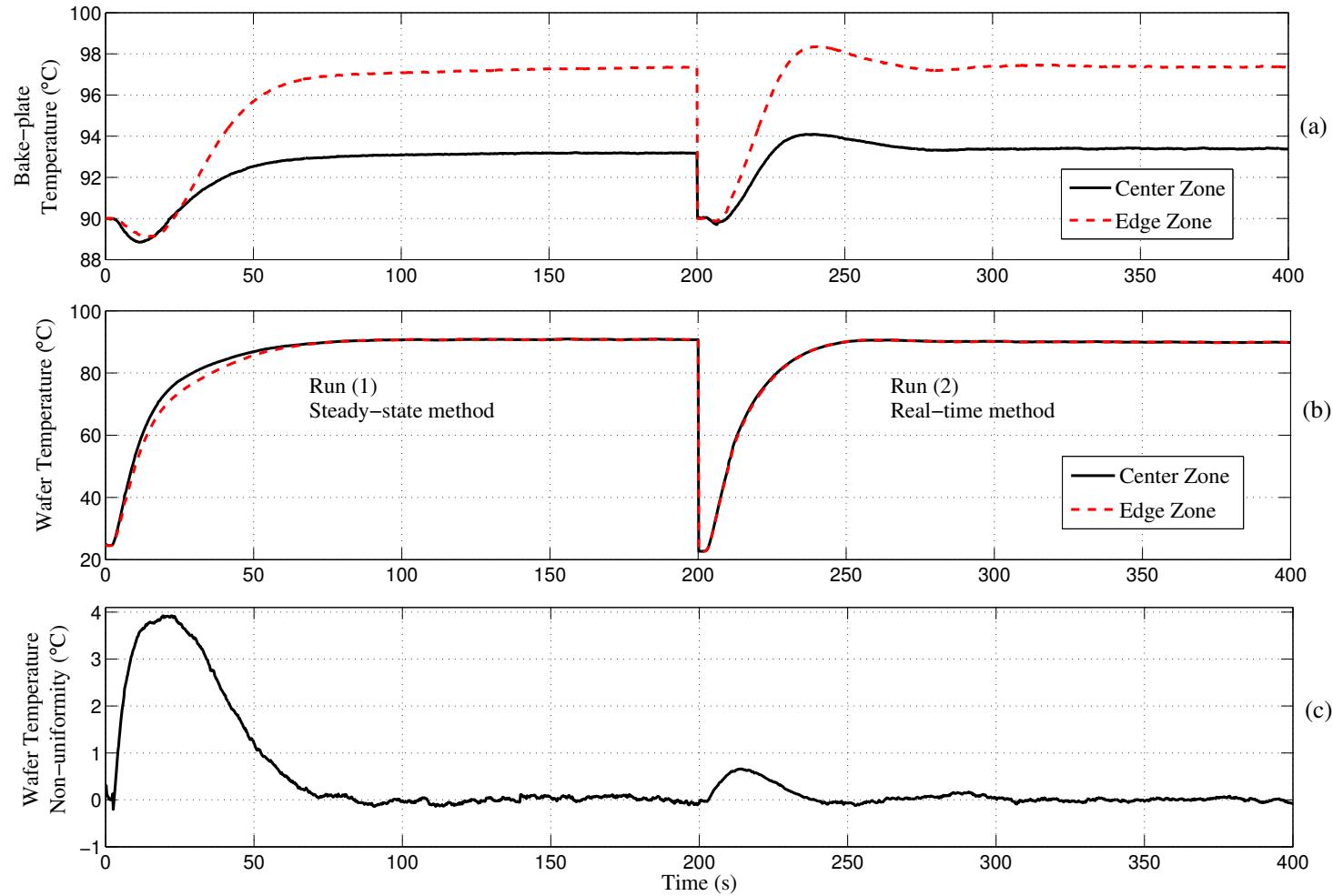
	property	value
wafer (silicon)	density, $\rho$	2330 kg m <sup>-3</sup>
	specific heat capacity, $c_v$	750 J K <sup>-1</sup> kg <sup>-1</sup>
	thermal conductivity, $k$	99 W m <sup>-1</sup> K <sup>-1</sup>
	convection coefficient, $h$	3.3824 W m <sup>-2</sup> K <sup>-1</sup>
	thickness, $z$	0.700 mm
air	diameter	200 mm
	density, $\rho$	1.1 kg m <sup>-3</sup>
	specific heat capacity, $c_v$	1000 J K <sup>-1</sup> kg <sup>-1</sup>
	thermal conductivity, $k$	0.03 W m <sup>-1</sup> K <sup>-1</sup>
bake plate (aluminum)	density, $\rho$	2700 kg m <sup>-3</sup>
	specific heat capacity, $c_v$	917 J K <sup>-1</sup> kg <sup>-1</sup>
	thermal conductivity, $k$	250 W m <sup>-1</sup> K <sup>-1</sup>
	convection coefficient, $h$	7.271 W m <sup>-2</sup> K <sup>-1</sup>
	thickness, $z$	6.8 mm
epoxy	diameter	220 mm
	thermal conductivity, $k$	0.35 W m <sup>-1</sup> K <sup>-1</sup>
cartridge (aluminum)	thickness, $z$	0.02 mm
	density, $\rho$	2700 kg m <sup>-3</sup>
	specific heat capacity, $c_v$	917 J K <sup>-1</sup> kg <sup>-1</sup>
	thermal conductivity, $k$	250 W m <sup>-1</sup> K <sup>-1</sup>
	convection coefficient, $h$	4.86 W m <sup>-2</sup> K <sup>-1</sup>
heater (aluminum)	thickness, $z$	4.4 mm
	diameter	10 mm
	density, $\rho$	2700 kg m <sup>-3</sup>
	specific heat capacity, $c_v$	917 J K <sup>-1</sup> kg <sup>-1</sup>
	thermal conductivity, $k$	250 W m <sup>-1</sup> K <sup>-1</sup>
	convection coefficient, $h$	2.7828 W m <sup>-2</sup> K <sup>-1</sup>
	thickness, $z$	5.4 mm
	diameter	6 mm

# Real-time Temperature Control

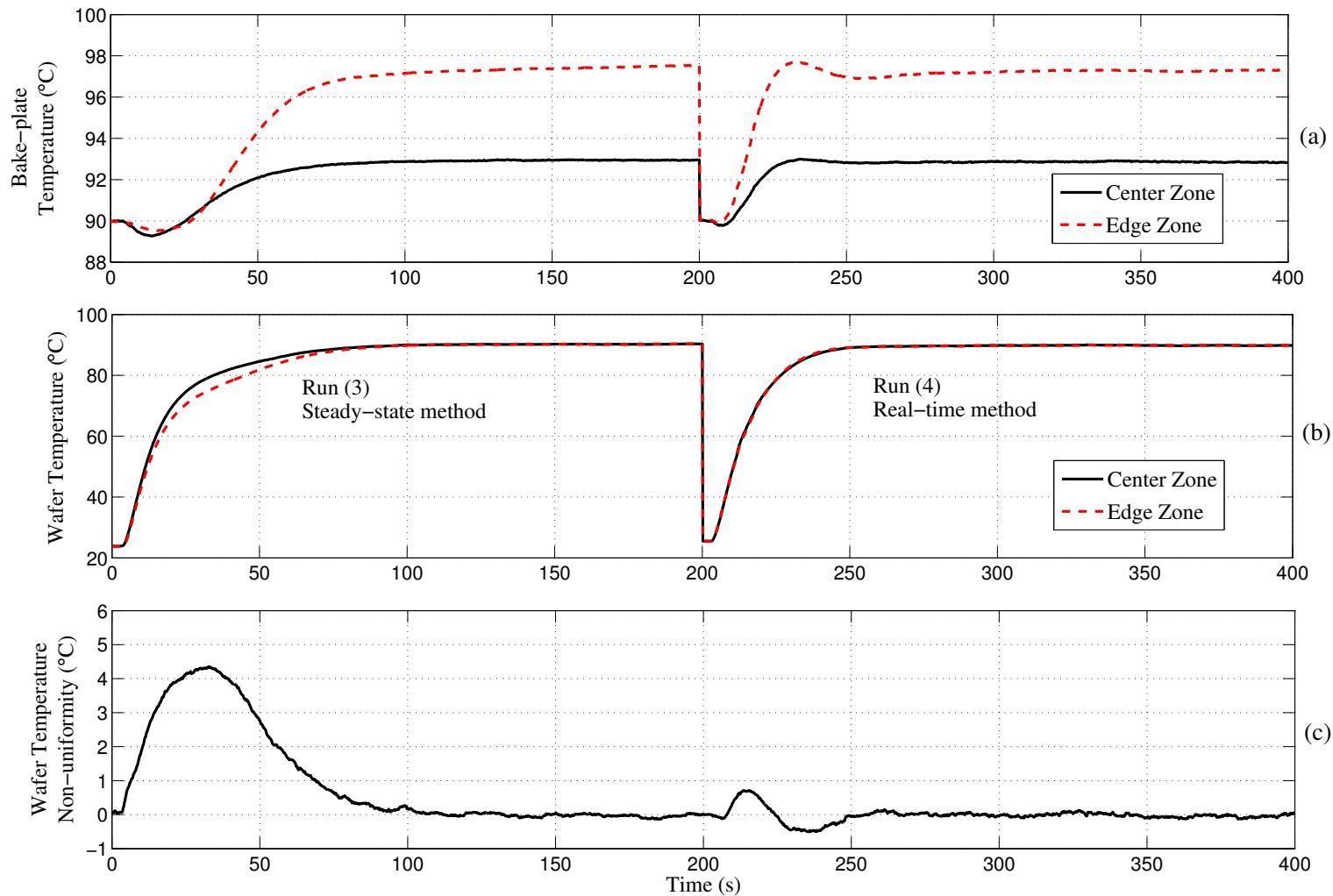
- Proposed approach:
  - Estimate the air-gap between wafer and plate in each zone based on the plate temperature via grey-box modeling.
  - Control the wafer temperature using the plate based on the known air-gap.



# Real-time Temperature Control (flat wafer)



# Real-time Temperature Control (warped wafer)



# Results: Estimated warpage, temperature non-uniformity

Table 2: Estimated air gap thickness and wafer warpage using the real-time control method with the proximity pin height of  $210\mu\text{m}$

wafer	Exp. run	<i>Estimated air gap thickness</i>		<i>Deviation from flat wafer</i>		Extracted wafer warpage ( $\mu\text{m}$ )
		center zone ( $\mu\text{m}$ )	edge zone ( $\mu\text{m}$ )	center zone ( $\mu\text{m}$ )	edge zone ( $\mu\text{m}$ )	
Flat wafer	(2)	208	214	-2	4	4
$70\mu\text{m}$ warpage	(4)	146	182	-64	-28	72
$140\mu\text{m}$ warpage	(6)	86	158	-124	-52	144

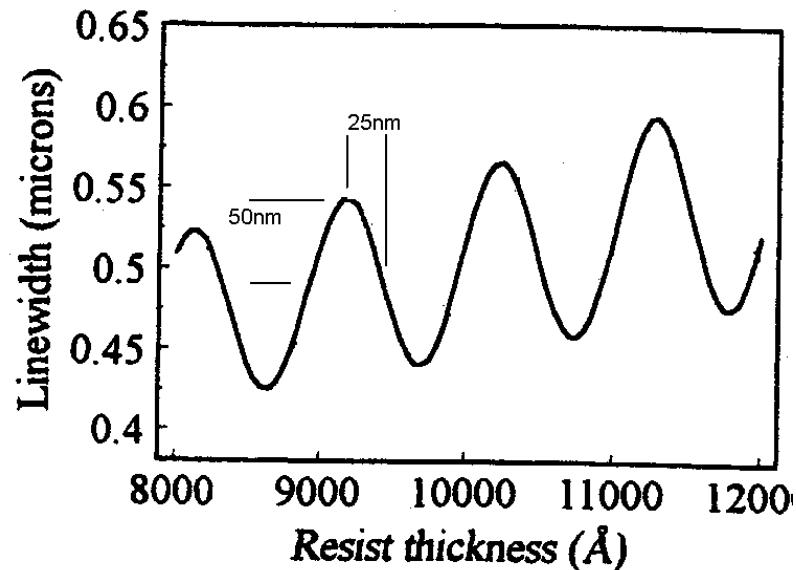
Table 3: Performance comparison of the steady-state wafer temperature control method<sup>4</sup> and our proposed method

Wafer	Method	Exp. run	Maximum nonuniformity ( $^{\circ}\text{C}$ )	RMS
Flat wafer	Steady-state	(1)	3.93	1.48
	Real-time	(2)	0.66	0.18
$70\mu\text{m}$ warpage	Steady-state	(3)	4.35	1.78
	Real-time	(4)	0.71	0.20
$140\mu\text{m}$ warpage	Steady-state	(5)	4.68	1.62
	Real-time	(6)	1.07	0.29

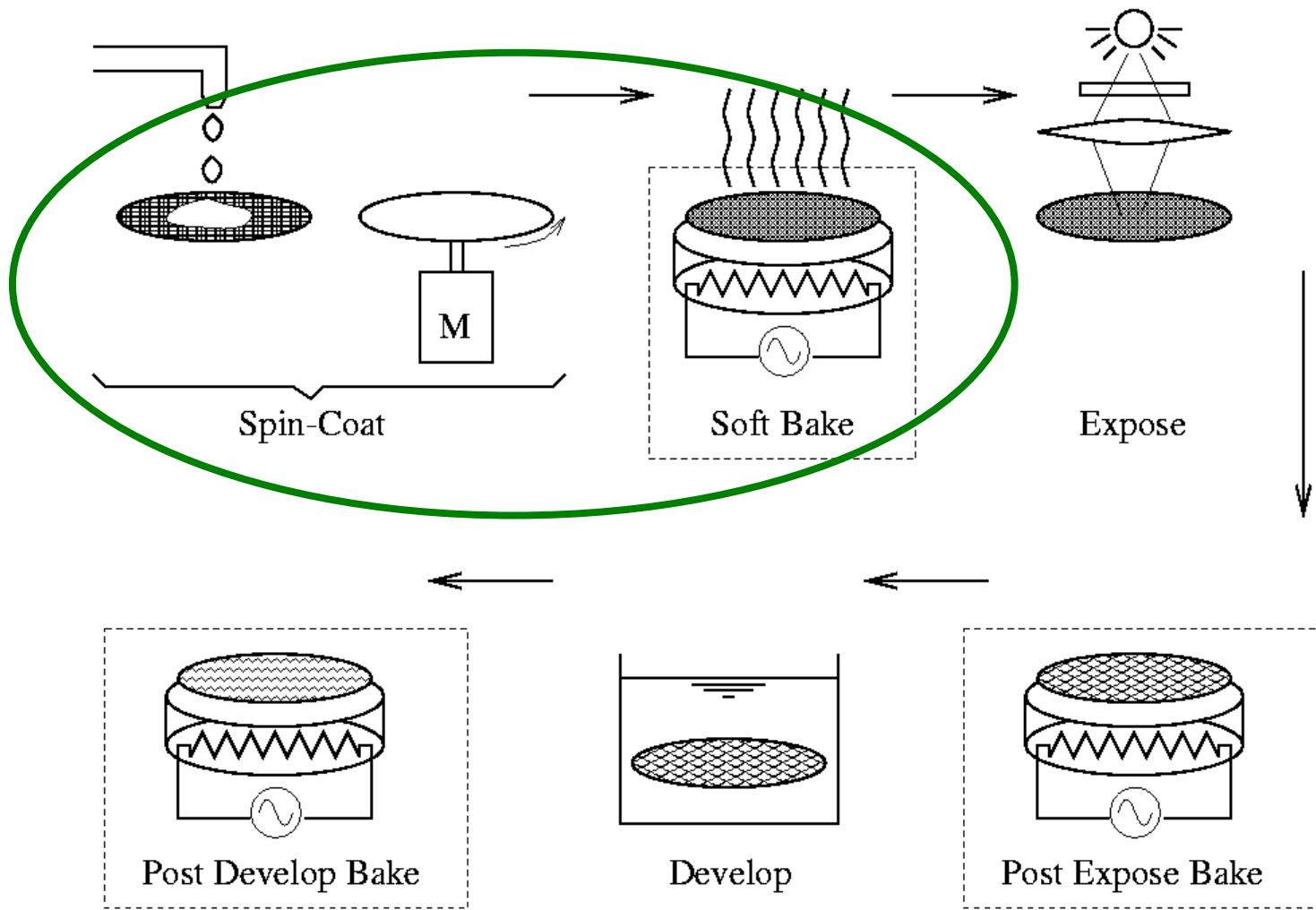
# Real-time Control of Photoresist Properties

# Monitoring and Control of Photoresist Film Properties

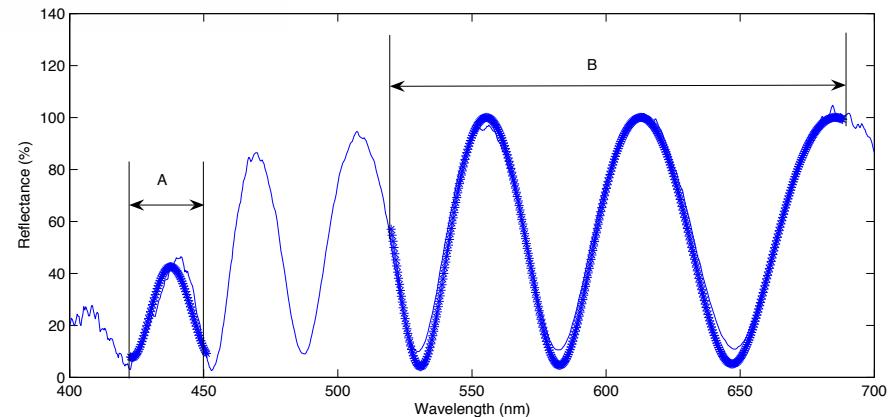
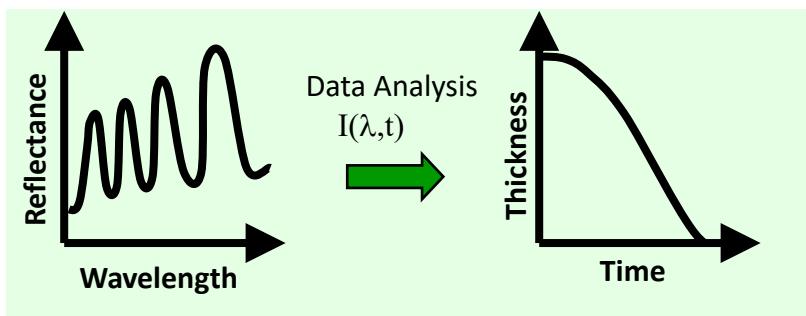
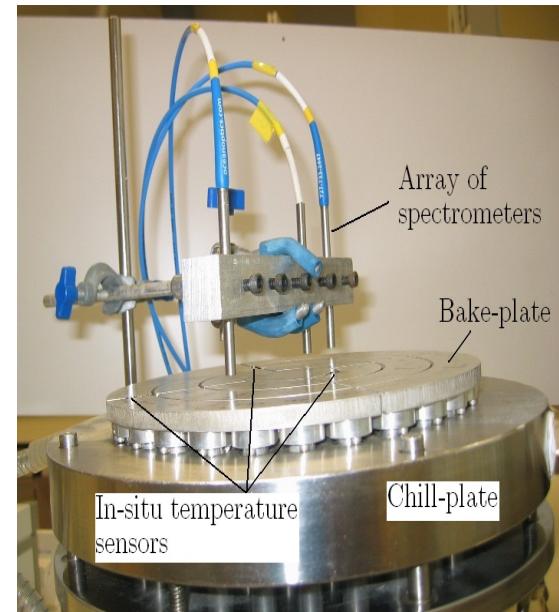
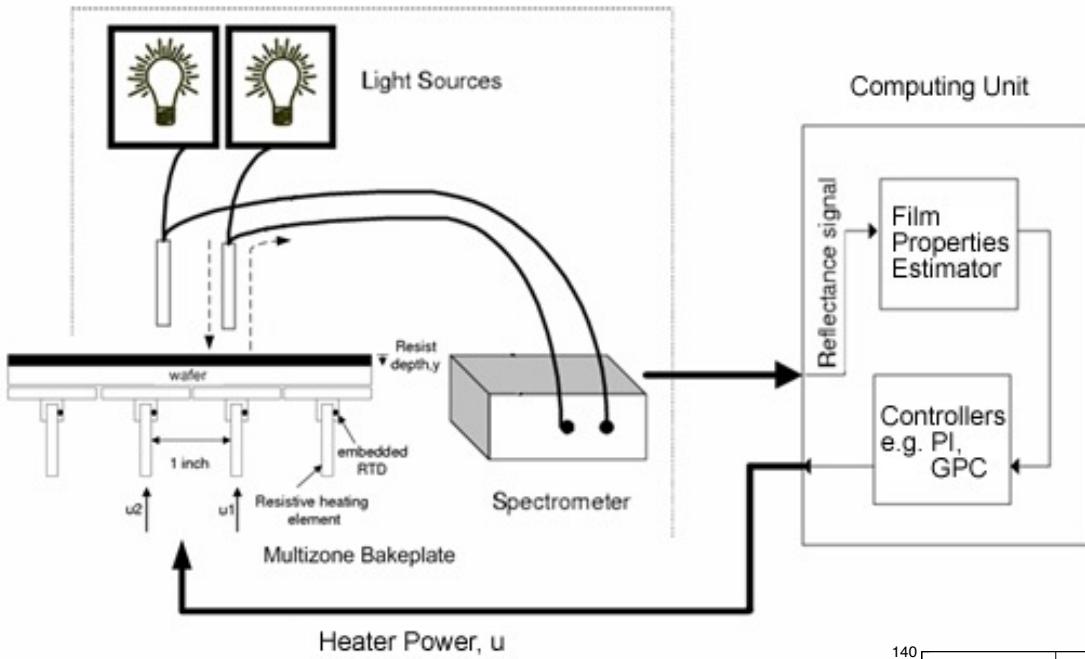
- Motivations: controlling various photoresist properties that have an impact on CD uniformity.
- Examples .
  - Photoresist thickness.
  - Photoresist extinction coefficient.
  - Photoresist development rate.



# The Lithography Sequence



# Experimental Setup



# Estimation of Resist Properties

- For an absorbing photoresist film with a complex index of refraction (function of wavelength), the reflectance intensity is given by

$$h(\lambda, k, y) = \frac{\rho_{12}^2 e^{2k\eta} + \rho_{23}^2 e^{-2k\eta} + 2\rho_{12}\rho_{23} \cos(\alpha)}{e^{2k\eta} + \rho_{12}^2 \rho_{23}^2 e^{-2k\eta} + 2\rho_{12}\rho_{23} \cos(\alpha)}$$

- where

$$\begin{aligned} \alpha &= \phi_{23} + \phi_{12} + 2n_r\eta & \phi_{12} &= \arctan \frac{2k}{n_r^2 + k^2 - 1}, \\ \rho_{12}^2 &= \frac{(n_a - n_r)^2 + k^2}{(n_a + n_r)^2 + k^2}, & \phi_{23} &= \arctan \frac{2kn_s}{n_r^2 + k^2 - n_s^2}, \\ \rho_{23}^2 &= \frac{(n_s - n_r)^2 + k^2}{(n_s + n_r)^2 + k^2}, & \eta &= \frac{2\pi}{\lambda}y; \end{aligned}$$

# Estimation of Resist Properties

- Least square estimation of the resist thickness,  $\hat{y}$ , can be obtained as follows:

$$h(\lambda, y) = h(\lambda, y_0) + \frac{\partial h}{\partial y} \Big|_{\lambda, y_0} \Delta y$$

$$\hat{y} = y_0 + \Delta y \quad \Delta y = \left( \frac{\partial h^T}{\partial y} \frac{\partial h}{\partial y} \right)^{-1} \frac{\partial h^T}{\partial y} (h - h_0)$$

- The extinction coefficient,  $\hat{k}$ , can then be estimated at the shorter wavelengths:

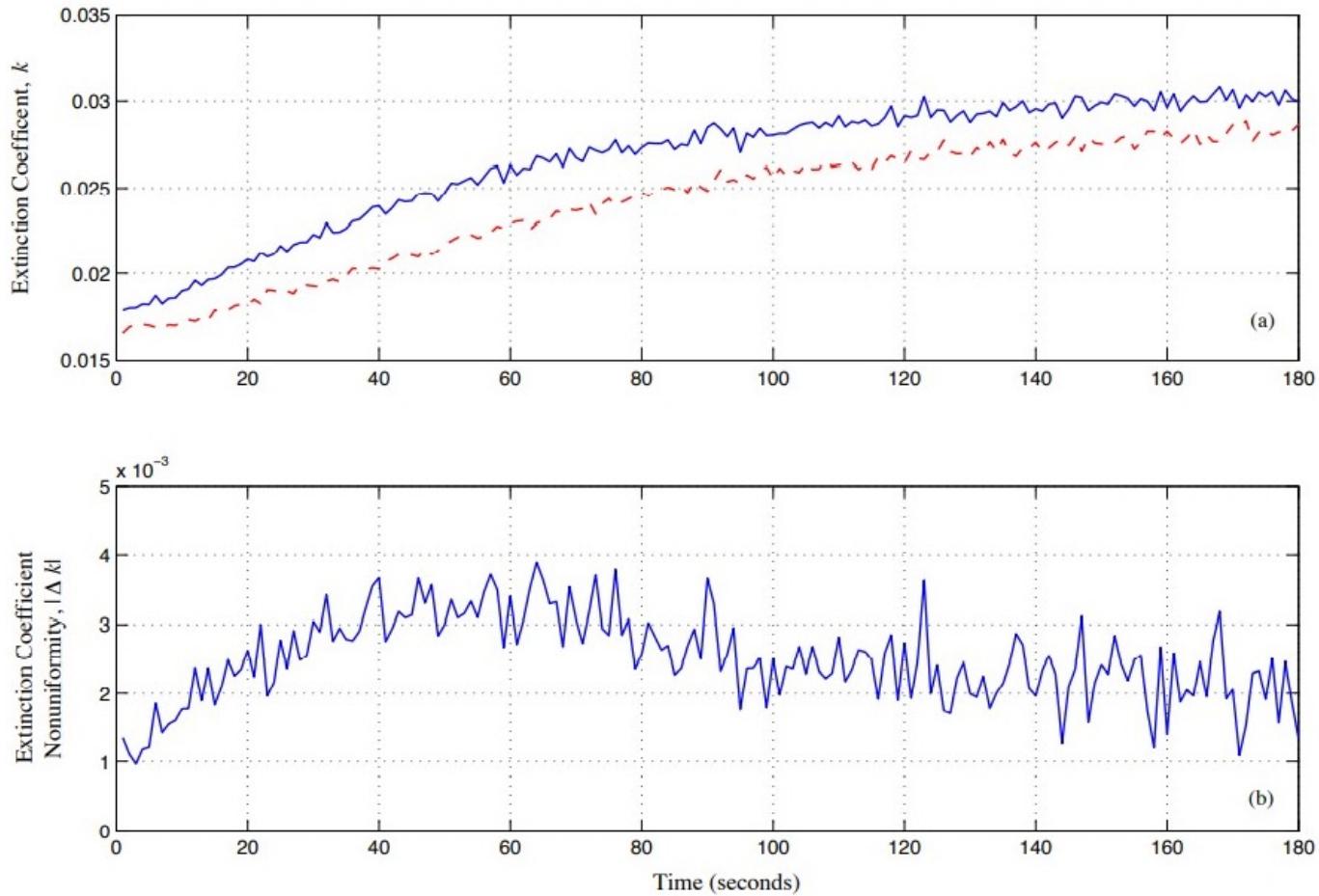
$$h(\lambda, k) = h(\lambda, k_0) + \frac{\partial h}{\partial k} \Big|_{\lambda, k_0} \Delta k$$

$$\hat{k} = k_0 + \Delta k \quad \Delta k = \left( \frac{\partial h^T}{\partial k} \frac{\partial h}{\partial k} \right)^{-1} \frac{\partial h^T}{\partial k} (h - h_0)$$

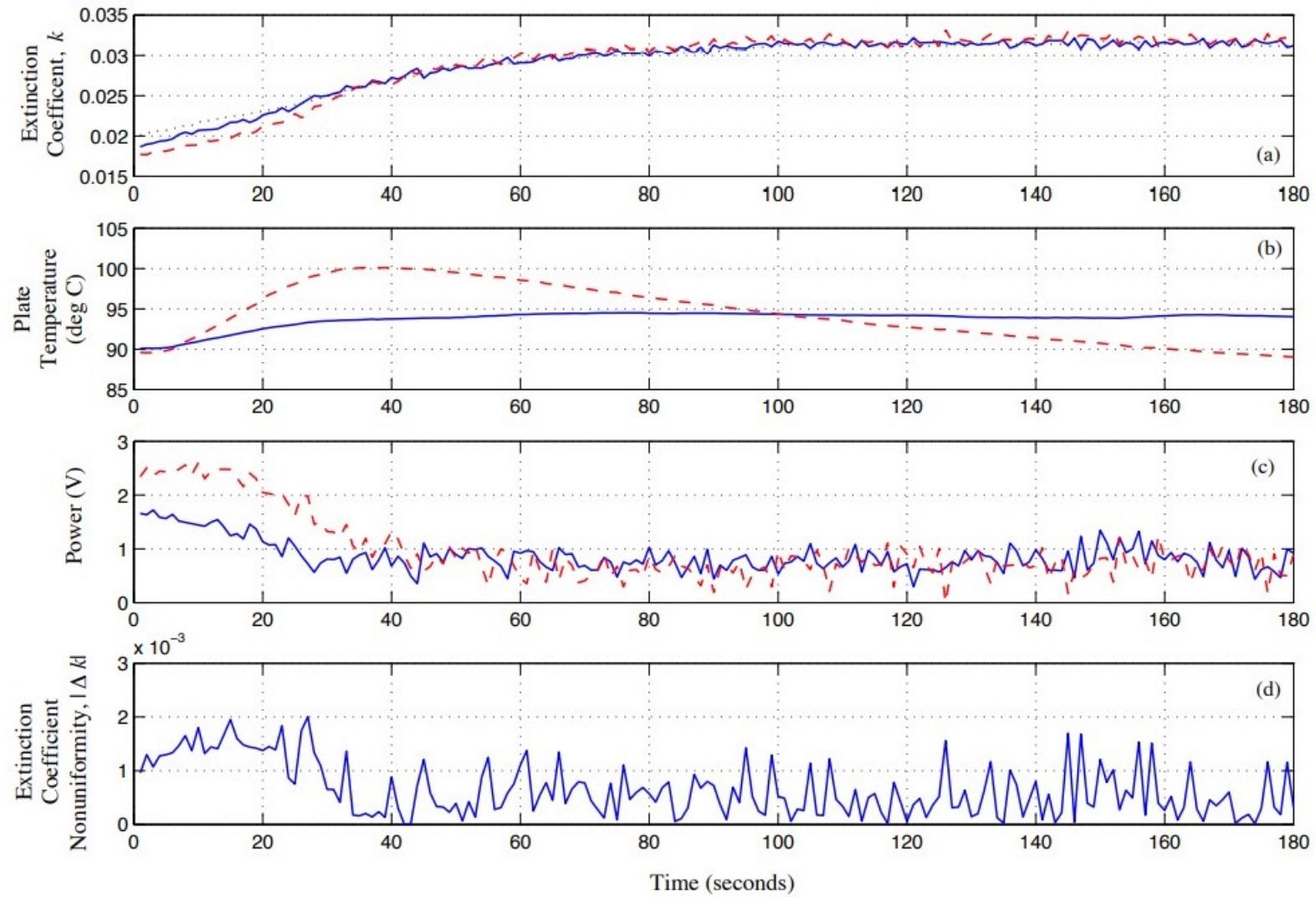
# Conventional Softbake: Extinction Coefficient Control

Uniform Temperature results in non-uniform extinction coefficient

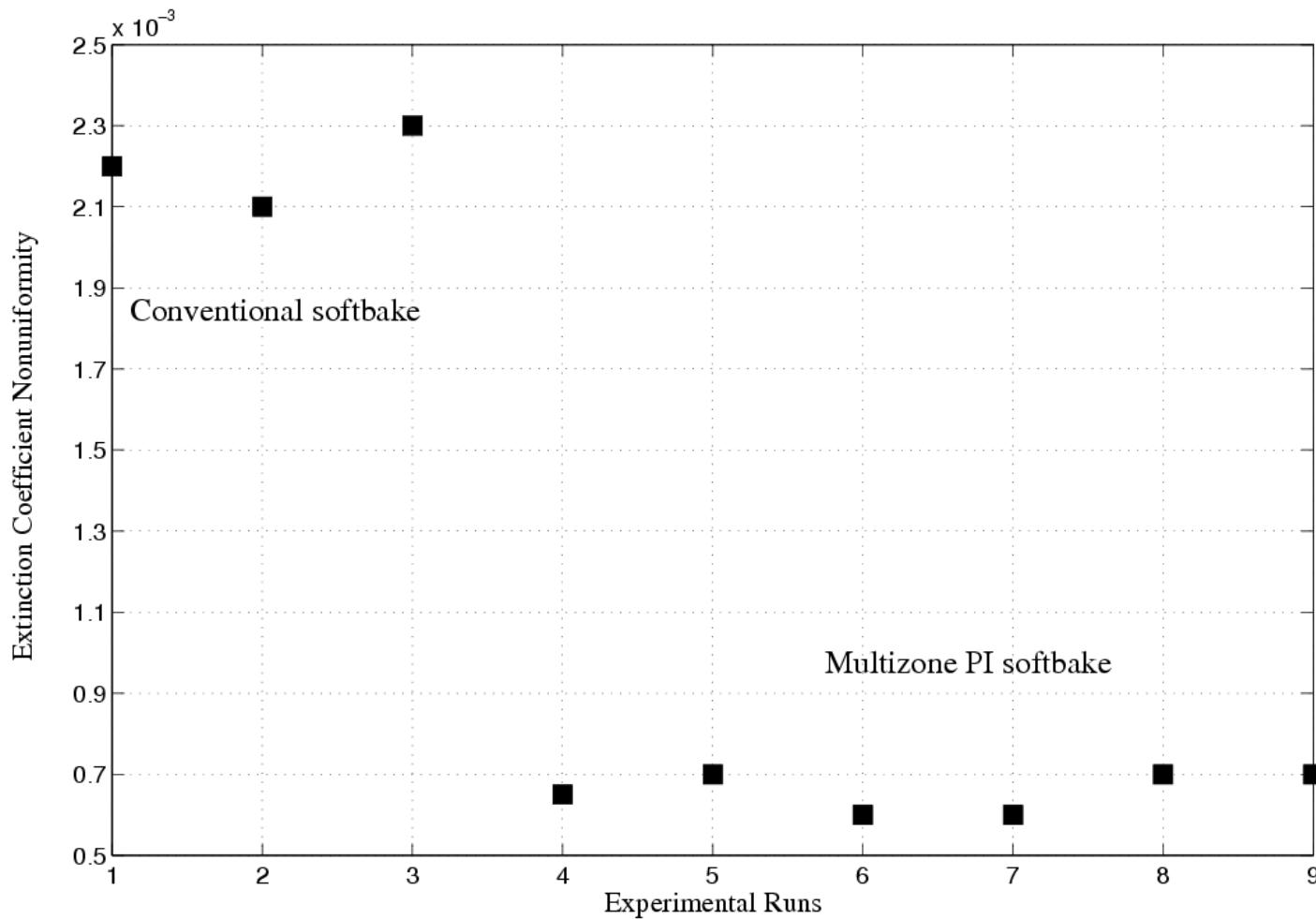
Need for distributed heating.



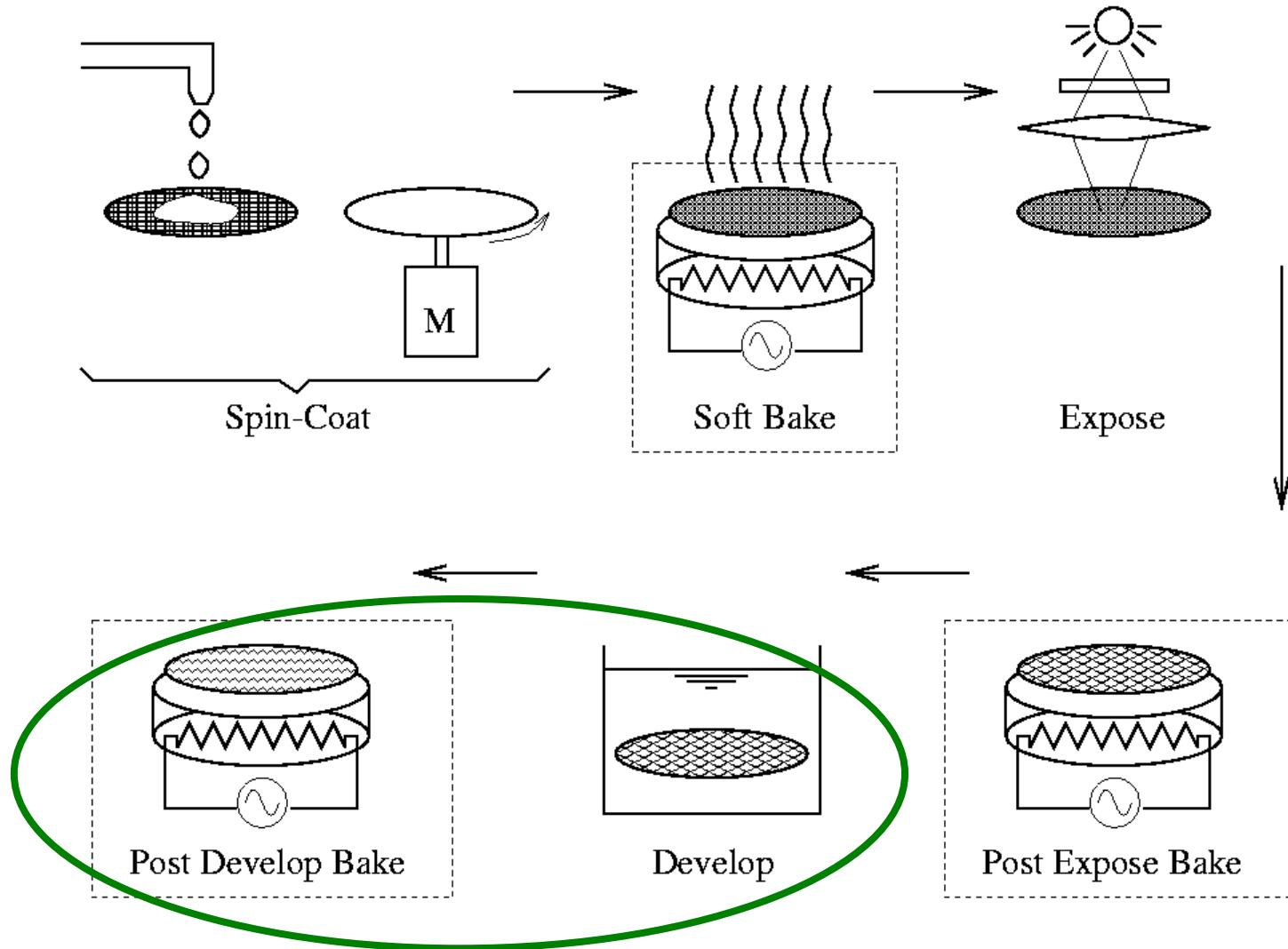
# Real-time control of Photoresist Extinction Coefficient Uniformity



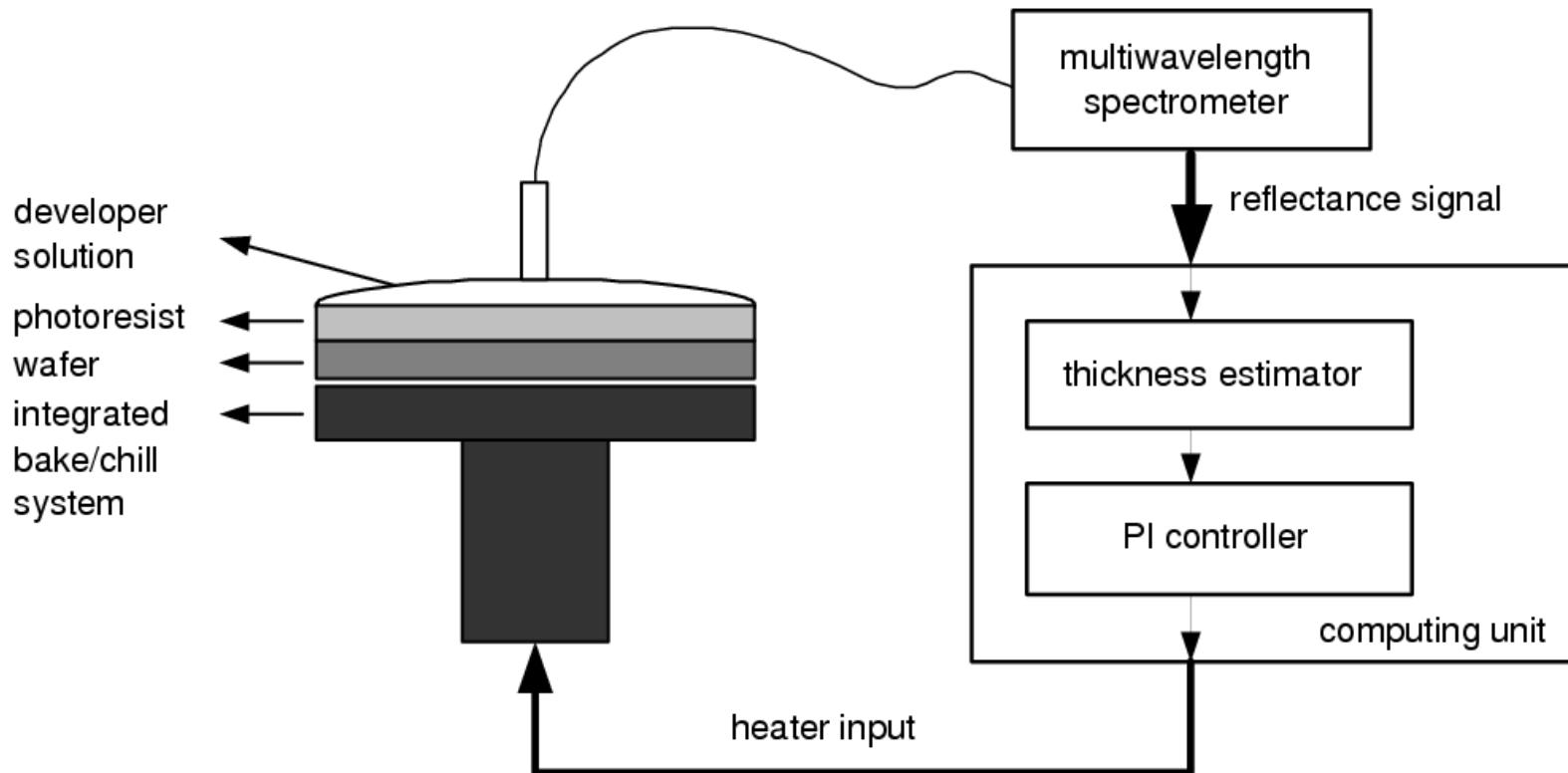
# Experimental Runs



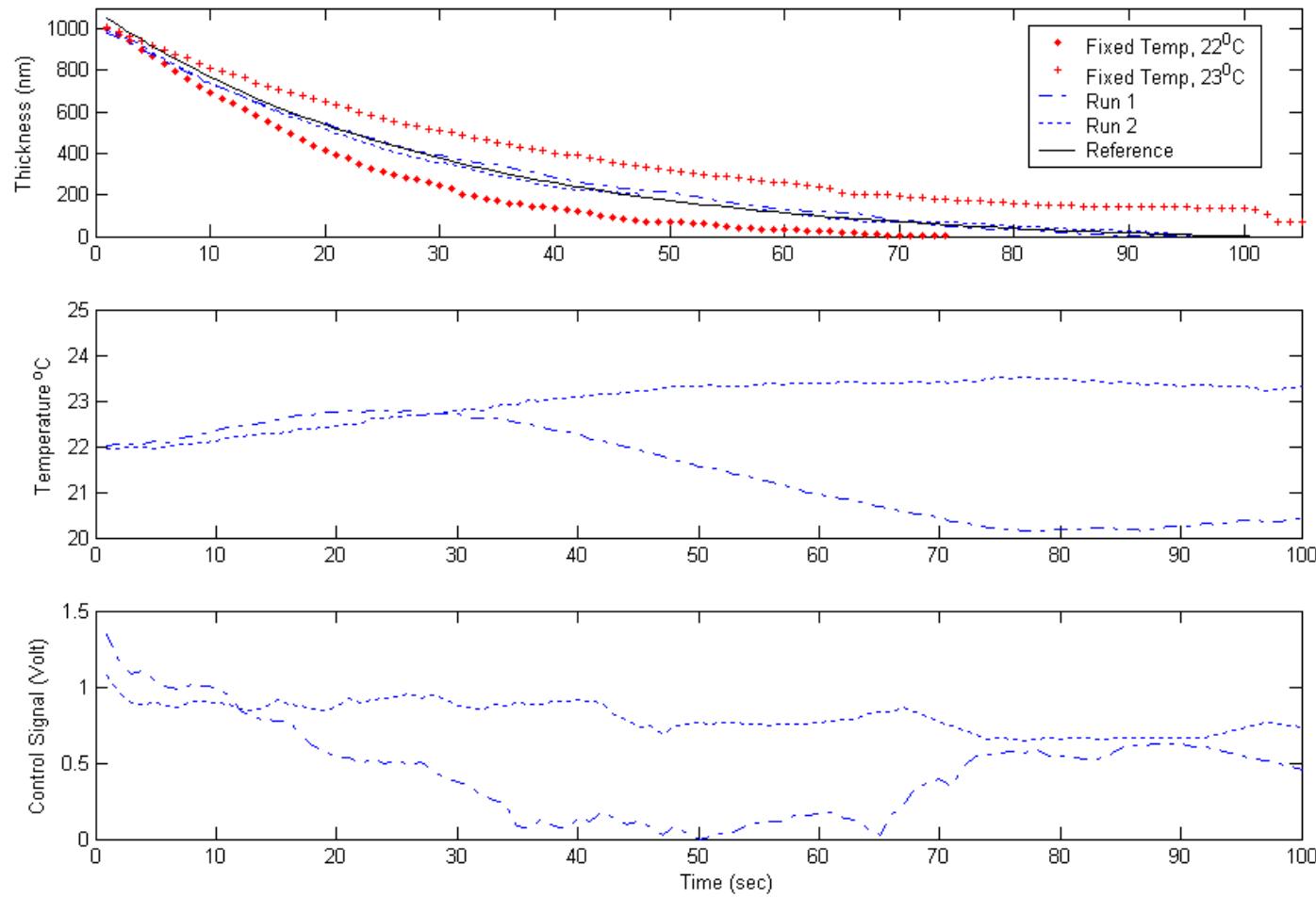
# The Lithography Sequence



# Real-Time Control of Photoresist Development

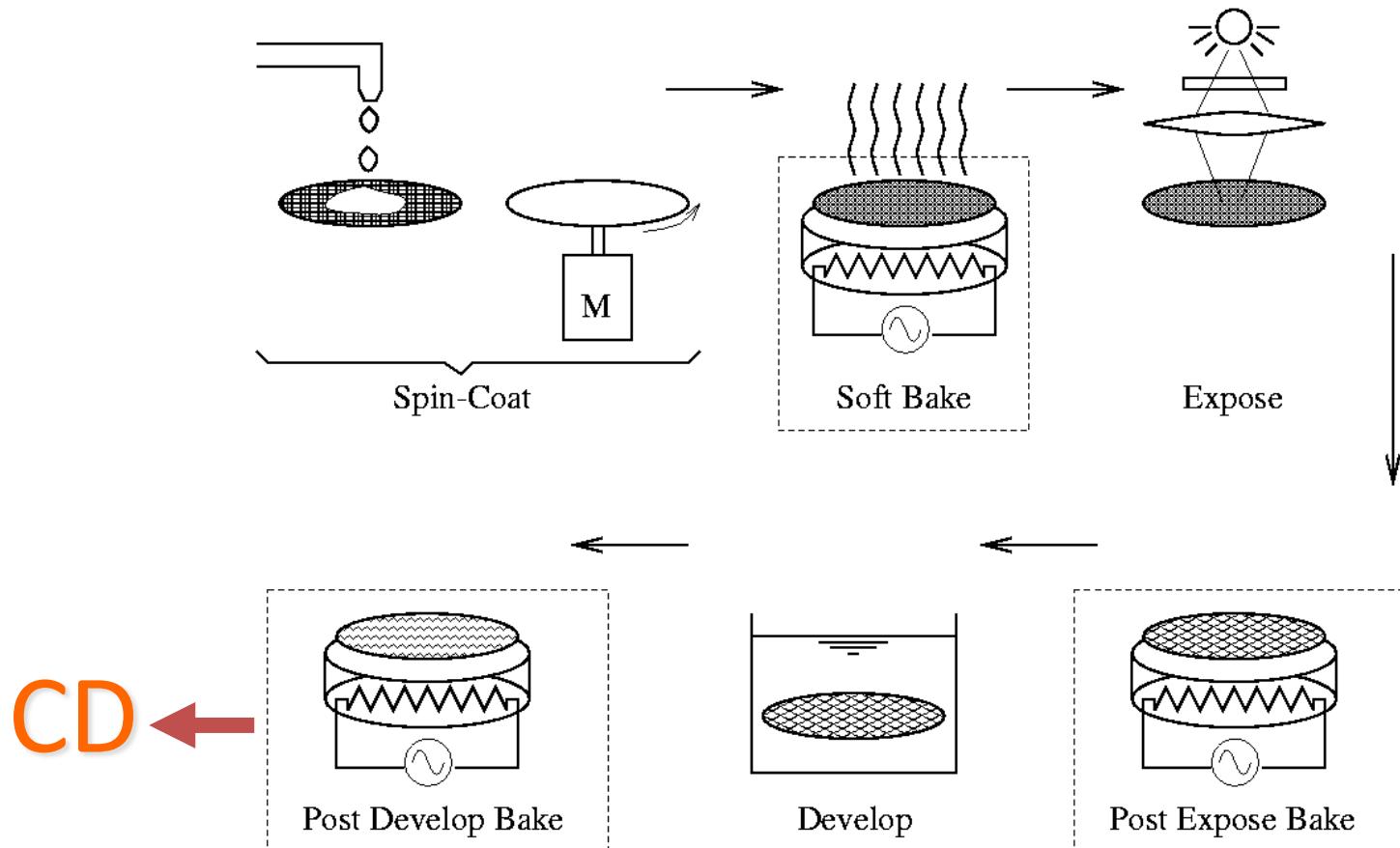


# Real-time Control of Photoresist Development Process



# Real-time CD Uniformity Control

# The Lithography Sequence



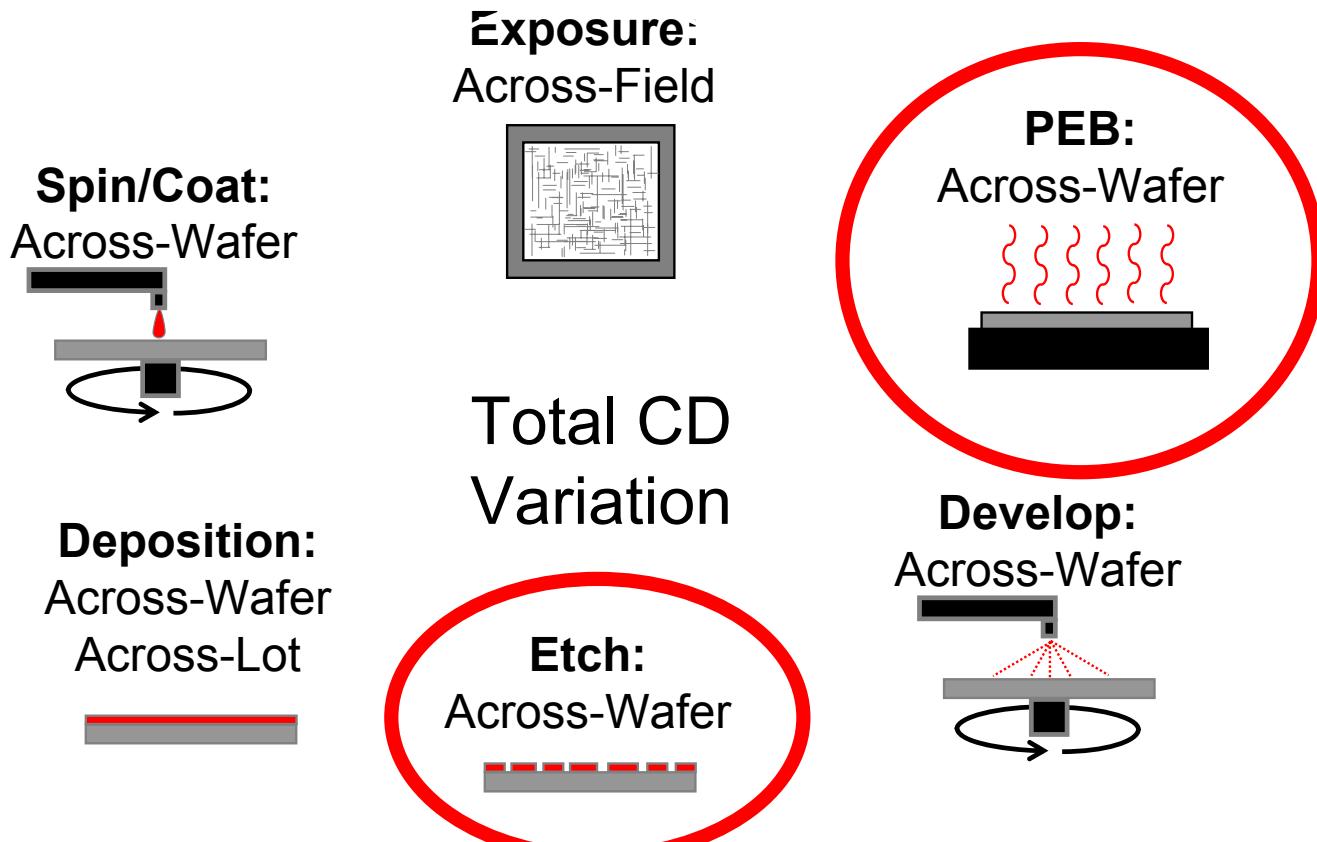
- Current generation of photoresist especially sensitive to temperature variation.
- Variation of feature size (Linewidth variation),  $\Delta CD: 1-10\text{nm}/^{\circ}\text{C}$ .

# Current Approach

Run-to-run (R2R) control is the dominant strategy in the manufacturing of microelectronics circuits.

1. while in-situ, real-time sensors are broadly deployed for detection and response to key equipment failure modes in many manufacturing steps, their application for real-time CD control are limited due primarily to a lack of control authority at the tool level;
2. in cases where these real-time sensors (e.g. scatterometer) are used to measure CD, correction is usually done in the subsequent processing steps (“feedforward control”) or in a R2R approach by changing the processing conditions for the next wafer (“feedback control”); and
3. in cases where real-time control is implemented in the lithography sequence, it is usually restricted to in-situ measurement of the intermediate variables (e.g. resist thickness, wafer temperature), and not on the actual CD of interest.

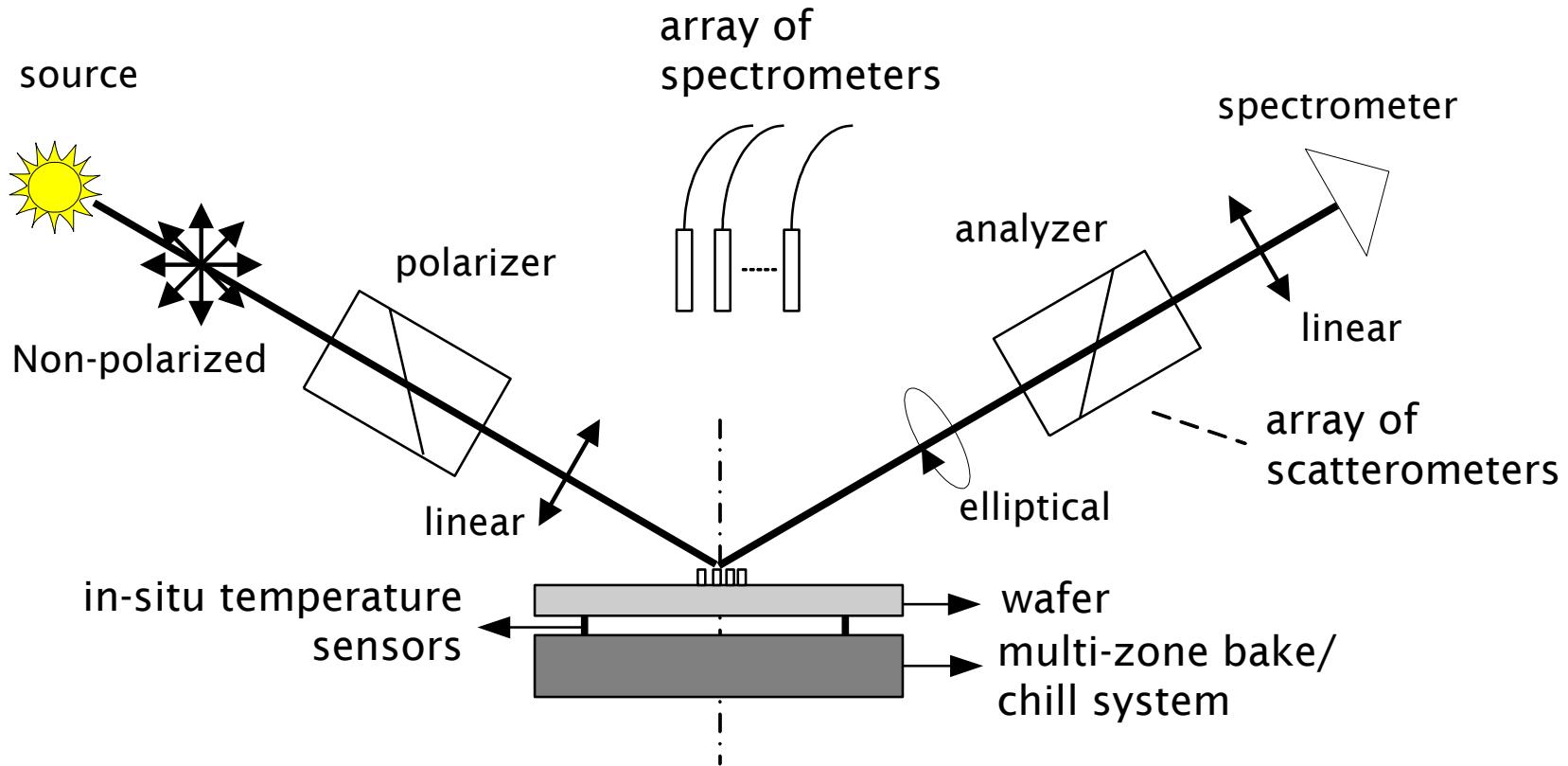
# Sources of CD variations



Systematic CD variation components with different frequencies are combined.

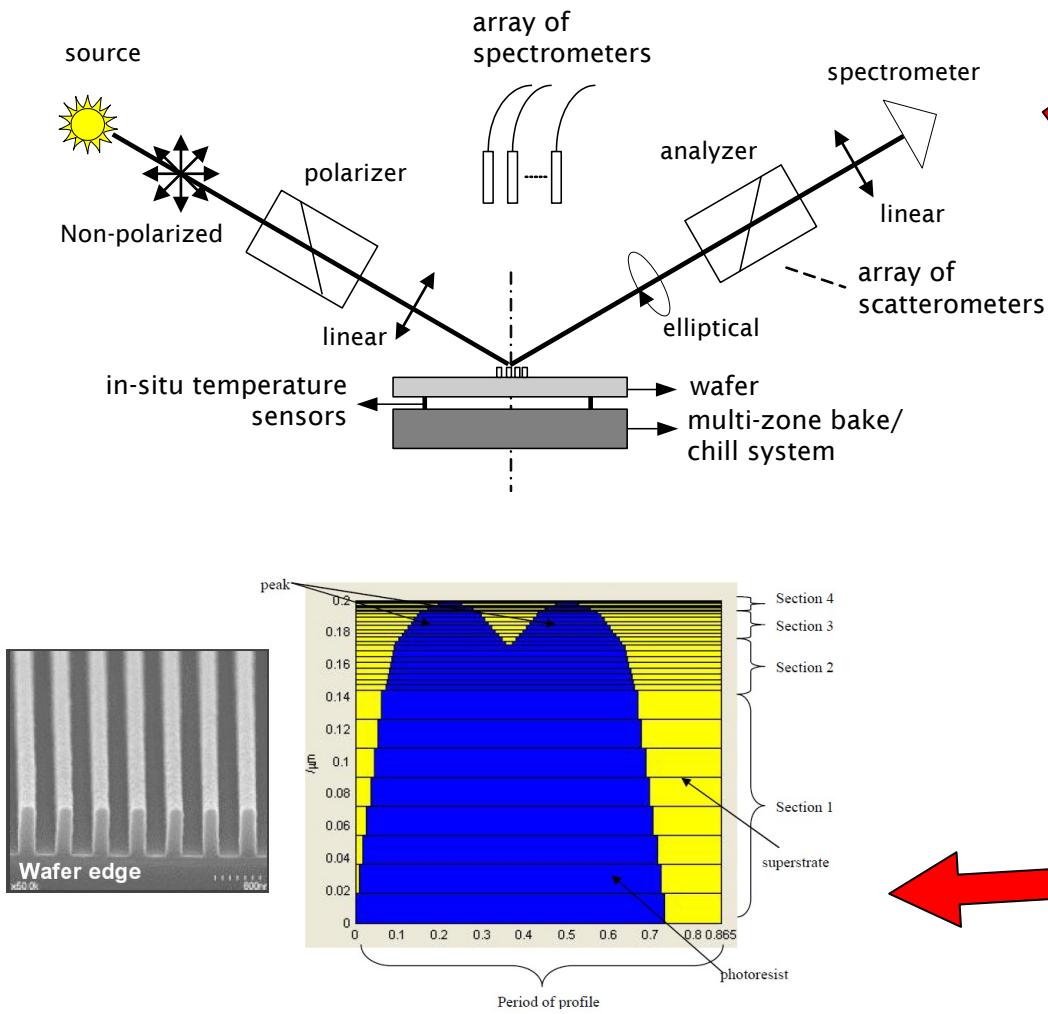
Source: Spanos, AIChE, 2005

# Proposed Approach

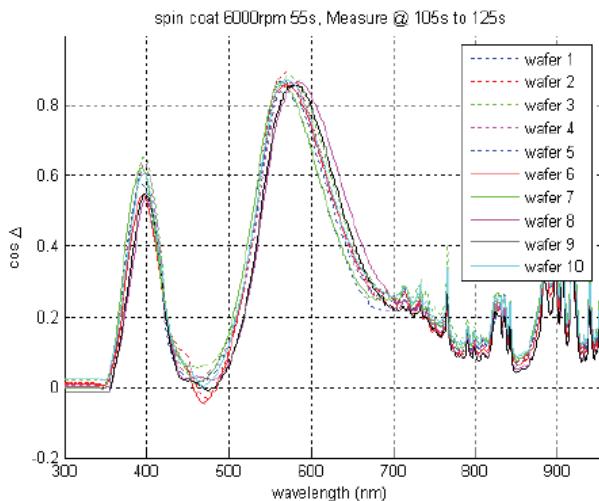


- Sensor: Scatterometer for CD measurement
- Actuator: Programmable Multi-zone thermal processing system

# Proposed Approach

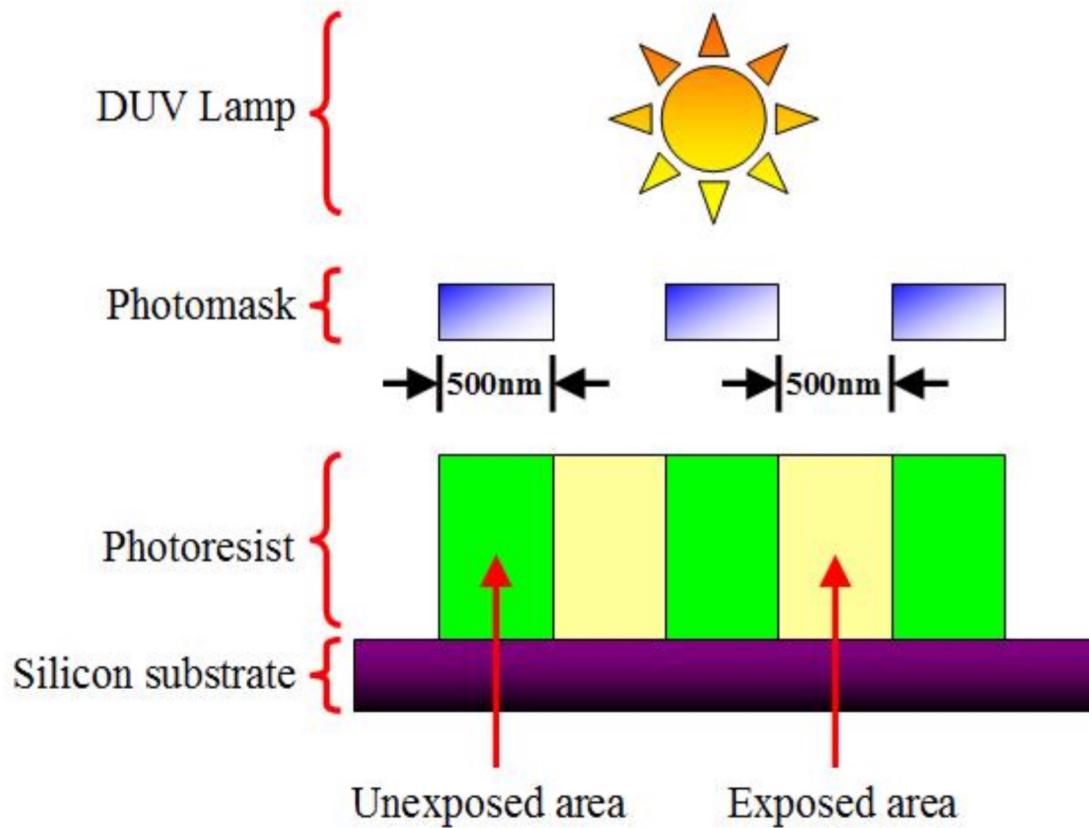


Signature plots from scatterometry



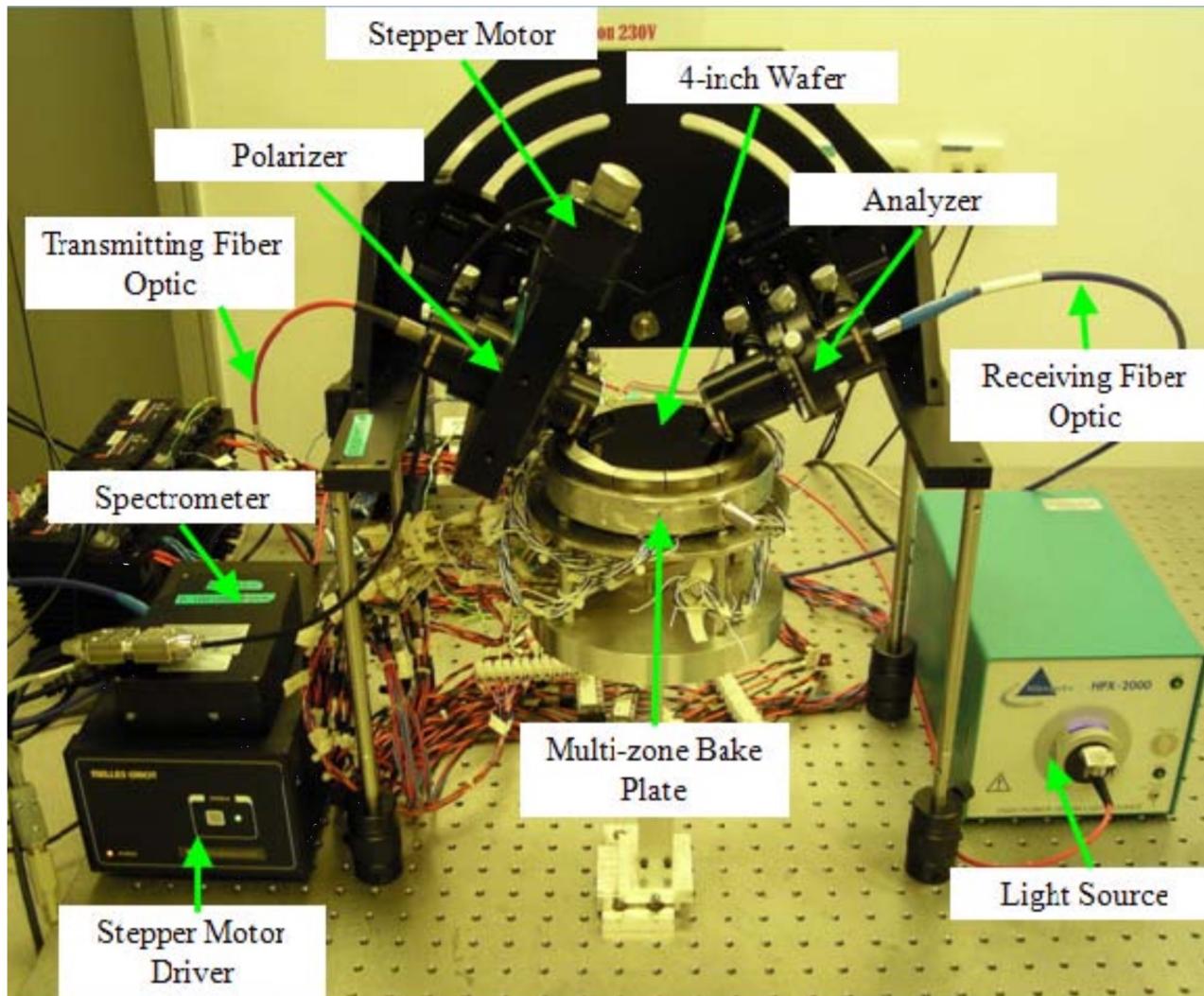
Reconstruction of profile (forward & inverse problems)

# Latent Image Formation

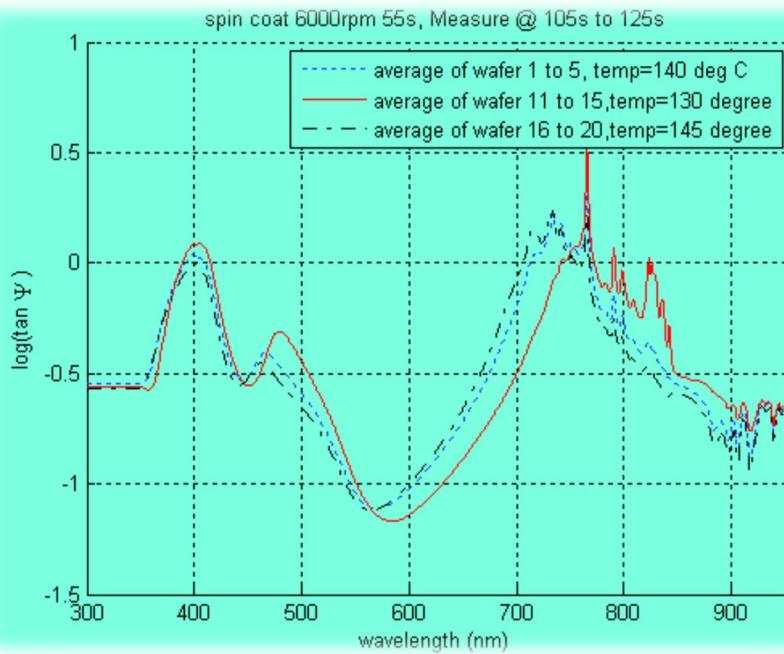


Rigorous coupled wave analysis (RCWA) used for in-situ extraction of CD information from scatterometry data.

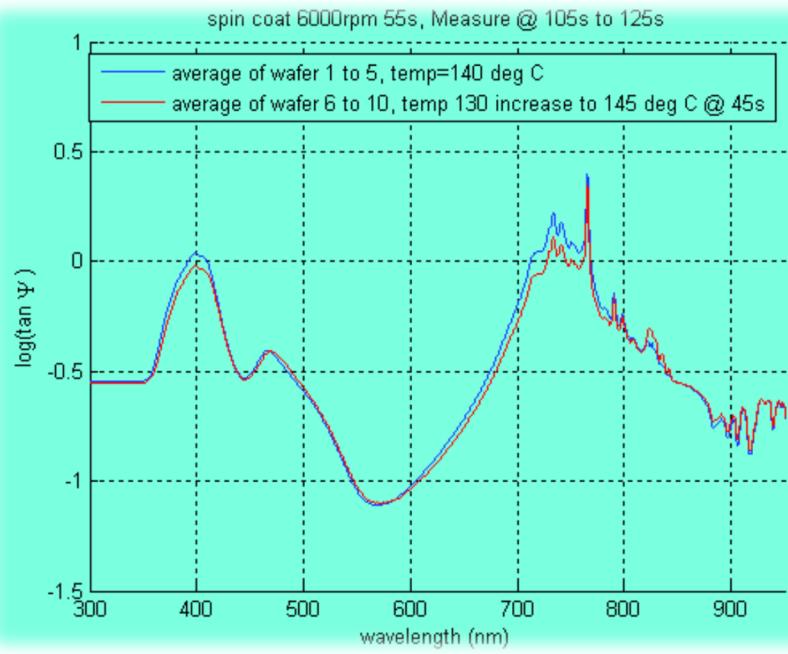
# Prototype System



# Experimental Results



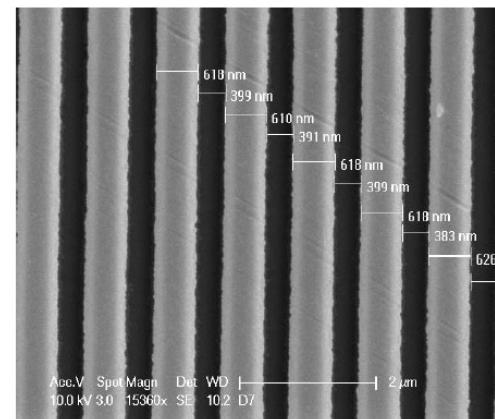
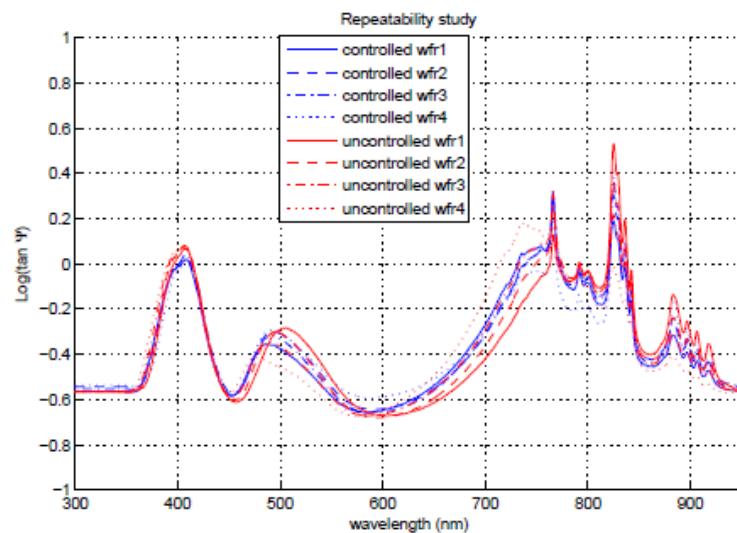
Conventional PEB, different temperature results in different signature plots



Proposed PEB, real-time monitoring and control of CD signature plots

# Experimental Results

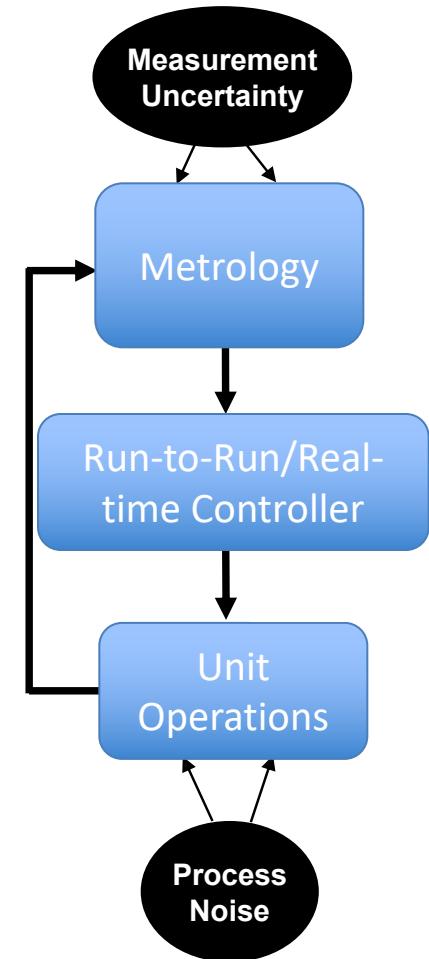
Experiment Series	Ridge (nm)	Valley (nm)
Reference wafer	618.0	392.6
Controlled wafer	625.6	366.5
Uncontrolled wafer	677.2	318.0



Controlled wafers

# Future Perspectives

- Systems thinking remains an important approach in solving many problems in Semiconductor Manufacturing
- Metrology key to Advanced Process Control (APC) success.
- No metrology mean no APC.
  - Reduce uncertainties
  - Develop new metrics for APC applications
- Actuator design for controllability



# Example: Smart Sampling

- Smart sampling – ability to change the sampling details (frequency, size, etc) based on prior observations.
- Sampling frequency increases when the process is drifting from intended value; and decreases when process is under control.
- A key consideration is to make sure that the algorithm is robust enough to respond to small process shifts during low sampling periods.
- Data from smart sampling is typically used along with other process data to feedforward information.

# Concluding Remarks

- Many opportunities to apply advanced modeling and control techniques in microelectronics manufacturing.
- Control changes will occur in two broad categories: real-time equipment control, and for run-to- run supervisory control systems.
- In-situ and on-line sensors will be critical – both feedback and feedforward control.
- Development of fundamental mathematical models for some equipment/process has reached a fairly high level of sophistication.
- Soft sensors, i.e., the fusion of sensor data to estimate another non-measured variable, has a role in the future.