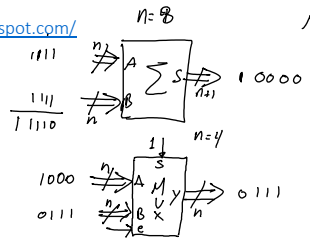
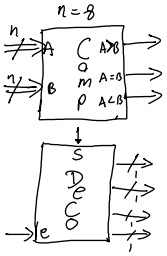
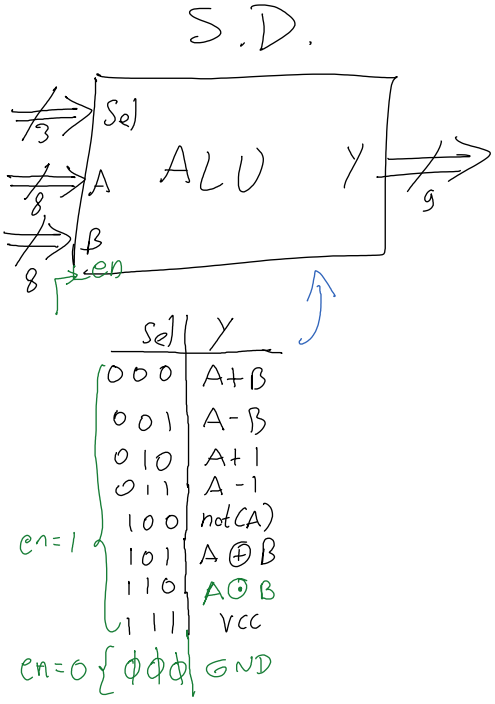
MSI - VHDL

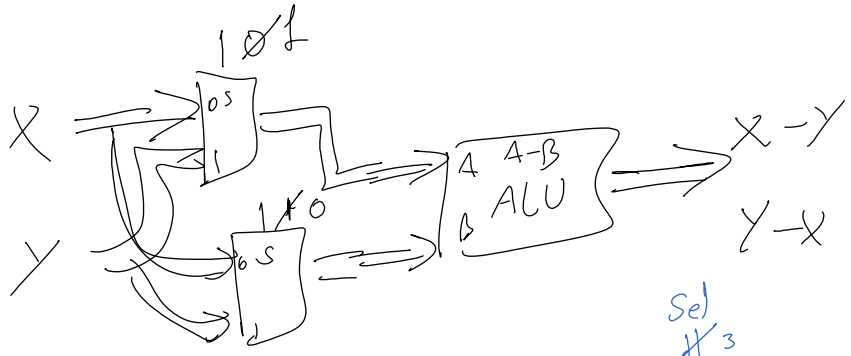






Sel	Y
000	A+B
001	A-B
010	A+1
011	A-1
100	not(A)
101	A ⊕ B
110	A ⊙ B
111	VCC
en=0 { ϕϕϕ	GND

en=1



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