



EK79007AD3

Rev. 1.0

DATA SHEET

1536-Output Source Driver with TCON
MIPI Interface

fitipower integrated technology inc.

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Single Chip 1536 Channel Source Driver with Timing Controller for 1024(RGB) × 600 TFT LCD

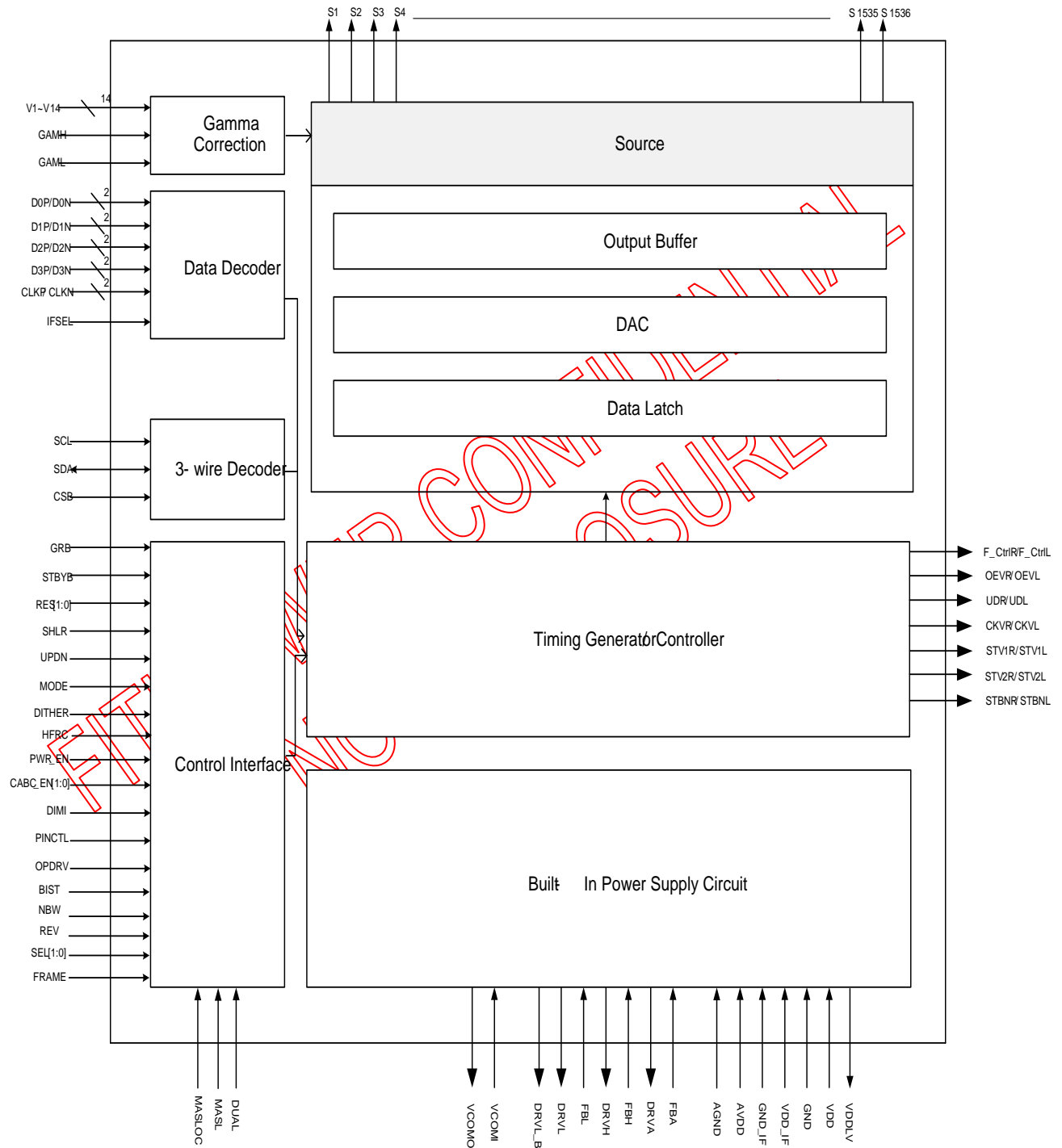
1. GENERAL DESCRIPTION

The EK79007AD is a highly integrated solution for small size to middle size a-Si TFT-LCD panels. This chip integrates 1536ch source driver with MIPI input interface.

2. FEATURES

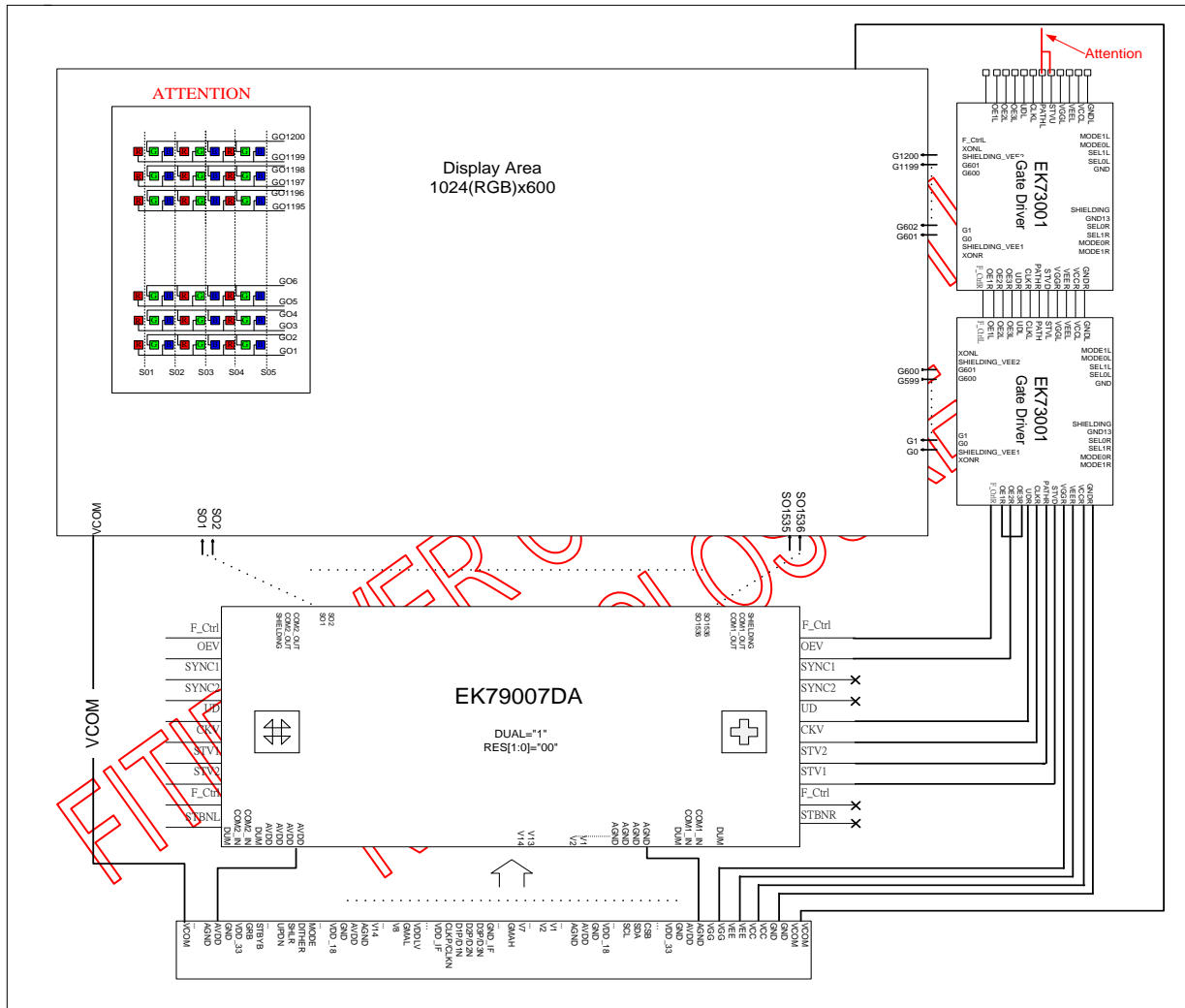
- Special design for middle size TFT LCD Panel with MIPI interface
- Integrate 1536 channel source driver and timing controller with dual gate function
- Support panel resolution (HxV): 1024(RGB)x768, 1024(RGB)x600, 800(RGB)x600, 800(RGB)x480
- 8-bit resolution 256 gray-scale with dithering (6-bits DAC +2 bits FRC or HFRC)
- Power for MIPI circuit(VDD_IF): 1.8V
- Power for digital circuit(VDD): 1.8V
- Power for analog circuit(AVDD): 8.0V ~ 13.5V
- Support interface: MIPI (4lane/3lane/2lane)
- Embedded Gamma Table for special customer request
- V1~V14 for adjusting Gamma correction
- 1+2 dot inversion architecture
- Built-In VCOM buffer
- Built-In AUTO pattern
- Built-In SDRRS function
- Support no. clock detection
- COG package
- Chip size = 24975um * 695um
- bump height=9um
- Output bump pitch = 15um

3. BLOCK DIAGRAM



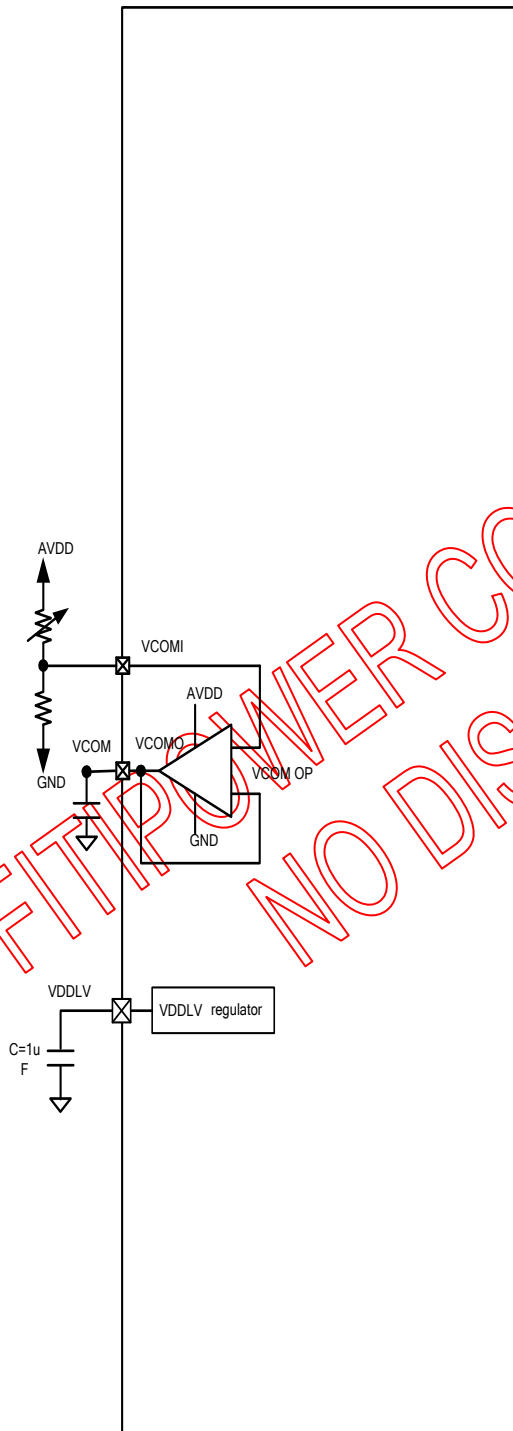
4. APPLICATION BLOCK DIAGRAM

4.1. Dual Gate (1024RGB x 600)



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6. APPLICATION POWER CIRCUIT



7. PIN DESCRIPTION

Pin Name	Pin Type	Description
D0P/D0N D1P/D1N D2P/D2N D3P/D3N	Input	MIPI data input.
CLKP/CLKN	Input	MIPI clock input.
IFSEL	Input	MIPI interface select (please pull GND or floating)
RES[1:0]	Input	RES[1:0]="01", for 1024(RGB)*768 display resolution RES[1:0]="00", for 1024(RGB)*600 display resolution (default) RES[1:0]="10", for 800(RGB)*600 display resolution (601~936 channel disable) RES[1:0]="11", for 800(RGB)*480 display resolution (601~936 channel disable)
DITHER	Input	Dithering function enable control. DITHER = "H" , Enable internal dithering function DITHER = "L" , Disable internal dithering function.(default).
HFRC	Input	H-FRC selection. HFRC = "L" : H-FRC disable(default) HFRC = "H" : H-FRC enable If "DITHER"="L" , disable dithering function(HFRC and FRC disable)
DUAL	Input	Dual Gate function enables control. Normally pull high DUAL = "H" , Enable Dual Gate Function. (Default) DUAL = "L" , TBD
V1~V14	Input	When INTERNAL Gamma Table is used. GAMH tied to AVDD , GAML tied to GND and V1~V14 pad are un-used. When using external gamma voltage, GAMH and GAML are floating , and V1~V14 are the external gamma correction points. The voltage of these pins must be: AGND<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1<AVDD .
GAMH	Input	GMAH tied to AVDD
GAML	Input	GMAL tied to GND via resistor.
GRB	Input	Global reset pin. Active Low to enter Reset State. Normally pull high. Connecting with an RC reset circuit for stability.
STBYB	Input	Standby mode. STBYB = "H" , normal operation(default) STBYB = "L" , timing controller, source driver will turn off, all output are GND.

Pin Name	Pin Type	Description															
SHLR	Input	Source right or left sequence control. SHLR = "L" , shift left: last data = S1←S2←S3.....←S1536 = first data. SHLR = "H" , shift right: first data = S1→S2→S3.....→S1536 = last data.(default)															
UPDN	Input	Gate up or down scan control. UPDN = "L" , STV2 output vertical start pulse and UD pin output logica "L" to Gate driver. (default) UPDN = "H" , STV1 output vertical start pulse and UD pin output logica "H" to Gate driver															
BIST	Input	Normal Operation/BIST pattern select. BIST = "H" : BIST(DCLK input is not needed) BIST = "L" : Normal Operation(default)															
NBW	Input	Normally black or normally white setting. NBW = "H" : Normally black NBW = "L" : Normally white(default)															
REV	Input	Controls whether the data of R[7:0]/G[7:0]/B[7:0] are inverted or not, normally pulled low. When REV="H" these data will be inverted. EX. "00"→"3F", "07"→"38", "15"→"2A", and so on.															
FRAME	Input	Frame inverse or not select. Normally pull low. FRAME = "H" , Uniform FRAME = "L" , Frame inverse (Default)															
SEL[1:0]	Input	Gate on sequence select. Normally pull low <table border="1"> <thead> <tr> <th>SEL[1]</th><th>SEL[0]</th><th>Pin control function</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>Z+2</td></tr> <tr> <td>1</td><td>0</td><td>3</td></tr> <tr> <td>0</td><td>1</td><td>2</td></tr> <tr> <td>0</td><td>0</td><td>Z(default)</td></tr> </tbody> </table>	SEL[1]	SEL[0]	Pin control function	1	1	Z+2	1	0	3	0	1	2	0	0	Z(default)
SEL[1]	SEL[0]	Pin control function															
1	1	Z+2															
1	0	3															
0	1	2															
0	0	Z(default)															
OEVR/OEVL	Output	Gate driver control signal															
UDR/UDL	Output	Gate driver control signal															
CKVR/CKVL	Output	Gate driver control signal															
STV1R/STV1L	Output	Gate driver control signal															
STV2R/STV2L	Output	Gate driver control signal															
STBNR/STBNL	Output	Gate driver control signal															
F_CtrlR/F_CtrlL	Output	Gate driver control signal (For special Gate on sequence). In Dual Gate structure , connect this pin to gate driver's F_Ctrl.															
DIMI	Input	Brightness control signal. Normally pull high.															
DIMO	Output	Backlight dimmer signal for external controller. DIMO = "L" , Turn off external backlight controller DIMO = "H" , Logical control signal to turn on external backlight controller NOTE : If CABC OFF , DIMO = DIMI . Else DIMO is controlled by CABC															

Pin Name	Pin Type	Description
PINCTL	Input	Enable pin control function. (for MIPI) PINCTL="L" , Disable pin control function. The following pin will be inactive: MIPI IF:SHLR, HFRC,DITHER,BIST,NBW,PWR_EN,REV, RES[1:0]. PINCTL="H" , Enable pin control function.(default)
OPDRV	Input	Source OP driving selection. OPDRV = "H" : 133% OPDRV = "L" : normal.(default)
LVBIT	Input	please floating
LVFMT	Input	please floating
AVDD	PI	Power supply for analog circuits
AGND	PI	Ground pins for analog circuits
GND	PI	Ground pins for digital circuits
VDD	PI	Power supply for digital circuits
VDD_IF	PI	MIPI power
GND_IF	PI	MIPI ground
VDDL	PO	VDDL LDO output for MIPI LP mode TX use. VDDL LDO enable on MIPI Interface.
PWR_EN	Input	PWR_EN = "H", enable VCOM buffer PWR_EN = "L", disable VCOM buffer(default)
VCOMI	Input	VCOM buffer in
VCOMO	Output	VCOM buffer out
SO1~SO1536	Output	Source Driver Output Signals All outputs will be of unknown values under stand-by mode.
COM1_IN COM1_OUT	S	Internal link together between input side and output side
COM2_IN COM2_OUT	S	Internal link together between input side and output side.
SHIELDING	SH	Those pins are internally connected to the AGND. DO NOT connect to any WOA on the panel. Data Bus Shielding pad
DASHD	SH	Those pins are internally connected to the GND. RECOMMEND to add shielding lines on the FPC to reduce EMI.
TP1~TP45	T	DO NOT connect to any WOA on the panel and floating on panel.

Note:

P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, PS: Power Setting, C: Capacitor pin.

Pass Line Description:

Pass Line No.	Pad Name	
1	COM1_IN	COM1_OUT
2	COM2_IN	COM2_OUT

7.1. Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Source wiring:

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
AVDD	<5	FRAME	<100
AGND	<5	SEL[1:0]	<100
VDD_IF	<5	REV	<100
VDD	<5	CABC_EN[1:0]	<100
GND_IF	<5	OPDRV	<100
VDDL	<5	BIST	<100
GND	<5	RES[1:0]	<100
V1~V14	<5	DCLKPOL	<100
DRVX	<5	STBYB	<100
FBX	<5	GRB	<100
VCOMI	<5	SHLR	<100
VCOMO	<5	UPDN	<100
D0P/D0N	<5	PINCTL	<100
D1P/D1N	<5	DUAL(Reserved)	<100
D2P/D2N	<5	MASL(Reserved)	<100
D3P/D3N	<5	MASLOC(Reserved)	<100
CLKP/CLKN	<5	MODE(Reserved)	<100
DIMI	<100	LVFMT	<100
DIMO	<100	LVBIT	<100
NBW	<100	DEN(Reserved)	<100
PINCTL	<100		
DITHER	<100		
IFSEL	<100		
HFRC	<100		

Gate wiring:

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VGH	<50	OEVS	<100
VGL	<30	UDX	<100
VCC	<50	CKVS	<100
GND	<40	STBNX	<100
STV1X/STV2X	<100	F_CtrlX	<100

8. MIPI INTERFACE (MOBILE INDUSTRY PROCESSING INTERFACE)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

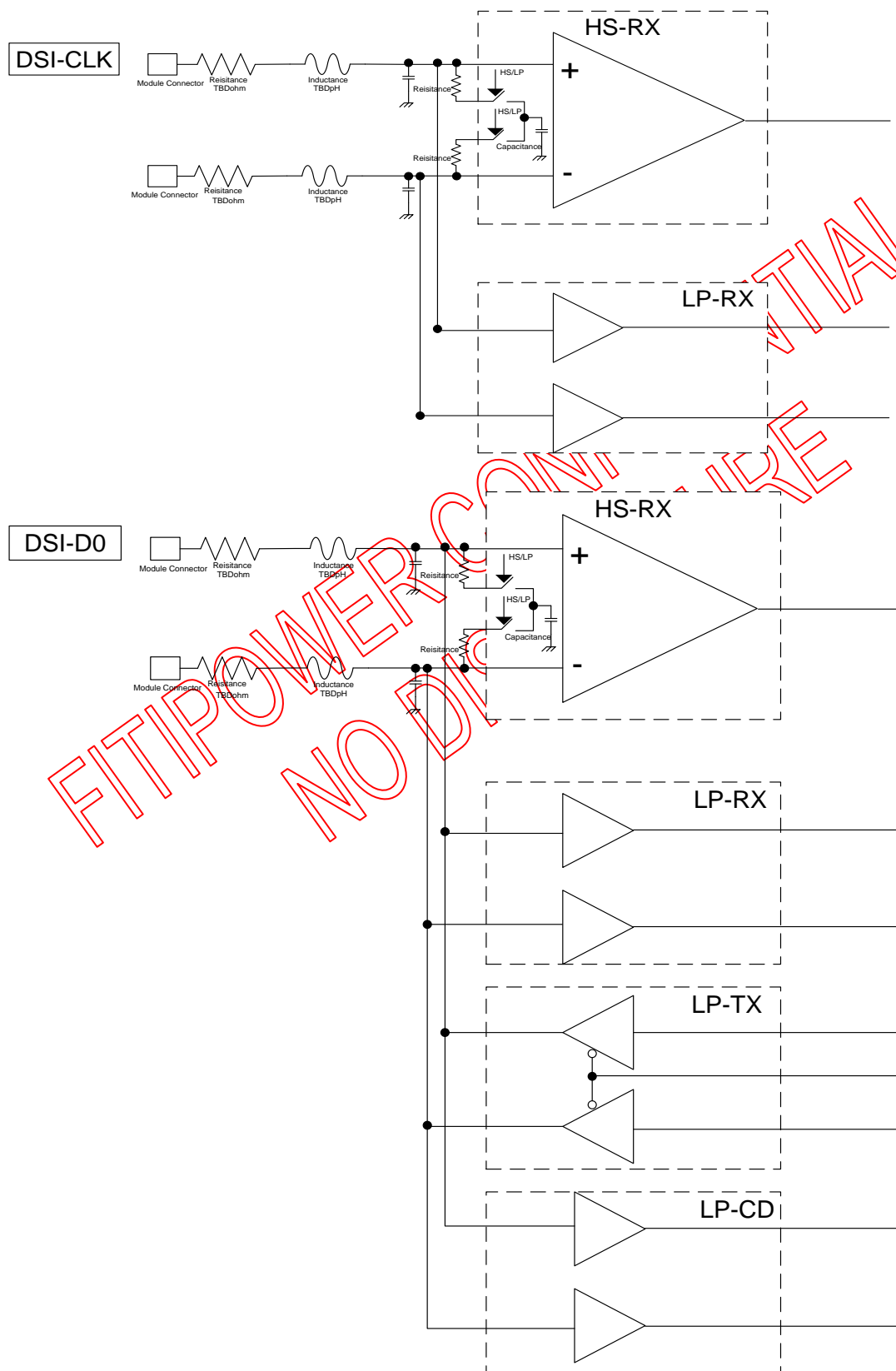
Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

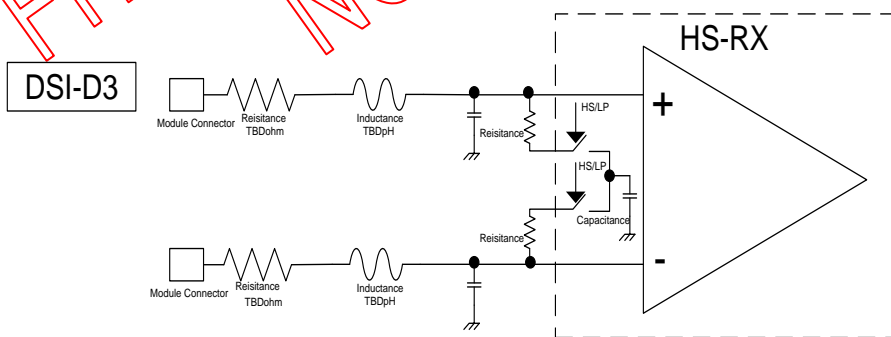
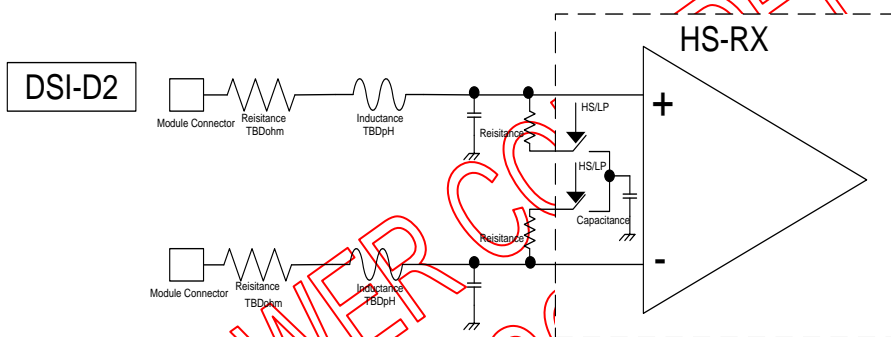
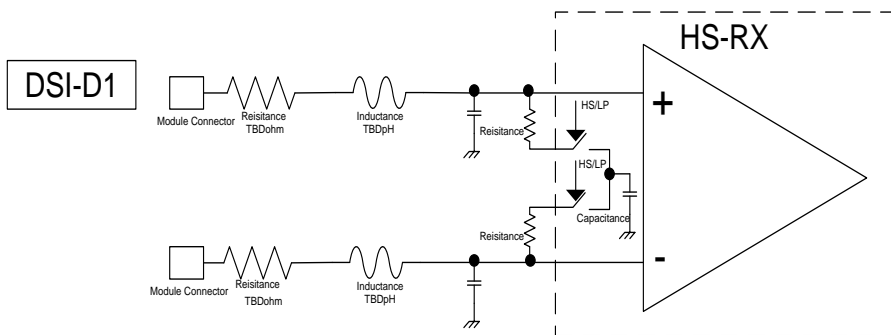
Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

MIPI Lane Configuration:

	MCU (Master)	Display Module (Slave)
Clock Lane	Unidirectional Lane <ul style="list-style-type: none"> • Clock Only • Escape Mode (ULPS Only) 	
Data Lane0	Bi-directional Lane <ul style="list-style-type: none"> ● Forward High-Speed ● Bi-directional Escape Mode ● Bi-directional LPDT 	
Data Lane1	Unidirectional <ul style="list-style-type: none"> ● Forward High speed 	
Data Lane2	Unidirectional <ul style="list-style-type: none"> ● Forward High speed 	
Data Lane3	Unidirectional <ul style="list-style-type: none"> ● Forward High speed 	

8.1. Display Module Pin Configuration for DSI





8.2. Display Serial Interface (DSI)

8.2.1. Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. These terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scanline during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero.

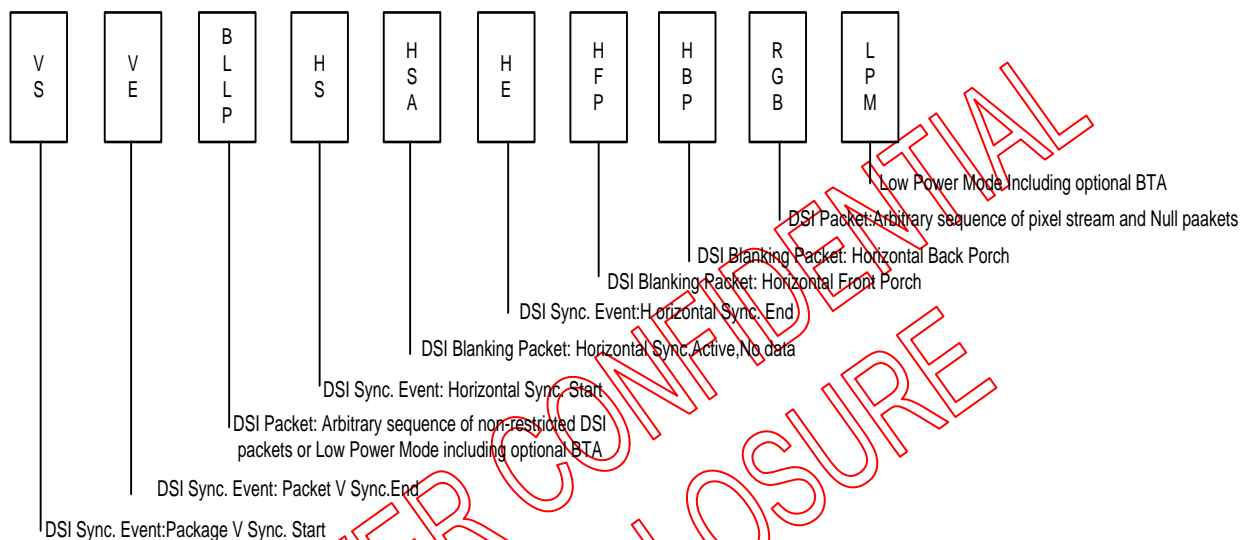
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX.
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode.
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode.
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode.
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when $VSA+VBP=0$. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. Individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



DSI Video Mode Interface Timing Legend

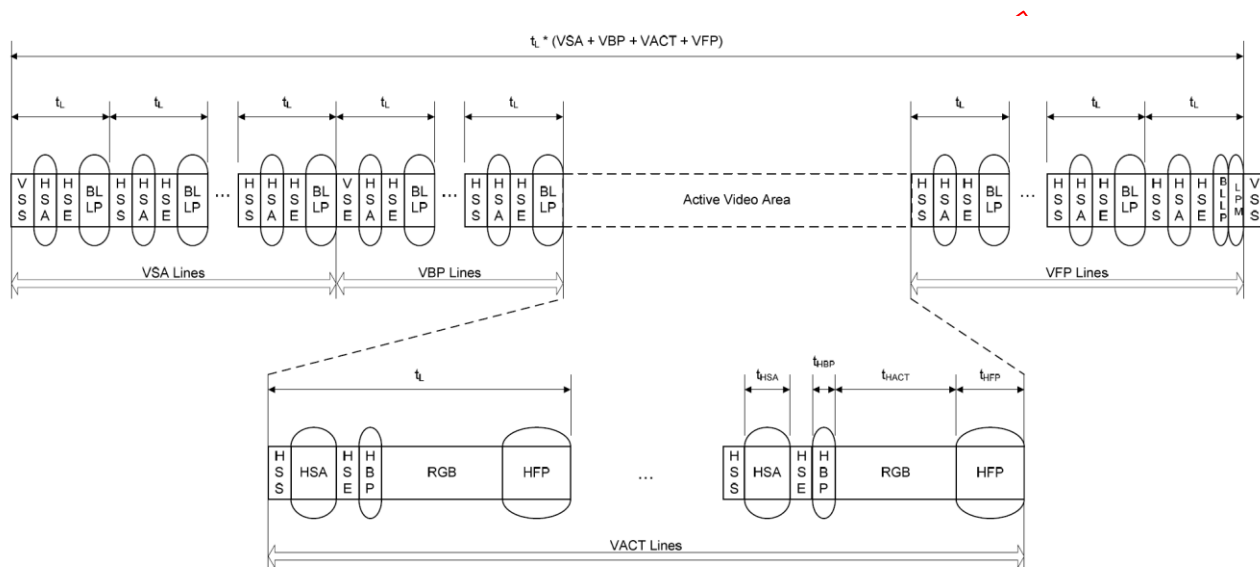
If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

Clock Requirements

A DSI host processor shall support continuous clock on the Clock Lane for display module that require it, so the host processor needs to keep the HS serial clock running.

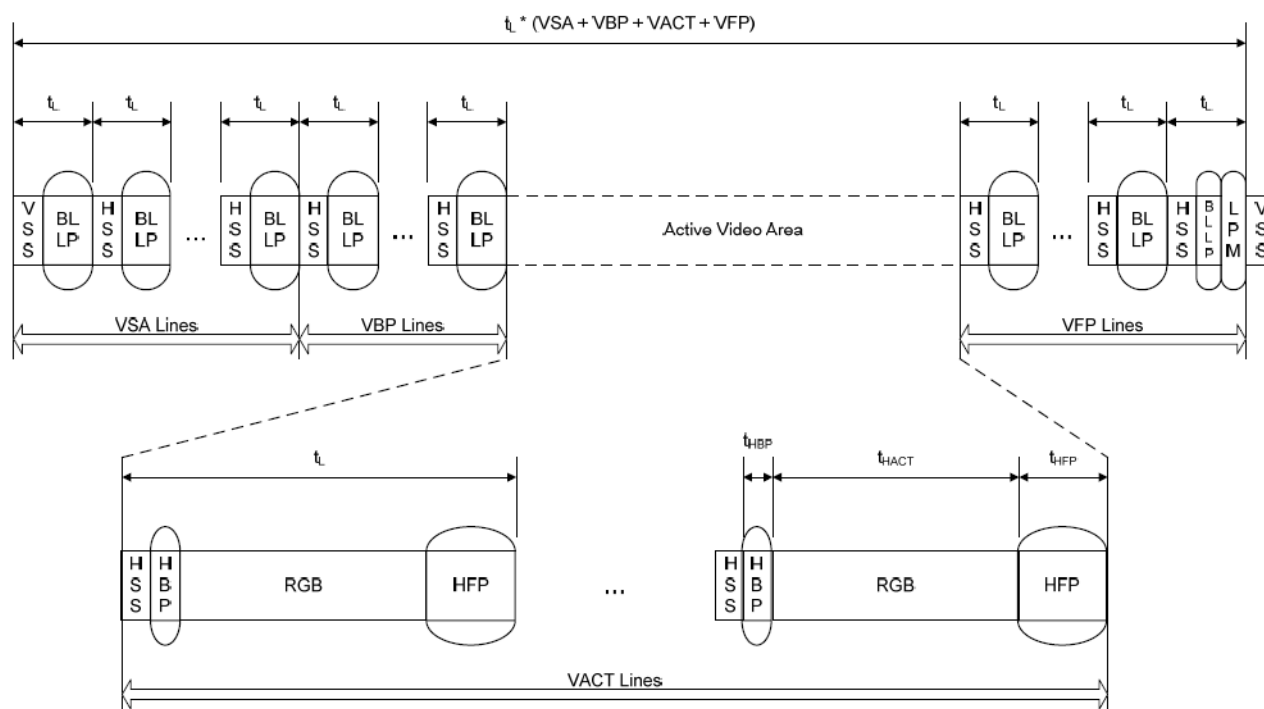
●Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.



Normally, periods shown as I (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

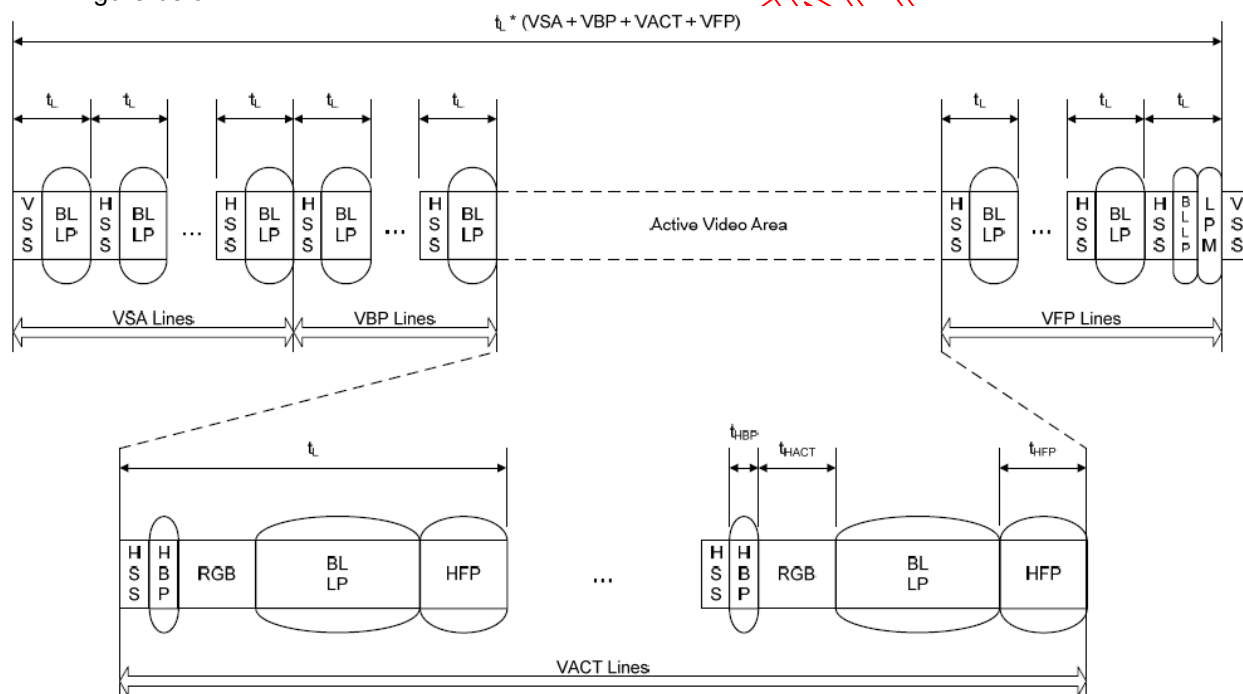
This mode is a simplification of the format described in section “Non-Burst Mode with Sync Pulse”. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.



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● Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.



Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

9. COMMAND DESCRIPTION

9.1. MIPI Control Register

Following table list all the MIPI control registers and bit name definition for EK79007AD. Refer to the next section for detail register function description, please.

Setting of all the MIPI registers will take effect at the coming valid Vsync signal except GRB bit.

All the MIPI control registers and bit name definition:

	Register address									MSB							LSB	default (hex)
No.	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	DO	
R00h	0	0	0	0	0	0	0	0	0	NOP								—
R01h	0	0	0	0	0	0	0	0	1	GRB								—
R05h	0	0	0	0	0	0	0	1	0	RDNUMED(TBD)								—
R0Ah	0	0	0	0	1	0	1	0	1	GET_POWER_Mode								—
R0Dh	0	0	0	0	1	1	0	1	1	GET_DISPLAY_Mode								—
R0Eh	0	0	0	0	1	1	1	0	1	GET_SIGNAL_Mode(TBD)								—
R0Fh	0	0	0	0	1	1	1	1	1	RDDSDR(TBD)								—
R10h	0	0	0	1	0	0	0	0	0	ENTER_SLEEP_MODE								—
R11h	0	0	0	1	0	0	0	1	0	EXIT_SLEEP_MODE								—
R20h	0	0	1	0	0	0	0	0	0	EXIT_INVERT_MODE								—
R21h	0	0	1	0	0	0	0	1	0	ENTER_INVERT_MODE								—
R36h	0	0	1	1	0	1	1	0	1/0	0	0	0	0	0	0	UPDN(0)	SHLR(1)	01
R80h	1	0	0	0	0	0	0	0	1/0	G2R[3:0] (1000)				G1R[3:0] (1000)				88
R81h	1	0	0	0	0	0	0	1	1/0	G4R[3:0] (1000)				G3R[3:0] (1000)				88
R82h	1	0	0	0	0	0	1	0	1/0	G6R[3:0] (1000)				G5R[3:0] (1000)				88
R83h	1	0	0	0	0	0	1	1	1/0	G8R[3:0] (1000)				G7R[3:0] (1000)				88
R84h	1	0	0	0	0	1	0	0	1/0	G10R[3:0] (1000)				G9R[3:0] (1000)				88
R85h	1	0	0	0	0	1	0	1	1/0	G12R[3:0] (1000)				G11R[3:0] (1000)				88
R86h	1	0	0	0	0	1	1	0	1/0	G14R[3:0] (1000)				G13R[3:0] (1000)				88
RB0h	1	0	1	1	0	0	0	0	1/0	PWR_EN(0)	—	—	—	—	—	—	—	00
RB1h	1	0	1	1	0	0	0	1	1/0			HFRC(0)	DITHER(0)	BIST(0)	RES[1:0] (00)	—	—	00
RB2h	1	0	1	1	0	0	1	0	1/0	—	NBW(0)	En_3lane(0)	En_2lane(0)	—	—	—	—	00
RB3h	1	0	1	1	0	0	1	1	1/0	—	—	—	—	—	FRAME(0)	SEL[1:0]	—	00

R00h: NOP (No Operation)

Address (MIPI I/F)	00h					Access Attribute			W
						Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								N/A
Description	This command performs no operation and is ignored by the device.								

R01h: GRB (Software Reset)

Address (MIPI I/F)	01h					Access Attribute			W
						Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								N/A
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset register values and all source are set to GND (display off).								
Restriction	(1)It will be necessary to wait 20 msec before sending new command following software reset. (2)The display module loads all display supplier's factory default values to the registers during 5 msec.								

R05h: RDNUMED (reserved)

R0Ah: GET_POWER_MODE (Read Display Power Mode)

Address (MIPI I/F)	0Ah					Access Attribute			R
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	D7	D6	D5	D4	D3	D2	D1	D0	00h
Description	D[4]:Sleep In/Out "0" =Sleep Out, "1" =Sleep In								

R0Dh: GET_DISPLAY_MODE (Read the Current Display Mode)

Address (MIPI I/F)	0Dh					Access Attribute			R
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	D7	D6	D5	D4	D3	D2	D1	D0	00h
Description	D[5]:Inversion On/Off "0" =Inversion off, "1" =Inversion on								

R0Eh: GET_SIGNAL_MODE (TBD)

Address (MIPI I/F)	0Fh					Access Attribute			R
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								00h
Description	D[0]:Error on DSI "1" :error, "0" =no error								
Restriction	-								

R0Fh:RDDSDR (Read Display Self-Diagnostic Result)(TBD)

R10h: ENTER_SLEEP_MODE (Enter the Sleep-In Mode)

Address (MIPI I/F)	10h					Access Attribute			W
						Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								Sleep In
Description	This command initiates the power-down sequence. The Sleep In profile will be executed when this command is received.								
Restriction	This command has no effect when the display module is already in Sleep Mode.								

R11h: EXIT_SLEEP_MODE (Exit the Sleep-In Mode)

Address (MIPI I/F)	11h					Access Attribute			W
						Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								Sleep In
Description	This command initiates the power-up sequence. The Sleep Out will load register value. It will be necessary to wait 5 msec before sending next command.								
Restriction	This command will not cause any visible effect on the display when the display is not in Sleep.								

R20h:EXIT_INVERT_MODE (Display Inversion Off)

Address (MIPI I/F)	20h					Access Attribute			W
						Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								Inversion Off
Description	This command is used to recover from display reverse mode and does not change any other status.								
Restriction	This command has no effect when the module is already in inversion off mode.								

R21h: ENTER_INVERT_MODE (Display Inversion On)

Address (MIPI I/F)	21h					Access Attribute			W
						Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default value
	No Argument								Inversion Off
Description	This command is used to enter display Inversion mode and does not change any other status. To exit from Display Inversion on, the Display Inversion off command (20h) should be written.								
Restriction	This command has no effect when the module is already in inversion on mode.								

R36h: SET_ADDRESS_MODE (Data Access Control)

Address (MIPI I/F)	36h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	0	0	0	0	0	0	UPDN	SHLR	01h
Description	UPDN: Gate up or down scan control. UPDN = "0", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver. (default) UPDN = "1", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver. SHLR: Source right or left sequence control. SHLR = "0", shift left: last data = S1←S2←S3.....←S1200 = first data. SHLR = "1", shift right: first data = S1→S2→S3.....→S1200 = last data. (default)								

R80h: Gamma Control Register

Address (MIPI I/F)	80h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	G2R				G1R				88h
Description	Gamma voltage setting.								

R81h: Gamma Control Register

Address (MIPI I/F)	81h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	G4R				G3R				88h
Description	Gamma voltage setting.								

R82h: Gamma Control Register

Address (MIPI I/F)	82h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	G6R				G5R				88h
Description	Gamma voltage setting.								

R83h: Gamma Control Register

Address (MIPI I/F)	83h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	G8R					G7R			88h
Description	Gamma voltage setting.								

R84h: Gamma Control Register

Address (MIPI I/F)	84h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	G10R					G9R			88h
Description	Gamma voltage setting.								

R85h: Gamma Control Register

Address (MIPI I/F)	85h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	G12R				G11R				88h
Description	Gamma voltage setting.								

R86h: Gamma Control Register

Address (MIPI I/F)	86h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	G14R				G13R				88h
Description	Gamma voltage setting.								

RB0h: Panel Control Register

Address (MIPI I/F)	B0h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	PWR_EN (0)	—	—	—	—	—	—	—	00h
Description	PWR_EN: POWER enable. PWR_EN = "1" , enable VCOM buffer PWR_EN = "0" , disable VCOM buffer (Default)								

RB1h: Panel Control Register

Address (MIPI I/F)	B1h					Access Attribute		R/W	
						Number of Parameter(s)		1	
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
			HFRC (0)	DITHER (0)	BIST (0)	RES[1:0] (00)		—	00h
Description	HFRC: H-FRC selection. HFRC = "1" : H-FRC enable HFRC = "0" : H-FRC disable (Default) If DITHER="0", disable dithering function(H-FRC and FRC disable) DITHER: Dithering function enable control. DITHER = "1", Enable internal dithering function DITHER = "0", Disable internal dithering function (Default) BIST: Normal Operation/BIST pattern select. BIST = "1" : BIST(DCLK input is not needed) BIST = "0" : Normal Operation (Default) RES[1:0]: = "01", for 1024(RGB)*768 display resolution = "00", for 1024(RGB)*600 display resolution (default) = "10", for 800(RGB)*600 display resolution (601~936 channel disable) = "11", for 800(RGB)*480 display resolution (601~936 channel disable)								

RB2h: Panel Control Register

Address (MIPI I/F)	B2h				Access Attribute				R/W
					Number of Parameter(s)				1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	—	NBW(0)	En_3lane(0)	En_2lane(0)	—	—	—	—	00h
Description	<p>NBW: Normally black or normally white setting. NBW="1" : Normally black. NBW="0" : Normally white(default). En_3lane: Enable or disable 3 lane MIPI interface En_3lane = "1" : Enable 3 lane MIPI interface En_3lane = "0" : Disable 3 lane MIPI interface(Default) En_2lane: Enable or disable 2 lane MIPI interface En_2lane = "1" : Enable 2 lane MIPI interface En_2lane = "0" : Disable 2 lane MIPI interface(Default) Note: If En_3lane and En_2lane = "1" simultaneously, the interface would be MIPI 4 lane.</p>								

RB3h: Panel Control Register

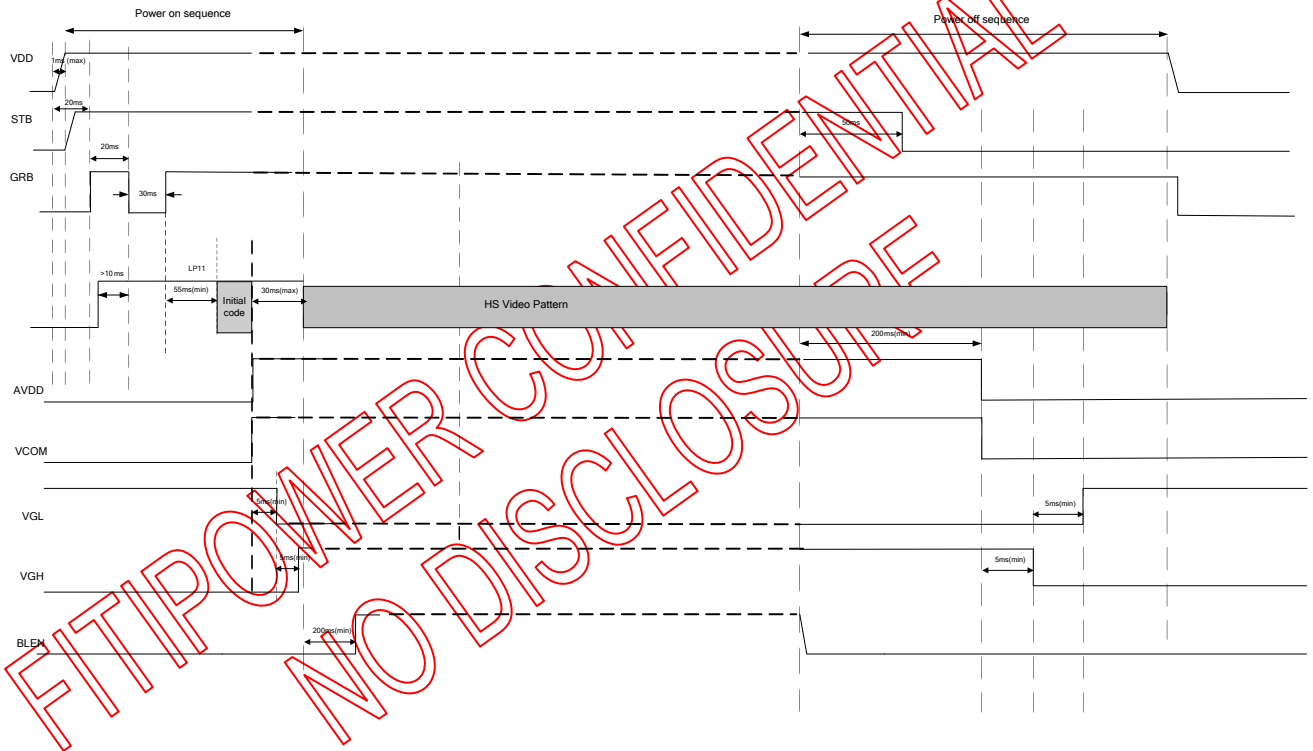
Address (MIPI I/F)	B2h					Access Attribute			R/W
						Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
		—		—	—	FRAME (0)	SEL[1:0] (00)		00h
Description	FRAME: Frame inverse or not select. FRAME = "1" , Uniform FRAME = "0" , Frame inverse(Default)								
	SEL[1:0]:Gate on sequence select.								
	SEL[1]	SEL[0]	Pin control function						
	1	1	Z+2						
	1	0	Z						
	0	1	Z						
0	0	Z(default)							

10. FUNCTION DESCRIPTION

10.1. Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

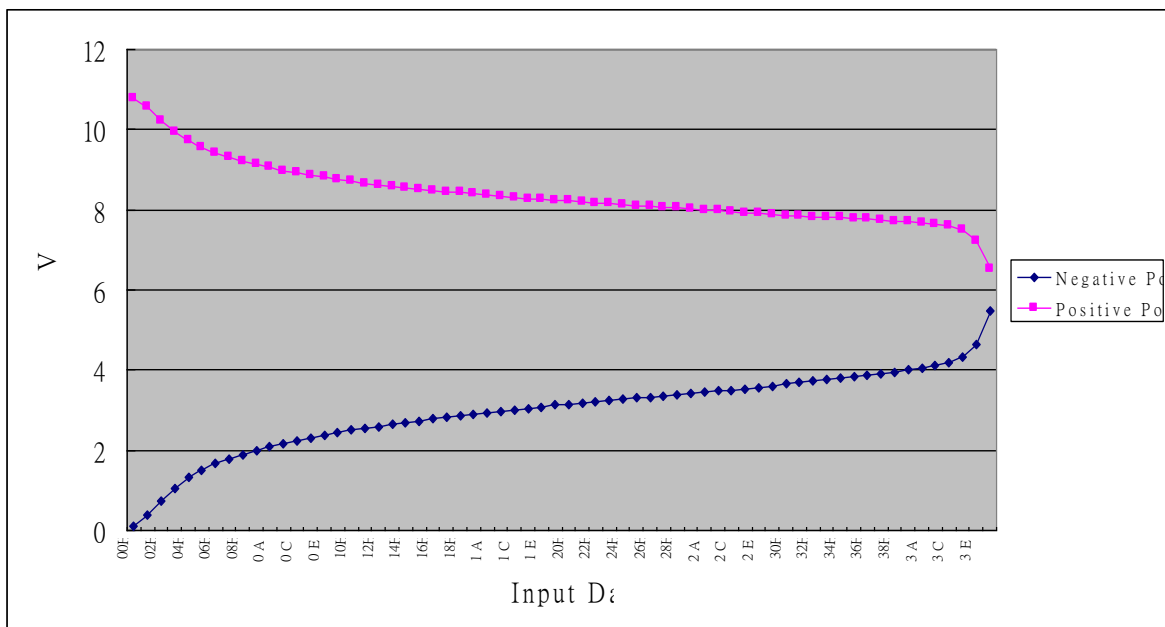
10.1.1. Power On/Off Sequence



Note: CLK and Data Lanes should keep in LP11(stop state) before GRB.

10.2. Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.



Remark: $AVDD-0.1 > V1 > V2 > V3 > V4 > V5 > V6 > V7; V8 > V9 > V10 > V11 > V12 > V13 > V14 > AGND+0.1V$

10.3. Input Data and Output Voltage Reference Table

Input Data and Output Voltage Reference Table

@AVDD=11V

V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14	Unit
10.78	10.569	8.708	8.213	7.866	7.243	6.51	5.49	4.63	3.653	3.146	2.493	0.373	0.11	V

Data	Positive
00H	AVDDx0.980
01H	AVDDx0.961
02H	AVDDx0.930
03H	AVDDx0.905
04H	AVDDx0.885
05H	AVDDx0.870
06H	AVDDx0.857
07H	AVDDx0.847
08H	AVDDx0.838
09H	AVDDx0.830
0AH	AVDDx0.823
0BH	AVDDx0.816
0CH	AVDDx0.811
0DH	AVDDx0.806
0EH	AVDDx0.801
0FH	AVDDx0.796
10H	AVDDx0.792
11H	AVDDx0.788
12H	AVDDx0.784
13H	AVDDx0.781
14H	AVDDx0.778
15H	AVDDx0.775
16H	AVDDx0.772
17H	AVDDx0.769
18H	AVDDx0.766
19H	AVDDx0.763
1AH	AVDDx0.761
1BH	AVDDx0.758
1CH	AVDDx0.756
1DH	AVDDx0.753
1EH	AVDDx0.751
1FH	AVDDx0.748

Data	Positive
20H	AVDDx0.747
21H	AVDDx0.745
22H	AVDDx0.743
23H	AVDDx0.741
24H	AVDDx0.739
25H	AVDDx0.737
26H	AVDDx0.735
27H	AVDDx0.732
28H	AVDDx0.731
29H	AVDDx0.729
2AH	AVDDx0.727
2BH	AVDDx0.725
2CH	AVDDx0.723
2DH	AVDDx0.721
2EH	AVDDx0.719
2FH	AVDDx0.717
30H	AVDDx0.715
31H	AVDDx0.713
32H	AVDDx0.711
33H	AVDDx0.710
34H	AVDDx0.709
35H	AVDDx0.707
36H	AVDDx0.706
37H	AVDDx0.704
38H	AVDDx0.702
39H	AVDDx0.700
3AH	AVDDx0.697
3BH	AVDDx0.694
3CH	AVDDx0.690
3DH	AVDDx0.681
3EH	AVDDx0.658
3FH	AVDDx0.592

Data	Negative
00H	AVDDx0.010
01H	AVDDx0.034
02H	AVDDx0.068
03H	AVDDx0.096
04H	AVDDx0.119
05H	AVDDx0.136
06H	AVDDx0.151
07H	AVDDx0.162
08H	AVDDx0.172
09H	AVDDx0.182
0AH	AVDDx0.189
0BH	AVDDx0.197
0CH	AVDDx0.204
0DH	AVDDx0.210
0EH	AVDDx0.215
0FH	AVDDx0.221
10H	AVDDx0.227
11H	AVDDx0.231
12H	AVDDx0.236
13H	AVDDx0.240
14H	AVDDx0.245
15H	AVDDx0.248
16H	AVDDx0.253
17H	AVDDx0.256
18H	AVDDx0.260
19H	AVDDx0.263
1AH	AVDDx0.266
1BH	AVDDx0.270
1CH	AVDDx0.273
1DH	AVDDx0.277
1EH	AVDDx0.280
1FH	AVDDx0.284

Data	Negative
20H	AVDDx0.286
21H	AVDDx0.289
22H	AVDDx0.292
23H	AVDDx0.294
24H	AVDDx0.297
25H	AVDDx0.300
26H	AVDDx0.302
27H	AVDDx0.305
28H	AVDDx0.308
29H	AVDDx0.311
2AH	AVDDx0.314
2BH	AVDDx0.316
2CH	AVDDx0.318
2DH	AVDDx0.321
2EH	AVDDx0.325
2FH	AVDDx0.328
30H	AVDDx0.332
31H	AVDDx0.336
32H	AVDDx0.339
33H	AVDDx0.342
34H	AVDDx0.345
35H	AVDDx0.348
36H	AVDDx0.351
37H	AVDDx0.355
38H	AVDDx0.359
39H	AVDDx0.364
3AH	AVDDx0.369
3BH	AVDDx0.375
3CH	AVDDx0.382
3DH	AVDDx0.394
3EH	AVDDx0.421
3FH	AVDDx0.499

10.4. Input Timing Table (4Lane)
For 1024RGB x 768 panel
DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	52	65	71	Mhz
Horizontal display area	thd	1024			DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	Tvd	768			H
VSYNC period time	Tv	778	806	845	H
VSYNC blanking	Tvb+Tvfp	10	38	77	H

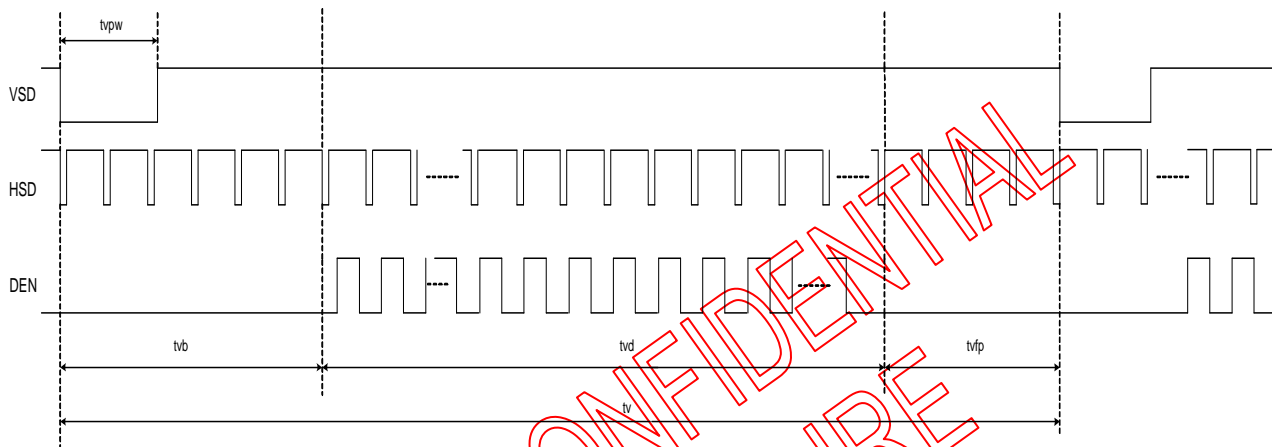
HV mode
Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	1024			DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	Mhz
			57	65	70.5	
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		70			
	Max.		140			
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

HV mode
Vertical input timing

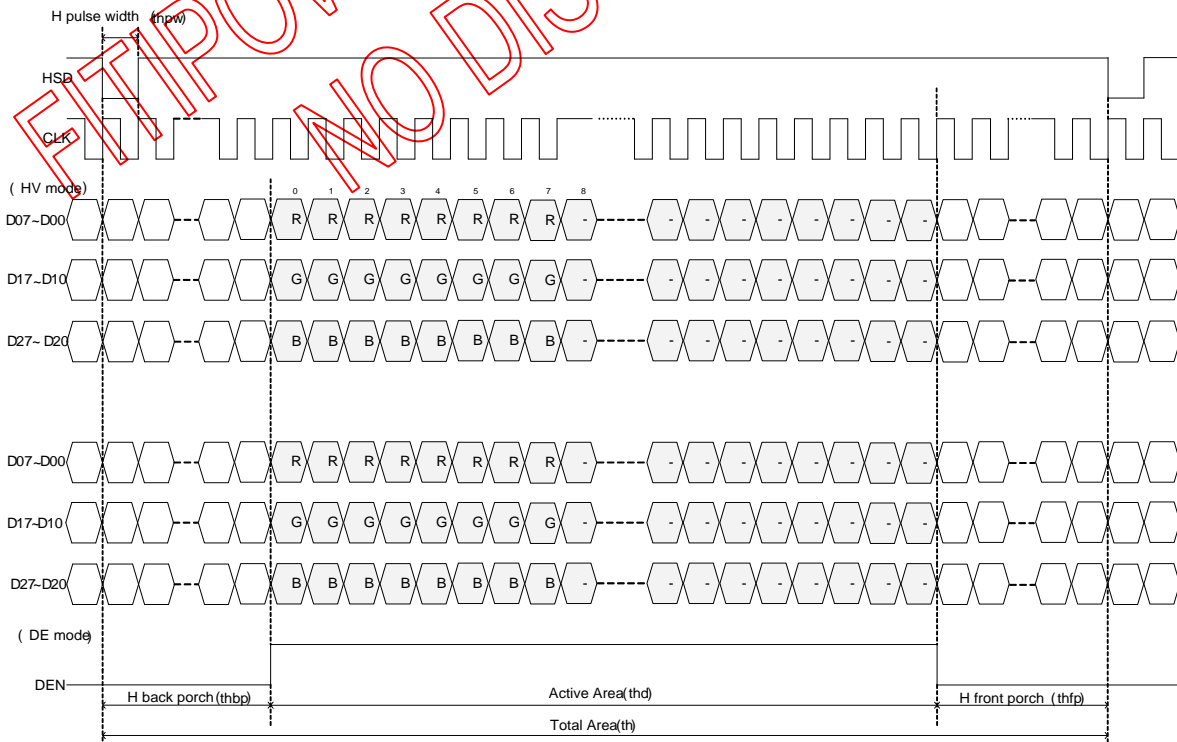
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd	768			H
VSYNC period time	tv	792	806	840	H
VSYNC pulse width	tvpw	1	10	20	H
VSYNC back porch	tvb	23	23	23	H
VSYNC front porch	tvfp	1	15	49	H

10.4.1. Vertical input timing



Vertical input timing

10.4.2. Horizontal input timing



Horizontal input timing

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	40.8	51.2	67.2	Mhz
Horizontal display area	thd	1024			DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	Tvd	600			H
VSYNC period time	Tv	610	635	800	H
VSYNC blanking	Tvb+Tvfp	10	35	200	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	1024			DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min. 44.9	Typ. 51.2	Max. 63	Mhz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		70			
	Max.		140			
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

HV mode

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tv	600			H
VSYNC period time	tv	624	635	750	H
VSYNC pulse width	tpw	1	10	20	H
VSYNC back porch	tvb	23	23	23	H
VSYNC front porch	tvfp	1	12	127	H

For 800RGB x 600 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	32.6	39.6	62.4	Mhz
Horizontal display area	thd	800			DCLK
HSYNC period time	th	890	1000	1300	DCLK
HSYNC blanking	thb+thfp	90	200	500	DCLK
Vertical display area	Tvd	600			H
VSYNC period time	Tv	610	660	800	H
VSYNC blanking	Tvb+Tvfp	10	60	200	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	800			DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	Mhz
			34.5	39.6	50.4	
1 Horizontal Line		th	900	1000	1200	DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		20			
	Max.		40			
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	112	312	

HV mode

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd	600			H
VSYNC period time	tv	640	660	700	H
VSYNC pulse width	tpw	1	10	20	H
VSYNC back porch	tvb	39	39	39	H
VSYNC front porch	tvfp	1	21	61	H

For 800RGB x 480 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	26.2	29.2	54.6	Mhz
Horizontal display area	thd	800			DCLK
HSYNC period time	th	890	928	1300	DCLK
HSYNC blanking	thb+thfp	90	128	500	DCLK
Vertical display area	Tvd	480			H
VSYNC period time	Tv	490	525	700	H
VSYNC blanking	Tvb+Tvfp	10	45	220	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	800			DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	Mhz
			27.7	29.2	39.6	
1 Horizontal Line		th	900	928	1100	DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		20			
	Max.		40			
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	40	212	

HV mode

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd	480			H
VSYNC period time	tv	513	525	600	H
VSYNC pulse width	tvpw	1	2	3	H
VSYNC back porch	tvb	32	32	32	H
VSYNC front porch	tvfp	1	13	88	H

10.5. Input Timing Table (2Lane)
For 1024RGB x 600 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	fclk	40.8	51.2		Mhz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344		DCLK
HSYNC blanking	thb+thfp	90	320		DCLK
Vertical display area	Tvd		600		H
VSYNC period time	Tv	610	635		H
VSYNC blanking	Tvb+Tvfp	10	35		H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	1024			DCLK
DCLK frequency @ Frame rate=60hz		fclk	Min.	Typ.	Max.	
			44.9	51.2		
1 Horizontal Line		th	1200	1344		DCLK
HSYNC pulse width	Min.	thpw	1			
	Typ.		70			
	Max.		140			
HSYNC blanking		thb	160	160		
HSYNC front porch		thfp	16	160		

HV mode

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd	600			H
VSYNC period time	tv	624	635		H
VSYNC pulse width	tvpw	1	20		H
VSYNC back porch	tvb	23	23		H
VSYNC front porch	tvfp	1	12		H

11. ABSOLUTE MAXIMUM RATING

VOLTAGE (TA = 25°C, GND = AGND = GND_IF = 0V)

	Min.	Max.	Unit
Digital Supply Voltage, VDD	-0.3	+2.0	V
Analog Supply Voltage, AVDD, V1~V14	-0.5	+15.0	V

TEMPERATURE

	Min.	Max.	Unit
Operating temperature	-20	+85	°C
Storage temperature	-55	+125	°C

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12. RECOMMENDED OPERATING RANGE

Recommended Operating Range (TA = -20 to 85°C, GND = AGND = GND_IF = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD	1.71	1.8	1.89	V
MIPI supply voltage	VDD_IF	1.71	1.8	1.89	V
Analog supply voltage	AVDD	8	-	13.5	V

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13. DC ELECTRICAL CHARACTERISTICS
13.1. Basic DC Characteristic

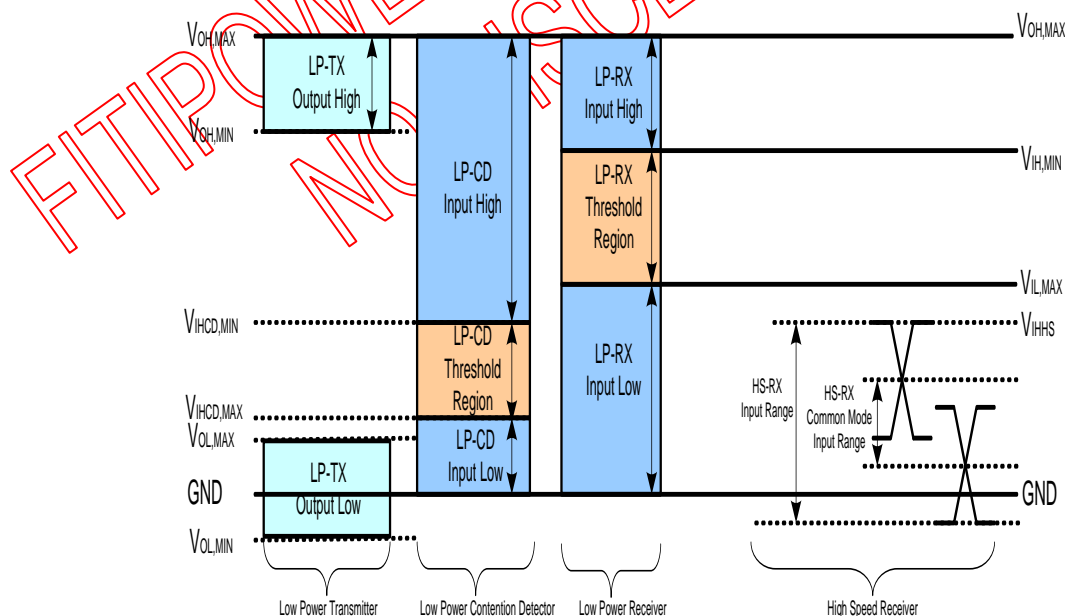
(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level input voltage	Vil	For the digital circuit	0	-	0.3×VDD	V
High level input voltage	Vih	For the digital circuit	0.7×VDD	-	VDD	V
Input leakage current	Ii	For the digital circuit	-	-	±1	μA
High level output voltage	Voh	Ioh= -400 μA	VDD - 0.4	-	-	V
Low level output voltage	Vol	Iol= +400 μA	-	-	GND+0.4	V
Pull low/high resistor	Ri	For the digital input pin @ VDD_IF=1.8V	200K	250K	300K	ohm
Digital Operation current	Idd	Fclk=51.2MHz, VDD=VDD_IF=1.8V	-	TBD	-	mA
Digital Stand-by current	Ist1	Clock and all functions are stopped	-	10	50	μA
Analog Operating Current	Idda	No load, Fclk=51.2MHz, @AVDD=13.5V, V1=13.4V, V14=0.1V	-	10	12	mA
Analog Stand-by current	Ist2	No load, clock and all functions are stopped	-	10	50	μA
Input level of V1 ~ V7	Vref1	Gamma correction voltage input	0.4*AVDD	-	AVDD-0.1	V
Input level of V8 ~ V14	Vref2	Gamma correction voltage input	0.1	-	0.6*AVDD	V
Output Voltage deviation	Vod1	Vo = AGND+0.1V ~ AGND+0.5V and Vo = AVDD-0.5V ~ AVDD-0.1V	-	±20	±35	mV
Output Voltage deviation	Vod2	Vo = AGND+0.5V ~ AVDD-0.5V	-	±15	±20	mV
Output Voltage Offset between Chips	Voc	Vo = AGND+0.5V ~ AVDD-0.5V	-	-	±20	mV
Dynamic Range of Output	Vdr	SO1 ~ 1536	0.1	-	AVDD-0.1	V
Sinking Current of Outputs	IOLy	SO1 ~ 1536; Vo=0.1V v.s 1.0V , AVDD=13.5V	80	-	-	uA
Driving Current of Outputs	IOHy	SO1 ~ 1536; Vo=13.4V v.s 12.5V , AVDD=13.5V	80	-	-	uA
Resistance of Gamma Table	Rg	Rn: Internal gamma resistor	0.7*Rn	1.0*Rn	1.3*Rn	ohm

13.2. MIPI Interface DC Characteristic

(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V, TA=-20°C to 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	VILHS	-40	-	-	mV
Single-ended input high voltage	VIHHS	-	-	460	mV
Common-mode voltage	VCDRXDC	70	-	330	mV
Differential input impedance	ZID		100		ohm
HS transmit differential voltage(VOD=VDP-VDN)	VOD	140	200	250	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	VI	-50	-	1350	mV
Ground shift	VGNDISH	-50	-	50	mV
Logic 0 input threshold	VIL	0	-	550	mV
Logic 1 input threshold	VIH	880	-	1350	mV
Input hysteresis	VHYST	25	-	-	mV
Output low level	VOL	-50	-	50	mV
Output high level	VOH	1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	ZOLP	80	100	125	ohm
Logic 0 contention threshold	VILCD,MAX	-	-	200	mV
Logic 0 contention threshold	VIHCD,MIN	450	-	-	mV



13.3. Power Block DC Characteristic

(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V, TA=-20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Base drive current for PWM	IDRV	-	-	60	mA	DRVA =0.7V
DRV output voltage for PWM	VDRV	0	-	VDD	V	
Feedback voltage for PWM	VFB	1.1	1.2	1.3	V	
Duty cycle maximum	Dmax	-	-	85	%	
VCOM buffer input voltage	VCOMI	1	-	AVDD	V	
VCOM buffer output voltage	VCOMO	VCOMI-0.2	VCOMI	VCOMI+0.2	V	
VCOM buffer output current	IVCOM	-	-	10	mA	VCOMO=5V vs 4.9V

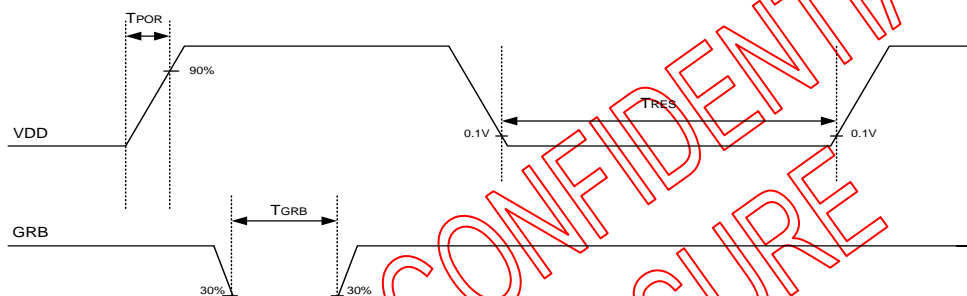
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14. AC ELECTRICAL CHARACTERISTIC
14.1. Basic AC Characteristic

(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V, TA=-20 to +85°C)

VDD/GRB AC characteristic

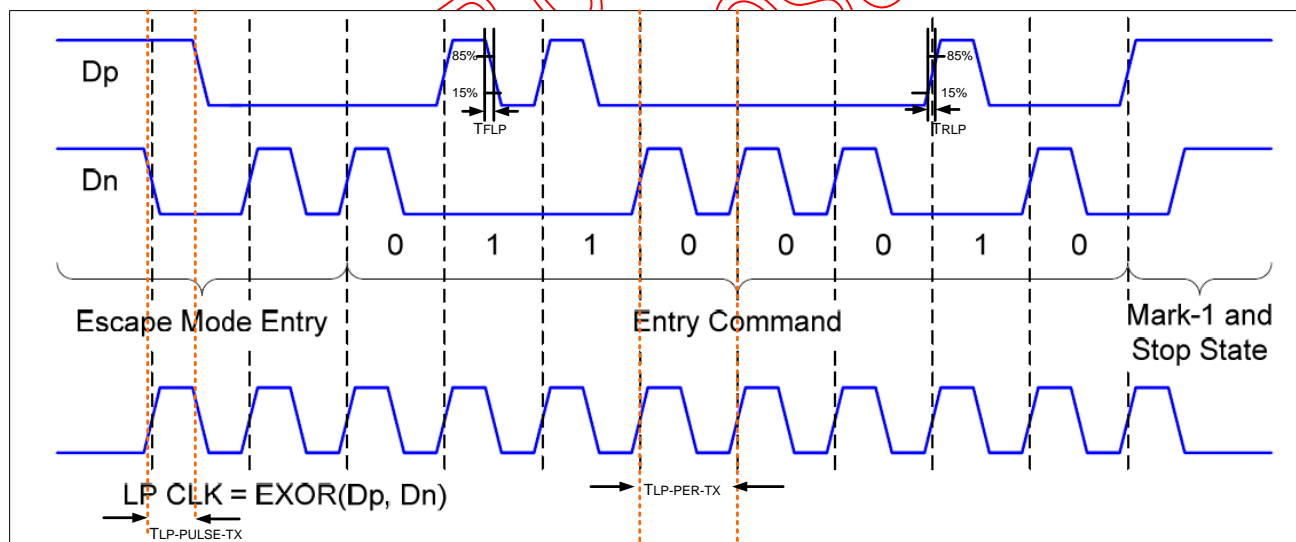
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VDD power slew rate	T _{POR}	-	-	20	ms	From 0 to 90% VDD
GRB active pulse width	T _{GRB}	1	-	-	ms	VDD=VDD_IF=1.8V
VDD resettle time	T _{RES}	1	-	-	s	



14.2. MIPI AC Characteristic

14.2.1. LP Transmitter AC Specification

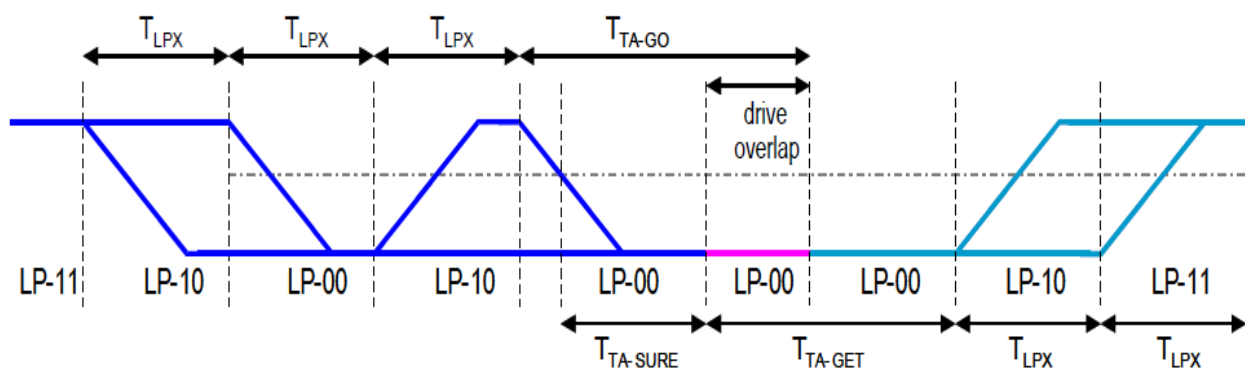
Parameter	Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time	T_{RLP} / T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time	T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR clock	$T_{LP-PULSE-TX}$	40	-	-	ns	-
		20	-	-	ns	-
Period of the LP EXOR clock	$T_{LP-PER-TX}$	90	-	-	mV/ns	-
Slew Rate @CLOAD =0pF	$\delta V / \delta t_{SR}$	30	-	500	mV/ns	-
Slew Rate @CLOAD =5pF		30	-	200	mV/ns	-
Slew Rate @CLOAD =20pF		30	-	150	mV/ns	-
Slew Rate @CLOAD =70pF		30	-	100	mV/ns	-
Load Capacitance	T_{RLP}	-	-	70	pF	-



14.2.2. Turnaround Procedure

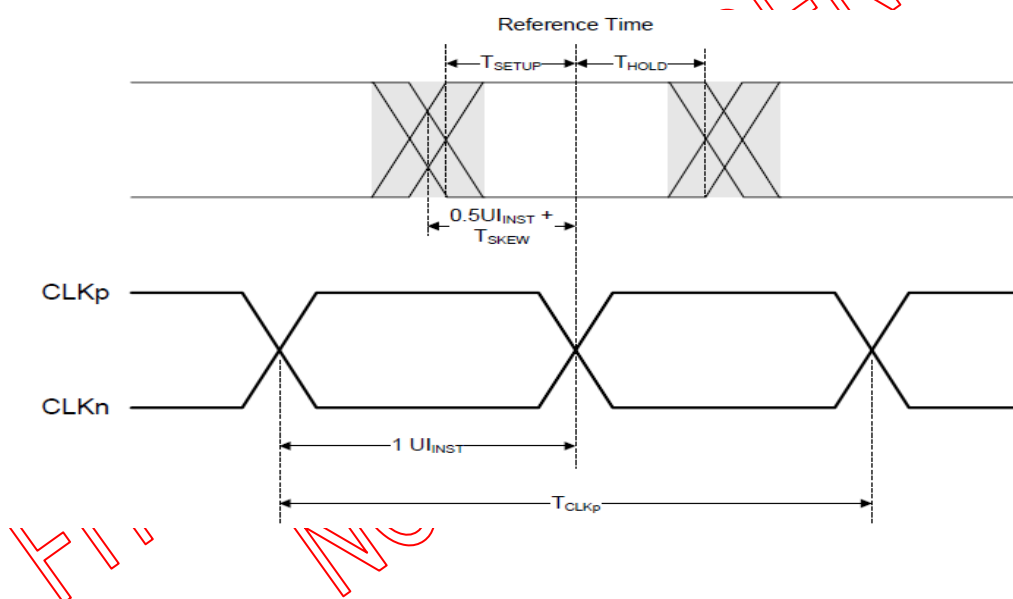
Turnaround Procedure Operation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period: Master side	T_{LPX}	50	-	75	ns
Length of any Low-Power state period: Slave side	T_{LPX}	50	55.56	58.34	ns
Ratio of $T_{LPX}(\text{Master})/T_{LPX}(\text{Slave})$ between Master and Slave side	Ratio T_{LPX}	2/3	-	3/2	
Time-out before new TX side start driving	$T_{TA-Sure}$	T_{LPX}	-	$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}	-	$5T_{LPX}$	-	ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}	-	$4T_{LPX}$	-	ns



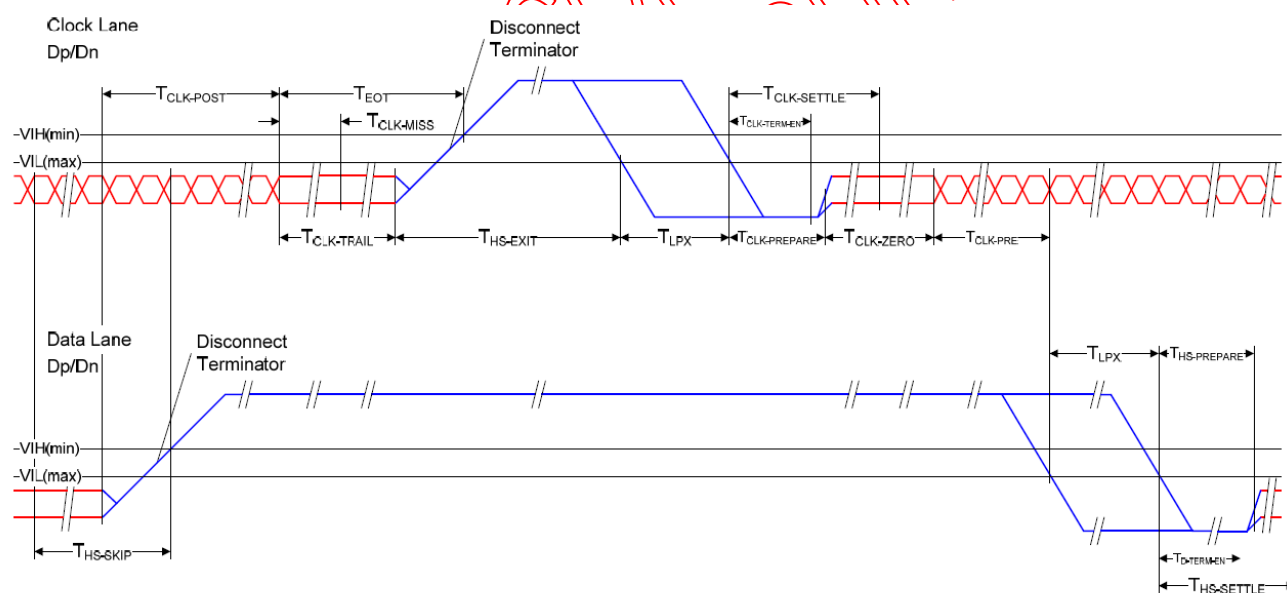
14.2.3. High speed transmission

Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UI_{INST}	2	-	12.5	ns
Data to Clock Skew(measured at transmitter)	$T_{SKEW(TX)}$	-0.15	-	0.15	UI_{INST}
Data to Clock Setup time(measured at receiver)	$T_{SETUP(RX)}$	0.15	-	-	UI_{INST}
Data to Clock Hold time(measured at receiver)	$T_{HOLD(RX)}$	0.15	-	-	UI_{INST}
20%~80% rise time and fall time	T_R, T_F	150	-	-	ps
		-	-	0.3	UI_{INST}

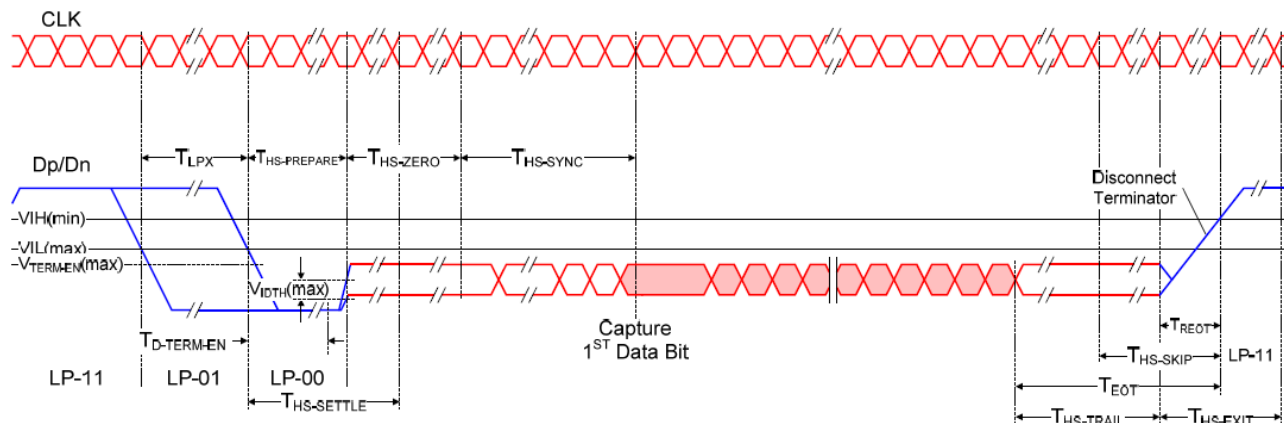


14.2.4. High Speed Clock Transmission

Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	TCLK-MISS	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	TCLK-PREPARE	38	-	95	ns
Minimum lead HS-0 drive period before starting clock	TCLK-PREPARE + TCLK-ZERO	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$	THS-TERM-EN	-	-	38	ns
Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode	TCLK-PRE	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK-TRAIL	60	-	-	ns



14.2.5. High Speed Data Transmission in Bursts

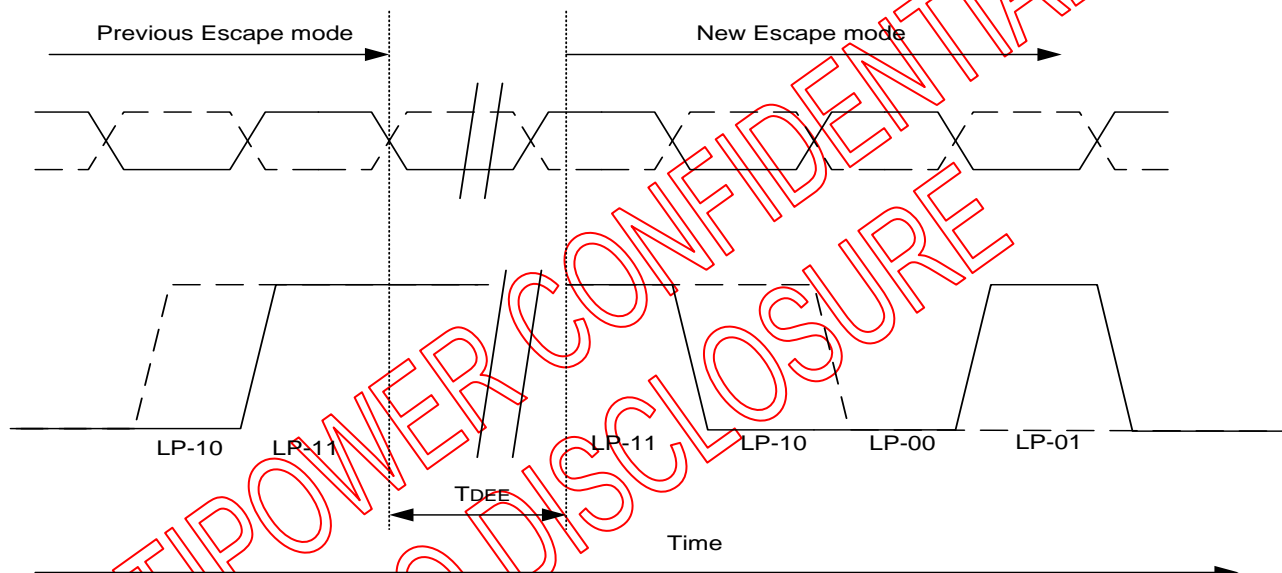


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14.2.6. LP11 timing request between data transformation

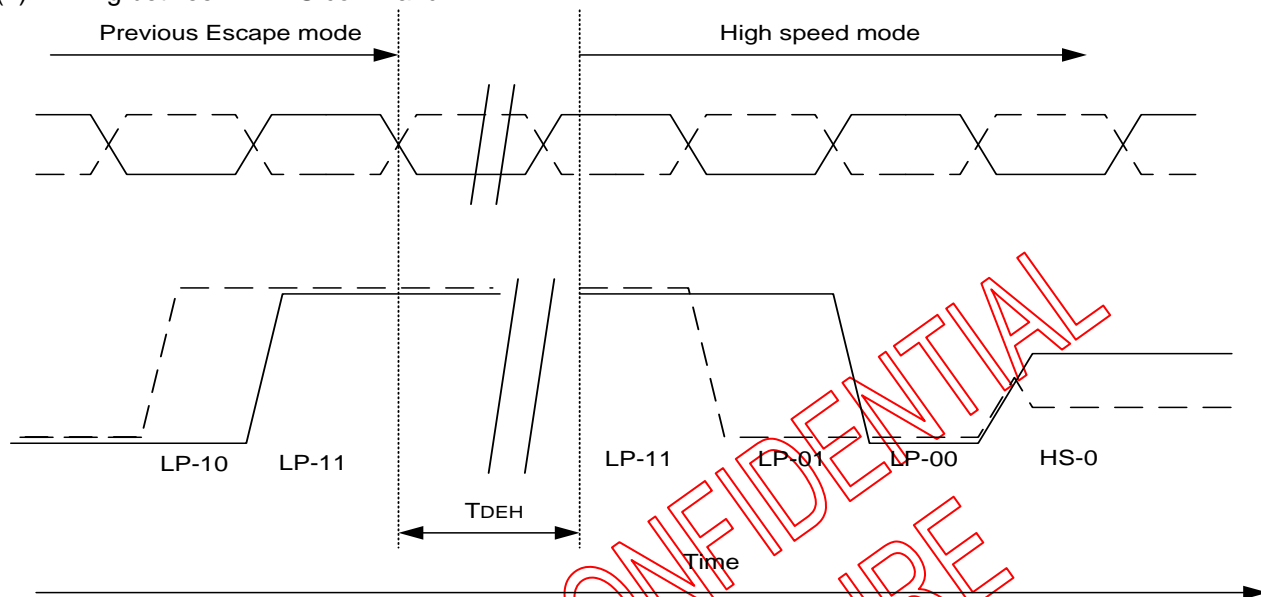
When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode or BTA. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode or BTA. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP-LP, LP-HS, HS-LP, HS-HS, BTA-BTA, LP-BTA, BTA-LP, HS-BTA, and BTA-HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP-LP command



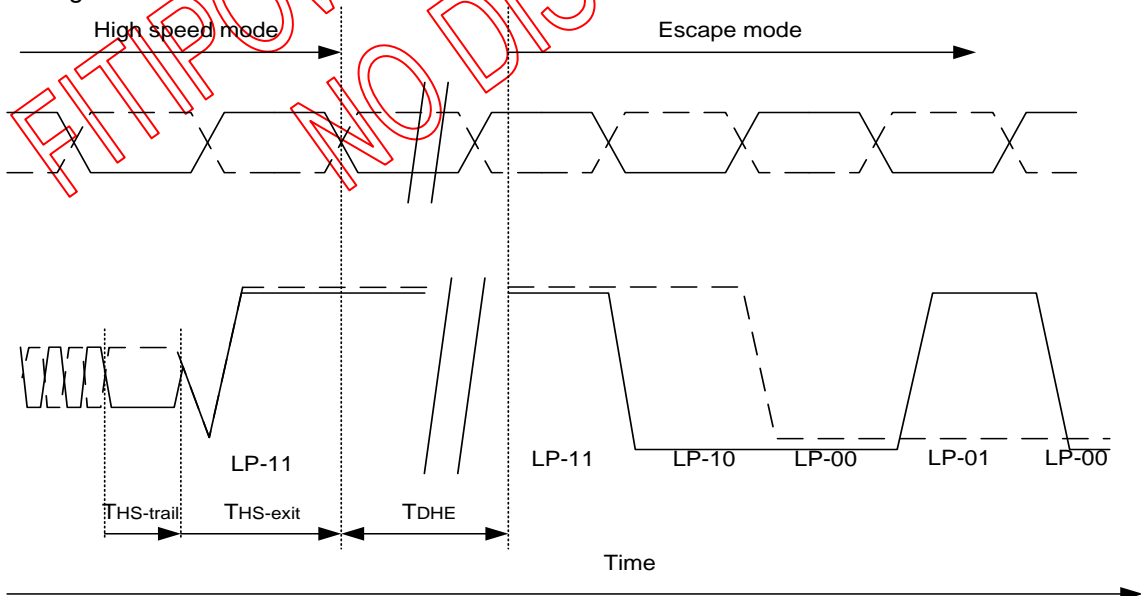
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new Escape Mode Entry	TDEE	150	-	-	ns

(2) Timing between LP-HS command



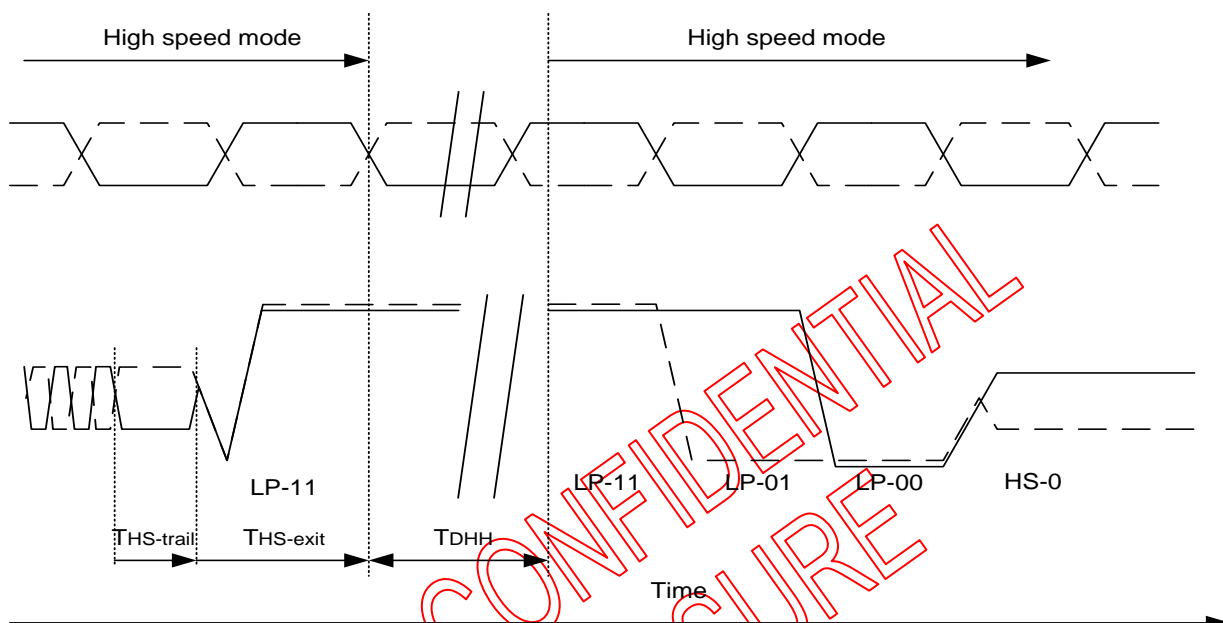
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	TDEH	Max(150,32UI)	-	-	ns

(3) Timing between HS-LP command



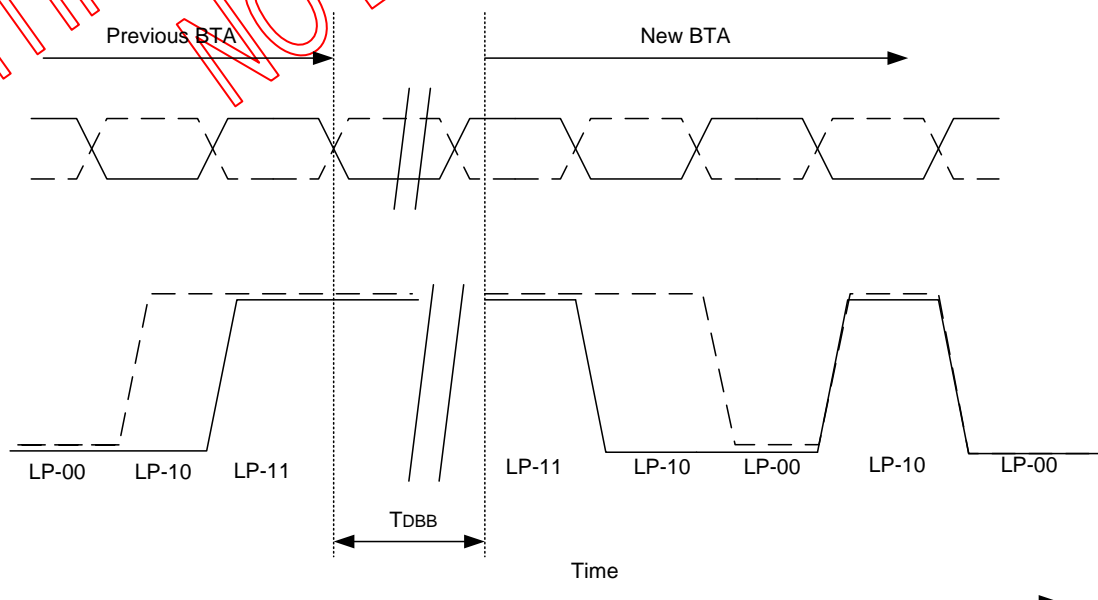
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Escape Mode Entry	TDHE	Max(150,32UI)	-	-	ns

(4) Timing between HS-HS command



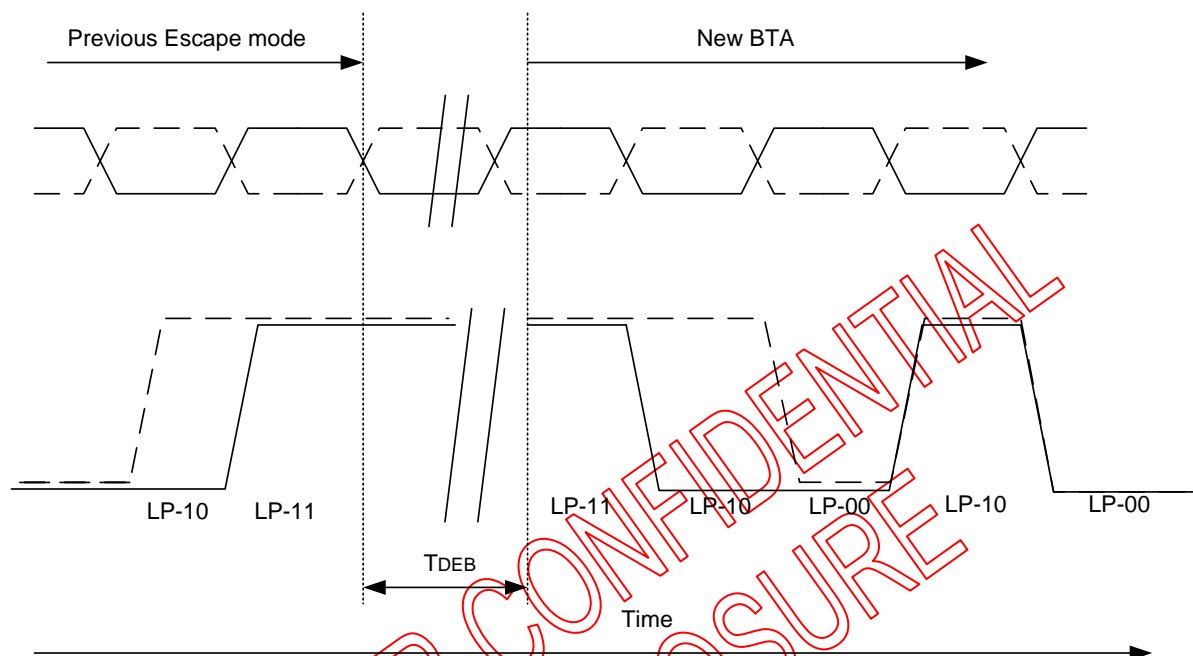
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	T _{DHH}	Max(150,32UI)	-	-	ns

(5) Timing between BTA-BTA command



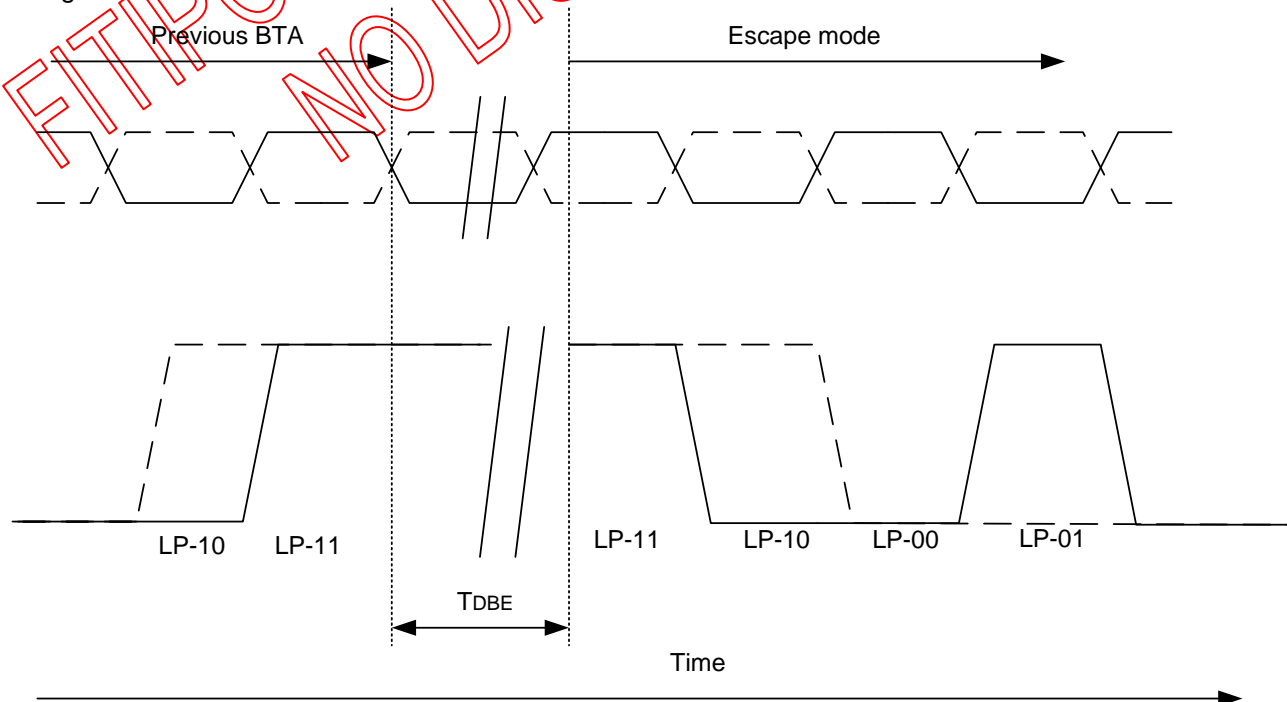
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new BTA	T _{DBB}	150	-	-	ns

(6) Timing between LP-BTA command



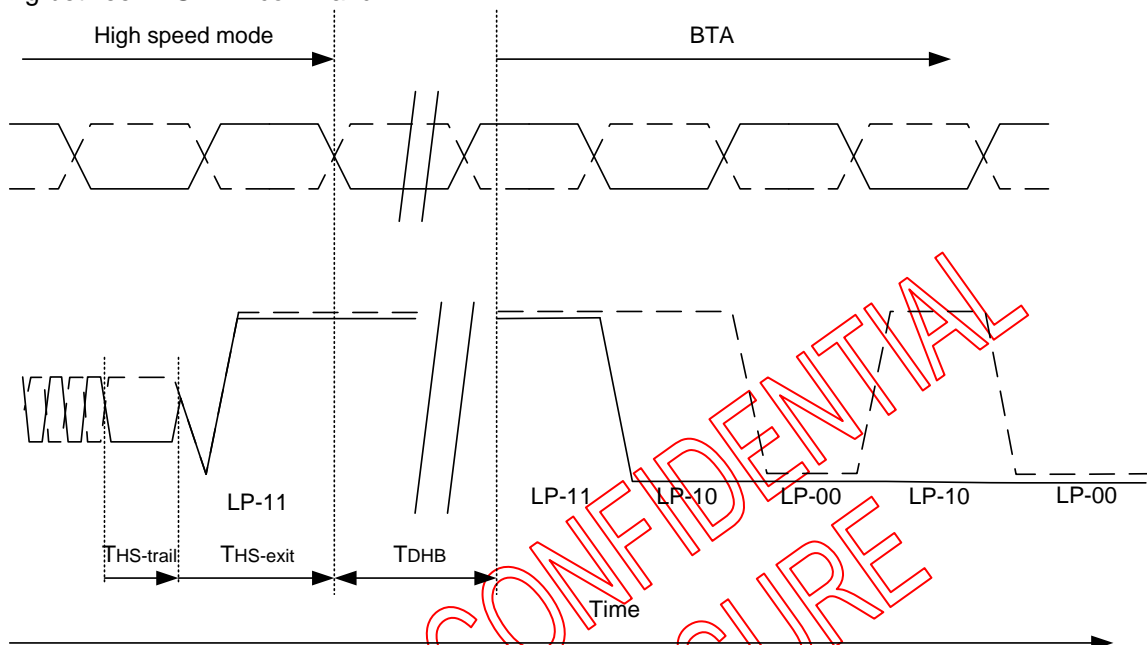
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new BTA	TDEB	150	-	-	ns

(7) Timing between BTA-LP command



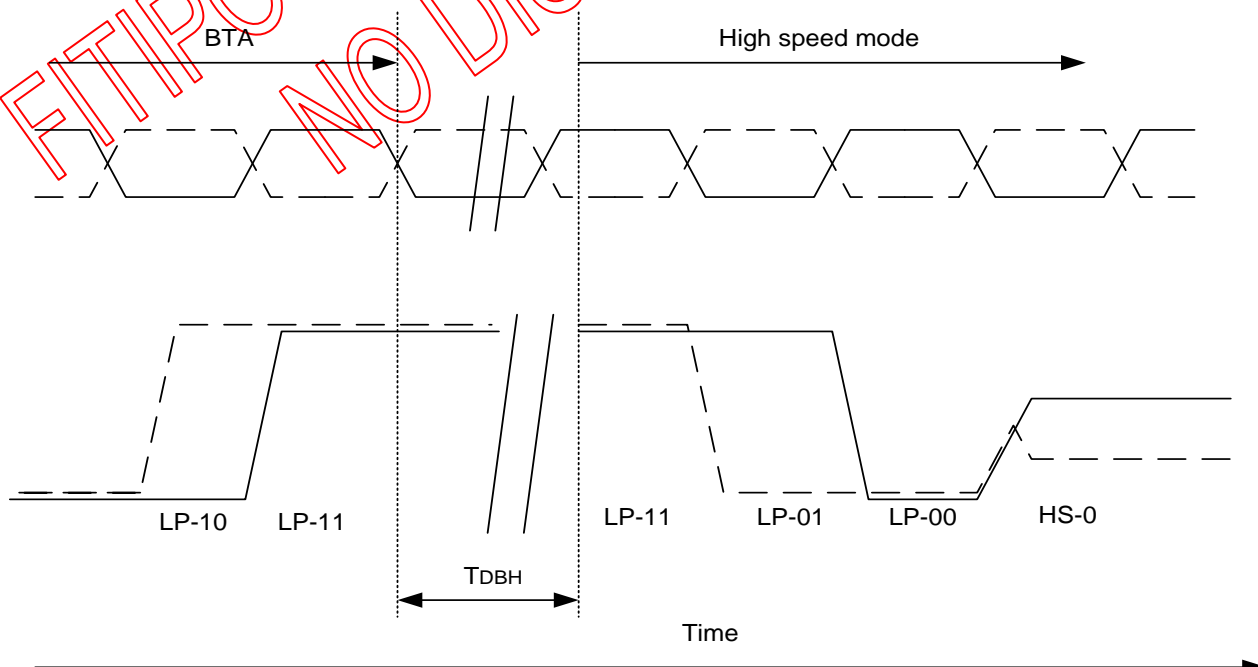
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Escape Mode Entry	TDBE	150	-	-	ns

(8) Timing between HS-BTA command



Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the BTA	TDBH	Max(150,32UI)	-	-	ns

(9) Timing between BTA-HP command



Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	TDBH	Max(150,32UI)	-	-	ns

14.3. Output Timing Table

- Dual gate mode

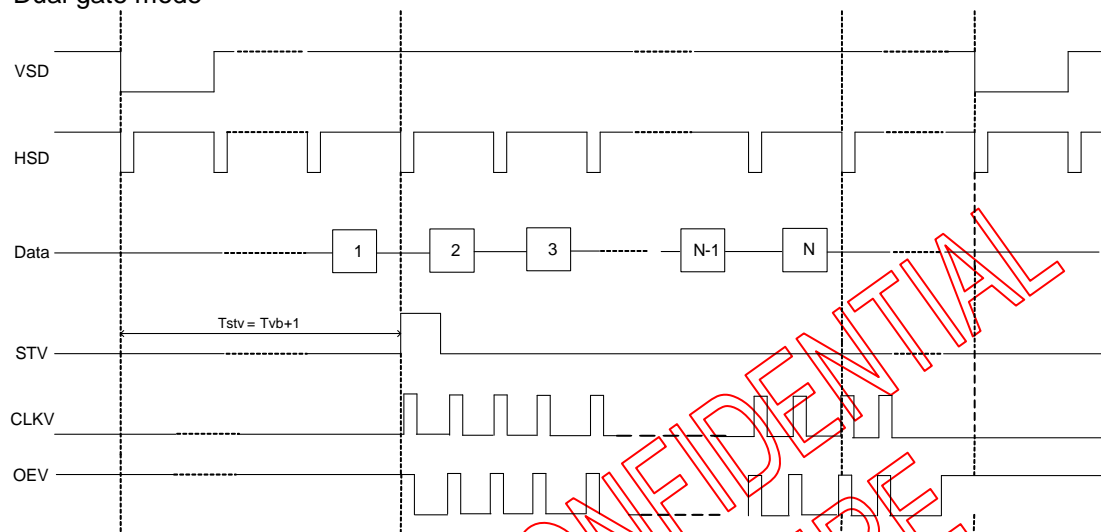


Fig. 11. Vertical output timing

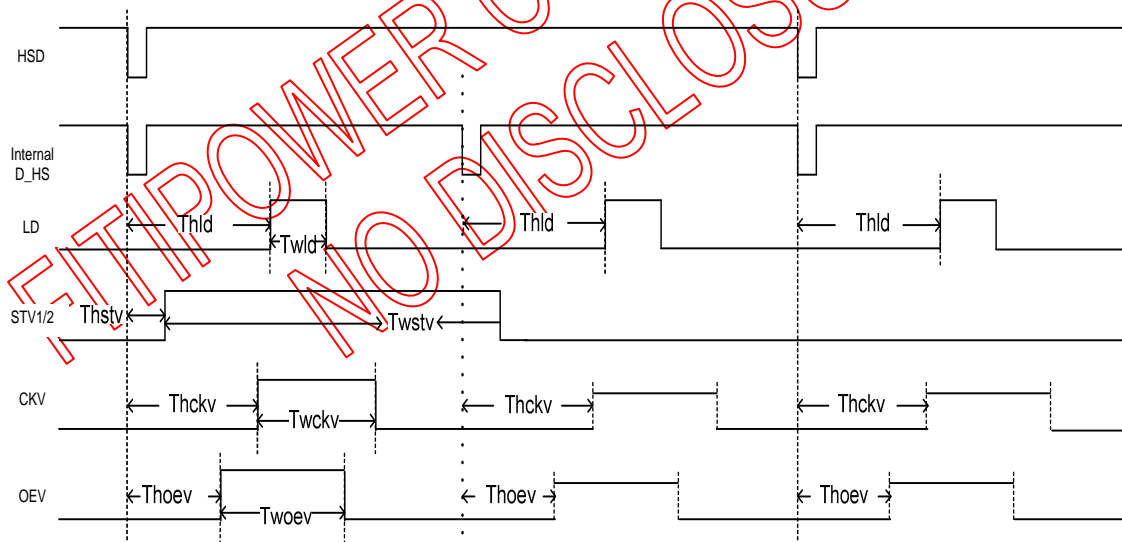
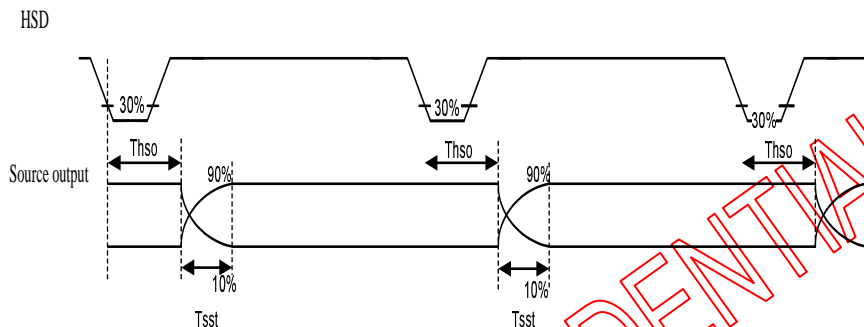


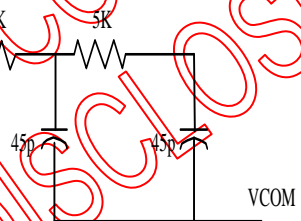
Fig. 11. Gate output timing

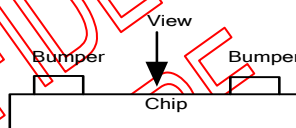
Analog output AC characteristic

Parameter	Symbol	Min.	Typ.	Max	Unit
Source Driver output stable time	Tsst	-	3	-	μs



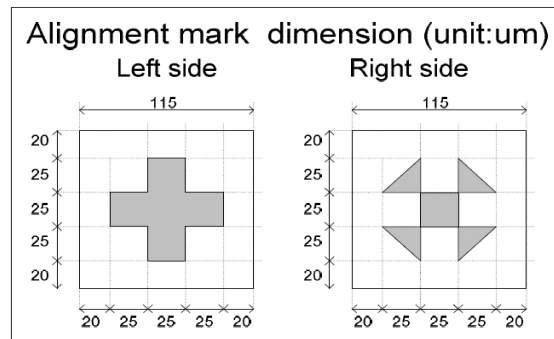
Measure point



[illegible]

Top view diagram of a chip. A central rectangular area is labeled "Chip". On either side of the chip, there is a smaller rectangular area labeled "Bumper". An arrow labeled "View" points down towards the chip area.

15.1. Alignment Mark



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16. PAD COORDINATE

Pin	Customer	X	Y	W	H
1	COM1_IN	-12377.5	-234	65	100
2	COM1_IN	-12292.5	-234	65	100
3	TP1	-12207.5	-234	65	100
4	TP2	-12122.5	-234	65	100
5	TP3	-12037.5	-234	65	100
6	TP4	-11952.5	-234	65	100
7	SHIELDING	-11867.5	-234	65	100
8	AGND	-11782.5	-234	65	100
9	AGND	-11697.5	-234	65	100
10	AGND	-11612.5	-234	65	100
11	AGND	-11527.5	-234	65	100
12	SHIELDING	-11442.5	-234	65	100
13	AVDD	-11357.5	-234	65	100
14	AVDD	-11272.5	-234	65	100
15	AVDD	-11187.5	-234	65	100
16	AVDD	-11102.5	-234	65	100
17	SHIELDING	-11017.5	-234	65	100
18	GND	-10932.5	-234	65	100
19	GND	-10847.5	-234	65	100
20	GND	-10762.5	-234	65	100
21	GND	-10677.5	-234	65	100
22	SHIELDING	-10592.5	-234	65	100
23	VDD	-10507.5	-234	65	100
24	VDD	-10422.5	-234	65	100
25	VDD	-10337.5	-234	65	100
26	VDD	-10252.5	-234	65	100
27	SHIELDING	-10167.5	-234	65	100
28	TP5	-10082.5	-234	65	100
29	TP6	-9997.5	-234	65	100
30	TP7	-9912.5	-234	65	100
31	TP8	-9827.5	-234	65	100
32	TP9	-9742.5	-234	65	100
33	TP10	-9657.5	-234	65	100
34	TP11	-9572.5	-234	65	100
35	TP12	-9487.5	-234	65	100
36	TP13	-9402.5	-234	65	100
37	TP14	-9317.5	-234	65	100
38	SHIELDING	-9232.5	-234	65	100
39	TP45	-9147.5	-234	65	100
40	TP46	-9062.5	-234	65	100
41	NBW	-8977.5	-234	65	100
42	NBW	-8892.5	-234	65	100
43	PINCTL	-8807.5	-234	65	100
44	PINCTL	-8722.5	-234	65	100
45	SHIELDING	-8637.5	-234	65	100
46	DIMO	-8552.5	-234	65	100
47	DIMO	-8467.5	-234	65	100
48	SHIELDING	-8382.5	-234	65	100
49	DITHER	-8297.5	-234	65	100
50	DITHER	-8212.5	-234	65	100
51	HFRC	-8127.5	-234	65	100
52	HFRC	-8042.5	-234	65	100
53	TP15	-7957.5	-234	65	100
54	TP16	-7872.5	-234	65	100
55	FRAME	-7787.5	-234	65	100
56	FRAME	-7702.5	-234	65	100
57	SEL[0]	-7617.5	-234	65	100
58	SEL[0]	-7532.5	-234	65	100
59	SEL[1]	-7447.5	-234	65	100
60	SEL[1]	-7362.5	-234	65	100

61	CSB	-7277.5	-234	65	100
62	CSB	-7192.5	-234	65	100
63	SHIELDING	-7107.5	-234	65	100
64	SDA	-7022.5	-234	65	100
65	SDA	-6937.5	-234	65	100
66	SHIELDING	-6852.5	-234	65	100
67	SCL	-6767.5	-234	65	100
68	SCL	-6682.5	-234	65	100
69	SHIELDING	-6597.5	-234	65	100
70	VDD	-6512.5	-234	65	100
71	VDD	-6427.5	-234	65	100
72	VDD	-6342.5	-234	65	100
73	VDD	-6257.5	-234	65	100
74	SHIELDING	-6172.5	-234	65	100
75	GND	-6087.5	-234	65	100
76	GND	-6002.5	-234	65	100
77	GND	-5917.5	-234	65	100
78	GND	-5832.5	-234	65	100
79	SHIELDING	-5747.5	-234	65	100
80	AVDD	-5662.5	-234	65	100
81	AVDD	-5577.5	-234	65	100
82	AVDD	-5492.5	-234	65	100
83	AVDD	-5407.5	-234	65	100
84	SHIELDING	-5322.5	-234	65	100
85	AGND	-5237.5	-234	65	100
86	AGND	-5152.5	-234	65	100
87	AGND	-5067.5	-234	65	100
88	AGND	-4982.5	-234	65	100
89	SHIELDING	-4897.5	-234	65	100
90	V1	-4812.5	-234	65	100
91	V1	-4727.5	-234	65	100
92	V2	-4642.5	-234	65	100
93	V2	-4557.5	-234	65	100
94	V3	-4472.5	-234	65	100
95	V3	-4387.5	-234	65	100
96	V4	-4302.5	-234	65	100
97	V4	-4217.5	-234	65	100
98	V5	-4132.5	-234	65	100
99	V5	-4047.5	-234	65	100
100	V6	-3962.5	-234	65	100
101	V6	-3877.5	-234	65	100
102	V7	-3792.5	-234	65	100
103	V7	-3707.5	-234	65	100
104	GAMH	-3622.5	-234	65	100
105	GAMH	-3537.5	-234	65	100
106	SHIELDING	-3452.5	-234	65	100
107	DASHD	-3367.5	-234	65	100
108	LVFMT	-3282.5	-234	65	100
109	DASHD	-3197.5	-234	65	100
110	LVBIT	-3112.5	-234	65	100
111	DASHD	-3027.5	-234	65	100
112	TP17	-2942.5	-234	65	100
113	GND_IF	-2857.5	-234	65	100
114	GND_IF	-2772.5	-234	65	100
115	GND_IF	-2687.5	-234	65	100
116	GND_IF	-2602.5	-234	65	100
117	D3P	-2517.5	-234	65	100
118	D3N	-2432.5	-234	65	100
119	DASHD	-2347.5	-234	65	100
120	D2P	-2262.5	-234	65	100
121	D2N	-2177.5	-234	65	100

122	DASHD	-2092.5	-234	65	100
123	CLKP	-2007.5	-234	65	100
124	CLKN	-1922.5	-234	65	100
125	DASHD	-1837.5	-234	65	100
126	D1P	-1752.5	-234	65	100
127	D1N	-1667.5	-234	65	100
128	DASHD	-1582.5	-234	65	100
129	D0P	-1497.5	-234	65	100
130	D0N	-1412.5	-234	65	100
131	DASHD	-1327.5	-234	65	100
132	VDD_IF	-1242.5	-234	65	100
133	VDD_IF	-1157.5	-234	65	100
134	VDD_IF	-1072.5	-234	65	100
135	VDD_IF	-987.5	-234	65	100
136	REV	-902.5	-234	65	100
137	DASHD	-817.5	-234	65	100
138	VDDL	-732.5	-234	65	100
139	VDDL	-647.5	-234	65	100
140	VDDL	-562.5	-234	65	100
141	VDDL	-477.5	-234	65	100
142	VDDL	-392.5	-234	65	100
143	VDDL	-307.5	-234	65	100
144	TP18	-222.5	-234	65	100
145	TP19	-137.5	-234	65	100
146	DASHD	-52.5	-234	65	100
147	TP20	32.5	-234	65	100
148	TP21	117.5	-234	65	100
149	DASHD	202.5	-234	65	100
150	TP22	287.5	-234	65	100
151	TP23	372.5	-234	65	100
152	DASHD	457.5	-234	65	100
153	TP24	542.5	-234	65	100
154	TP25	627.5	-234	65	100
155	DASHD	712.5	-234	65	100
156	TP26	797.5	-234	65	100
157	TP27	882.5	-234	65	100
158	TP28	967.5	-234	65	100
159	TP29	1052.5	-234	65	100
160	TP30	1137.5	-234	65	100
161	DASHD	1222.5	-234	65	100
162	SHIELDING	1307.5	-234	65	100
163	GAML	1392.5	-234	65	100
164	GAML	1477.5	-234	65	100
165	V8	1562.5	-234	65	100
166	V8	1647.5	-234	65	100
167	V9	1732.5	-234	65	100
168	V9	1817.5	-234	65	100
169	V10	1902.5	-234	65	100
170	V10	1987.5	-234	65	100
171	V11	2072.5	-234	65	100
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173	V12	2242.5	-234	65	100
174	V12	2327.5	-234	65	100
175	V13	2412.5	-234	65	100
176	V13	2497.5	-234	65	100
177	V14	2582.5	-234	65	100
178	V14	2667.5	-234	65	100
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182	AGND	3007.5	-234	65	100

183	AGND	3092.5	-234	65	100
184	SHIELDING	3177.5	-234	65	100
185	AVDD	3262.5	-234	65	100
186	AVDD	3347.5	-234	65	100
187	AVDD	3432.5	-234	65	100
188	AVDD	3517.5	-234	65	100
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190	GND	3687.5	-234	65	100
191	GND	3772.5	-234	65	100
192	GND	3857.5	-234	65	100
193	GND	3942.5	-234	65	100
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195	VDD	4112.5	-234	65	100
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215	IFSEL	5812.5	-234	65	100
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218	RES[0]	6067.5	-234	65	100
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222	TP_TEST	6407.5	-234	65	100
223	TP_TEST	6492.5	-234	65	100
224	STBYB	6577.5	-234	65	100
225	STBYB	6662.5	-234	65	100
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248	VDD	8617.5	-234	65	100
249	VDD	8702.5	-234	65	100
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251	VDD	8872.5	-234	65	100
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253	GND	9042.5	-234	65	100
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258	AVDD	9467.5	-234	65	100
259	AVDD	9552.5	-234	65	100
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261	AVDD	9722.5	-234	65	100
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267	SHIELDING	10232.5	-234	65	100
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274	FBL	10827.5	-234	65	100
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281	DRVA	11422.5	-234	65	100
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283	DRVH	11592.5	-234	65	100
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289	VCOMO	12102.5	-234	65	100
290	VCOMO	12187.5	-234	65	100
291	COM2_IN	12272.5	-234	65	100
292	COM2_IN	12357.5	-234	65	100
293	STBNL	12303	-72	80	30
294	F_CtrlL	12403	-32	80	30
295	STV2L	12303	8	80	30
296	STV1L	12403	48	80	30
297	CKVL	12303	88	80	30
298	UDL	12403	128	80	30
299	SYNC2L	12303	168	80	30
300	SYNC1L	12403	208	80	30
301	OEVL	12303	248	80	30
302	F_CtrlL	12403	288	80	30
303	SHIELDING	12205	268	30	70
304	COM2_OUT	12155	268	30	70

305	COM2_OUT	12105	268	30	70
306	SHIELDING	12055	268	30	70
307	SO1	12012.5	133	14	80
308	SO2	11997.5	263	14	80
309	SO3	11982.5	133	14	80
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315	SO9	11892.5	133	14	80
316	SO10	11877.5	263	14	80
317	SO11	11862.5	133	14	80
318	SO12	11847.5	263	14	80
319	SO13	11832.5	133	14	80
320	SO14	11817.5	263	14	80
321	SO15	11802.5	133	14	80
322	SO16	11787.5	263	14	80
323	SO17	11772.5	133	14	80
324	SO18	11757.5	263	14	80
325	SO19	11742.5	133	14	80
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643	SO337	6972.5	133	14	80
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970	SO664	2067.5	263	14	80
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974	SO668	2007.5	263	14	80
975	SO669	1992.5	133	14	80

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977	SO671	1962.5	133	14	80
978	SO672	1947.5	263	14	80
979	SO673	1932.5	133	14	80
980	SO674	1917.5	263	14	80
981	SO675	1902.5	133	14	80
982	SO676	1887.5	263	14	80
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1080	SHIELDING	-50	268	30	70
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1100	SO785	-747.5	263	14	80
1101	SO786	-762.5	133	14	80
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1521	SO1206	-7062.5	133	14	80
1522	SO1207	-7077.5	263	14	80
1523	SO1208	-7092.5	133	14	80
1524	SO1209	-7107.5	263	14	80

1525	SO1210	-7122.5	133	14	80
1526	SO1211	-7137.5	263	14	80
1527	SO1212	-7152.5	133	14	80
1528	SO1213	-7167.5	263	14	80
1529	SO1214	-7182.5	133	14	80
1530	SO1215	-7197.5	263	14	80
1531	SO1216	-7212.5	133	14	80
1532	SO1217	-7227.5	263	14	80
1533	SO1218	-7242.5	133	14	80
1534	SO1219	-7257.5	263	14	80
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1537	SO1222	-7302.5	133	14	80
1538	SO1223	-7317.5	263	14	80
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1541	SO1226	-7362.5	133	14	80
1542	SO1227	-7377.5	263	14	80
1543	SO1228	-7392.5	133	14	80
1544	SO1229	-7407.5	263	14	80
1545	SO1230	-7422.5	133	14	80
1546	SO1231	-7437.5	263	14	80
1547	SO1232	-7452.5	133	14	80
1548	SO1233	-7467.5	263	14	80
1549	SO1234	-7482.5	133	14	80
1550	SO1235	-7497.5	263	14	80
1551	SO1236	-7512.5	133	14	80
1552	SO1237	-7527.5	263	14	80
1553	SO1238	-7542.5	133	14	80
1554	SO1239	-7557.5	263	14	80
1555	SO1240	-7572.5	133	14	80
1556	SO1241	-7587.5	263	14	80
1557	SO1242	-7602.5	133	14	80
1558	SO1243	-7617.5	263	14	80
1559	SO1244	-7632.5	133	14	80
1560	SO1245	-7647.5	263	14	80
1561	SO1246	-7662.5	133	14	80
1562	SO1247	-7677.5	263	14	80
1563	SO1248	-7692.5	133	14	80
1564	SO1249	-7707.5	263	14	80
1565	SO1250	-7722.5	133	14	80
1566	SO1251	-7737.5	263	14	80
1567	SO1252	-7752.5	133	14	80
1568	SO1253	-7767.5	263	14	80
1569	SO1254	-7782.5	133	14	80
1570	SO1255	-7797.5	263	14	80
1571	SO1256	-7812.5	133	14	80
1572	SO1257	-7827.5	263	14	80
1573	SO1258	-7842.5	133	14	80
1574	SO1259	-7857.5	263	14	80
1575	SO1260	-7872.5	133	14	80
1576	SO1261	-7887.5	263	14	80
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1584	SO1269	-8007.5	263	14	80
1585	SO1270	-8022.5	133	14	80

1586	SO1271	-8037.5	263	14	80
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1588	SO1273	-8067.5	263	14	80
1589	SO1274	-8082.5	133	14	80
1590	SO1275	-8097.5	263	14	80
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1593	SO1278	-8142.5	133	14	80
1594	SO1279	-8157.5	263	14	80
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1596	SO1281	-8187.5	263	14	80
1597	SO1282	-8202.5	133	14	80
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1602	SO1287	-8277.5	263	14	80
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1613	SO1298	-8442.5	133	14	80
1614	SO1299	-8457.5	263	14	80
1615	SO1300	-8472.5	133	14	80
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1617	SO1302	-8502.5	133	14	80
1618	SO1303	-8517.5	263	14	80
1619	SO1304	-8532.5	133	14	80
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1626	SO1311	-8637.5	263	14	80
1627	SO1312	-8652.5	133	14	80
1628	SO1313	-8667.5	263	14	80
1629	SO1314	-8682.5	133	14	80
1630	SO1315	-8697.5	263	14	80
1631	SO1316	-8712.5	133	14	80
1632	SO1317	-8727.5	263	14	80
1633	SO1318	-8742.5	133	14	80
1634	SO1319	-8757.5	263	14	80
1635	SO1320	-8772.5	133	14	80
1636	SO1321	-8787.5	263	14	80
1637	SO1322	-8802.5	133	14	80
1638	SO1323	-8817.5	263	14	80
1639	SO1324	-8832.5	133	14	80
1640	SO1325	-8847.5	263	14	80
1641	SO1326	-8862.5	133	14	80
1642	SO1327	-8877.5	263	14	80
1643	SO1328	-8892.5	133	14	80
1644	SO1329	-8907.5	263	14	80
1645	SO1330	-8922.5	133	14	80
1646	SO1331	-8937.5	263	14	80

1647	SO1332	-8952.5	133	14	80
1648	SO1333	-8967.5	263	14	80
1649	SO1334	-8982.5	133	14	80
1650	SO1335	-8997.5	263	14	80
1651	SO1336	-9012.5	133	14	80
1652	SO1337	-9027.5	263	14	80
1653	SO1338	-9042.5	133	14	80
1654	SO1339	-9057.5	263	14	80
1655	SO1340	-9072.5	133	14	80
1656	SO1341	-9087.5	263	14	80
1657	SO1342	-9102.5	133	14	80
1658	SO1343	-9117.5	263	14	80
1659	SO1344	-9132.5	133	14	80
1660	SO1345	-9147.5	263	14	80
1661	SO1346	-9162.5	133	14	80
1662	SO1347	-9177.5	263	14	80
1663	SO1348	-9192.5	133	14	80
1664	SO1349	-9207.5	263	14	80
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1666	SO1351	-9237.5	263	14	80
1667	SO1352	-9252.5	133	14	80
1668	SO1353	-9267.5	263	14	80
1669	SO1354	-9282.5	133	14	80
1670	SO1355	-9297.5	263	14	80
1671	SO1356	-9312.5	133	14	80
1672	SO1357	-9327.5	263	14	80
1673	SO1358	-9342.5	133	14	80
1674	SO1359	-9357.5	263	14	80
1675	SO1360	-9372.5	133	14	80
1676	SO1361	-9387.5	263	14	80
1677	SO1362	-9402.5	133	14	80
1678	SO1363	-9417.5	263	14	80
1679	SO1364	-9432.5	133	14	80
1680	SO1365	-9447.5	263	14	80
1681	SO1366	-9462.5	133	14	80
1682	SO1367	-9477.5	263	14	80
1683	SO1368	-9492.5	133	14	80
1684	SO1369	-9507.5	263	14	80
1685	SO1370	-9522.5	133	14	80
1686	SO1371	-9537.5	263	14	80
1687	SO1372	-9552.5	133	14	80
1688	SO1373	-9567.5	263	14	80
1689	SO1374	-9582.5	133	14	80
1690	SO1375	-9597.5	263	14	80
1691	SO1376	-9612.5	133	14	80
1692	SO1377	-9627.5	263	14	80
1693	SO1378	-9642.5	133	14	80
1694	SO1379	-9657.5	263	14	80
1695	SO1380	-9672.5	133	14	80
1696	SO1381	-9687.5	263	14	80
1697	SO1382	-9702.5	133	14	80
1698	SO1383	-9717.5	263	14	80
1699	SO1384	-9732.5	133	14	80
1700	SO1385	-9747.5	263	14	80
1701	SO1386	-9762.5	133	14	80
1702	SO1387	-9777.5	263	14	80
1703	SO1388	-9792.5	133	14	80
1704	SO1389	-9807.5	263	14	80
1705	SO1390	-9822.5	133	14	80
1706	SO1391	-9837.5	263	14	80
1707	SO1392	-9852.5	133	14	80

1708	SO1393	-9867.5	263	14	80
1709	SO1394	-9882.5	133	14	80
1710	SO1395	-9897.5	263	14	80
1711	SO1396	-9912.5	133	14	80
1712	SO1397	-9927.5	263	14	80
1713	SO1398	-9942.5	133	14	80
1714	SO1399	-9957.5	263	14	80
1715	SO1400	-9972.5	133	14	80
1716	SO1401	-9987.5	263	14	80
1717	SO1402	-10002.5	133	14	80
1718	SO1403	-10017.5	263	14	80
1719	SO1404	-10032.5	133	14	80
1720	SO1405	-10047.5	263	14	80
1721	SO1406	-10062.5	133	14	80
1722	SO1407	-10077.5	263	14	80
1723	SO1408	-10092.5	133	14	80
1724	SO1409	-10107.5	263	14	80
1725	SO1410	-10122.5	133	14	80
1726	SO1411	-10137.5	263	14	80
1727	SO1412	-10152.5	133	14	80
1728	SO1413	-10167.5	263	14	80
1729	SO1414	-10182.5	133	14	80
1730	SO1415	-10197.5	263	14	80
1731	SO1416	-10212.5	133	14	80
1732	SO1417	-10227.5	263	14	80
1733	SO1418	-10242.5	133	14	80
1734	SO1419	-10257.5	263	14	80
1735	SO1420	-10272.5	133	14	80
1736	SO1421	-10287.5	263	14	80
1737	SO1422	-10302.5	133	14	80
1738	SO1423	-10317.5	263	14	80
1739	SO1424	-10332.5	133	14	80
1740	SO1425	-10347.5	263	14	80
1741	SO1426	-10362.5	133	14	80
1742	SO1427	-10377.5	263	14	80
1743	SO1428	-10392.5	133	14	80
1744	SO1429	-10407.5	263	14	80
1745	SO1430	-10422.5	133	14	80
1746	SO1431	-10437.5	263	14	80
1747	SO1432	-10452.5	133	14	80
1748	SO1433	-10467.5	263	14	80
1749	SO1434	-10482.5	133	14	80
1750	SO1435	-10497.5	263	14	80
1751	SO1436	-10512.5	133	14	80
1752	SO1437	-10527.5	263	14	80
1753	SO1438	-10542.5	133	14	80
1754	SO1439	-10557.5	263	14	80
1755	SO1440	-10572.5	133	14	80
1756	SO1441	-10587.5	263	14	80
1757	SO1442	-10602.5	133	14	80
1758	SO1443	-10617.5	263	14	80
1759	SO1444	-10632.5	133	14	80
1760	SO1445	-10647.5	263	14	80
1761	SO1446	-10662.5	133	14	80
1762	SO1447	-10677.5	263	14	80
1763	SO1448	-10692.5	133	14	80
1764	SO1449	-10707.5	263	14	80
1765	SO1450	-10722.5	133	14	80
1766	SO1451	-10737.5	263	14	80
1767	SO1452	-10752.5	133	14	80
1768	SO1453	-10767.5	263	14	80

1769	SO1454	-10782.5	133	14	80
1770	SO1455	-10797.5	263	14	80
1771	SO1456	-10812.5	133	14	80
1772	SO1457	-10827.5	263	14	80
1773	SO1458	-10842.5	133	14	80
1774	SO1459	-10857.5	263	14	80
1775	SO1460	-10872.5	133	14	80
1776	SO1461	-10887.5	263	14	80
1777	SO1462	-10902.5	133	14	80
1778	SO1463	-10917.5	263	14	80
1779	SO1464	-10932.5	133	14	80
1780	SO1465	-10947.5	263	14	80
1781	SO1466	-10962.5	133	14	80
1782	SO1467	-10977.5	263	14	80
1783	SO1468	-10992.5	133	14	80
1784	SO1469	-11007.5	263	14	80
1785	SO1470	-11022.5	133	14	80
1786	SO1471	-11037.5	263	14	80
1787	SO1472	-11052.5	133	14	80
1788	SO1473	-11067.5	263	14	80
1789	SO1474	-11082.5	133	14	80
1790	SO1475	-11097.5	263	14	80
1791	SO1476	-11112.5	133	14	80
1792	SO1477	-11127.5	263	14	80
1793	SO1478	-11142.5	133	14	80
1794	SO1479	-11157.5	263	14	80
1795	SO1480	-11172.5	133	14	80
1796	SO1481	-11187.5	263	14	80
1797	SO1482	-11202.5	133	14	80
1798	SO1483	-11217.5	263	14	80
1799	SO1484	-11232.5	133	14	80
1800	SO1485	-11247.5	263	14	80
1801	SO1486	-11262.5	133	14	80
1802	SO1487	-11277.5	263	14	80
1803	SO1488	-11292.5	133	14	80
1804	SO1489	-11307.5	263	14	80
1805	SO1490	-11322.5	133	14	80
1806	SO1491	-11337.5	263	14	80
1807	SO1492	-11352.5	133	14	80
1808	SO1493	-11367.5	263	14	80
1809	SO1494	-11382.5	133	14	80
1810	SO1495	-11397.5	263	14	80
1811	SO1496	-11412.5	133	14	80
1812	SO1497	-11427.5	263	14	80
1813	SO1498	-11442.5	133	14	80
1814	SO1499	-11457.5	263	14	80
1815	SO1500	-11472.5	133	14	80
1816	SO1501	-11487.5	263	14	80
1817	SO1502	-11502.5	133	14	80
1818	SO1503	-11517.5	263	14	80
1819	SO1504	-11532.5	133	14	80
1820	SO1505	-11547.5	263	14	80
1821	SO1506	-11562.5	133	14	80
1822	SO1507	-11577.5	263	14	80
1823	SO1508	-11592.5	133	14	80
1824	SO1509	-11607.5	263	14	80
1825	SO1510	-11622.5	133	14	80
1826	SO1511	-11637.5	263	14	80
1827	SO1512	-11652.5	133	14	80
1828	SO1513	-11667.5	263	14	80
1829	SO1514	-11682.5	133	14	80

1830	SO1515	-11697.5	263	14	80
1831	SO1516	-11712.5	133	14	80
1832	SO1517	-11727.5	263	14	80
1833	SO1518	-11742.5	133	14	80
1834	SO1519	-11757.5	263	14	80
1835	SO1520	-11772.5	133	14	80
1836	SO1521	-11787.5	263	14	80
1837	SO1522	-11802.5	133	14	80
1838	SO1523	-11817.5	263	14	80
1839	SO1524	-11832.5	133	14	80
1840	SO1525	-11847.5	263	14	80
1841	SO1526	-11862.5	133	14	80
1842	SO1527	-11877.5	263	14	80
1843	SO1528	-11892.5	133	14	80
1844	SO1529	-11907.5	263	14	80
1845	SO1530	-11922.5	133	14	80
1846	SO1531	-11937.5	263	14	80
1847	SO1532	-11952.5	133	14	80
1848	SO1533	-11967.5	263	14	80
1849	SO1534	-11982.5	133	14	80
1850	SO1535	-11997.5	263	14	80
1851	SO1536	-12012.5	133	14	80
1852	SHIELDING	-12055	268	30	70
1853	COM1_OUT	-12105	268	30	70
1854	COM1_OUT	-12155	268	30	70
1855	SHIELDING	-12205	268	30	70
1856	F_CtrlR	-12403	288	80	30
1857	OEVR	-12303	248	80	30
1858	SYNC1R	-12403	208	80	30
1859	SYNC2R	-12303	168	80	30
1860	UDR	-12403	128	80	30
1861	CKVR	-12303	88	80	30
1862	STV2R	-12403	48	80	30
1863	STV1R	-12303	8	80	30
1864	F_CtrlR	-12403	-32	80	30
1865	STENR	-12303	-72	80	30

ALM		
LEFT	-12131.5	125.5
RIGHT	12131.5	125.5

17. REVISION HISTORY

Reversion	Content	Date
1.0	New version	2020/07/22

FITIPOWER CONFIDENTIAL
NO DISCLOSURE

Appendix A : BIST pattern

R→G→B→Black→White→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern
→Chess board (L255/L0)→Flicker pattern→Black background with white out frame

