SPECIFICATION

☐ Preliminary Specification
■ Final Specification

Customer Approve:

QC 品 质 : _____

R&D 研 发 : _____

Approved 批准: _____

产品型号**(Description):** HT070IBC-27N7EK-HD 30PTT3558

Compile by 编制	Quality/Engineer 品质/工程	Checked 审核	Approved 批准

REVISION RECORD

REV NO	REV DATE	CONTENTS	REMARKS
V.0	2021-02-23	First Release	

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1.0 General description

1.1 Introduction

HT0701BC-27N7EK-HD 30PTT3558**is model a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses**

amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit and a back light system. This TFT LCD has a 7.0 inch diagonally measured active display area with WSVGA (1024 horizontal by 600 vertical pixel array) resolution. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.

1.2 Features

- **4 lanes MIPI Interface**
- Low driving voltage and low power consumption
- ROHS Compliant

1.3 General information

Item	Specification	Unit	Remarks
Outline Dimension	165(H) x 100(V) x 3.5(body)	mm	Tolerance: ±0.2mm
Display area	154.2144(W) x85.92(H)	mm	
Number of Pixel	1024(H) x RGB x600(V)	pixels	
Pixel pitch	0.1506(H) x 0.1432(V)	mm	
Pixel arrangement	Pixels RGB stripe arrangement		
Display mode	Normally Black		
Surface treatment	IPS		
Back-light	Single LED (Side-Light type)		

1.4 Mechanical Information

Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal(H)	164.8	165	165.2	mm
	Vertical(V)	99.8	100	100.2	mm
	Depth(D)	3.3	3.5	3.7	mm

- **4 lanes MIPI Interface**
- Low driving voltage and low power consumption
- ROHS Compliant

2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Electrical Absolute Rating

2.1.1 TFT LCD Module

Item		Specification	Unit
Outline Dimension		165(H) x 100(V) x 3.5(body)	mm
Display area		154.2144(W) x85.92(H)	mm
Number of Pixel		1024(H) x RGB x600(V)	pixels
Pixel pitch		0.1506(H) x 0.1432(V)	mm
Pixel arrangement		Pixels RGB stripe arrangement	
Display mode		Normally Black	
Surface treatment		IPS Film	
Weight		TBD (Typ.)	gram
Back-light		Single LED (Side-Light type)	
Power Consumption	B/L System	TBD(Max.)	watt

2.1.2 Back-Light Unit

Item	Symbol	Typ	MIN.	TYP.	MAX.	Unit	Note
Forward voltage	Vf	9.0	8.4	9.0	9.9	V	(1)(2)
Forward current	If	180	--	--	--	mA	(1)(2) (3)
Power Consumption	PBL	--	--	--	--	mW	

Note:

(1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2) Ta =25±2℃

(3) Test Condition: LED current 180 mA

3.0 OPTICAL CHARACTERISTICS

3.1 Optical Specifications

Item		Symbol	Temp	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle range		Horizontal	θ	CR > 10	80	85	--	Deg	Note 1
		Vertical	θ		80	85	--	Deg	
Luminance Contrast ratio			CR	θ = 0°	600：1	800	--	--	Note 2
Brightness			YL		350	400	--	Cd/cm2	
Transmittance			T(%)	θ = 0°	--	5.0	--	%	Note 3
Color Gamut (C light)					45	50	--	%	
White chromaticity			Wx	Θ=0°	TYP. -0.02	0.303	TYP. +0.02		Note 4
			Wy			0.333			
Reproduction of color （C-light）		Red	Rx			0.618			
			Ry			0.326			
		Green	Gx			0.285			
			Gy			0.539			
		Blue	Bx			0.146			
			By			0.148			
Response Time (Rising + Falling)		Trt		Ta= 25°C θ = 0°	--	25	40	ms	Note 5

3.2 Measuring Condition

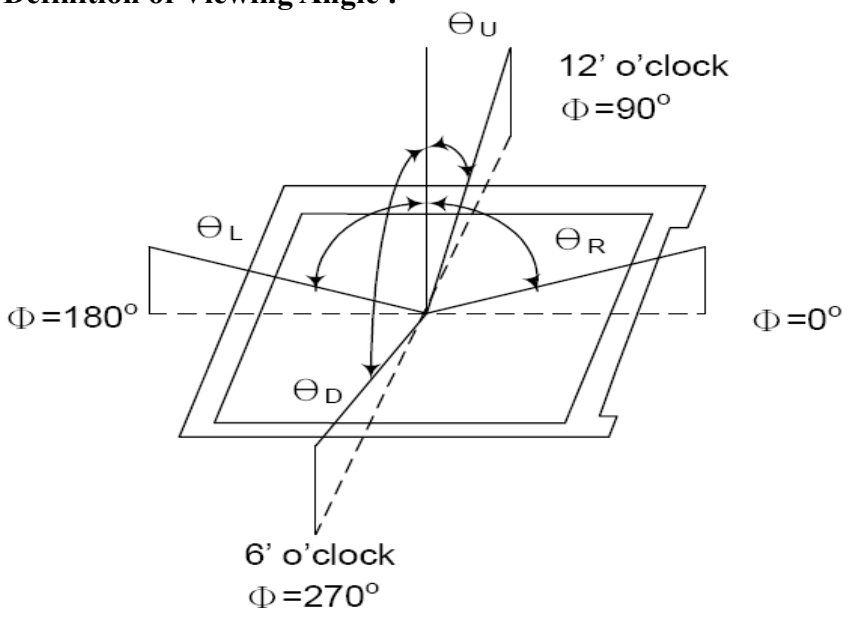
Measuring surrounding: dark room ,LED current IL :180mA

Ambient temperature: 25±2℃ 15min. warm-up time.

3.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics. Measuring spot size: 20 ~ 21 mm

Note (1) Definition of Viewing Angle :

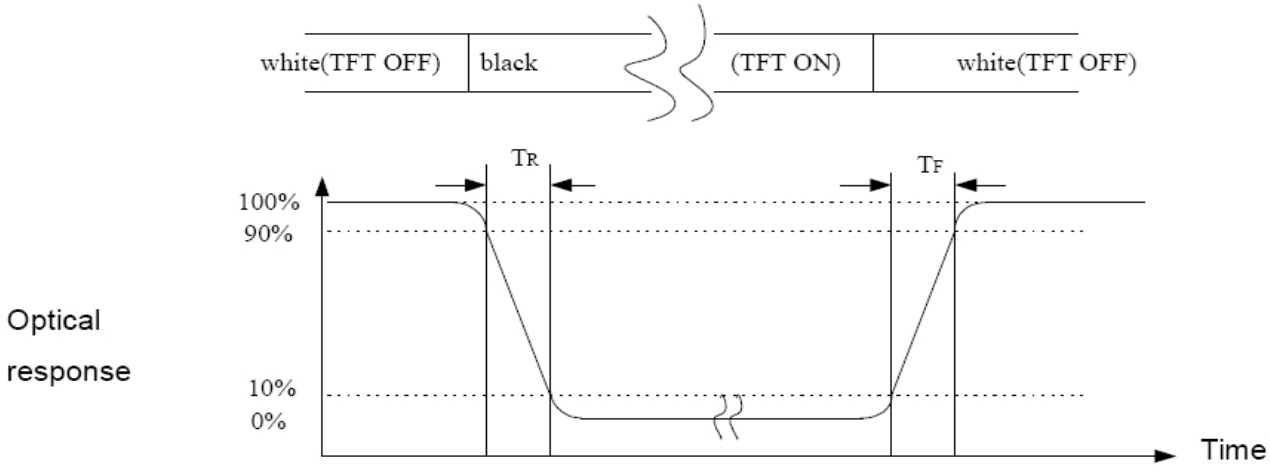


Note (2) Definition of Contrast Ratio (CR):

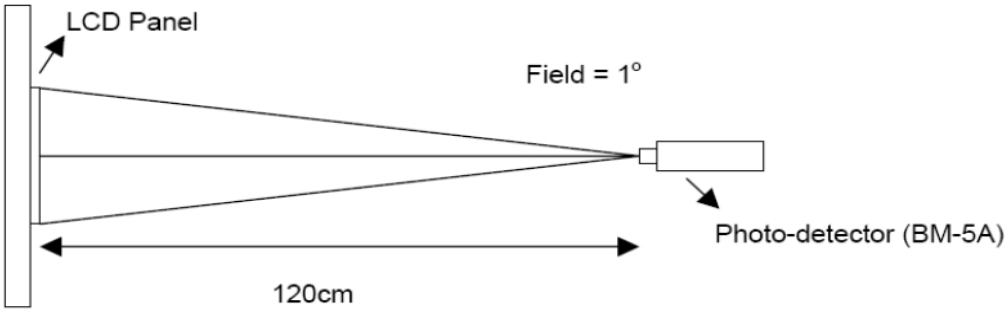
Measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

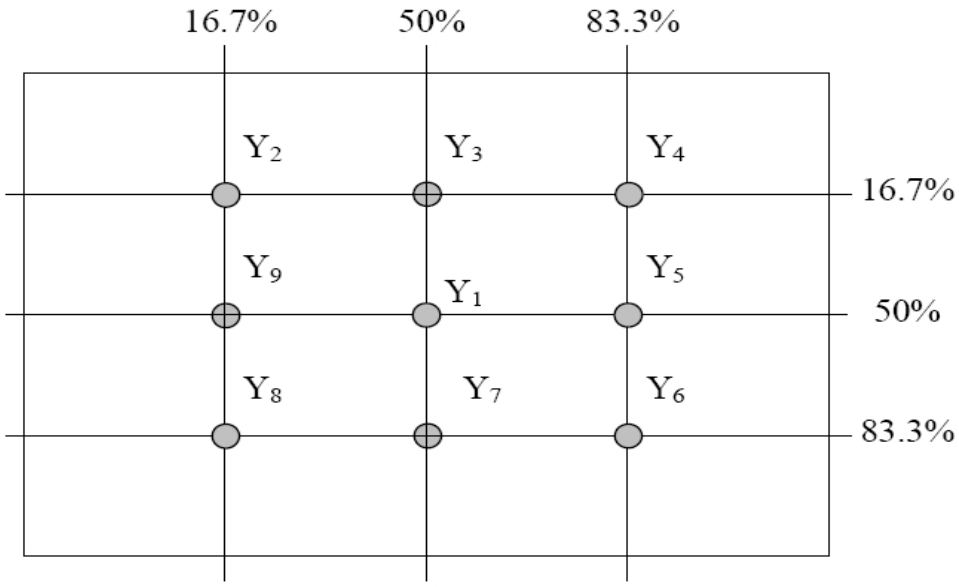
Note (3) Definition of Response Time: Sum of TR and TF



Note (4) Definition of optical measurement setup



Note (5) Definition of brightness uniformity



$$\text{Luminance uniformity} = \frac{\text{(Min Luminance of 9 points)}}{\text{(Max Luminance of 9 points)}} \times 100\%$$

4.0 INTERFACE PIN CONNECTION

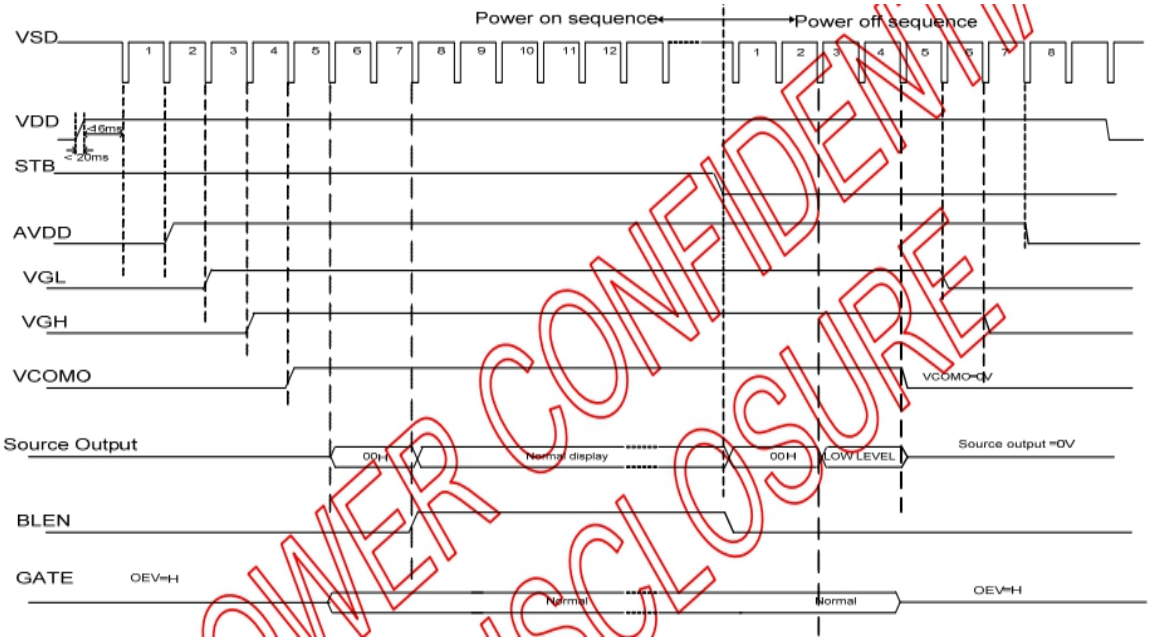
4.1 Signal of interface

Terminal No.	Symbol	I/O	Functions
1--2	VLED+	P	Power for LED backlight (Anode)
3	VGH	P	Gate ON Voltage
4	VGL	P	Gate OFF Voltage
5	UPDN	I	Up/down selection
6	SHLR	I	Left / right selection
7--8	VLED-	P	Power for LED backlight (Cathode)
9	AVDD	P	Power for Analog Circuit
10	GND	P	Ground
11	MIPI_D3+	I	Positive MIPI differential data inputs3+
12	MIPI_D3-	I	Negative MIPI differential data inputs3-
13	GND	P	Ground
14	MIPI_D2+	I	Positive MIPI differential data inputs2+
15	MIPI_D2-	I	Negative MIPI differential data inputs2-
16	GND	P	Ground
17	MIPI_CLK+	I	Positive MIPI differential clock inputs+
18	MIPI_CLK-	I	Negative MIPI differential clock inputs-
19	GND	P	Ground
20	MIPI_D1+	I	Positive MIPI differential data inputs1+
21	MIPI_D1-	I	Negative MIPI differential data inputs1-
22	GND	P	Ground
23	MIPI_D0+	I	Positive MIPI differential data inputs0+
24	MIPI_D0-	I	Negative MIPI differential data inputs0-
25	GND	P	Ground
26	STBYB	I	Standby mode, normally pull high STBYB="1", normally operation STBYB="0", timing control, source driver will turn off
27	RESET	P	Global reset pin.
28	DVDD	P	Power for Digital Circuit
29	DVDD	P	Power for Digital Circuit
30	VCOM	P	Common voltage

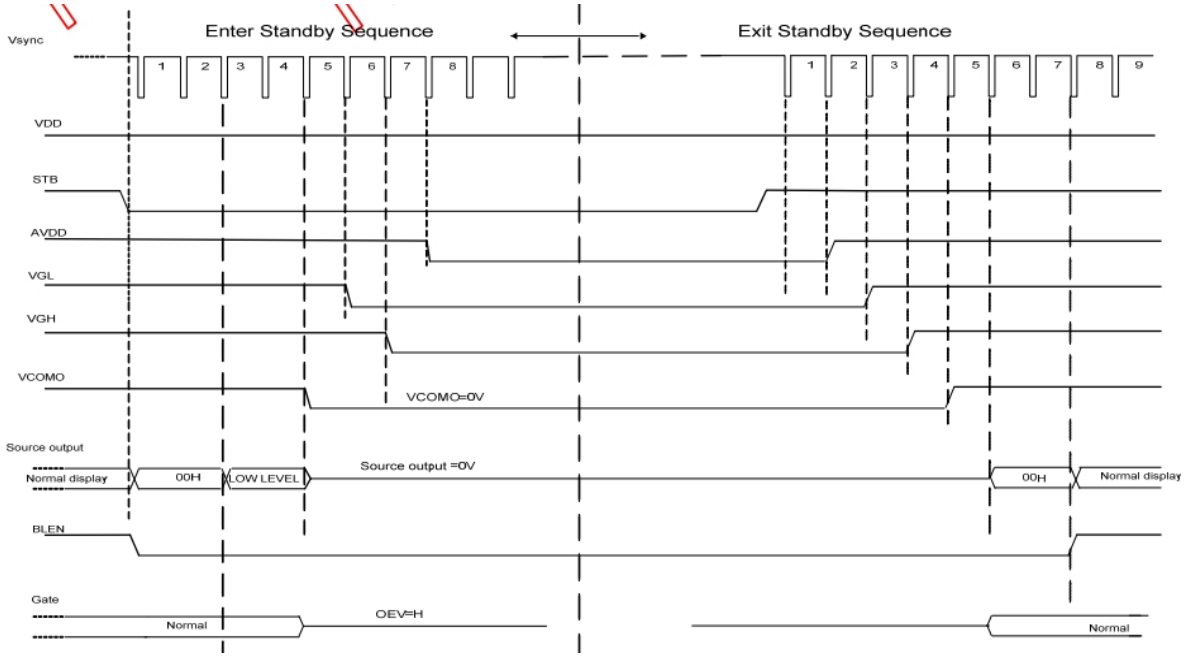
5.0 FUNCTION DESCRIPTION

5.1.1 Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications. Refer to "AC Characteristics" for more detail on timing. To prevent the device damage from latch up,the power on/off sequence shown below must be followed.



5.1.1 Enter and Exit Sleep Mode Sequence



Note: Low Level=3Fh, when NBW=" L" (Normally white)
Low Level=00h, when NBW=" H" (Normally Black)

6.0 ELECTRICAL CHARACTERISTICS

6.1 TFT LCD Module

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	1.71	1.8	1.89	V
	VGH	17	18	19	V
	VGL	-7.5	-6.5	-5.5	V
	AVDD	9.4	9.6	9.8	V
VCOM	VCOM	3.0	(3.2)	3.4	V

Note:

(1) VGH is TFT Gate operating voltage.

(2) VGL is TFT Gate operating voltage. The low voltage level of VGH signal must be fluctuates with same phase as Vcom.

6.2 Back-Light Unit

The backlight system is an edge-lighting type with 27 LED.

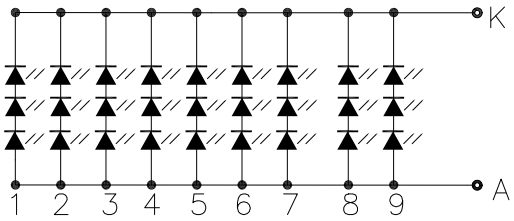
The characteristics of the LED are shown in the following tables.

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED current	IL	-	180	-	mA	(2)
LED Voltage	VL	-	9.0	-	V	
Operating LED life time	Hr	20000	-	-	Hour	(1)(2)

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=180mA. The LED lifetime could be decreased if operating IL is larger than 180mA. The constant current driving method is suggested.

LED CIRCUIT DIAGRAM： 3 x 9 = 27 LED



6.3 DC Characteristics

(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V)

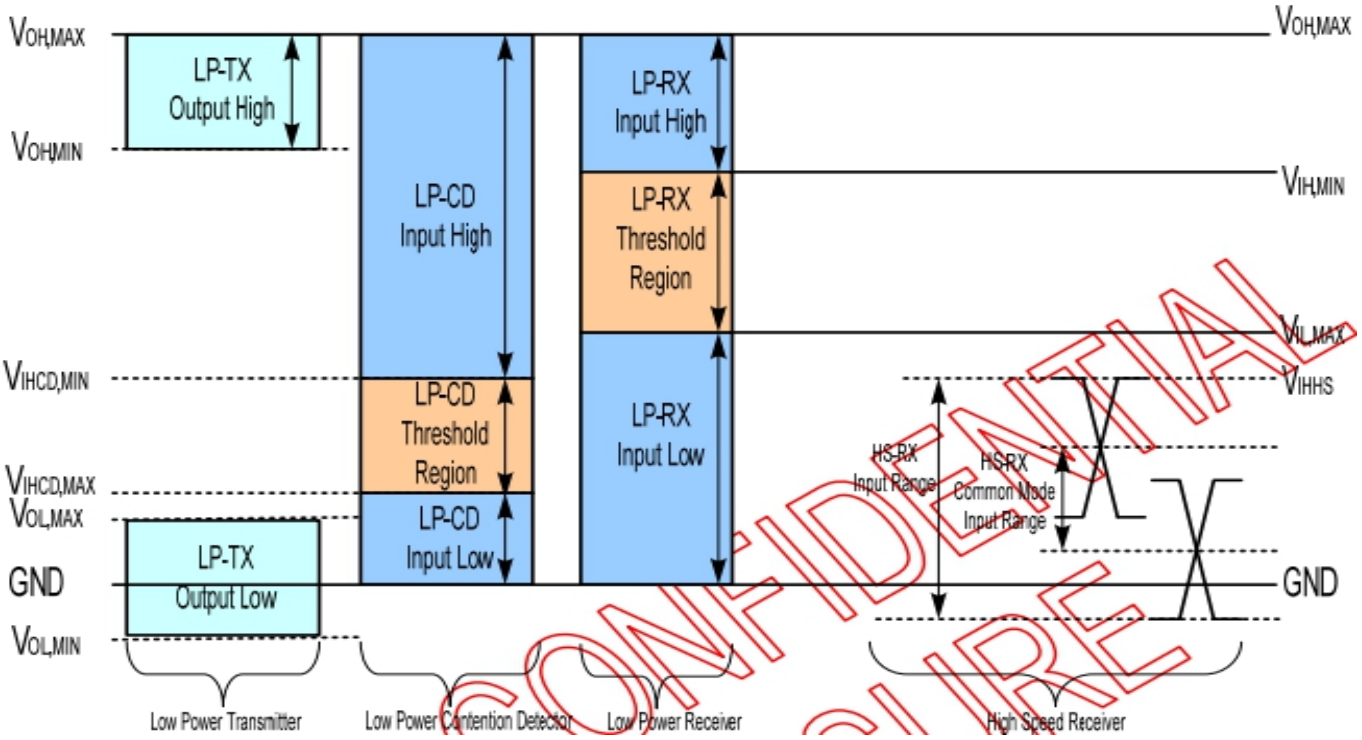
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level input voltage	Vil	For the digital circuit	0	-	0.3×VD	V
High level input voltage	Vih	For the digital circuit	0.7×VDD	-	VDD	V
Input leakage current	Ii	For the digital circuit	-	-	±1	μA
High level output voltage	Voh	Ioh= -400 μA	VDD- 0.4	-	-	V
Low level output voltage	Vol	Iol= +400 μA	-	-	GND+0.	V
Pull low/high resistor	Ri	For the digital input pin @	200K	250	300K	ohm
Digital Operation current	Idd	Fclk=51.2MHz,VDD=VDD_IF=1.8V	-	TB	-	mA
Digital Stand-by current	Ist1	Clock and all functions are stopped	-	10	50	μA
Analog Operating Current	Idda	No load, Fclk=51.2MHz, @AVDD=13.5V,V1=13.4V, V14=0.1V	-	10	12	mA

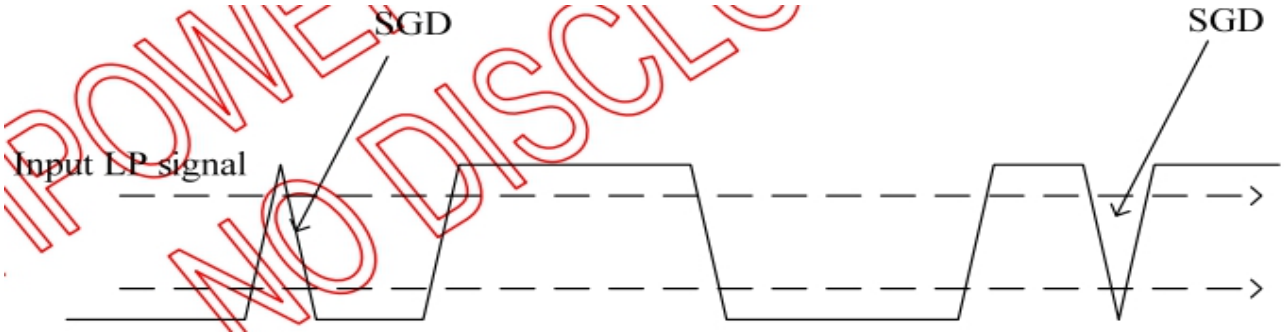
Analog Stand-by current	Ist2	No load, clock and all functions are stopped	-	10	50	μA
Input level of V1 ~ V7	Vref1	Gamma correction voltage input	0.4*AVDD	-	AVDD-	V
Input level of V8 ~ V14	Vref2	Gamma correction voltage input	0.1	-	0.6*AVD	V
Output Voltage deviation	Vod1	Vo = AGND+0.1V ~AGND+0.5V and Vo = AVDD-0.5V ~ AVDD-0.1V	-	±20	±35	mV
Output Voltage deviation	Vod2	Vo = AGND+0.5V ~ AVDD-0.5V	-	±15	±20	mV
Output Voltage Offset between Chips	Voc	Vo = AGND+0.5V ~ AVDD-0.5V	-	-	±20	mV
Dynamic Range of Output	Vdr	SO1 ~ 1536	0.1	-	AVDD-0.1	V
Sinking Current of Outputs	IOLy	SO1 ~ 1536; Vo=0.1V v.s 1.0V , AVDD=13.5V	80	-	-	uA
Driving Current of Outputs	IOHy	SO1 ~ 1536; Vo=13.4V v.s12.5V , AVDD=13.5V	80	-	-	uA
Resistance of Gamma Table	Rg	Rn: Internal gamma resistor	0.7*Rn	1.0*Rn	1.3*Rn	ohm

(VDD=VDD_IF=1.8V,AVDD=8 to 13.5V,GND=AGND=GND_IF=0V,TA=-20℃ to 85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage(DSI-CLKP/N,DSI-DnP/N)	VILHS	-40	—	—	mV
Single-ended input high voltage (DSI-CLKP/N,DSI-DnP/N)	VIHHS	—	—	460	mV
Input Common-mode voltage (DSI-CLKP/N,DSI-DnP/N)	VCDRXDC	70	—	330	mV
Differential input impedance	ZID		100		ohm
HS transmit differential voltage(VOD=VDP-VDN)	|VOD|	140	200	250	mV
Low-level differential input voltage threshold	VTHLCLK VTHLDATA	-70	—	—	mV
High-level differential input voltage threshold	VTHHCLK VTHHDATA	—	—	—	mV
Single-ended threshold voltage for termination	VTERN_EN	—	—	450	mV
Termination capacitor	CTERM		—	14	pf
Input voltage common mode variation(<=450Mhz)	VCMRCLK VCMRDATAL	-50	—	50	mV
Input voltage common mode variation(>=450Mhz)	VCMRCLKM VCMRDATAM	—	—	100	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	VI	-50	—	1350	mV
Ground shift	VGNDSH	-50	—	50	mV
Logic 0 input threshold	VIL	0	—	550	mV
Logic 1 input threshold	VIH	880	—	1350	mV
Logic 0 input voltage LPRX(CLK,ULP mode)	VILLPRXULP	0	—	300	mV
Input hysteresis	VHYST	25	—	—	mV
Output low level	VOL	-50	—	50	mV
Output high level	VOH	1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	ZOLP	90	100	110	ohm

Logic 0 contention threshold	VILCD,MAX	—	—	200	mV
Logic 1 contention threshold	VIHCD,MIN	450	—	1350	mV
Logic high level input current	IIH	—	—	10	uA
Logic low level input current	IIL	-10	—	—	uA
Input pulse rejection (DSI-CLKP/N,DSI-DnP/N)	SGD	—	—	300	Vps





6.4 AC Characteristics

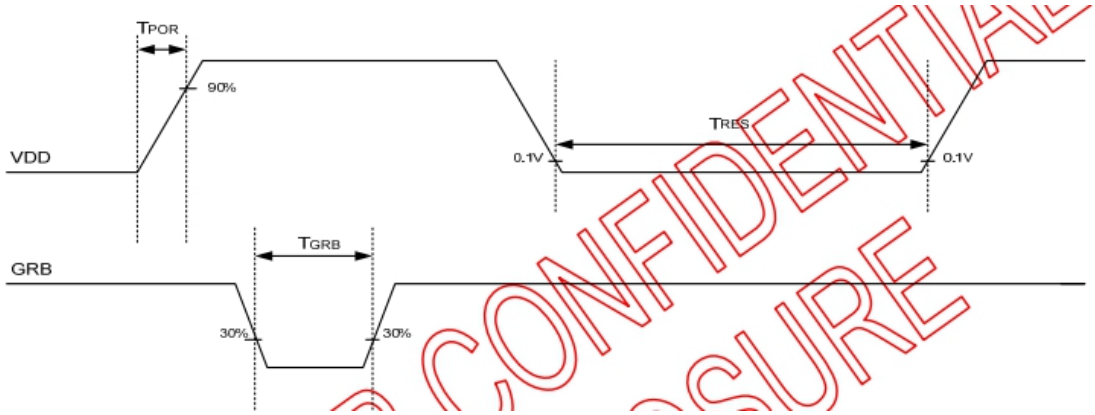
6.4.1 Basic AC Characteristic

(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V,TA=-20 to +85℃)

VDD/GRB AC characteristic

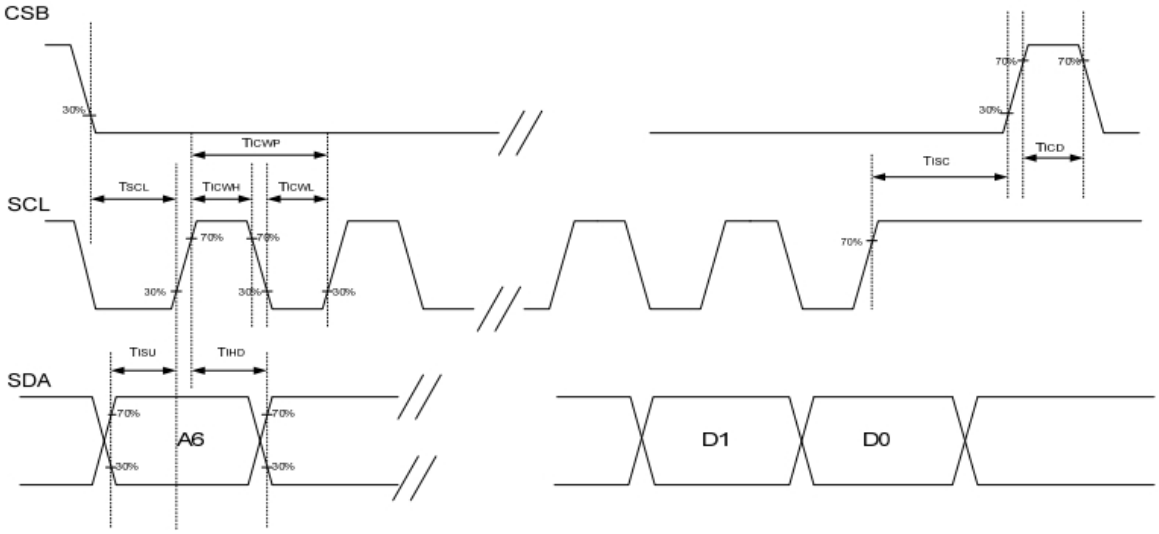
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VDD power slew rate	TPOR	—	—	-20	ms	From 0 to 90% VDD
GRB active pulse width	TGRB	1	—	—	ms	VDD=VDD_IF=1.8V

VDD resettle time	TRES	1	—	—	s	



3-wire interface AC characteristic:

Parameter	Symbol	Min.	Typ.	Max.	Unit
CSB falling to SCL rising	TSCL	200	-	-	ns
SCL pulse high period	TICWH	100	-	-	ns
SCL pulse low period	TICWL	100	-	-	ns
SCL pulse width	TICWP	250	-	-	ns
SDA data input setup time	TISU	100	-	-	ns
SDA data input hold time	TIHD	100	-	-	ns
SCL to CSB rising time	TISC	250	-	-	ns
CSB rising to failing time	TICD	1	-	-	us

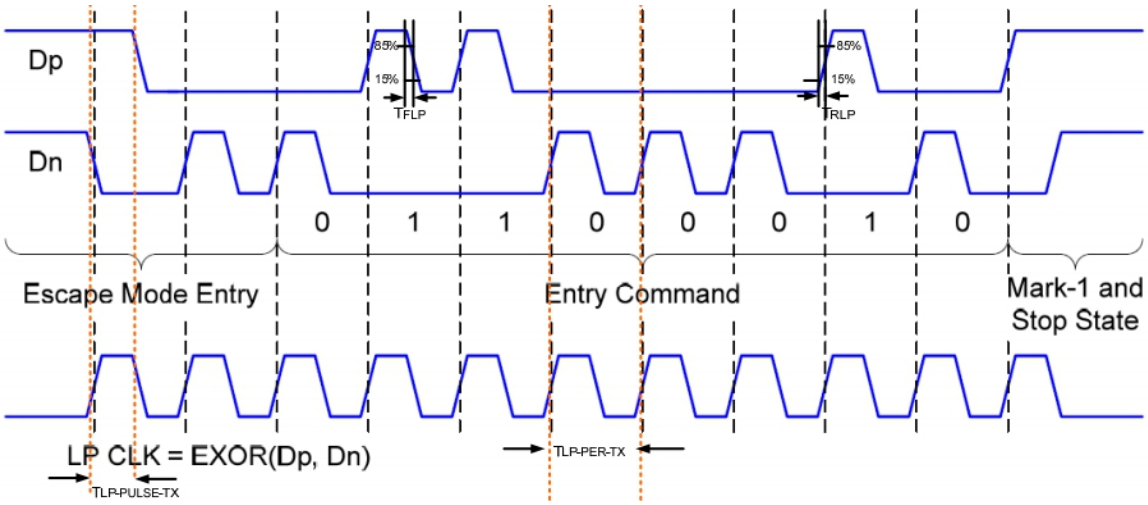


6.4.2 MIPI AC Characteristic

- **LP Transmitter AC Specification**

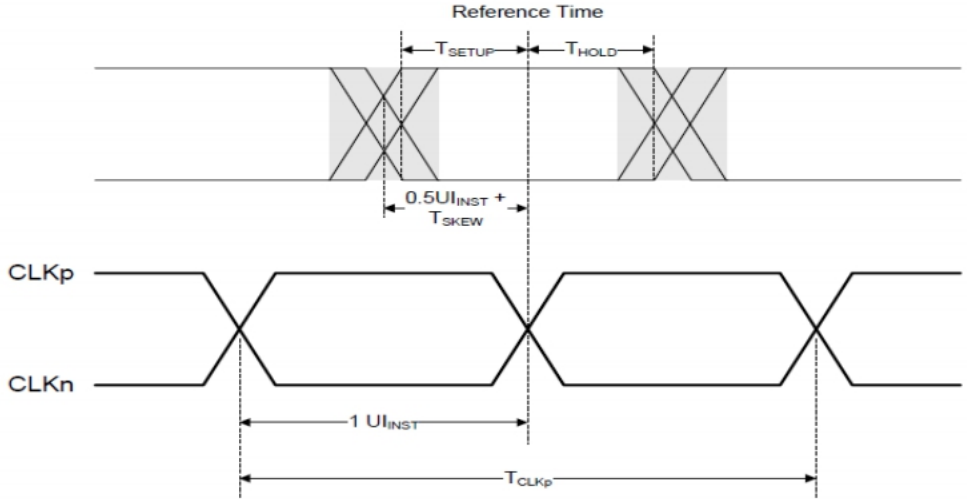
Parameter		Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time		TRLP /TFLP	-	-	25	ns	-
30%~85% rising time and falling time		TREOT	-	-	35	ns	-
Pulse width of LP exclusive-OR	First LP EXOR clock pulse after STOP state or Last pulse before stop state	TLP-PULSE-TX	40	-	-	ns	-

	All other pulses		20	-	-	ns	-
Period of the LP EXOR clock		$T_{LP-PER-TX}$	90	-	-	mV/ns	-
Slew Rate @CLOAD =0pF		$\delta V/\delta t_{SR}$	30	-	500	mV/ns	-
Slew Rate @CLOAD =5pF			30	-	200	mV/ns	-
Slew Rate @CLOAD =20pF			30	-	150	mV/ns	-
Slew Rate @CLOAD =70pF			30	-	100	mV/ns	-
Load Capacitance		T_{RLP}	-	-	70	pF	-



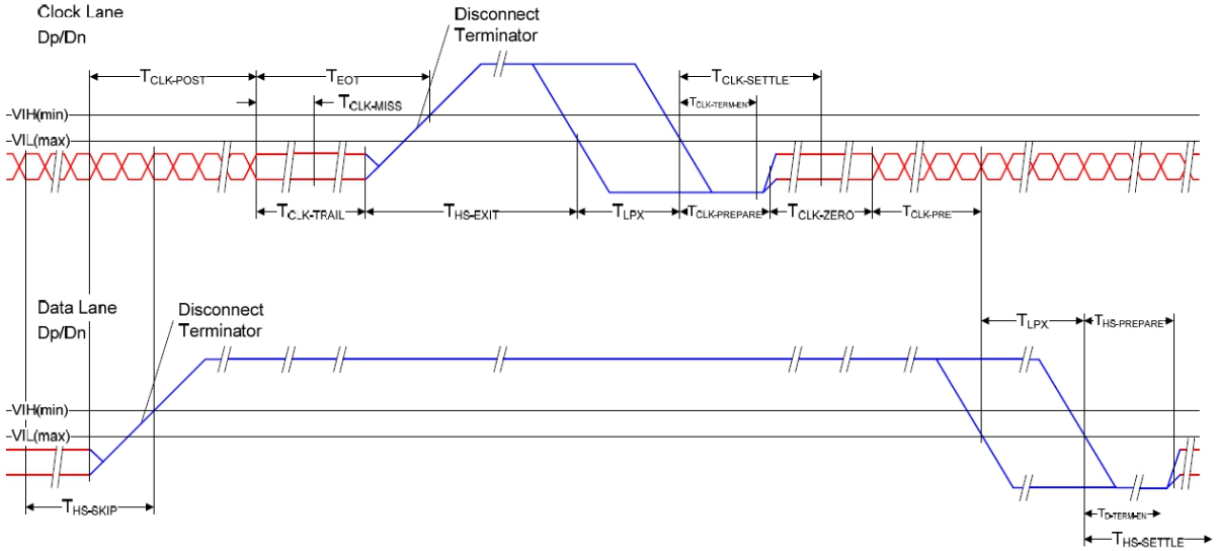
- **High Speed Transmission**

Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UI_{INST}	2	-	12.5	ns
Data to Clock Skew(measured at transmitter)	$T_{SKEW(TX)}$	-0.15	-	0.15	UI_{INST}
Data to Clock Setup time(measured at receiver)	$T_{SETUP(RX)}$	0.15	-	-	UI_{INST}
Data to Clock Hold time(measured at receiver)	$T_{HOLD(RX)}$	0.15	-	-	UI_{INST}
20%~80% rise time and fall time	TR, TF	150	-	-	ps
		-	-	0.3	UI_{INST}



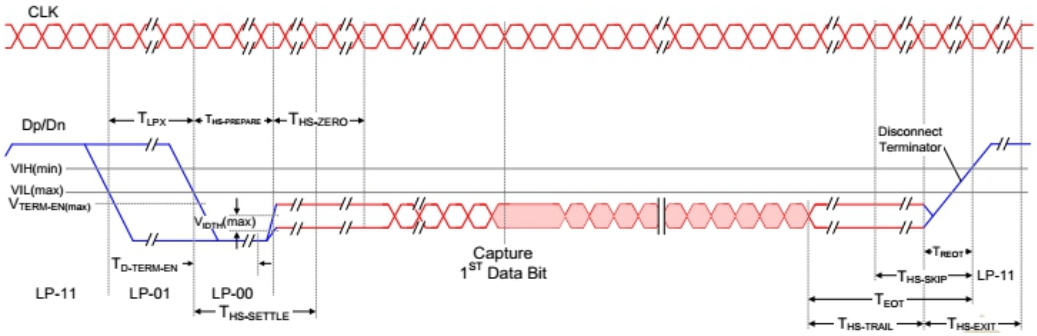
- **High Speed Clock Transmission**

Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300		-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$	$T_{HS-TERM-EN}$	-		38	ns
Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns



- **Bursts Mode Data Transmission**

Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
Time from start of $t_{HS-TRAIL}$ or $t_{CLK-TRAIL}$ period to start of LP-11 state	T_{EOT}	-	-	105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$	$T_{HS-TERM-EN}$	-	-	35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI	-	-	ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40	-	55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
Length of any Low-Power state period	T_{LPX}	50	-	-	ns
Sync sequence period	$T_{HS-SYNC}$	-	8UI	-	ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI	-	-	ns



6.4.3 Input Timing for MIPI

HV mode
Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		H
VSYNC period time	tv	624	635	800	H
VSYNC pulse width	tvpw	1	—	20	H
VSYNC back porch	tvb	23	23	23	H
VSYNC front porch	tvfp	1	12	177	H

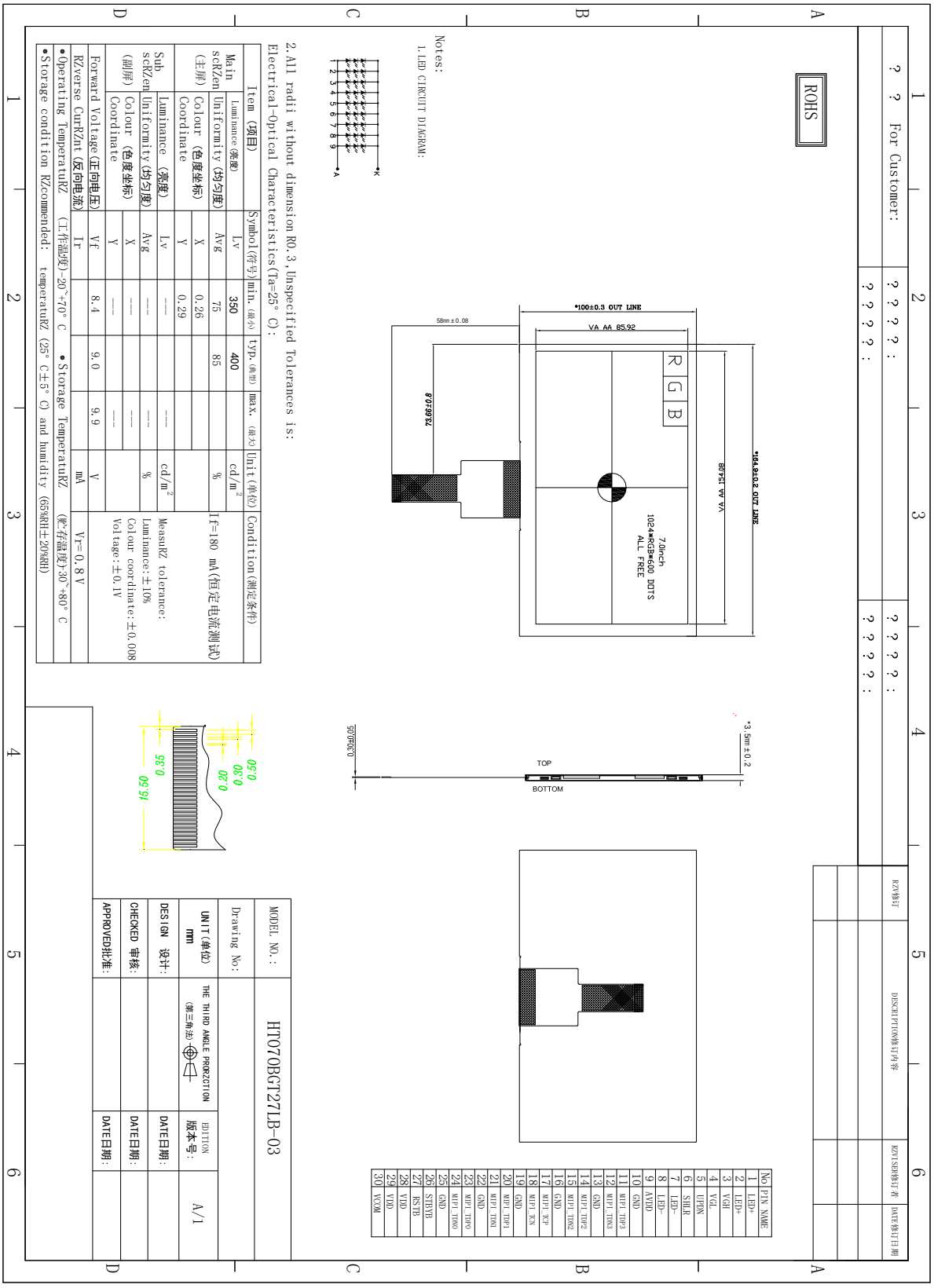
HV mode
Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		1024		DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	
			44.9	51.2	70.3	Mhz
1 Horizontal Line		th	1200	1344	1464	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			—		
	Max.			140		
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

7.0 Reliability test items

Test Item	Test Conditions	Notes
High temperature Operation	Ta= +70℃, 120hrs	
Low temperature Operation	Ta= -20℃, 120hrs	
High Temperature Storage	Ta= +80℃, 120hrs	
Low Temperature Storage	Ta= -30℃, 120hrs	
Humidity Test	60℃ ,Humidity 90% ,96hrs	
Thermal Shock Test	-20℃,30min ~ +60℃,30min (30 cycle)	
Vibration Test(Packing)	Sine Wave 1.04G, 5~500Hz, XYZ 30min/each direction	

8.0 OUTLINE DIMENSION



No.	PIN NAME
1	LED+
2	LED+
3	VGH
4	VGL
5	UPDN
6	SHLR
7	LED-
8	LED-
9	AVDD
10	GND
11	MIPI_TDP3
12	MIPI_TDN3
13	GND
14	MIPI_TDP2
15	MIPI_TDN2
16	GND
17	MIPI_TCP
18	MIPI_TCN
19	GND
20	MIPI_TDP1
21	MIPI_TDN1
22	GND
23	MIPI_TDP0
24	MIPI_TDN0
25	GND
26	STBYB
27	RESTB
28	VDD
29	VDD
30	VCOM

Item (项目)		Symbol(符号)	min.(最小)	typ.(典型)	max.(最大)	Unit(单位)	Condition(测定条件)
Main scRZen (主屏)	Luminance (亮度)	Lv	350	400		cd/m²	If=180 mA(恒定电流测试)
	Uniformity (均匀度)	Avg	75	85		%	
	Colour (色度坐标)	X	0.26				
	Coordinate	Y	0.29				
Sub scRZen (副屏)	Luminance (亮度)	Lv	——		——	cd/m²	MeasuRZ tolerance: Luminance:±10% Colour coordinate:±0.008 Voltage:±0.1V
	Uniformity (均匀度)	Avg	——		——	%	
	Colour (色度坐标)	X	——		——		
	Coordinate	Y	——		——		
Forward Voltage(正向电压)		Vf	8.4	9.0	9.9	V	Vr=0.8 V
RZverse CurRZnt (反向电流)		Ir	——		——	mA	(贮存温度)-30°~+80° C

• Operating TemperatuRZ (工作温度)-20°~+70° C • Storage TemperatuRZ
• Storage condition RZcommended: temperatuRZ (25° C±5° C) and humidity (65%RH±20%RH)

9.0 General precaution

9.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life threatening or otherwise catastrophic.

9.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. RFH does not warrant the module, if customers disassemble or modify the module.

9.3 Breakage of LCD Panel

9.3.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

9.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

9.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

9.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

9.4 Electric Shock

9.4.1. Disconnect power supply before handling LCD module.

9.4.2. Do not pull or fold the LED cable.

9.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

9.5 Absolute Maximum Ratings and Power Protection Circuit

9.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

8.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

8.5.3. It's recommended to employ protection circuit for power supply.

9.6 Operation

9.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

9.6.2 Use finger stalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

9.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

9.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

9.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

9.7 Mechanism

Please mount LCD module by using mouting holes arranged in four corners tightly.

9.8 Static Electricity

9.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

9.8.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

9.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

9.10 Disposal

When disposing LCD module, obey the local environmental regulations.