LCD MODULE

SPECIFICATION

Model:	UE021WV-RB40-L002B
Version:	V1.2
Date:	20211229

Customer Confirmation

Approved by	Notes

Please return one of the copies of the specification with your signature to us within two weeks after you receive this document. If it is not returned, we will assume that you agree to the entire contents of this specification document.

VIEWE Confirmation

Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision	Date	Contents of Revision Change	Remark
V1.0	20210930	Preliminary release	All
V1.1	20211208	Fix CAD	
V1.2	20211229	Update CAD	

TABLE of CONTENTS

1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB Vertical Stripe
2) Interface Mode：3 Wire SPI + RGB 24bits
3) Driver IC：GC9503CV
4) Operation Temperature：-20~70℃
5) Storage Temperature：-30~80℃
6) Backlight Type：White LED
7) Display mode： Normally black,
8) Pixel Density：323 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item	Specification	Unit	Remark
Pixel Driving element	IPS TFT	-	-
Screen Size	2.1	Inch	Diagonal
Resolution	480(W)*3(RGB)*480(H)	Dots	-
Interface	3 Wire SPI + RGB 24bits	-	-
Module Power Consumption	0.405	Watt	Typ.
Active Area	53.28(W)*53.28(H)	mm	-
Pixel pitch (W*H)	111(W)*111(H)	um	-
Module Size (W*H*D)	56.18(W)*59.71(H)*2.22(D)	mm	-
Luminance	450	cd/m^2	Typ.
Viewing Direction	All	O'clock	-
Display Color	16.7M	Colors	24 Bits

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remark
Power supply1 voltage	VDD	-0.3	4.6	V	Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1
Operating temperature	T_{op}	-20	70	°C	Note1,2
Storage temperature	T_{st}	-30	80	°C	Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

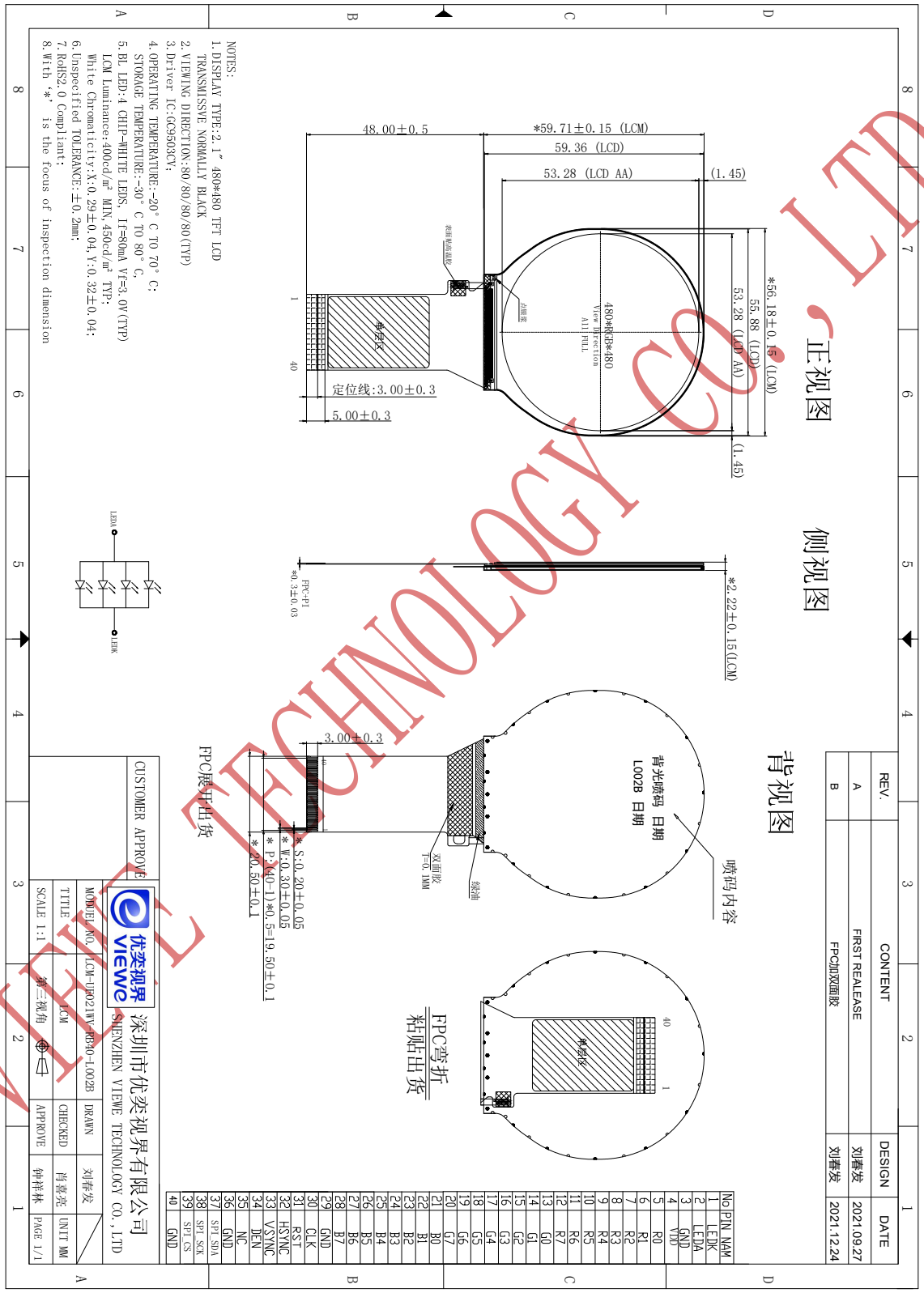
(Ta=+25°C,DGND=AVSS=0V)

Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.
Temp. ＞60℃ , Absolute humidity shall be less than 90% RH.

3. MECHANICAL DRAWING



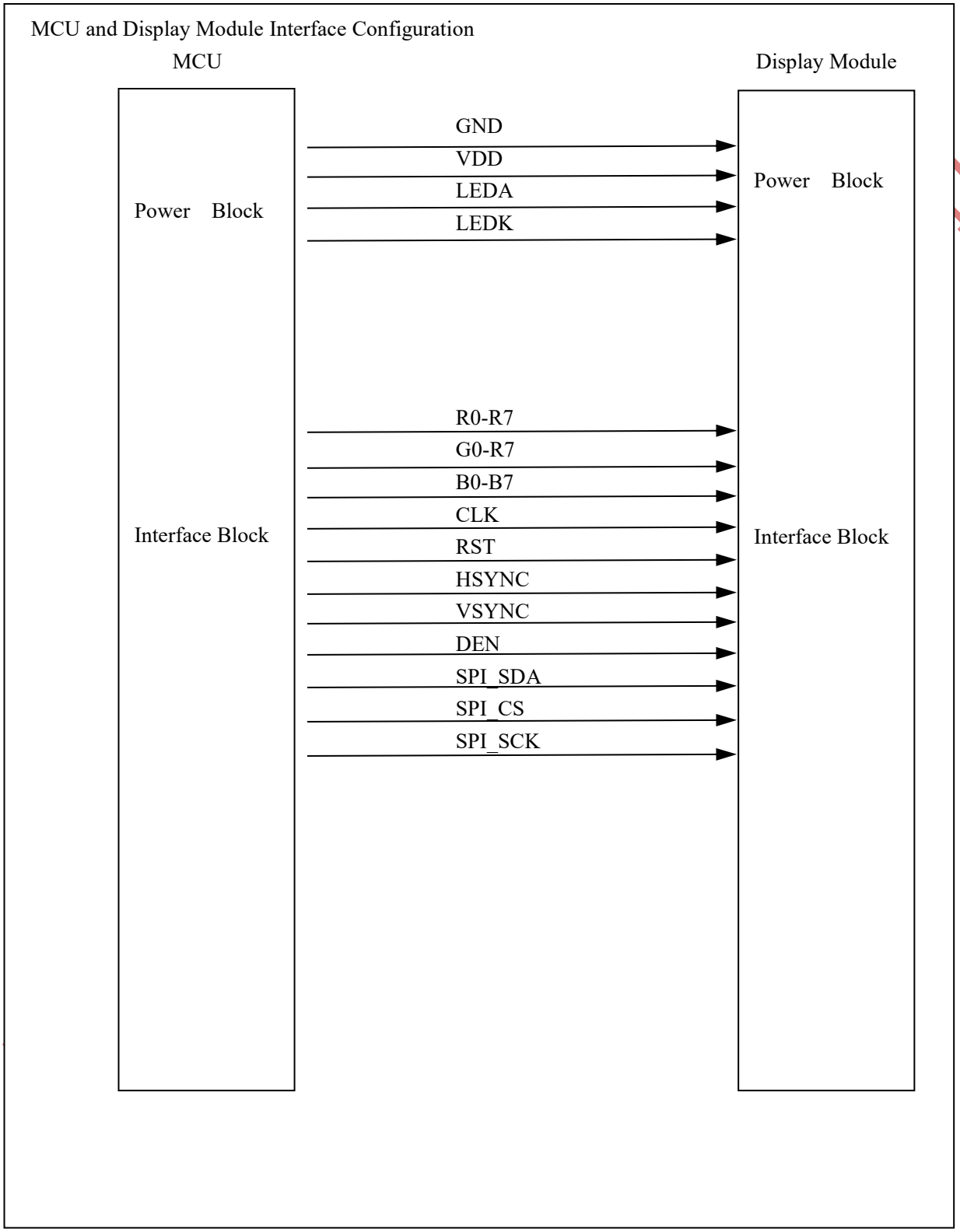
4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

Pin No.	Symbol	I/O	Description
1	LEDK	P	Power supply for backlight cathode
2	LEDA	P	Power supply for backlight anode
3	GND	P	Power Ground
4	VDD	P	Power supply for analog circuits
5-12	R0-R7	I	Red data input.(R0-LSB;R7-MSB)
13-20	G0-G7	I	Green data input.(G0-LSB;G7-MSB)
21-28	B0-B7	I	Blue data input.(B0-LSB;B7-MSB)
29	GND	P	Power Ground
30	CLK	I	Dot clock signal for RGB interface operation
31	RST	I	The signal will reset the LCM, Signal is active low.
32	HSYNC	I	Horizontal sync signal, Negative polarity
33	VSYNC	I	Horizontal sync signal, Negative polarity
34	DEN	I	Data input enable. Display access is enabled when DE is “H”
35	NC	-	No connected
36	GND	P	Power Ground
37	SPI_SDA	I/O	Data select pin for SPI interface
38	SPI_SCK	I	Clock select pin for SPI interface
39	SPI_CS	I	Chip select pin for SPI interface
40	GND	P	Power Ground

I：Input；O：Output；P：Power

4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply1 Voltage	VDD	2.5	3.3	3.3	V	
Power Supply1 Current	I_{VDD}	-	50	-	mA	Note1
Logic Input High Voltage	V_{IH}	0.7VDD	-	VDD	V	-
Logic Input Low Voltage	V_{IL}	0	-	0.3VDD	V	-
Panel Power Consumption	P_{VDD}	-	0.165	-	Watt	Note1
Module Power Consumption	P_{LCM}	-	0.405	-	Watt	Note1,2

(Ta=+25°C, DGND=AVSS=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=3.3V,60Hz Refresh.

Note2: P_{LCM}= P_{VDD}+ P_{BL}， About P_{BL} information, inference to 5.2 Back Light Driving Section.

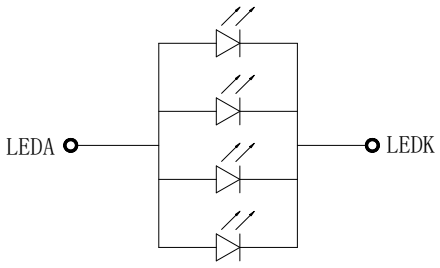
5.2 Back Light Driving Section

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward Voltage	V_F	-	3	-	V	Note1
Forward Current	I_F	-	80	-	mA	Note1
Backlight Power consumption	P_{BL}	-	0.24	-	Watt	Note1
LED life time	-	30000	-	-	Hrs	Note2
LED Quantity			4		PCS	

(Ta=+25°C, DGND=AVSS=0V)

Note1: The LED driving condition is defined for

Note2:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.

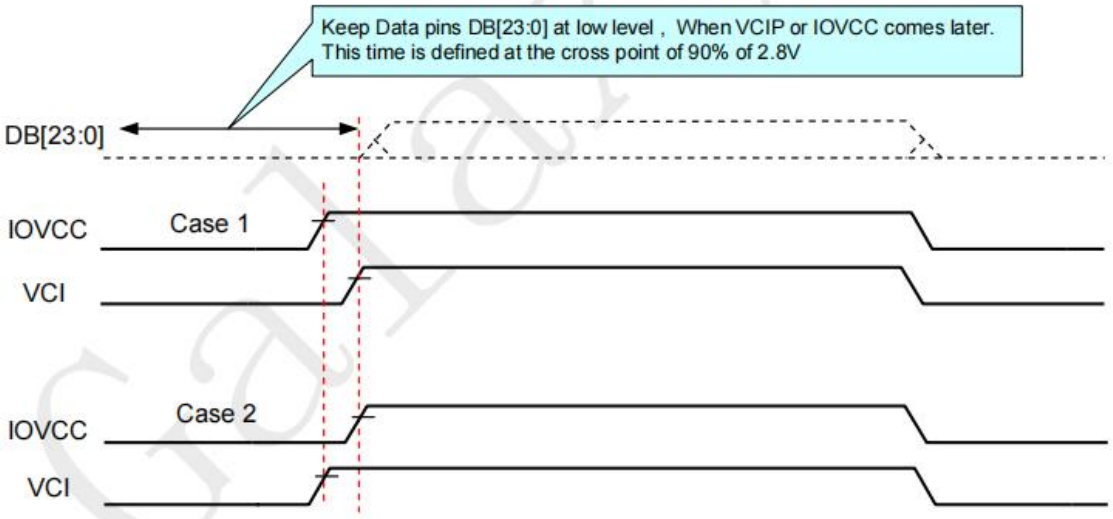


5.3 Power On/Off Sequence

IOVCC and VCI can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VCI and IOVCC can be powered down with minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

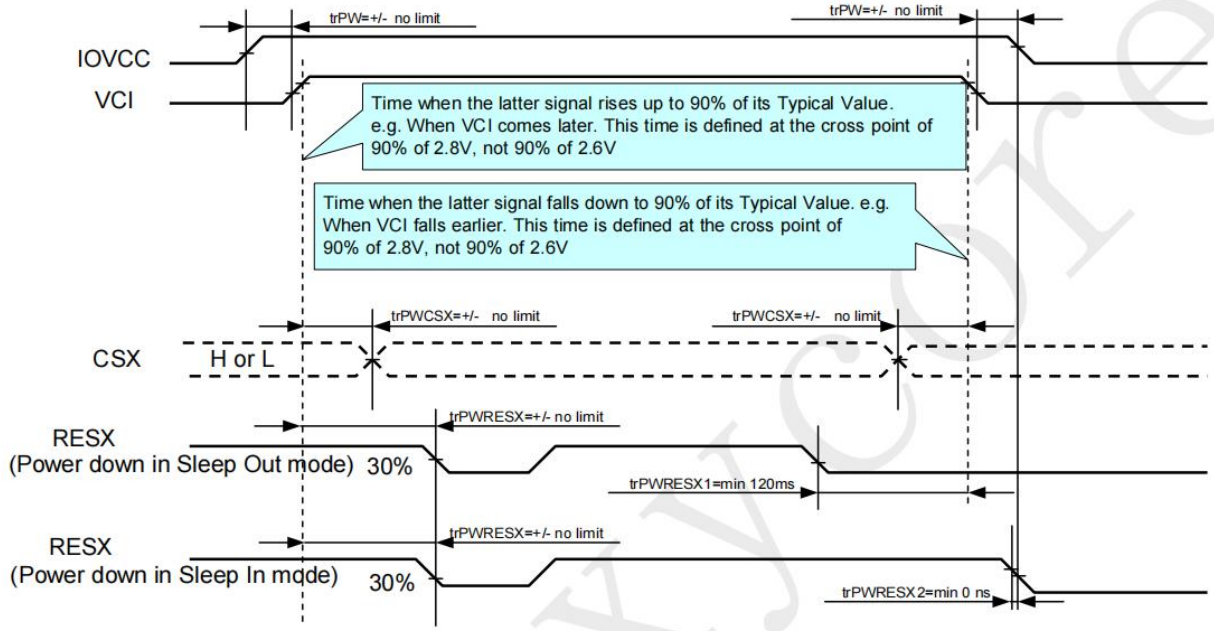
Note:

1. There will be no damage to GC9503V if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 7.1 and 7.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. Keep data pins DB[23:0] at low level, when VCIP or IOVCC comes later



5.3.1 RESX line is held High or Unstable by Host at Power ON

If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

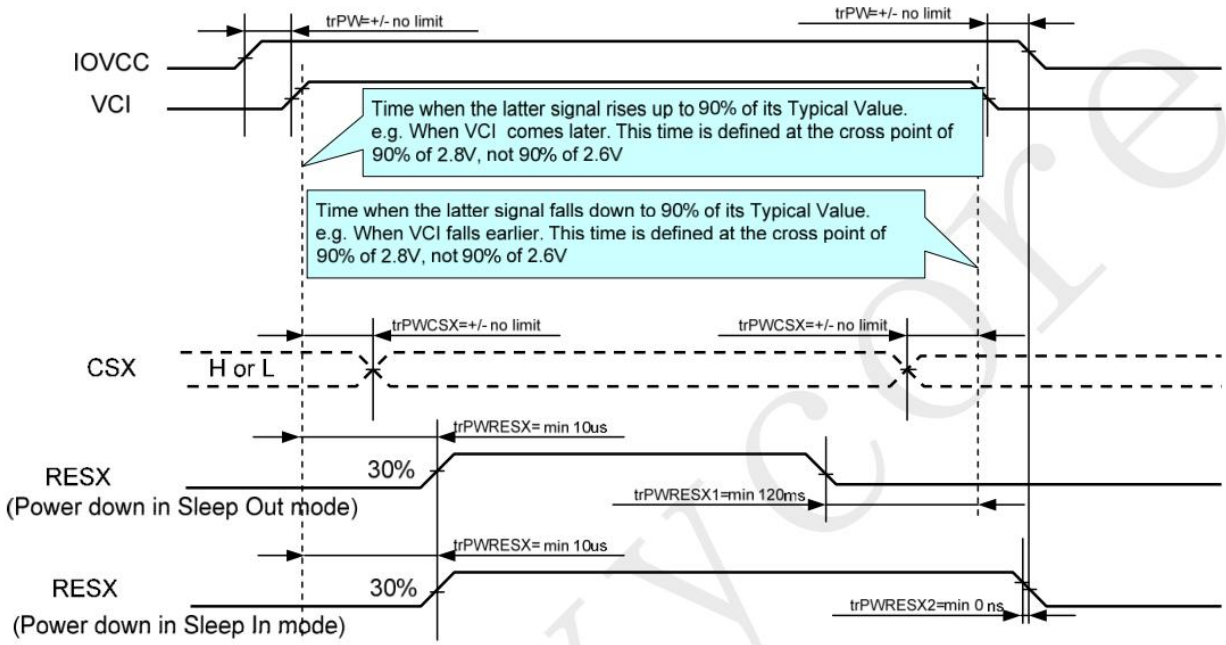


trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

5.3.2 RESX line is held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Figure 99 Case 2 – RESX line is held Low by Host at Power ON

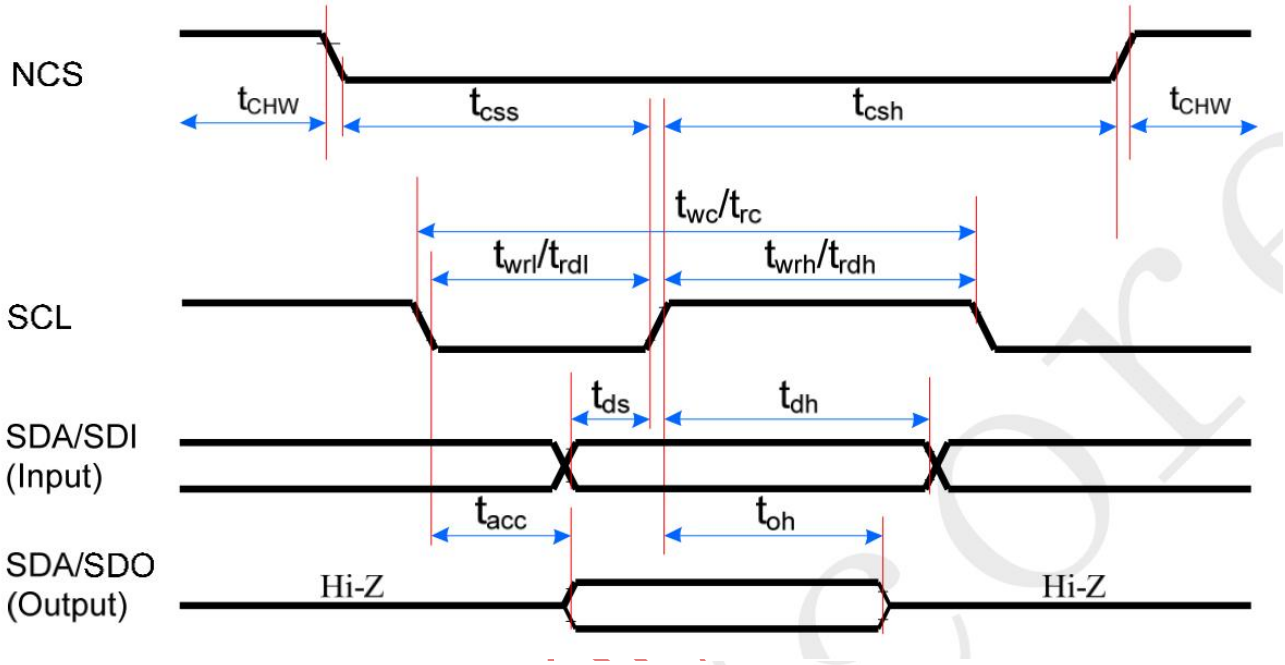
Note: 1. Unless otherwise specified, timings herein show cross point at 50% of signal power level.

5.3.3 Abnormal Power Off

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, GC9503V will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” powers it up

5.4 Timing Characteristics

5.4.1 Display Serial Interface Timing Characteristics (3-line SPI system)

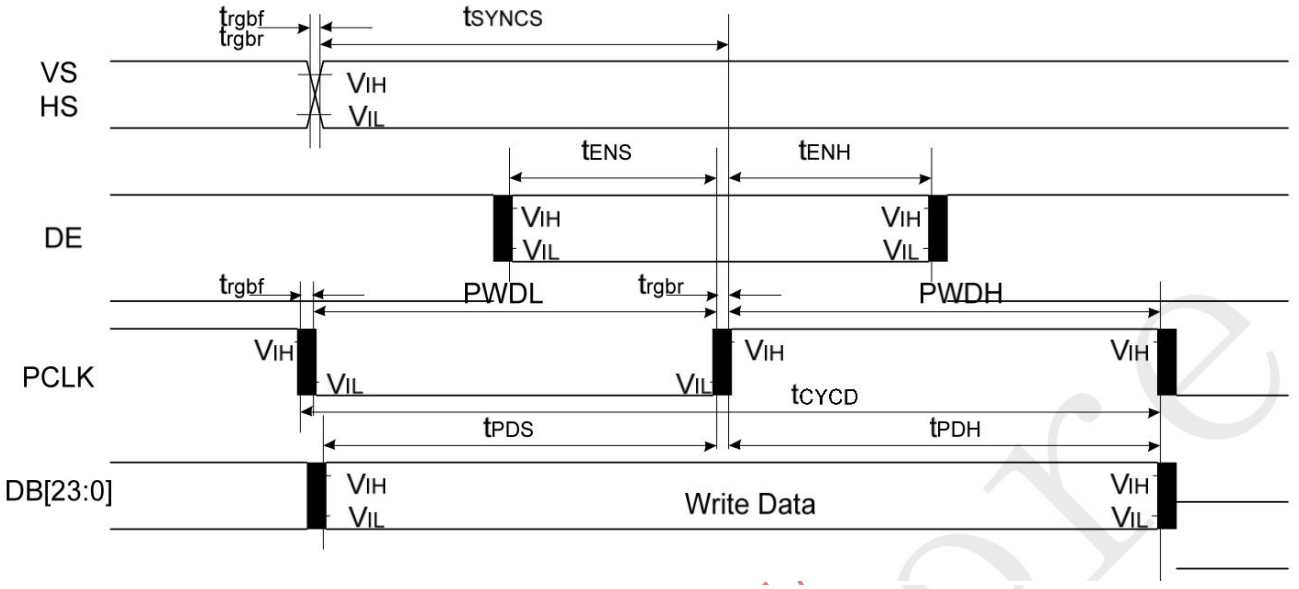


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS “H” pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL “H” pulse width (Write)	10	-	ns	
	twrl	SCL “L” pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	100	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA/SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	

Note:

1. Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, T=10+/-0.5ns.
2. Does not include signal rise and fall times.

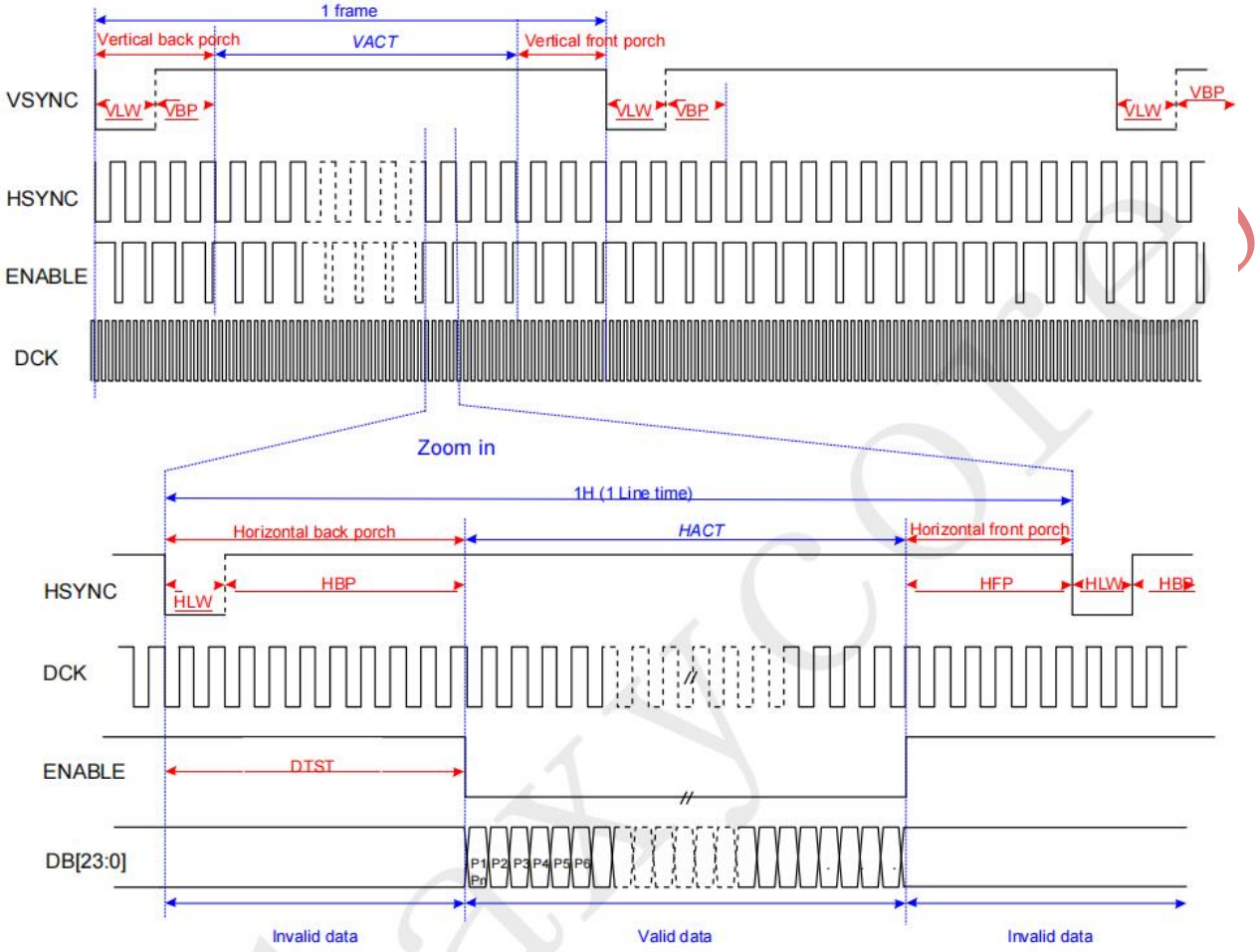
5.4.2 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	t_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VS/HS hold time	5	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	5	-	ns	
DB[23:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	t_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr} , t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, DGND=0V

5.5 Timing Diagram



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2···, pixel n.

Parameter	Symbol	Conditio	Min	Typ	Max	Units
Frame Rate	FR		54		6	fps
Horizontal Low Pulse width	HLW		1		-	DOTCL
Horizontal Back Porch	HBP		2		126	DOTCL
Horizontal Address	HACT			48		DOTCL
Horizontal Front Porch	HFP		2		-	DOTCL
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				864	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.		35.	MHz

Figure 12 DPI Interface Timing diagram[Note1,Note2]

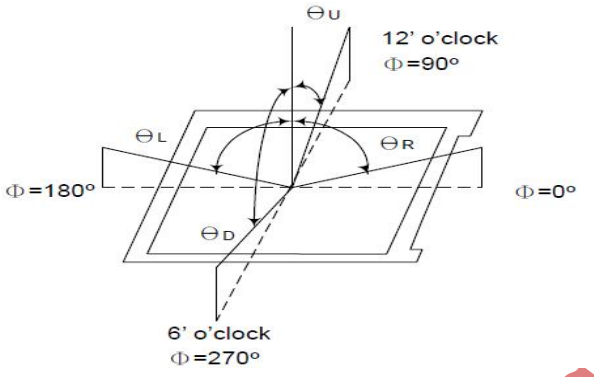
6. OPTICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast Ratio	C/R	θ = 0°	800	1000	-	-	Note(4)
NTSC Ratio	S	θ =0°	64	69	-	%	Note(7)
Luminance	L	θ =0°	400	450	-	cd/m2	Note(5)
Luminance uniformity	U_W	θ =0°	70	80	-	%	Note(3)
Response Time	T_R+ T_F	25 °C	-	30	35	ms	Note(2)
Color Coordination	W_X	θ = 0° (Center) Normal viewing angle B/L On	-0.04	0.29	+0.02	NTSC (x,y)	Note(6)
	W_Y			0.32			
	R_X			0.655			
	R_Y			0.327			
	G_X			0.284			
	G_y			0.594			
	B_X			0.138			
	B_Y			0.111			
Viewing Angle	θ_L	C/R>10	80	85	-	Degree	Note(1)
	θ_R		80	85	-		
	θ_U		80	85	-		
	θ_D		80	85	-		

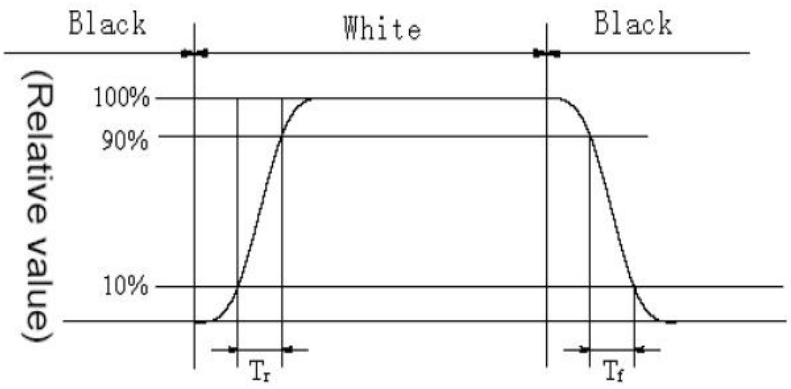
Test Conditions:

1. VDD=3.3V, I_F=20mA (Backlight current), the ambient temperature is+25°C.
2. The test systems refer to Note 8.

Note1: Definition of Viewing Angle: The viewing angle range that the CR>10

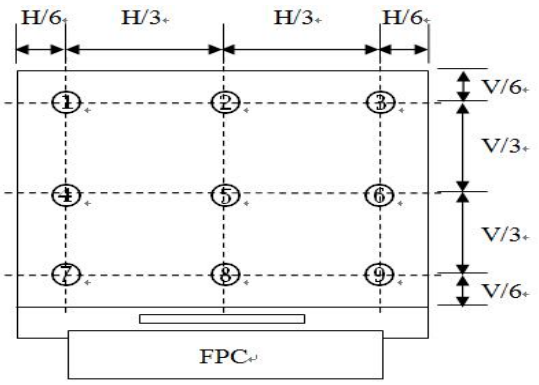


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \text{ x100\%}$$



Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

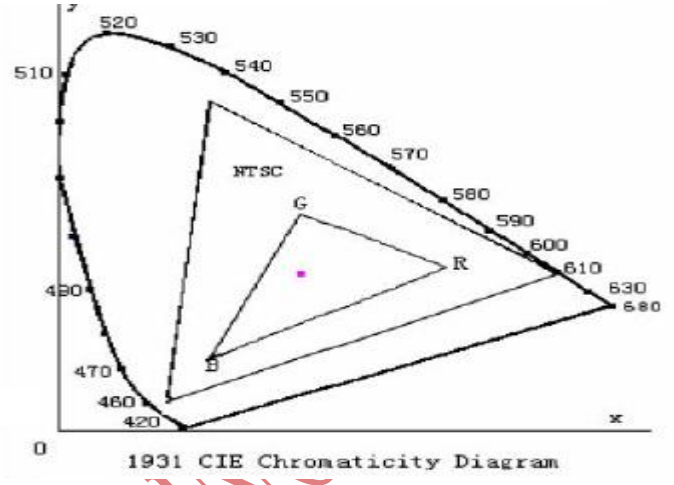
Note 5: Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.

Note 6: Definition of Color Chromaticity (CIE 1931)

Color coordinates of white & red, green, blue measured at center point of LCD.

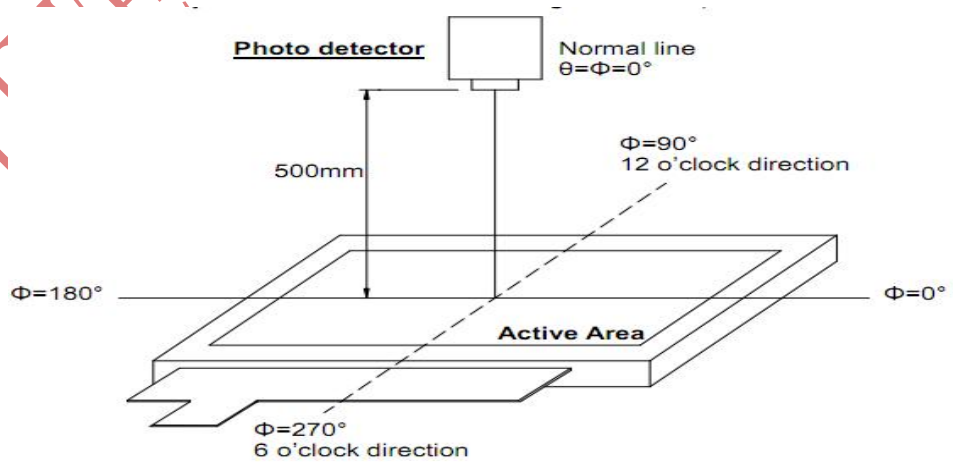
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



7. RELIABILITY

Item	Test Condition	Remark
High Temperature Storage	Ta =+80°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-30°C/30min Δ+80°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	60°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
ESD	C=150PF,R=330 Ohm Air: ±8kv,5times(Center) Contact: ±4kv,5times(Center)	Note4

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

8. PACKAGE DRAWING