LCD MODULE
SPECIFICATION

Model:	UE040WV-RH40-A044C
Version:	V1.2
Date:	20201220

Customer Confirmation

Approved by	Notes

Please return one of the copies of the specification with your signature to us within two weeks after you receive this document. If it is not returned, we will assume that you agree to the entire contents of this specification document.

VIEWE Confirmation

Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision	Date	Contents of Revision Change	Remark
V1.0	2020.03.11	Preliminary release	
V1.1	2020.07.09	Change the rounding Angle of the TP cover to 1.9mm	
V1.2	2020.11.06	Modify brightness	
V1.3	2020.12.20	Fix some bugs	

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1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB Vertical Stripe
2) Interface Mode：3SPI-RGB 18bits
3) Driver IC： GC9503V TP IC: FT6336U
4) Operation Temperature：-20~70℃
5) Storage Temperature：-30~80℃
6) Backlight Type：White LED
7) Display mode： Normally Black,
8) Pixel Density：169 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item	Specification	Unit	Remark
Pixel Driving element	A-Si TFT	-	
Screen Size	4.0	Inch	Diagonal
Resolution	480(W)*3(RGB)*480(H)	Dots	
Interface	3SPI_RGB 18bits	-	40PIN
Module Power Consumption	0.883	Watt	Typ.
VActive VArea	72.46(W)*71.78(H)	mm	
CTP_Pixel pitch (W*H)	0.1497(W)*0.1462(H)	mm	
Module Size (W*H*D)	84(W)*84(H)*3.22(D)	mm	
Luminance	350	cd/m^2	Typ.
Viewing Direction	All	O'clock	-
Display Color	262K	Colors	18bits

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remark
Power supply voltage	VDD	-0.3	4.6	V	
Power supply voltage	TP_VCI	-0.3	4.6	V	
LED forward current	I_F	-0.001	30	mA	For each led,Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1
Operating temperature	T_{op}	-20	70	°C	Note1,2
Storage temperature	T_{st}	-30	80	°C	Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

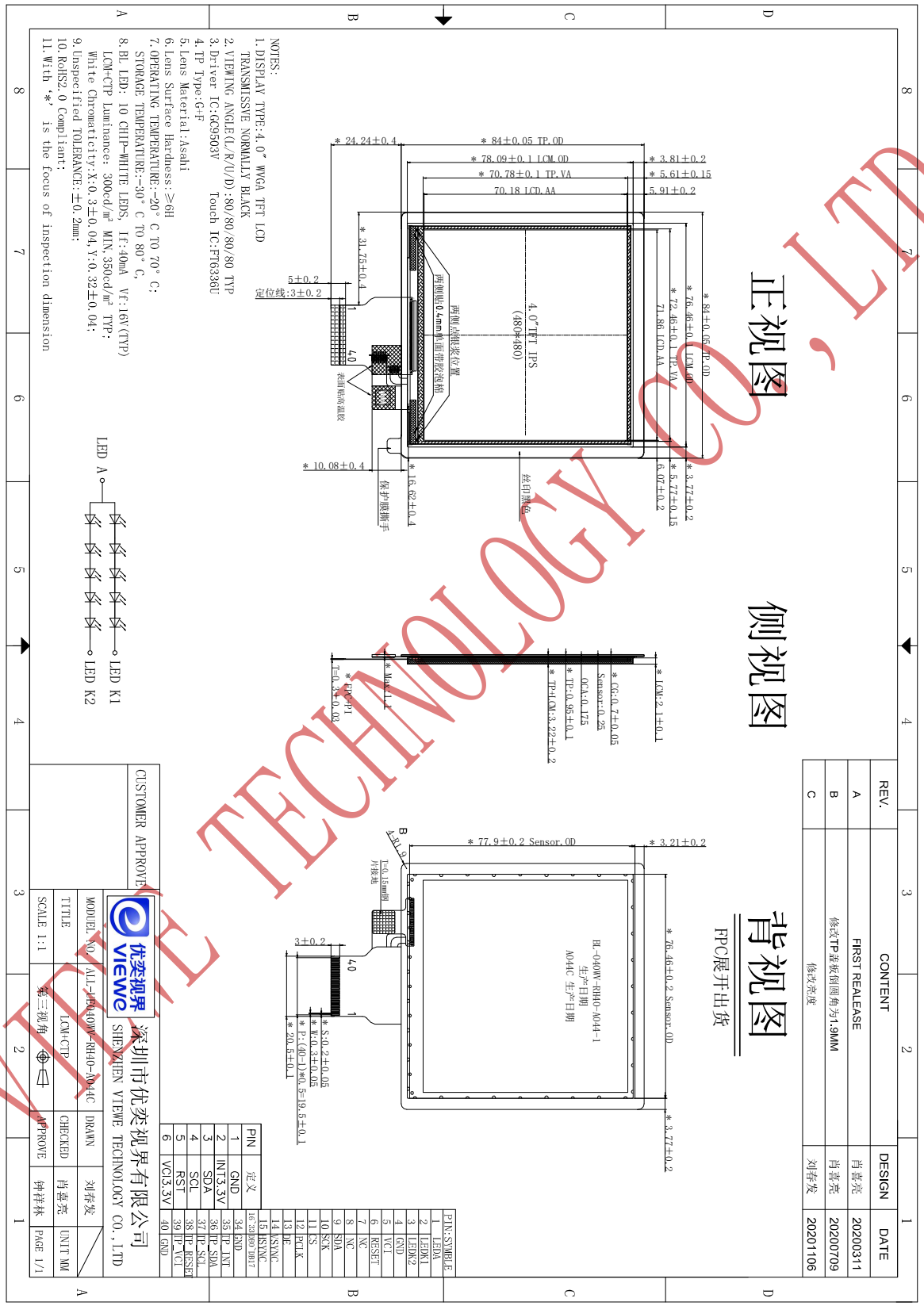
(Ta=+25°C,GND=0V)

Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.
Temp. ＞60℃ , Absolute humidity shall be less than 90% RH.

3. MECHANICAL DRAWING

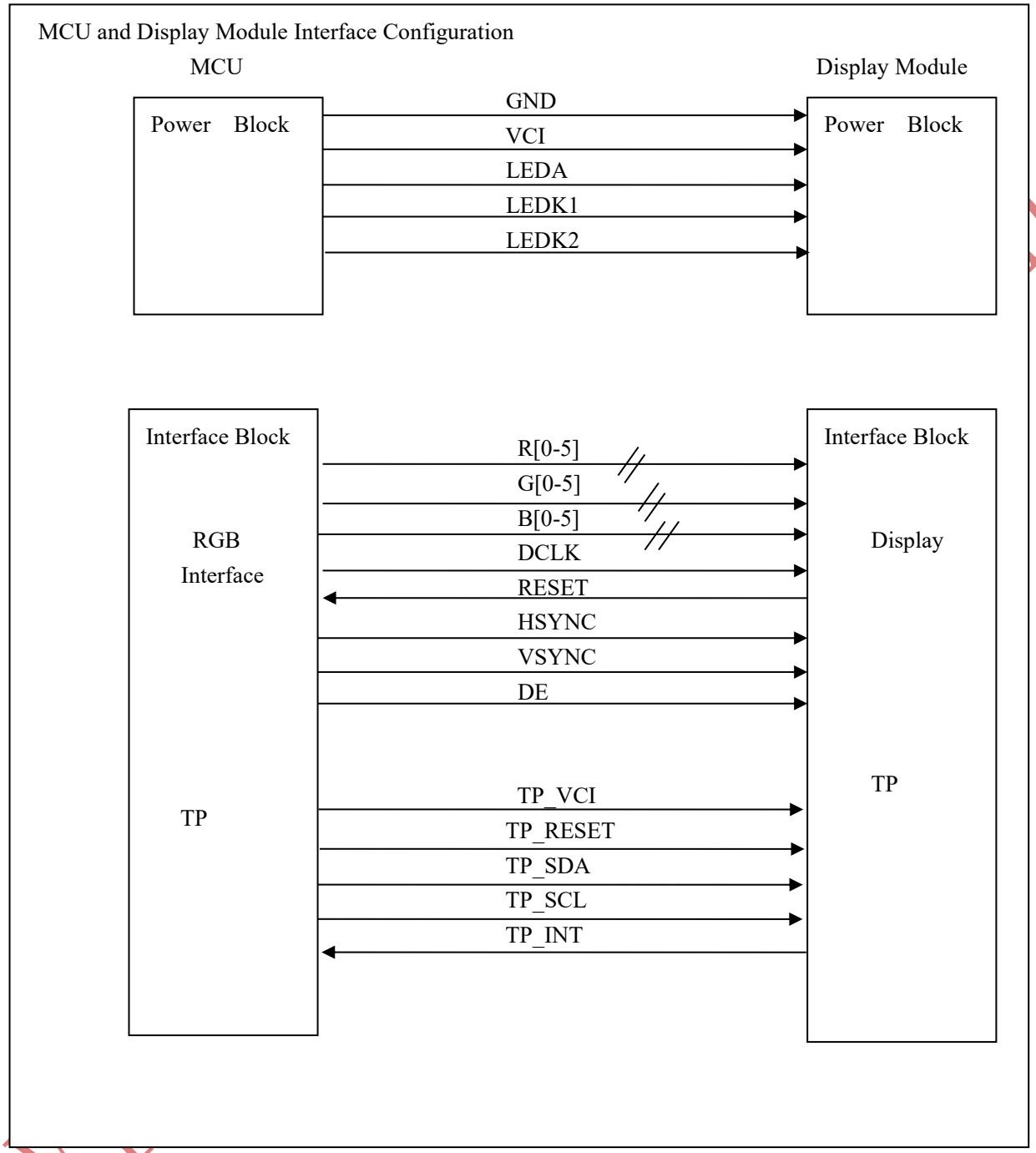


4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

Pin No.	Symbol	I/O	Description
1	LEDA	P	Power supply for backlight anode
2	LEDK1	P	Power supply for backlight cathode
3	LEDK2	P	Power supply for backlight cathode
4	GND	P	Power Ground
5	VCI	P	Power supply to the internal logic power regulator(3.3V)
6	RESET	I	The signal will reset the LCM, Signal is active low.
7-8	NC	-	No conneted
9	SDA	I/O	Serial in/out signal，for initial RGB I/F。
10	SCK	I	serial interface clock，for initial RGB I/F。
11	CS	I	Chip select input pin (“Low” enable)，for initial RGB I/F。
12	PCLK	I	Pixel clock input pin, Negative polarity
13	DE	I	Data input enable. Display access is enabled when DE is “H”
14	VSYNC	I	Vorizontal sync signal, Negative polarity
15	HSYNC	I	Hertical sync signal, Negative polarity
16-21	B0-B5	I	Blue data input.
22-27	G0-G5	I	Green data input.
28-33	R0-R5	I	Red data input.
34	GND	P	Power Ground
35	TP_INT	O	Interrupt signals for TP
36	TP_SDA	I/O	I2C data signals for TP
37	TP_SCL	I	I2C clock signals for TP
38	TP_RST	I	The signal will reset the TP, Signal is active low
39	TP_VCI	P	TP_VDD(2.8V) Power Supply for TP
40	GND	P	Power Ground

4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply Voltage	VCI	2.5	2.8	3.3	V	
Power Supply Voltage	TP_VCI	2.8	3.3	3.3	V	
Power Supply1 Current	I_{VDD}	-	35	-	mA	Note1
Power Supply2 Current	I_{TP_VCI}	-	44	-	mA	Note1
Logic Input High Voltage	V_{IH}	0.7VCI	-	VCI	V	-
Logic Input Low Voltage	V_{IL}	0	-	0.3VCI	V	-
Panel Power Consumption	P_{VDD}	-	0.243	-	Watt	Note1
Module Power Consumption	P_{LCM}	-	0.883	-	Watt	Note1,2

(Ta=+25°C,GND=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=3.3V,60Hz Refresh.

Note2: $P_{ALL}= P_D+ P_{BL}$， About P_{BL} information, inference to 5.2 Back Light Driving Section.

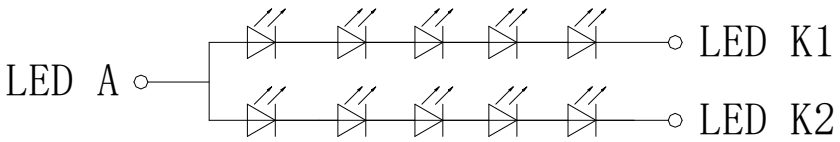
5.2 Back Light Driving Section

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward Voltage	V_F	-	16		V	Note1
Forward Current	I_F	-	40	-	mA	Note1
Backlight Power consumption	P_{BL}	-	0.64	-	Watt	Note1
LED life time	-	30000	-	-	Hrs	Note2
LED Quantity			10		PCS	

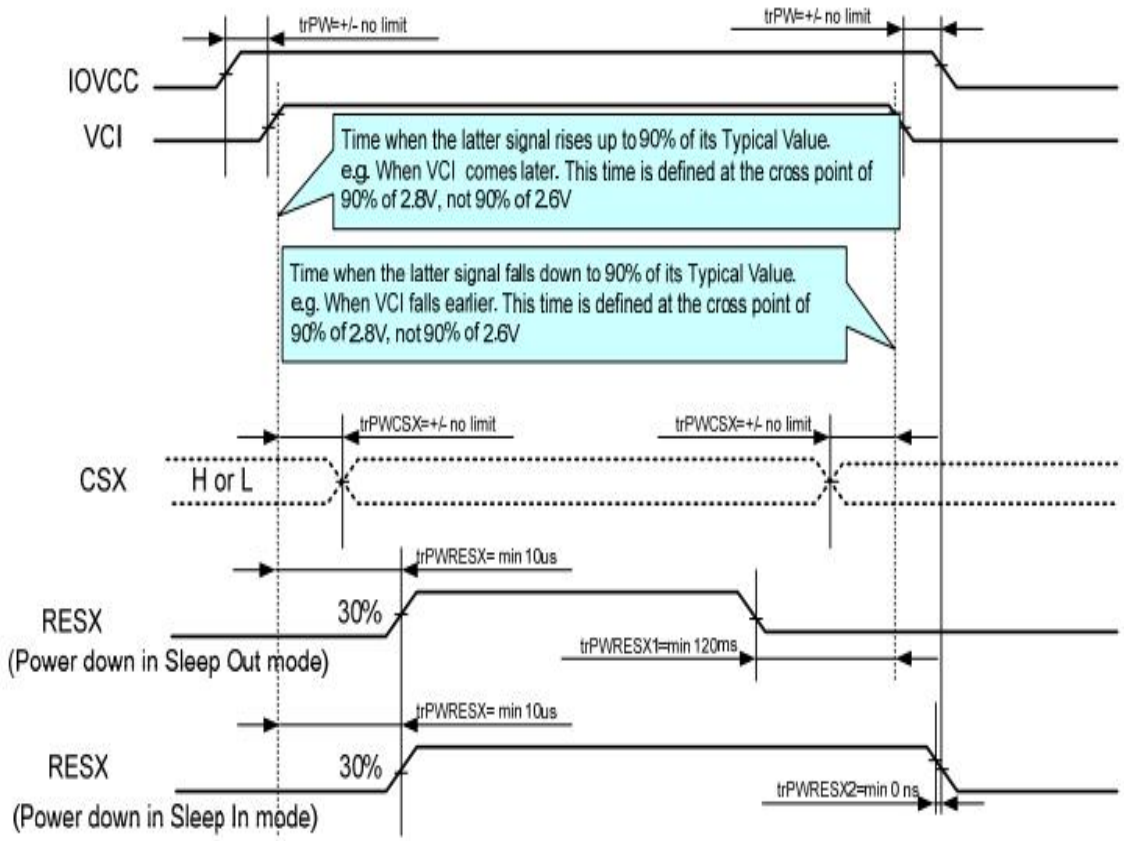
(Ta=+25°C,GND=0V)

Note1: The LED driving condition is defined for each LED module (5 LED Serial, 2 LED Parallel)。
For each LED ： IF=20mA,VF=3.2V(Typ.)/3.4V(Max.),Ta=25℃。

Note2:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.



5.3 Power On/Off Sequence



trPWRESX1 is applied to RESX falling in the Sleep Out Mode

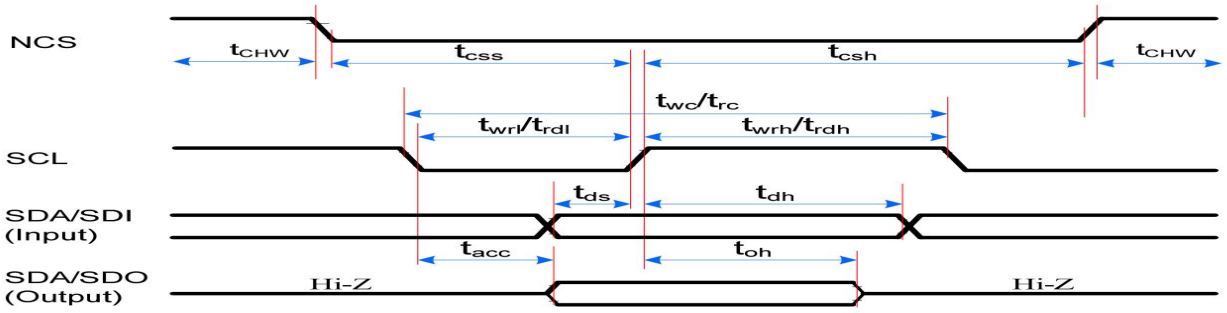
trPWRESX2 is applied to RESX falling in the Sleep In Mode

5.31 Power Off Sequence

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, ILI9806E will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until "Power On Sequence" powers it up.

5.4 Timing Characteristics

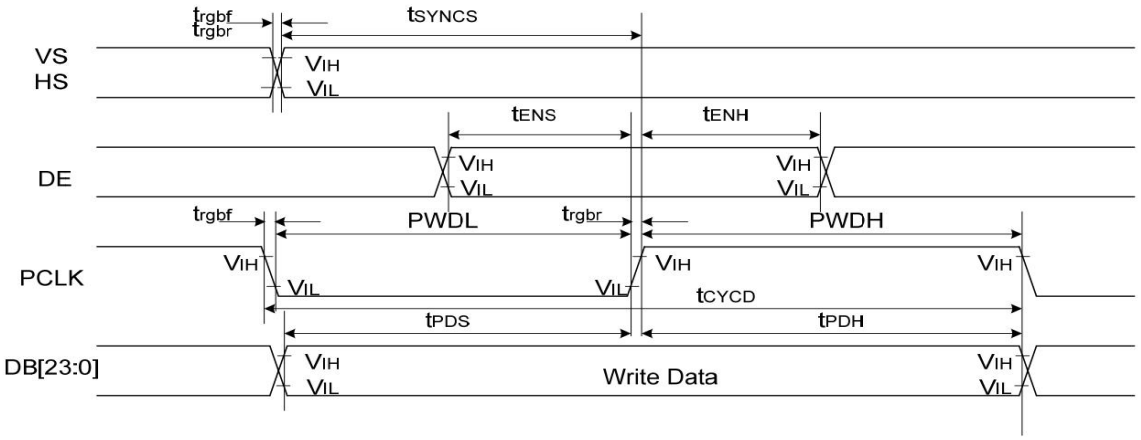
5.4.1 Timing for 3-Wire SPI Interface



(Ta=+25°C,GND=0V)

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS “H” pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL “H” pulse width (Write)	10	-	ns	
	twrl	SCL “L” pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	100	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA/SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	

5.5 Timing Diagram



Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	t_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VS/HS hold time	5	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	5	-	ns	
DB[23:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	t_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr} , t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

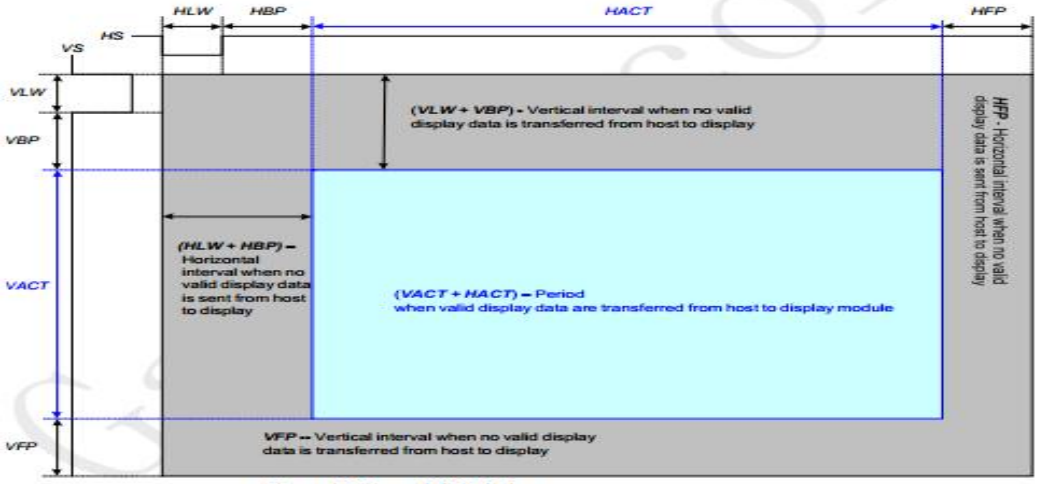


Figure 11 General DPI timing diagram

Parameter	Symbol	Conditio	Min	Typ	Max	Units
Frame Rate	FR		54		6	fps
Horizontal Low Pulse width	HLW		1		-	DOTCL
Horizontal Back Porch	HBP		2		126	DOTCL
Horizontal Address	HACT			48		DOTCL
Horizontal Front Porch	HFP		2		-	DOTCL
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				864	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.		35.	MHz

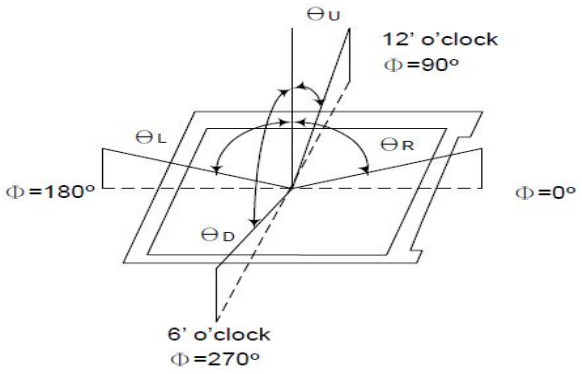
6. OPTICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast Ratio	C/R	θ = 0°	640	800	-	-	Note(4)
NTSC Ratio	S	θ =0°	50	55	-	%	Note(7)
Luminance	L	θ =0°	300	350	-	cd/m2	Note(5)
Luminance uniformity	U_W	θ =0°	-	80	-	%	Note(3)
Response Time	T_R+ T_F	25 °C	-	25	35	ms	Note(2)
Color Coordination	W_X	θ = 0° (Center) Normal viewing angle B/L On	-0.04	0.3	+0.04	NTSC (x,y)	Note(6)
	W_Y			0.32			
	R_X			TBD			
	R_Y			TBD			
	G_X			TBD			
	G_y			TBD			
	B_X			TBD			
	B_Y			TBD			
Viewing Angle	θ_L	C/R>10	-	80	-	Degree	Note(1)
	θ_R		-	80	-		
	θ_U		-	80	-		
	θ_D		-	80	-		

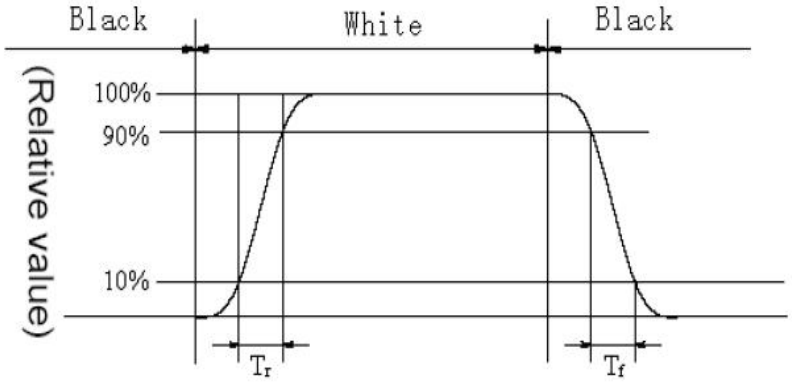
Test Conditions:

1. VDD=2.8V, I_F=40mA (Backlight current), the ambient temperature is+25°C.
2. The test systems refer to Note 8.

Note1: Definition of Viewing Angle: The viewing angle range that the CR>10

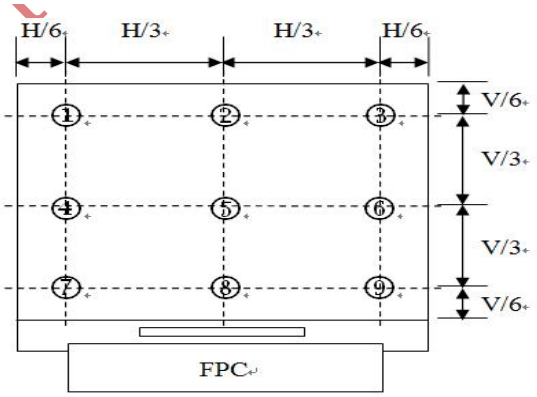


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \times 100\%$$

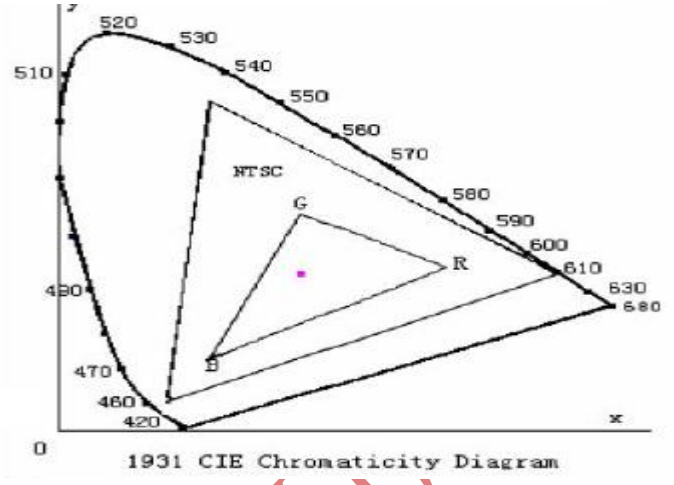


Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

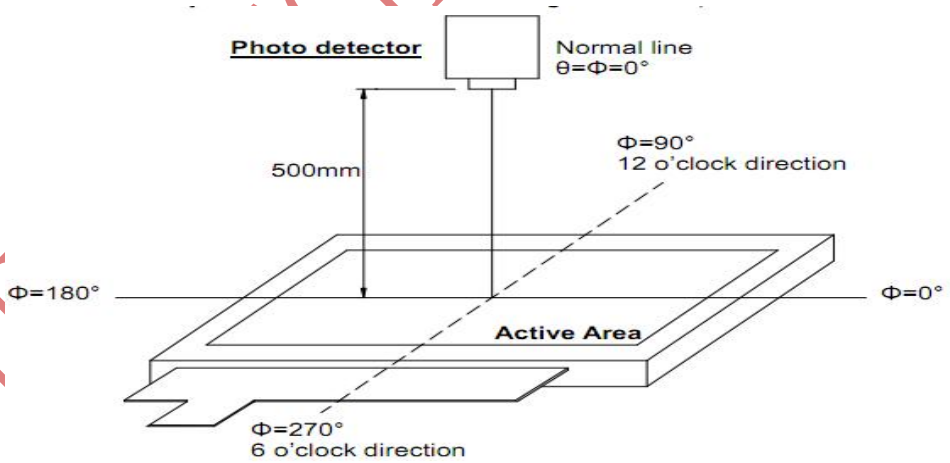
Note 5: Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.
Note 6: Definition of Color Chromaticity (CIE 1931)
Color coordinates of white & red, green, blue measured at center point of LCD.
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



7. RELIABILITY

Item	Test Condition	Remark
High Temperature Storage	Ta =+80°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-30°C/30min Δ+70°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	80°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
Packing shock test	Drop to the ground from 60cm height, 1 corner, 3 edges, 6 surfaces.	Note2
ESD test	Contact: ±4KV Air: ±8KV	ESD

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

8. PACKAGE DRAWING