Indian Institute of Information Technology
Vadodara

End-Sem Exam.: Basic Electronic Circuits (EC100)
Time Duration: 60 Minutes & Max. Marks: 54 (+ 6 Bonus)

Note: You can make assumptions, however, you are requested to state your assumptions clearly and prove if required. Unless otherwise specified, assume Temp. = 300 K if required.

---------- All The Best ----------

Q. 1: A full wave bridge rectifier is designed using Si diodes. Each diode has a forward resistance of 120 Ω. If input is a Sine wave with 24 V (peak-to-peak) and load resistance is of 1.76 KΩ, then determine: (i) DC output voltage; (ii) RMS output voltage; and (iii) Actual rectification efficiency. Use diode model based on third approximation. (6)

Q. 2: In Fig. 1, find the resistance of Ge diode at this particular operating point. Consider the reverse saturation current of the diode is 100 nA. (3)

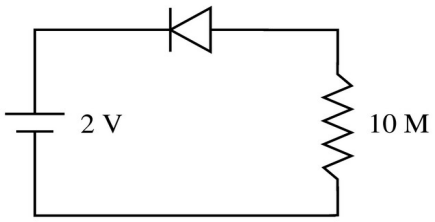

Fig. 1

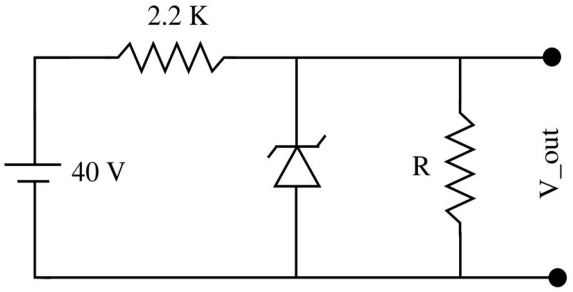

Fig. 2

Q. 3: In voltage regulator circuit shown in Fig. 2, the Zener diode has V_Z = 8 V, I_Z(min) = 500 μA, and I_Z(max) = 12 mA. Find the range of load resistor R so that the output voltage (V_out) remains constant 8 V without damaging the diode. (5)

Q. 4: In Fig. 3: (i) Draw the load line for first stage; and (ii) Find the Q-point of first stage. Further, using pi model, determine: (iii) Input resistance of first stage; (iv) Voltage gain of first stage; (v) AC voltage at node x. Consider the transistor is made of Silicon and Bita is 100. Hint: Z_in of second stage will act as R_L for first stage. (2+3+3+3+3)

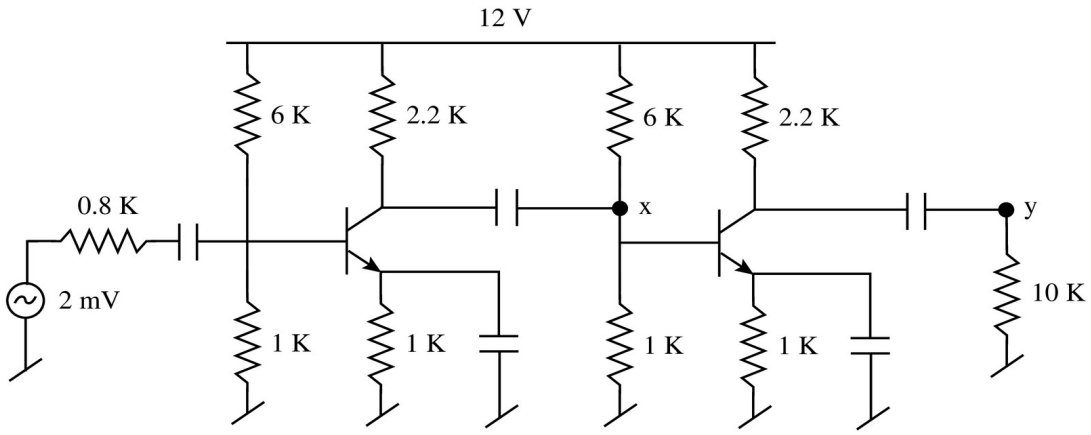

Fig. 3

Q. 5: Find the exact voltage gain (V_out/V_in) of the circuit shown in Fig. 4. Consider the Op-amp is non-ideal and has an open loop gain of 200000. (2)

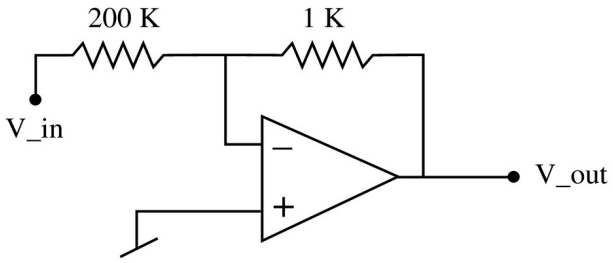

Fig. 4

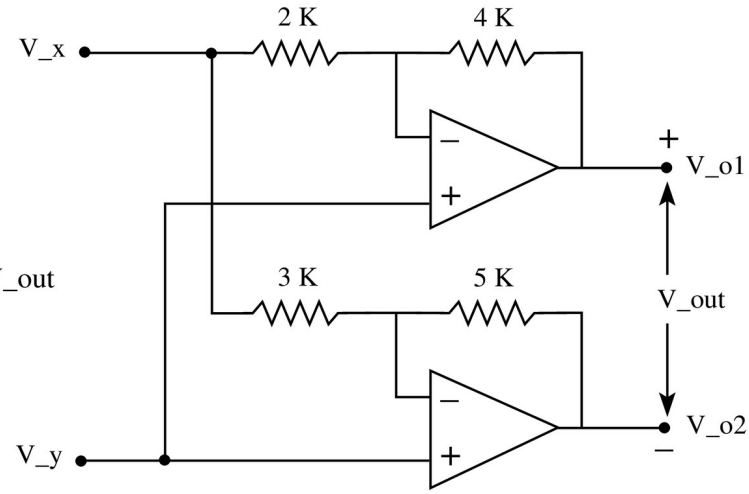

Fig. 5

Q. 6: Find the output voltage (V_out) in Fig. 5, where V_out = V_o1 – V_o2. Consider Op-amps are ideal. Hint: Use superposition theorem. (6)

Q. 7: The N-channel JFET shown in Fig. 6 has V_P = 4 V and I_DSS = 10 mA. Find the drain current (I_D) and drain voltage (V_D). (4)

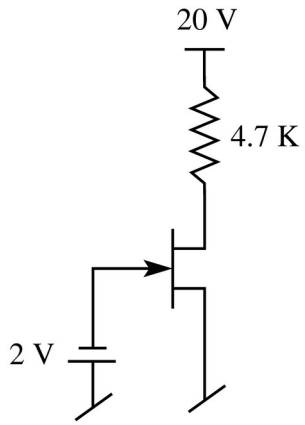

Fig. 6

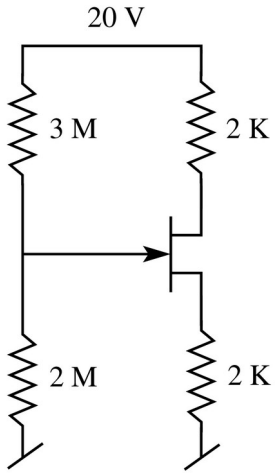

Fig. 7

Q. 8: Draw the load line of the circuit shown in Fig. 7. Also, find the Q-point (V_DS and I_D) of N-channel JFET and locate it on the load line. (4)

Q. 9: An nMOS has V_th = 1 V and u_n × C_ox × (W/L) = 1 mA/V^2. Determine the drain current (I_D) when: (i) V_GS = 0.5 V and V_DS = 2 V; (ii) V_GS = 4 V and V_DS = 2 V, and (iii) V_GS = 4 V and V_DS = 4 V. (1+2+2)

Q. 10: Implement the following Boolean expression using CMOS, where ' represents the NOT, **.** represents the AND and + represents the OR operations. (5)

$$Z = \big((A + B) \,.\, (C' + D \,.\, E) + F\big) \,.\, G$$

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