

5 BIT ADC

EE23BTECH11052 - Abhilash Rapolu

EE23BTECH11036 - Kurre Vinay

Aim of the experiment:

Prepare an 8-hour digital clock.

ABSTRACT

This lab report details the design, functionality, and operation of a 5-bit Analog-to-Digital Converter (ADC). It includes an overview of ADCs, Successive Approximation Register (SAR) methodology, and Digital-to-Analog Converters (DACs). The primary focus of this lab is to understand the principles underlying ADC design and how SAR ADCs work in conjunction with a DAC to perform the analog-to-digital conversion.

INTRODUCTION

In the realm of modern electronics, data conversion between analog and digital signals is crucial. Many real-world signals, like sound and temperature, are analog in nature, but most computing and processing systems operate in the digital domain. Therefore, Analog-to-Digital Converters (ADCs) are fundamental components in mixed-signal systems.

WHAT IS AN ADC?

An **Analog-to-Digital Converter (ADC)** is a device that converts an analog input signal into a corresponding digital output. The analog signal is a continuous waveform, while the digital output is a discrete representation of this input. ADCs are widely used in applications such as audio processing, sensor data acquisition, and communications. The resolution of an ADC is determined by the number of bits it uses to represent the digital output. In our case, a 5-bit ADC provides:

$$2^5 = 32 \text{ discrete levels.}$$

TYPES OF ADCs

There are several types of ADC architectures, including:

- **Flash ADC**
- **Sigma-Delta ADC**
- **Successive Approximation Register (SAR) ADC**

Our focus in this lab is the SAR ADC, known for its balance between speed and power consumption.

WHAT IS SAR (SUCCESSIVE APPROXIMATION REGISTER)?

The **Successive Approximation Register (SAR)** ADC is a type of ADC that uses a binary search algorithm to convert an analog input into a digital output. It works iteratively by comparing the analog input with a generated reference voltage from a Digital-to-Analog Converter (DAC).

How SAR ADC Works:

- 1) The SAR ADC starts by setting the most significant bit (MSB) and uses a DAC to generate a reference voltage.
- 2) It compares the input voltage with this reference. If the input voltage is higher, the bit remains set; otherwise, it is cleared.
- 3) The SAR logic then moves to the next most significant bit and repeats the process.
- 4) This continues until all bits are determined, resulting in a digital output representing the analog input voltage.

SAR ADCs are known for their moderate speed and high resolution, making them suitable for applications that require a good trade-off between speed and accuracy.

WHAT IS A DAC?

A **Digital-to-Analog Converter (DAC)** performs the inverse operation of an ADC. It converts a digital input signal into a corresponding analog output. DACs are used in applications such as audio playback devices, signal generation, and control systems.

Types of DACs:

- **Resistor Ladder DAC:** Uses a series of resistors arranged in a ladder-like configuration to generate analog voltages.
- **Binary-Weighted DAC:** Uses binary-weighted resistors to create an analog output.
- **Current Steering DAC:** Commonly used in high-speed applications.

In our 5-bit SAR ADC design, the DAC generates precise reference voltages for each comparison step, ensuring the accurate operation of the ADC.

DESIGN AND IMPLEMENTATION OF A 5-BIT ADC

The design of a 5-bit Analog-to-Digital Converter (ADC) involves understanding how to convert a continuous analog input signal into a 5-bit digital representation using the Successive Approximation Register (SAR) technique. The following section provides a detailed, step-by-step explanation of the design and implementation process.

1. Understanding the Requirements

- **Goal:** To design a 5-bit ADC, which means we need to convert an analog input voltage into a digital output of 5 bits. This provides:

$$2^5 = 32 \text{ discrete levels}$$

meaning the full range of the input voltage will be divided into 32 equally spaced voltage levels.

- **Components Needed:**
 - A 5-bit Successive Approximation Register (SAR)
 - A 5-bit Digital-to-Analog Converter (DAC)
 - A voltage comparator
 - Control logic circuitry

2. Components Overview

- 1) **SAR (Successive Approximation Register):** The SAR is a digital control block that sequentially approximates the analog input signal by setting or clearing each bit, starting from the most significant bit (MSB) and working down to the least significant bit (LSB).
- 2) **DAC (Digital-to-Analog Converter):** The DAC takes the digital output from the SAR and converts it into an analog voltage. This voltage is used as a reference for comparison with the input analog voltage.
- 3) **Comparator:** The comparator compares the input analog voltage with the reference voltage from the DAC. It outputs a high or low signal, indicating whether the input voltage is greater than or less than the reference voltage.

STEP-BY-STEP PROCESS OF THE ADC OPERATION

Step 1: Initialization

The SAR ADC begins the conversion process by setting the MSB to '1' and all other bits to '0'.

Example: If the SAR is 5 bits, it starts with the digital code 10000.

Step 2: DAC Generates a Reference Voltage

The DAC receives the initial digital code (10000) from the SAR and converts it into an analog reference voltage.

If the full-scale input voltage range is, say, 0V to 5V, and assuming a linear DAC, 10000 would correspond to 2.5V (half of the range).

Step 3: Comparison

The comparator checks if the input analog voltage (V_{in}) is greater than or less than the reference voltage generated by the DAC.

- If $V_{in} > \text{Reference Voltage}$, the comparator outputs '1'.
- If $V_{in} \leq \text{Reference Voltage}$, the comparator outputs '0'.

Step 4: Bit Decision and Update

The SAR reads the output from the comparator:

- If the output is '1', the MSB remains set to '1'.
- If the output is '0', the MSB is cleared (set to '0').

The SAR then moves to the next bit (the second most significant bit), sets it to '1', and repeats the process.

Step 5: Iteration for All Bits

This process continues iteratively for all 5 bits. Each time, the DAC generates a new reference voltage based on the updated digital code, and the comparator determines if the bit should remain set or be cleared.

Step 6: Final Digital Output

Once all 5 bits have been determined, the SAR produces the final digital output code, representing the analog input voltage as a 5-bit digital number. The digital code is then sent for further digital processing or used as needed in the application.

EXAMPLE OF THE SAR ADC CONVERSION PROCESS

Assumptions

- Full-scale input voltage range: 0V to 5V
- Input analog voltage: 3.1V

Conversion Steps

- **Iteration 1:**
 - SAR sets 10000 → DAC outputs 2.5V
 - Comparator: $3.1V > 2.5V$, so bit remains '1'
- **Iteration 2:**
 - SAR sets 11000 → DAC outputs 3.75V
 - Comparator: $3.1V < 3.75V$, so bit is cleared to '0'
- **Iteration 3:**
 - SAR sets 10100 → DAC outputs 3.125V
 - Comparator: $3.1V < 3.125V$, so bit is cleared to '0'
- **Iteration 4:**
 - SAR sets 10010 → DAC outputs 2.8125V
 - Comparator: $3.1V > 2.8125V$, so bit remains '1'
- **Iteration 5:**
 - SAR sets 10011 → DAC outputs 3.0625V
 - Comparator: $3.1V > 3.0625V$, so bit remains '1'

Final Output

The 5-bit digital output is 10011, corresponding to an approximate analog input of 3.1V.

CONCLUSION OF DESIGN IMPLEMENTATION

The 5-bit SAR ADC successfully converts analog input voltages into corresponding digital outputs through a binary search process. This design is efficient, with a moderate speed and high accuracy suitable for various applications. The SAR logic, DAC precision, and comparator performance are crucial for the accuracy of the ADC.

R 2R DAC CIRCUIT

:

