VLSI Assignment-2

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General Points

- All subparts have been answered accordingly.
- Few explanations were given at last for questions instead of mentioning in respective subparts to maintain a flow
- Plot titles couldn’t be attached to all plots hence I didn’t crop the title bar to include the title of the netlist.
- Codes and supporting files can be found here 

Question 3

3. Consider a CMOS inverter with size $'W'$, which has the following parameters : $L = 0.18\mu m$, $W_n = W = 1.8\mu m$ and $W_p = 2.5 \times W$.

   (a) Using NGSPICE, plot VTC of inverter-1 (I_1) for the case when the inverter is driving a same sized inverter (I_2) as shown in Fig. 1.

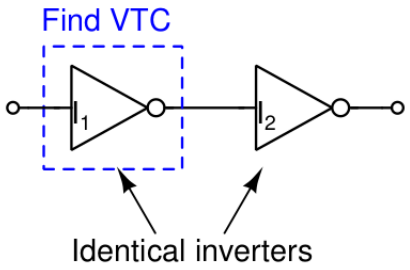


Figure 1

   (b) As discussed in class, derive the expressions for noise-margins NM_H and NM_L for a CMOS inverter.

   (c) From the VTC plot in (a) find the noise margin parameters ($V_{IH}, V_{IL}, V_{OH}, V_{OL}$) and calculate NM_H and NM_L. Compare the noise-margins obtained from simulation with the theoretical values obtained in part (b) for which you can use V_T values that you extracted in assignment-1.

   (d) Draw layout for case (a), extract the netlist and run post layout simulation to plot VTC of I_1 and find its NM_H and NM_L by clearly showing all noise-margin parameters on the plot. Tabulate theoretical, pre-layout and post-layout noise-margins for I_1. Do you observe any difference (pre-layout vs post-layout)? Comment.

Part a)

NETLIST

```
hello
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

*vin a 0 pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
Vdd vdd gnd 'SUPPLY'
vin a gnd 1.8
.subckt inv y x vdd gnd
.param width_P={50*LAMBDA}
.param width_N={20*LAMBDA}
M1 y x gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA}
+ PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 y x vdd vdd CMOSP W={width_P} L={2*LAMBDA} AS={5*width_P*LAMBDA}
+ PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv

x1 b a vdd gnd inv
x2 c b vdd gnd inv

*.tran 0.1n 2n
.dc vin 0 1.8 0.01

.control
run
plot v(a) v(b)
set curplottile = "Viswanadh 2019112011"

.endc
```

- We’ve designed our two-inverter system using the subckt command which is similar to one used in previous assignment codes. Then accordingly I’ve plotted the VTC for one of those inverters.

Plot

Plot of V_{OUT} vs time and V_{IN} vs time for I_1.

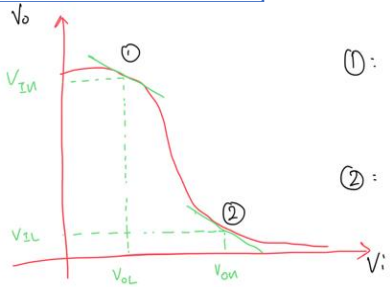
X-axis: time(in S) Y-axis: Voltage(in V)

---- V_{OUT}

---- V_{IN}

Line segments are drawn at points where |slope| is 1. These points make up the coordinates {(V_{IL},V_{OH}) and (V_{IH},V_{OL})} as the region between these points give us gain greater than 1 which is an undesired characterstic when preparing an Inverter

Part b)



① : NMOS – saturation
PMOS – linear

② : NMOS – linear
PMOS – saturation

① → $I_{D,N_{sat}} = I_{D,P_{lin}}$

$$\Rightarrow \frac{K_n}{2}(V_i - V_{Tn})^2 = K_P\left[(V_{DD} - V_i - |V_{TP}|)(V_{DD} - V_o) - \frac{(V_{DD} - V_o)^2}{2}\right]$$

Taking $K_n = K_P$ & $V_{DD} - V_o = a$,

$$\frac{(V_i - V_{Tn})^2}{2} = (V_{DD} - V_i - |V_{TP}|)(a) - \frac{a^2}{2}$$

$$\Rightarrow \frac{a^2}{2} - a(V_{DD} - V_i - |V_{TP}|) + (V_i - V_{Tn})^2/2 = 0$$

Solving the quadratic equation in a, $\{a = V_{DD} - V_o\}$

$$a = (V_{DD} - V_i - |V_{TP}|) \pm \sqrt{(V_{DD} - V_i - |V_{TP}|)^2 - (V_i - V_{Tn})^2}$$

$$\Rightarrow V_o = V_i + |V_{TP}| \pm \sqrt{(V_{DD} - V_i - |V_{TP}|)^2 - (V_i - V_{Tn})^2} \quad -(a)$$

Now we get ① when $\frac{\partial V_o}{\partial V_i} = -1$

ie $$1 \pm \left[\frac{-(V_{DD} - V_i - |V_{TP}|) - (V_i - V_{Tn})}{\sqrt{(V_{DD} - V_i - |V_{TP}|)^2 - (V_i - V_{Tn})^2}}\right] = -1$$

$$\Rightarrow (2)^2 = \frac{(V_{DD} - V_{Tn} - |V_{TP}|)^2}{(V_{DD} - V_{Tn} - |V_{TP}|)(V_{DD} - |V_{TP}| - V_{Tn} - 2V_i)}$$

Keeping $V_i = V_{iL}$,

$$V_{iL} = \frac{3V_{DD} - 3|V_{TP}| + 5V_{TN}}{8}$$

Keeping V_{iL} value in (a) to get V_{OH},

$$V_{OH} = \frac{7V_{DD} + |V_{TP}| + V_{TN}}{8}$$

② $I_{D,N_{lin}} = I_{D,P_{sat}}$

$$\Rightarrow K_N\left[(V_i - V_{TN})V_o - \frac{V_o^2}{2}\right] = \frac{K_P}{2}(V_i - V_{DD} - |V_{TP}|)^2$$

Taking $K_N = K_P$

$$(V_i - V_{TN})V_o - \frac{V_o^2}{2} = \frac{(V_i - V_{DD} - |V_{TP}|)^2}{2}$$

$$\Rightarrow \frac{V_o^2}{2} - (V_i - V_{TN})V_o + \frac{(V_i - V_{DD} - |V_{TP}|)^2}{2} = 0$$

Solving the quadratic equation in terms of V_o,

$$V_o = (V_i - V_{TN}) \pm \sqrt{(V_i - V_{TN})^2 - (V_i - V_{DD} - |V_{TP}|)^2} \quad -(b)$$

Again finding $\frac{\partial V_o}{\partial V_i} = -1$, similar to previous workings

$$\frac{V_{DD} + |V_{TP}| - V_{TN}}{-(V_{TN} + V_{DD} + |V_{TP}| - 2V_i)} = 4$$

Substituting $V_i = V_{IH}$,

$$V_{IH} = \frac{5V_{DD} - 5|V_{TP}| + 3V_{TN}}{8}$$

Substituting V_{IH} value in (b), then $V_o = V_{OL}$:

$$V_{OL} = \frac{V_{DD} - |V_{TP}| - V_{TN}}{8}$$

Now finally,

$$NM_H = V_{OH} - V_{IH} = \frac{V_{DD} + 3|V_{TP}| - V_{TN}}{4}$$

$$NM_L = V_{IL} - V_{OL} = \frac{V_{DD} + 3V_{Tn} - |V_{TP}|}{4}$$

Part c)

- The slope of V_{OUT} vs V_{IN} graph is =|1| at 2 points P_1 and P_2 (say). From the VTC plot in a, we get P_1 (0.7396, 1.69629) and P_2 (0.997239, 0.103097) which are correspondingly (VIL,VOH) and (VIH,VOL).
- Now,

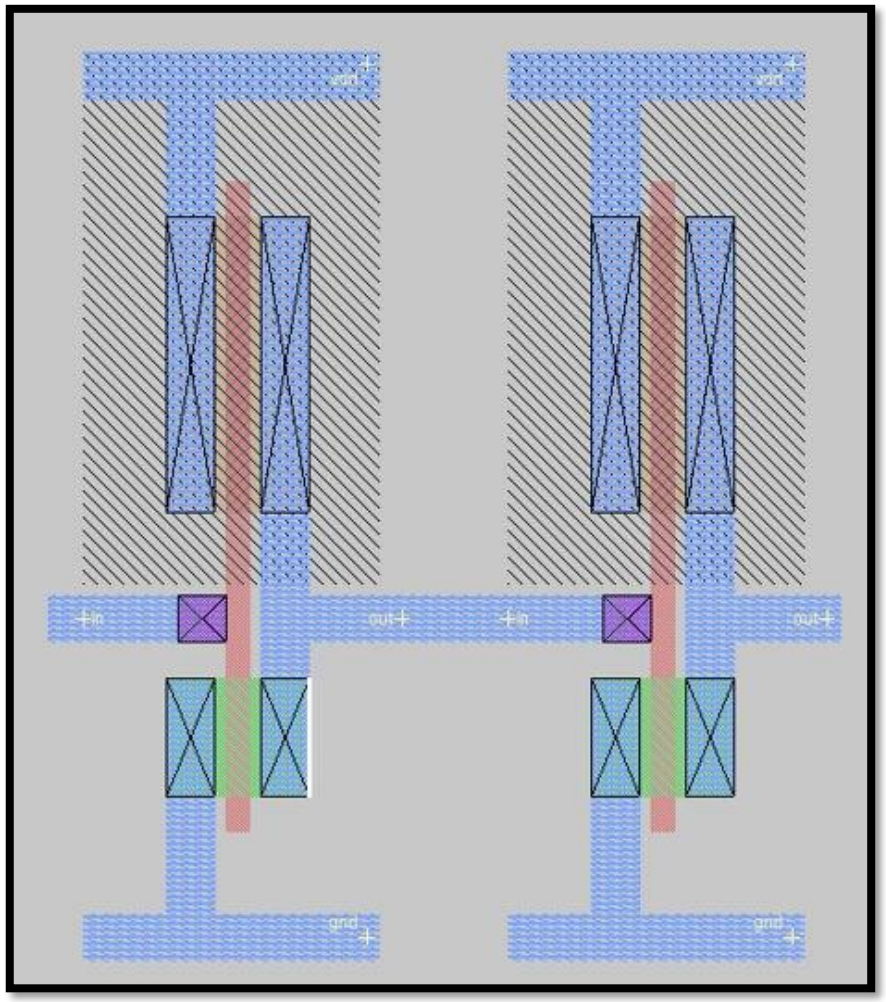
$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

ie NM_H = 1.69629 - 0.9972 = 0.69909 and NM_L= 0.636503. Tabulated data and comparison with the theoretical values is presented in the coming slides.

Part d)

L A Y O U T



Parameters taken:

P-diffusion – 12λ / 50λ
N-diffusion – 12λ / 20λ

Netlist extracted from MAGIC

```
VTC for post layout ckt
.option scale=0.09u
.include TSMC_180nm.txt
.param SUPPLY=1.8
.global gnd vdd

Vdd vdd gnd 'SUPPLY'
vin a gnd 1.8

M0 c b vdd inverter_0/w_n8_n5# CMOSP w=50 l=2
+  ad=250 pd=110 as=250 ps=110
M1 c b gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=100 ps=50
M2 b a vdd inverter_1/w_n8_n5# CMOSP w=50 l=2
+  ad=250 pd=110 as=250 ps=110
M3 b a gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=100 ps=50
C0 inverter_0/w_n8_n5# b 0.06fF
C1 b vdd 0.54fF
C2 gnd c 0.21fF
C3 b vdd 0.02fF
C4 b c 0.05fF
```

```
C5 inverter_0/w_n8_n5# vdd 0.13fF
C6 inverter_0/w_n8_n5# c 0.07fF
C7 vdd c 0.54fF
C8 a inverter_1/w_n8_n5# 0.06fF
C9 a gnd 0.05fF
C10 a b 0.05fF
C11 inverter_1/w_n8_n5# b 0.07fF
C12 b gnd 0.21fF
C13 a vdd 0.02fF
C14 gnd b 0.05fF
C15 inverter_1/w_n8_n5# vdd 0.13fF
C16 gnd Gnd 0.13fF
C17 vdd Gnd 0.03fF
C18 a Gnd 0.12fF
C19 inverter_1/w_n8_n5# Gnd 1.68fF
C20 gnd Gnd 0.13fF
C21 c Gnd 0.07fF
C22 vdd Gnd 0.03fF
C23 b Gnd 0.20fF
C24 inverter_0/w_n8_n5# Gnd 1.68fF

.dc vin 0 1.8 0.01

.control
run
plot v(a) v(b)
set curplottile = "Viswanadh 2019112011"

.endc
```

- We’ve designed our two-inverter system by taking the netlist from MAGIC including the parasitic capacitances. Then accordingly I’ve plotted the VTC for one of those inverters.

Plot

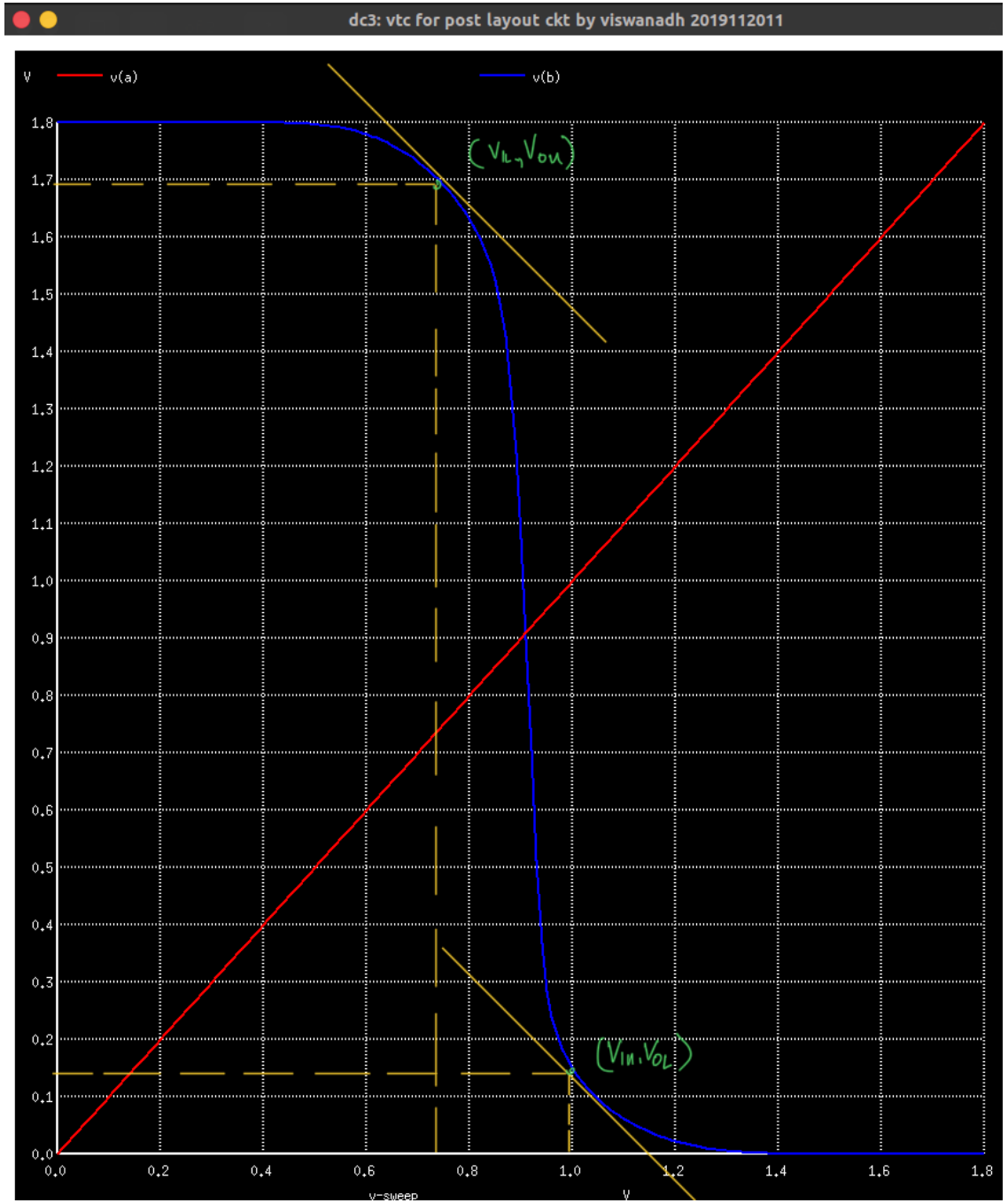
Plot of V_{OUT} vs time and V_{IN} vs time for I_1.

X-axis: time(in S) Y-axis: Voltage(in V)

---- V_{OUT}

---- V_{IN}

Line segments are drawn at points where |slope| is 1. These points make up the coordinates {(V_{IL},V_{OH}) and (V_{IH},V_{OL})} as the region between these points give us gain greater than 1 which is an undesired characterstic when preparing an Inverter

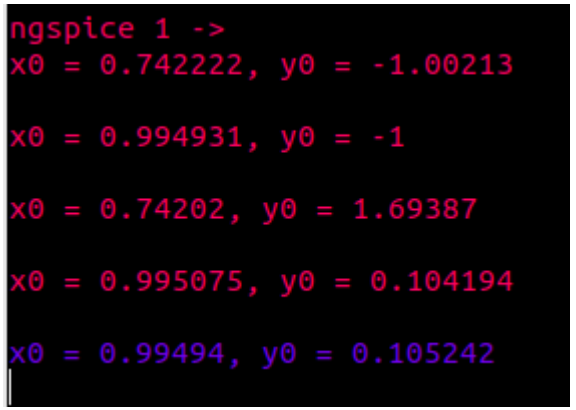


- The slope of V_{OUT} vs V_{IN} graph is =|1| at 2 points P_1 and P_2 (say). From the VTC plot in a, we get P_1 (0.742222, 1.69387) and P_2 (0.994931, 0.105242) which are correspondingly (VIL,VOH) and (VIH,VOL).
- Now,

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

ie NM_H = 1.69387 - 0.994931 = 0.698939 and NM_L= 0.63698.



	V_{OL} (in V)	V_{IL} (in V)	V_{IH} (in V)	V_{OH} (in V)	NM_H (in V)	NM_L (in V)
Theoretical	0.1	0.853	1.05	1.69	0.648	0.753
Pre-Layout	0.103	0.74	0.997	1.696	0.69909	0.636503
Post-Layout	0.105	0.742	0.995	1.694	0.698939	0.63698

We can observe that in our theoretical and Pre-layout calculations we didn't consider the internal capacitances. But still NGSPICE takes up good approximations for MOSFET than our manual calculations hence resulting in a better voltage readings in Pre-layout readings which are most accurate. Also it can be noted that Post-layout values which are obtained from MAGIC are almost similar to pre-Layout readings. Also VTCs obtained are in line to our theory

Question 4

4. A typical CMOS inverter is considered to drive 4 similar inverters or having a fan-out of 4 (FO4 inverter). We want to characterize the delay of FO4 inverter, for which input and output waveforms should also be typical in nature. Consider the figure 2, where an inverter with size 'W' has following parameters : $L = 0.18\mu m$, $W_n = W = 1.8\mu m$ and $W_p = 2.5 \times W_n$. Write a net-list for the given configuration and apply a piece wise linear input at node 'A' as follows : *V_{in} vin A 0 pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V).*

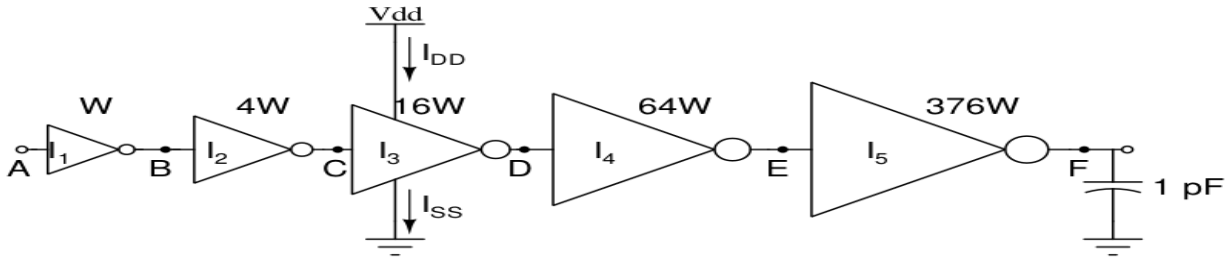


Figure 2

(a) As discussed in class, derive the expressions for rise-time (τ_{rise}) and fall-time (τ_{fall}) for an inverter in terms of noise margin parameters, supply voltage, threshold voltages of devices, K_n, K_p and load capacitance (C_L). Calculate $K_p\tau_{rise}/C_L$ and $K_n\tau_{fall}/C_L$ using the required values from the results obtained in problem 2(d), where $K = \mu C_{ox}\frac{W}{L}$.

(b) Run transient simulation for 5 ns in step size of 10 ps for the given circuit and plot the signals at node 'C' and 'D' in the same graph. From the graphs, find the values of τ_{rise} and τ_{fall} at both the nodes C and D (You may consider 10% to 90% of the transient for finding rise/fall times. Use .measure for accuracy). Are they same? Comment.

(c) Use .MEASURE command in NGSPICE and tabulate the propagation delays (input to output) of inverters I_3 and I_4. Are they same? Discuss.

(d) Plot the supply current I_{DD} as shown in the figure and explain the plot obtained.

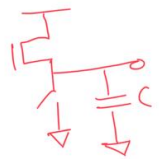
(e) Plot the ground current I_{SS} as shown in the figure and explain the plot obtained.

Part A) For T_{RISE}

Qn 4)

Consider an inverter I

(i)



here, PMOS is ON
CMOS is OFF

now T_{rise} : time for C to charge from 0 to V_{on}

where I_{dp} is current through PMOS

$$\text{ie } \int_0^{t_{rise}} \frac{1}{C}\cdot dt = \int_0^{V_{on}} \frac{dV_o}{I_{dp}}$$

$$\Rightarrow \frac{T_{rise}}{C} = \int_0^{V_{on}} \frac{dV_o}{I_{dp}}$$

here I_{dp} is not constant { it can be either linear or saturation }

$$\therefore \frac{T_{rise}}{C} = \int_0^{V_i+|V_{TP}|} \frac{1}{I_{dpsat}}\cdot dV_o + \int_{V_i+|V_{TP}|}^{V_{on}} \frac{1}{I_{dplin}}\cdot dV_o$$

(1) (2)

here, $I_{dpsat} = \frac{K_p}{2}\cdot(V_{SG}-|V_{TP}|)^2$

$I_{dplin} = K_p\left[(V_{SG}-|V_{TP}|)V_{SD} - \frac{V_{SD}^2}{2}\right]$

$$\text{(1)} \rightarrow \int_0^{V_i+|V_{TP}|} \frac{2}{K_p\cdot(V_{SG}-|V_{TP}|)^2}\cdot dV_o = \int_0^{V_i+|V_{TP}|} \frac{2}{K_p(V_{iL}-|V_{TP}|-V_{DD})^2}\cdot dV_o$$

$$= \frac{2(V_{iL}+|V_{TP}|)}{K_p(V_{iL}-|V_{TP}|-V_{DD})^2}$$

$$\text{(2)} \rightarrow \int_{V_i+|V_{TP}|}^{V_{on}} \frac{dV_o}{K_p\left[(V_{DD}-V_i-|V_{TP}|)(V_{DD}-V_o) - \frac{(V_{DD}-V_o)^2}{2}\right]}$$

{ then $V_{tp} = |V_{tp}|$ }

$$= \frac{-2}{K_p}\int \frac{dV_o}{(V_o-V_{dd})^2 - (2V_{tp}+2V_i-2V_{dd})(V_o-V_{dd})}$$

completing it as a perfect square,

Consider $u = \frac{V_o - V_{tp} - V_i}{\sqrt{-(V_{tp}+V_i)^2+2V_{dd}(V_{tp}+V_i-V_{dd})+V_{dd}^2}}$

$$= \frac{1}{\sqrt{-(V_{tp}+V_i)^2+2V_{dd}(V_{tp}+V_i-V_{dd})+V_{dd}^2}}\cdot\int \frac{1}{u^2+1}\cdot du$$

Plugging in the value of u after the integration & substituting the limits, we get

$$= \frac{\ln(V_{DD}+V_{on}-2V_{in}-2|V_{TP}|) - \ln(V_{DD}-V_{on})}{K_p(V_{DD}-V_{iL}-|V_{TP}|)}$$

$$\therefore T_{rise} = \frac{2C(V_{iL}+|V_{TP}|)}{K_p(V_{DD}-V_{iL}-|V_{TP}|)^2} + \frac{C\cdot\ln\left(\frac{V_{DD}+V_{on}-2V_{in}-2|V_{TP}|}{V_{DD}-V_{on}}\right)}{K_p(V_{DD}-V_{iL}-|V_{TP}|)}$$

$V_{DD} = 1.8V$

Substituting $L = 0.18\mu m$, $W_n = W = 1.8\mu m$, $W_p = 2.5\times W_n$, $|V_{TP}| = 0.44$,

$V_{Tn} = 0.55V$ (~), $V_{OL} = 0.1V$, $V_{iL} = 0.853V$, $V_{in} = 1.05V$, $V_{on} = 1.69V$,

$$\frac{K_p T_{rise}}{C_L} = 2\left(\frac{V_{iL}+|V_{TP}|}{(V_{DD}-V_{iL}-|V_{TP}|)^2}\right) + \ln\left(\frac{V_{DD}+V_{on}-2V_{in}-2|V_{TP}|}{V_{DD}-V_{on}}\right)\Big/(V_{DD}-V_{iL}-|V_{TP}|)$$

Here, we use theoretical values for ie

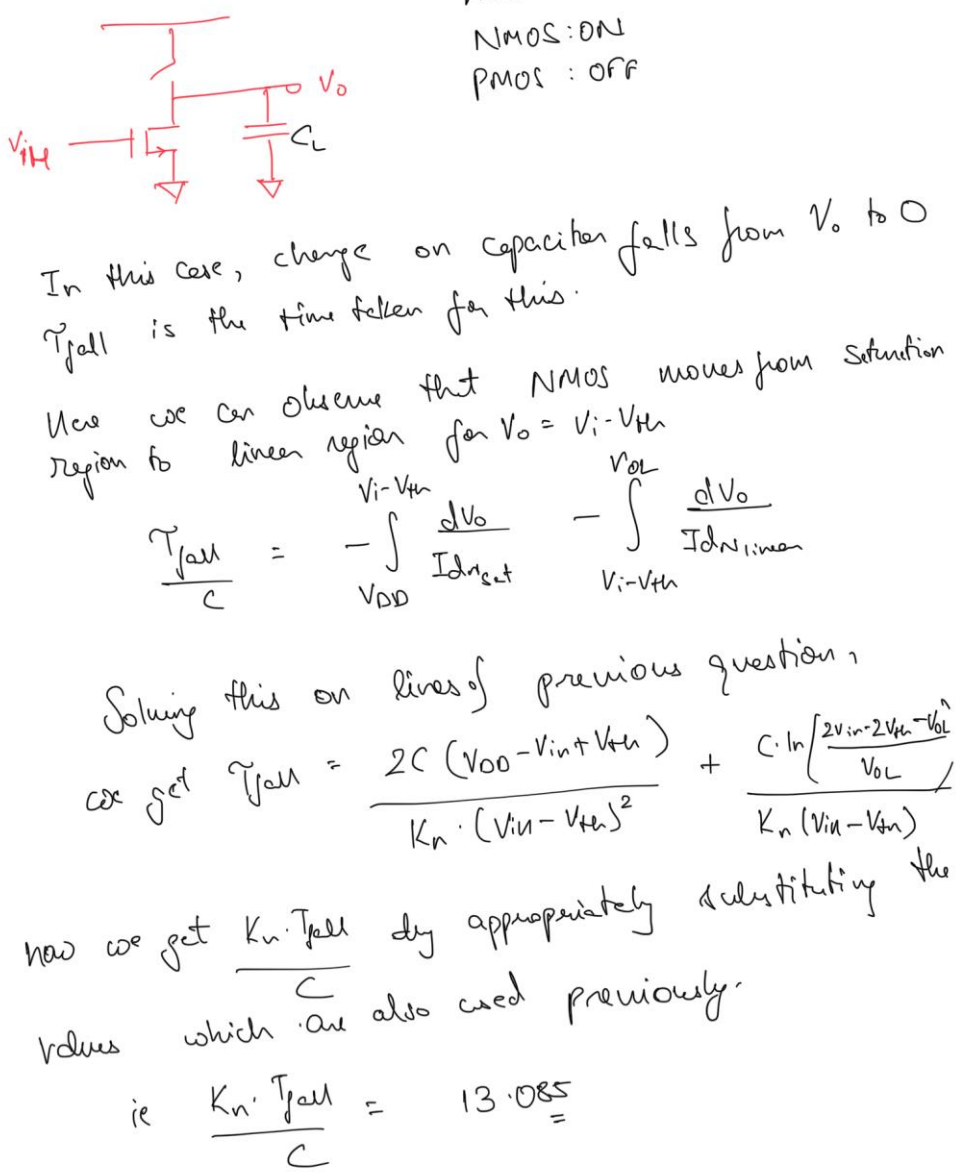
$V_{on} = \frac{7V_{DD}+V_{tn}+|V_{TP}|}{8}$; $V_{iL} = \frac{3V_{DD}+5V_{tn}-3|V_{TP}|}{8}$

$V_{in} = \frac{5V_{DD}+3V_{tn}-5|V_{TP}|}{8}$; $V_{OL} = \frac{V_{DD}-V_{tn}-|V_{TP}|}{8}$

for $W = 1.8\mu m$, $\frac{K_p T_{rise}}{C_L} = 13.085$

Calculation used for finding $K_P T_{RISE}/C_L$ =
2*(0.853+0.44)÷(1.8−0.853−0.44)^2 +
ln((1.8+1.69−2×1.05−2×0.44)÷(1.8−1.69)) ÷ (1.8−0.853−0.44)

For T_{FALL}



We can notice that we are getting equal values for $K_P T_{RISE}/C_L$ and $K_N T_{FALL}/C_L$

- Calculation used for finding $K_N T_{FALL}/C_L$ = 2*(1.8−1.05+0.55)÷(1.05−0.55)^2 + ln((2×1.05−2×0.55−0.1)÷(0.1)) ÷ (1.05−0.55)

Part B)

NETLIST

```
hello
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

vin a 0 pwl 0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V
Vdd vdd gnd 'SUPPLY'

.subckt inv0 y x vdd gnd
.param width_P={50*LAMBDA}
.param width_N={20*LAMBDA}
M1 y x gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA}
+ PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 y x vdd vdd CMOSP W={width_P} L={2*LAMBDA} AS={5*width_P*LAMBDA}
+ PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv0

.subckt inv1 y x vdd gnd
.param width_P={4*50*LAMBDA}
.param width_N={4*20*LAMBDA}
M1 y x gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA}
+ PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 y x vdd vdd CMOSP W={width_P} L={2*LAMBDA} AS={5*width_P*LAMBDA}
+ PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv1

*.subckt inv2 y x vdd gnd
.param width_P={16*50*LAMBDA}
.param width_N={16*20*LAMBDA}
lol vdd d1 0
lol2 d2 gnd 0
M1 d c d2 gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA}
+ PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 d c d1 vdd CMOSP W={width_P} L={2*LAMBDA} AS={5*width_P*LAMBDA}
+ PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
*.ends inv2
```

```
.subckt inv3 y x vdd gnd
.param width_P={64*50*LAMBDA}
.param width_N={64*20*LAMBDA}
M1 y x gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA}
+ PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 y x vdd vdd CMOSP W={width_P} L={2*LAMBDA} AS={5*width_P*LAMBDA}
+ PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv3

.subckt inv4 y x vdd gnd
.param width_P={376*50*LAMBDA}
.param width_N={376*20*LAMBDA}
M1 y x gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA}
+ PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 y x vdd vdd CMOSP W={width_P} L={2*LAMBDA} AS={5*width_P*LAMBDA}
+ PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv4


x1 b a vdd gnd inv0
x2 c b vdd gnd inv1
*x3 d c vdd gnd inv2
x4 e d vdd gnd inv3
x5 f e vdd gnd inv4

C1 f gnd 100p
*vin a 0 pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)
.tran 10ps 5n
*.dc vin 0 1.8 0.01
*---------------------B
$for C
.measure tran tpdrC
+ TRIG v(c) VAL='0.1*SUPPLY' RISE=1
+ TARG v(c) VAL='0.9*SUPPLY' RISE=1

.measure tran tpdfC
+ TRIG v(c) VAL='0.9*SUPPLY' FALL=1
+ TARG v(c) VAL='0.1*SUPPLY' FALL=1

$for D
.measure tran tpdrD
+ TRIG v(d) VAL='0.1*SUPPLY' RISE=1
+ TARG v(d) VAL='0.9*SUPPLY' RISE=1

.measure tran tpdfD
+ TRIG v(d) VAL='0.9*SUPPLY' FALL=1
+ TARG v(d) VAL='0.1*SUPPLY' FALL=1
```

```
.control
run
let idd = (-lol#branch)
let iss = (-lol2#branch)
set curplottile = "Viswanadh 2019112011"
plot v(c) v(d)
plot idd iss

.endc
```

Here we designed a FO4 Inverter for an inverter. I've used subckt for each CMOS inverter as they have different values of W. Also I've used .MEASURE function to accurately get the RISE and FALL times.

We define them as follows for this case:

T_{RISE}: Time taken for the voltage to change from 10% to 90% of the supply value.

T_{FALL}: Time taken for the voltage to change from 90% to 10% of the supply value.

Also I've created new terminal to get the current through the terminal/branch.

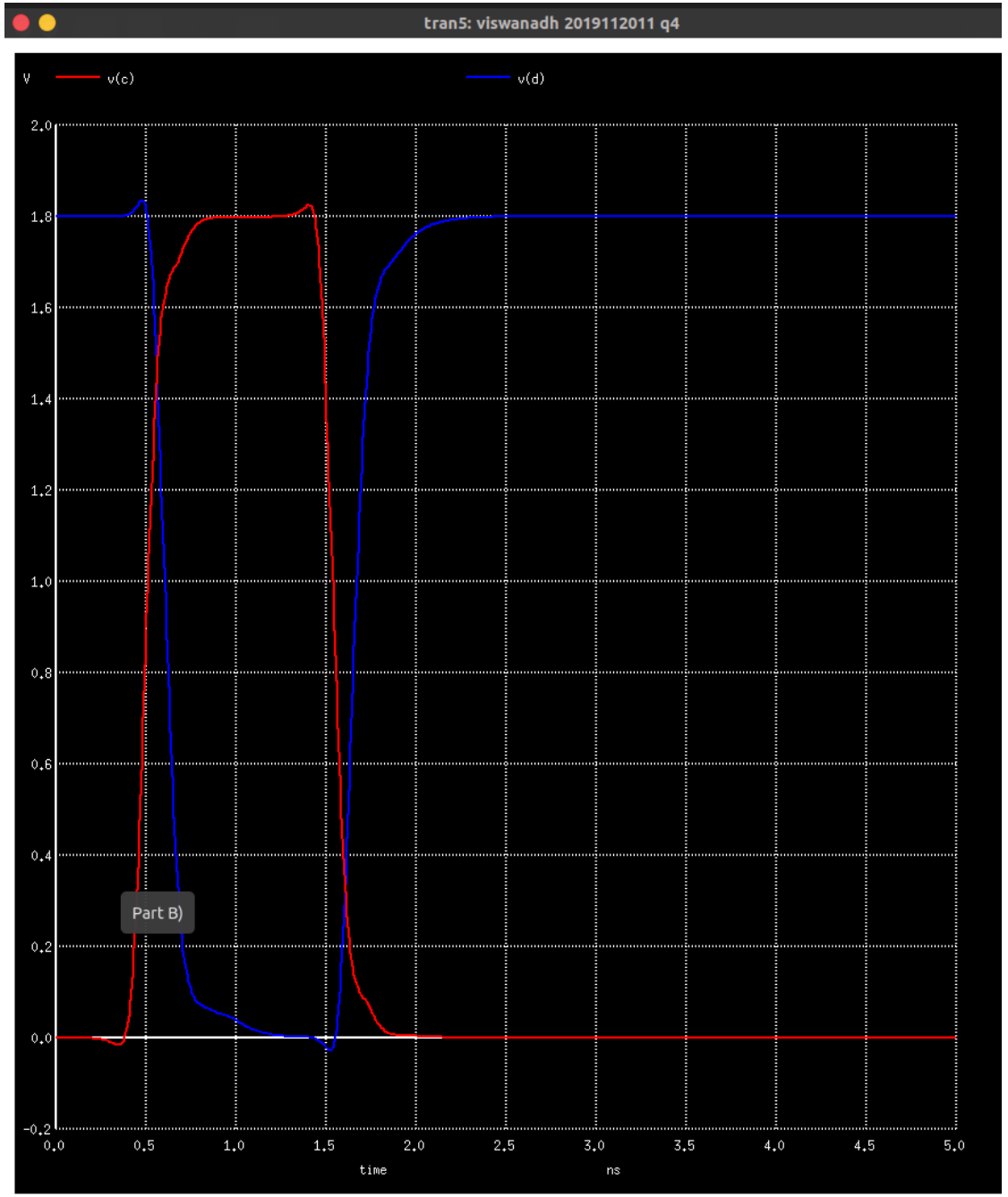
Plot

Plot of V_C vs time and V_D vs time .

X-axis: time(in S) Y-axis: Voltage(in V)

---- V_C

---- V_D



```
tpdrc                =  1.699407e-10
tpdfc                =  1.616961e-10
tpdrd                =  1.865388e-10
tpdfd                =  1.681677e-10
```

*Time values obtained from NGSPICE simulation

	TRISE (10^{-10}s)	**TFALL (in 10^{-10}s)**
C	1.6994	1.6169
D	1.86538	1.6816

Generally T_{RISE} and T_{FALL} are governed by the measurements of PMOS and NMOS respectively. We can observe the rise and Fall times of inverter C and D aren’t the same and this can be attributed to the fact that their widths aren't the same which in turn changes their parasitic capacitance values directly affecting the RISE and FALL times of the inverter.

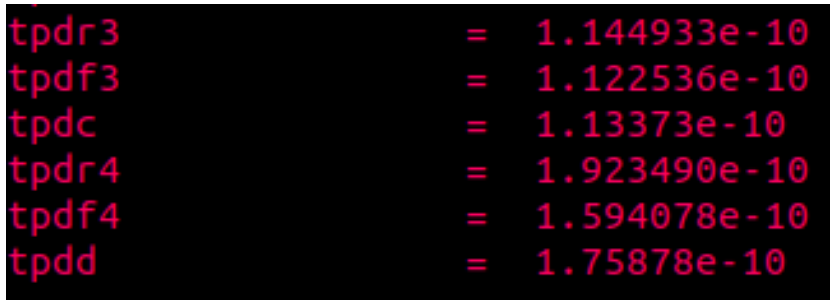
Part C)

NETLIST

```
*----------------------C

.measure tran Tpdr3
+ TRIG v(c) VAL='SUPPLY/2' FALL=1
+ TARG v(d) VAL='SUPPLY/2' RISE=1

.measure tran Tpdf3
+ TRIG v(c) VAL='SUPPLY/2' RISE=1
+ TARG v(d) VAL='SUPPLY/2' FALL=1

.measure tran tpdC param='(Tpdr3+Tpdf3)/2' goal=0

.measure tran Tpdr4
+ TRIG v(d) VAL='SUPPLY/2' FALL=1
+ TARG v(e) VAL='SUPPLY/2' RISE=1

.measure tran Tpdf4
+ TRIG v(d) VAL='SUPPLY/2' RISE=1
+ TARG v(e) VAL='SUPPLY/2' FALL=1

.measure tran tpdD param='(Tpdr4+Tpdf4)/2' goal=0
```

*This is continuation for the previous NETLIST

- We simply used the measure function to find out the propagation delay values. Here, we define propagation delay as the sum of RISE and FALL times of the chosen inverter.
- Here suffix ‘3’ refers to the Inverter 3 while ‘4’ refers to the inverter 4 while ‘r’ and ‘f’ refer to RISE and FALL.



*Time values obtained from NGSPICE simulation

Inverter	**Propagation Delay (in 10^{-10}s)**
Inverter C	1.13373
Inverter D	1.75878

We can observe that Propogation delays are again not the same for both the inverters and this can be attributed to the fact that they are driving different capacitive loads. Here I_3 has series capacitance of both I_4 and I_5 whose C_{eff} would be less than both I_4 and I_5 while I_4 has load resistance equal to capacitance of I_5 thus increasing the rise, fall times leading to high propagation delays

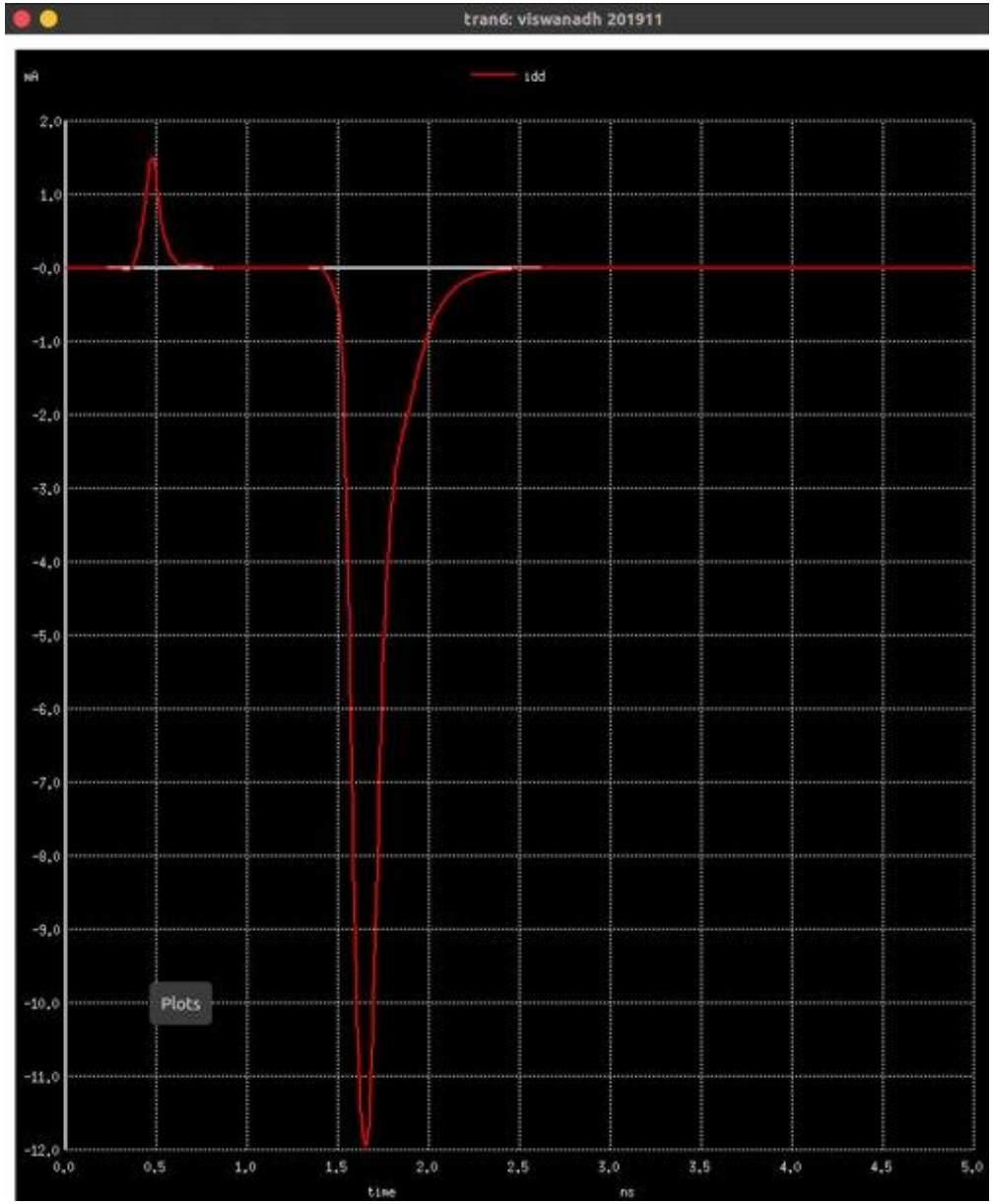
Part D)

P L O T S

Plot of I_{DD} vs time .

X-axis: time(in S) Y-axis: Voltage(in mA)

---- I_{DD}



- Here we are plotting $-I_{DD}$. So initially we have a small spike of positive current as Gate voltage of the inverter is negative. Then we can observe a positive spike as the input voltage turns out to be greater than the output voltage {Linear}. Then the current falls back again as input voltages becomes less than the output voltage {Cut-off}

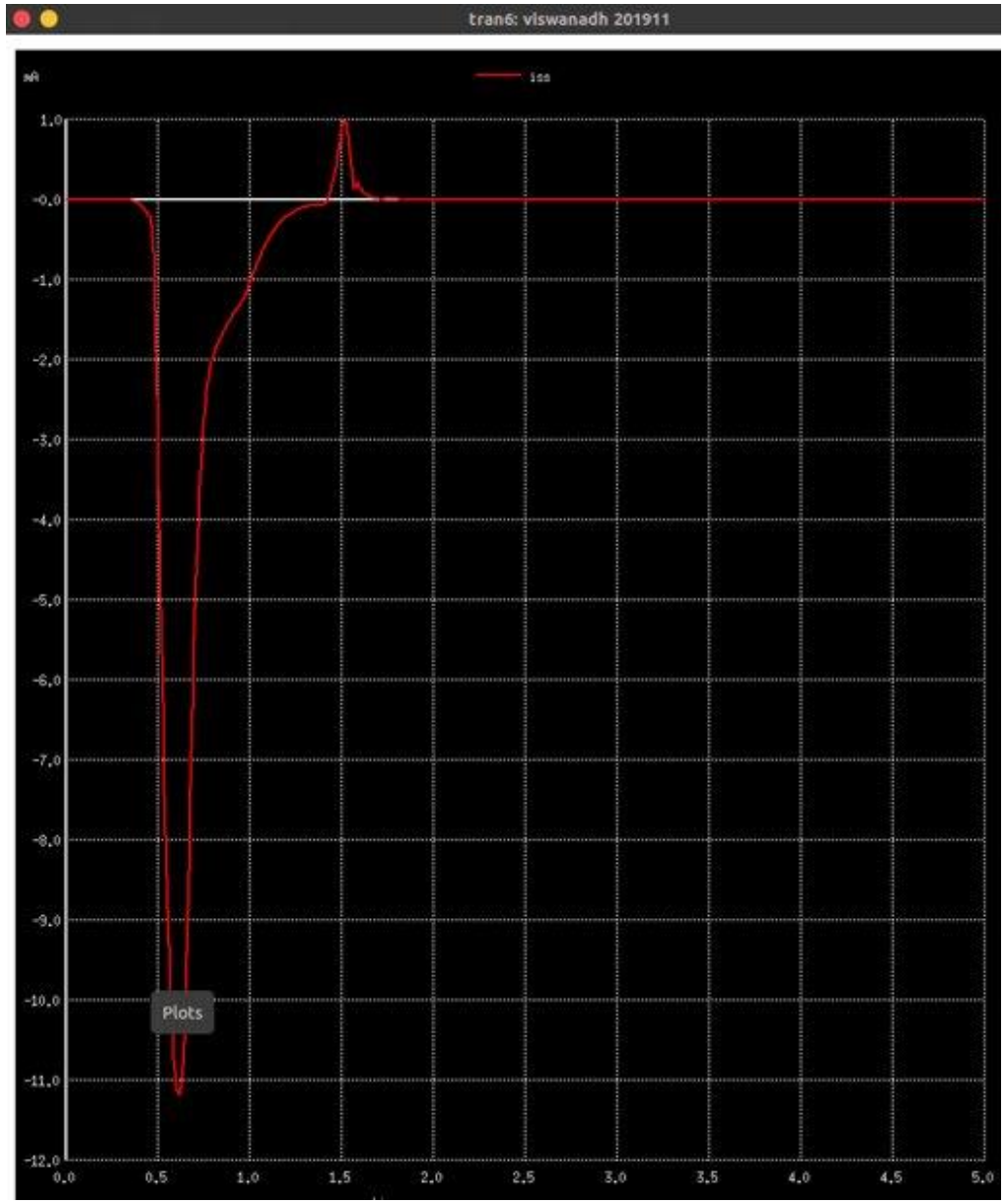
Part E)

P L O T S

Plot of I_{SS} vs time .

X-axis: time(in S) Y-axis: Voltage(in mA)

---- I_{SS}



- Here we are plotting $-I_{SS}$ .It's very intuitive to see that we get almost same shape as the before plot with an offset as we are replacing a PMOS with NMOS. Both NMOS and PMOS act the same way except their region of operations change thus creating the offset in x-axis and different V_T values result in different magnitudes for both which is also clearly noticeable in the plots.

Question 5)

5. Design a 31 stage ring oscillator (RO) using $L = 2\lambda$, $W_n = 10\lambda$ and $W_p = 25\lambda$, where $\lambda = 0.09\mu m$.

   (a) Write NGSPICE netlist for the RO and find frequency (f_{RO}) of oscillation and delay (τ_D) of a single inverter from simulation results. Do the values obtained from simulation results satisfy $f_{RO} = \frac{1}{62\tau_D}$, comment.

   (b) Draw an optimized layout for the 31 stage RO using MAGIC layout editor.
   (Hint: Some useful magic commands- :getcell inverter-layout-name, :array <columns> <rows>, :upsidedown)

   (c) Extract the netlist of the RO from the layout with parasitics and use NGSPICE to find f_{RO} and τ_D

   (d) Compare the pre-layout and post-layout simulation results and comment on the difference (if any).

Part A)

NETLIST

```
hello
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

*vin a 0 pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
Vdd vdd gnd 'SUPPLY'
*vin a gnd 1.8

.subckt inv y x vdd gnd
.param width_P={25*LAMBDA}
.param width_N={10*LAMBDA}
M1 y x gnd gnd CMOSN W={width_N} L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N}
+ AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 y x vdd vdd CMOSP W={width_P} L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P}
+ AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv

x1 a2 a1 vdd gnd inv
x2 a3 a2 vdd gnd inv
x3 a4 a3 vdd gnd inv
x4 a5 a4 vdd gnd inv
x5 a6 a5 vdd gnd inv
x6 a7 a6 vdd gnd inv
x7 a8 a7 vdd gnd inv
x8 a9 a8 vdd gnd inv
x9 a10 a9 vdd gnd inv
x10 a11 a10 vdd gnd inv
x11 a12 a11 vdd gnd inv
x12 a13 a12 vdd gnd inv
x13 a14 a13 vdd gnd inv
x14 a15 a14 vdd gnd inv
x15 a16 a15 vdd gnd inv
x16 a17 a16 vdd gnd inv
x17 a18 a17 vdd gnd inv
x18 a19 a18 vdd gnd inv
x19 a20 a19 vdd gnd inv
x20 a21 a20 vdd gnd inv
```

```
x21 a22 a21 vdd gnd inv
x22 a23 a22 vdd gnd inv
x23 a24 a23 vdd gnd inv
x24 a25 a24 vdd gnd inv
x25 a26 a25 vdd gnd inv
x26 a27 a26 vdd gnd inv
x27 a28 a27 vdd gnd inv
x28 a29 a28 vdd gnd inv
x29 a30 a29 vdd gnd inv
x30 a31 a30 vdd gnd inv
x31 a1 a31 vdd gnd inv

.tran 0.1n 20n
*.dc vin 0 1.8 0.01

.ic v(a1) = 1.8V

.measure tran tperiod
+ TRIG v(a1) VAL='SUPPLY/2' RISE=1
+ TARG v(a1) VAL='SUPPLY/2' RISE=2

.measure tran tpdr
+ TRIG v(a1) VAL='SUPPLY/2' FALL=1
+ TARG v(a2) VAL='SUPPLY/2' RISE=1

.measure tran tpdf
+ TRIG v(a1) VAL='SUPPLY/2' RISE=1
+ TARG v(a2) VAL='SUPPLY/2' FALL=1

.measure tran tpd param='(tpdr+tpdf)/2' goal=0

.control
run
plot a1 a2
.endc
```

- For preparing the Ring Oscillator (RO) , we use subckt to get the 31 CMOS inverters and connect the output of final inverter to the input of initial inverter. Theory says that RO should have odd number of inverters (here 31) to get a oscillator. Since all inverters are chained up , delays of each inverter gets added up at every stage.

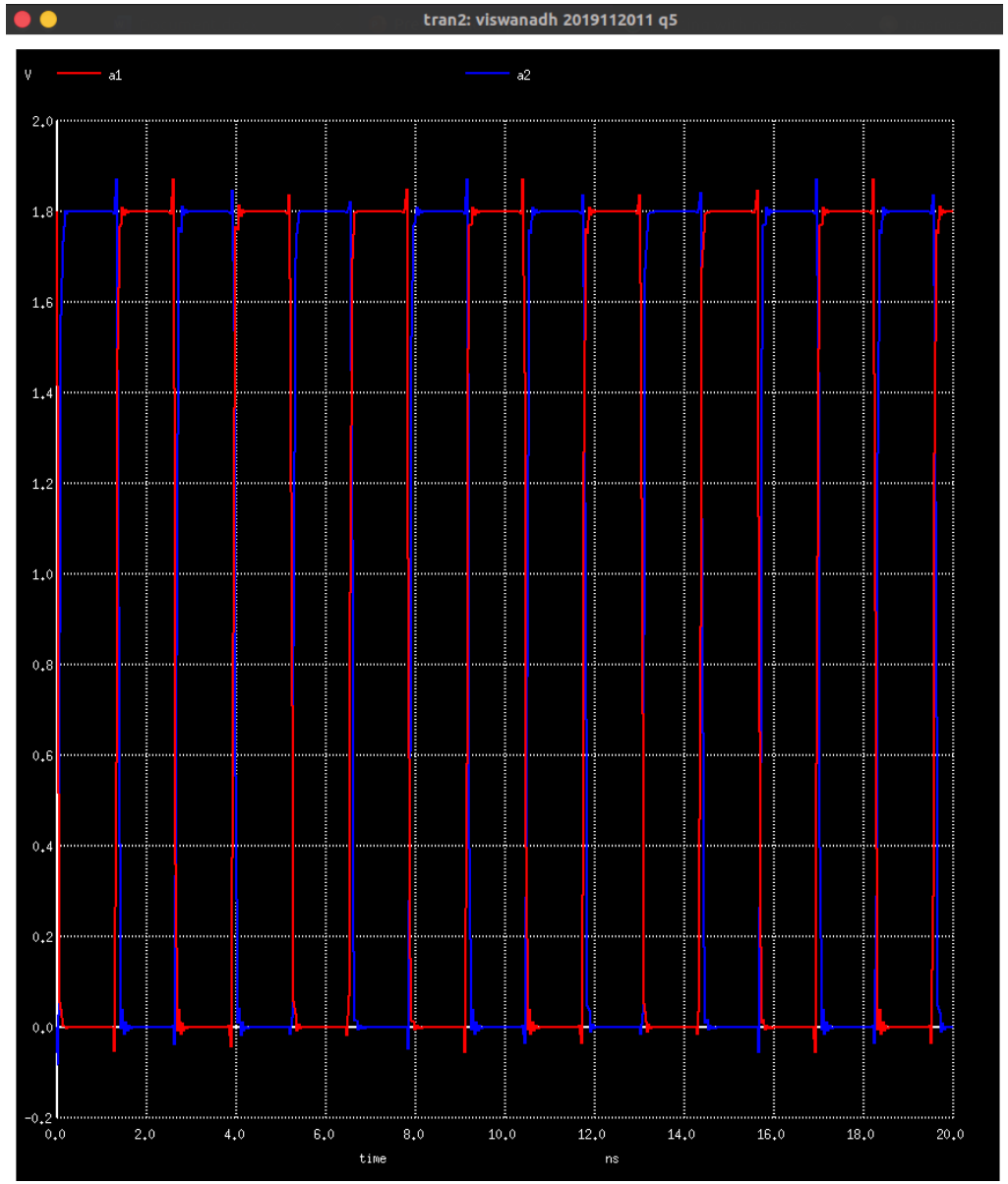
PLOTS

Plot of V_A vs time and V_B vs time where A and B are two terminals of an inverter/

X-axis: time(in S) Y-axis: Voltage(in V)

---- V_A

---- V_B



```
tperiod                =   2.607751e-09
tpdr                   =   4.100509e-11
tpdf                   =   4.185947e-11
tpd                    =   4.14323e-11
```

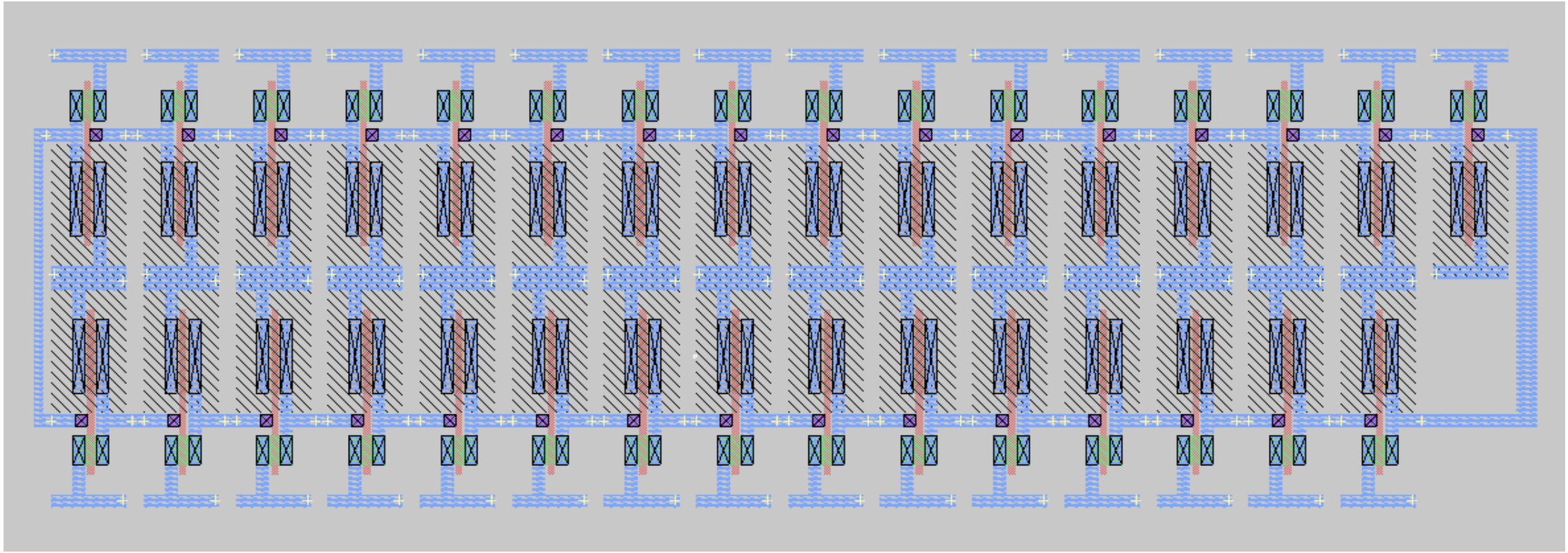
Here we can note that $T_{PD} = 4.143 * 10^{-11}$ while $F_{RO} = 1/t_{period} = 1/(2.607 * 10^{-9})$.Here Time period is the time between two rising edges. We can note that

$$F_{RO} = 1/62\tau_D$$

is approximately satisfied with the values obtained.

Part B)

LAYOUT



Here for creating the ring oscillator, I've initially designed a single CMOS inverter with parameters mentioned. This used *getcell* function to get a copy of inverter in another MAGIC file and then used *array 15 1* and *array 16 1* to get two the inverters in two rows. And then later flipped and mirror imaged using *upsidedown* for a row of inverters and then connected the initial and final inverter using Metal 1. We can note that we have created 2 rows of inverters instead of 1 to get better capacitances as supposed to a linear one which would result in higher capacitance value that would substantially increase the RISE and FALL times.

Parameters used:

- P-diffusion – 12λ / 25λ
- N-diffusion – 12λ / 10λ

Part C) Netlist

```
Q5 Viswanadh 2019112011
.include TSMC_180nm.txt
.param SUPPLY=1.8
.option scale=0.09u
.global gnd vdd

Vdd vdd gnd 'SUPPLY'
.option scale=0.09u
```

```
M1000 orio orin vdd inverter_1[0]w_n8_n5# CMOSP w=25 l=2
+  ad=125 pd=60 as=250 ps=120
M1001 orio orin gnd Gnd CMOSN w=10 l=2
+  ad=50 pd=30 as=50 ps=30
M1002 inverter_0[2]in orio vdd inverter_1[1]w_n8_n5# CMOSP w=25 l=2
+  ad=125 pd=60 as=250 ps=120
M1003 inverter_0[2]in orio gnd Gnd CMOSN w=10 l=2
+  ad=50 pd=30 as=50 ps=30
```

*
*
*

```
C362 gnd Gnd 0.11fF
C363 vdd Gnd 0.06fF
C364 orio Gnd 0.21fF
C365 inverter_1[1]w_n8_n5# Gnd 2.21fF
C366 gnd Gnd 0.11fF
C367 vdd Gnd 0.06fF
C368 inverter_1[0]w_n8_n5# Gnd 2.21fF
```

I got around ~350 capacitances

```
.tran 0.1ns 20n
.ic v(orin) = 1.8V

.measure tran tperiod
+ TRIG v(orin) VAL='SUPPLY/2' RISE=1
+ TARG v(orin) VAL='SUPPLY/2' RISE=2

.measure tran tpdr
+ TRIG v(orin) VAL='SUPPLY/2' FALL=1
+ TARG v(orio) VAL='SUPPLY/2' RISE=1

.measure tran tpdf
+ TRIG v(orin) VAL='SUPPLY/2' RISE=1
+ TARG v(orio) VAL='SUPPLY/2' FALL=1

.measure tran tpd param='(tpdr+tpdf)/2' goal=0

.control
run
plot orin orio
.endc
```

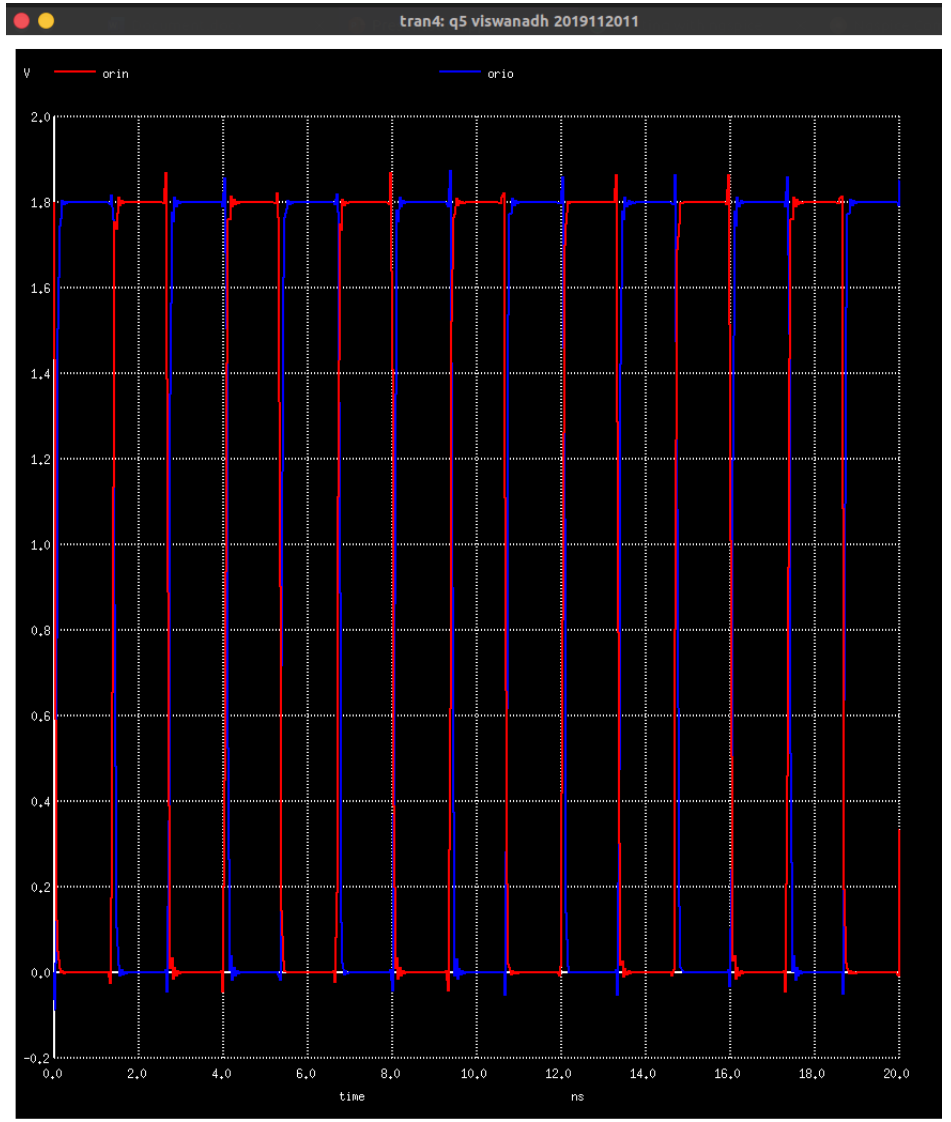
PLOTS

Plot of V_A vs time and V_B vs time where A (orin) and B (orio) are two terminals of an inverter.

X-axis: time(in S) Y-axis: Voltage(in V)

---- V_A

---- V_B



```
  Measurements for Transient Analys

tperiod                =  2.662498e-09
tpdr                   =  4.013288e-11
tpdf                   =  4.662410e-11
tpd                    =  4.33785e-11
```

Here we can note that TPD = $4.33 * 10^{-11}$ while $F_{RO} = 1/t_{period} = 1/(2.6624 * 10^{-9})$.Here I defined Time period as the time between two rising edges. We can note that

$$F_{RO} = 1/62\tau_D$$

is approximately satisfied with the values obtained.

Part D)

	Propagation delay (T_D in nS)	Time period (T_{period} in nS)	2*31*delay (in nS)
Pre-layout	0.041	2.607	2.542
Post-layout	0.0433	2.66	2.6846

We can observe difference in Delays and time periods between Pre and Post layouts as parasitic capacitances are excluded in the Pre layout while they are included in the Post layout hence giving higher timings for delay and time period.