VLSI Design : Assignment-1

Each question has sections like Netlist, Plot, Tables , Explanations .

Codes are uploaded here for reference

Question 1: No report for this Question.

Question 2: Plot I D vs V GS for NMOS transistor and estimate its V T from the graph for the following cases :

(a) V_{DS} = 50 mV and V GS is swept from 0 to 1.8 V in a step of 0.1 V

(b) V_{DS} = 1.8 V and V GS is swept from 0 to 1.8 V in a step of 0.1 V

(c) Do you observe any difference in V T values in case (a) and (b) ? If yes, explain why.

Netlist:

A)

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 'SUPPLY'
VDS D gnd 0.05

M1 D G gnd gnd CMOSN W={width_N} L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.dc VGS 0 1.8 0.1

.control
*set hcopypscolor = 1 *White background for saving plots
*set color0=white
*set color1=black

run

let x = (-VDS#branch)
set curplottitle="id vs vgs"
plot x deriv(x)

hardcopy 2.eps (-VDS#branch)
.endc
~
```

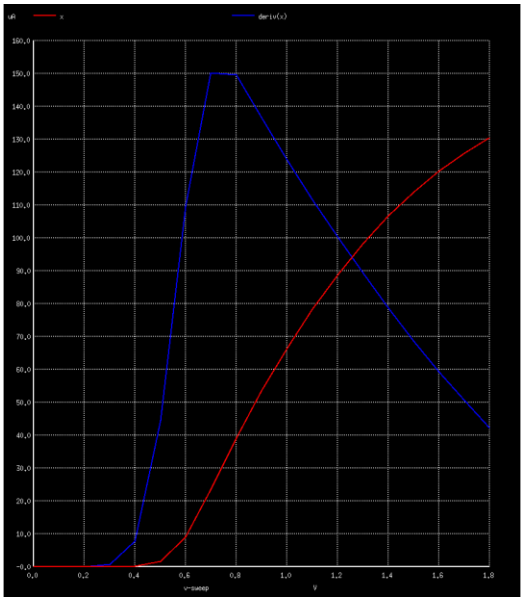
B)

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 'SUPPLY'
VDS D gnd 1.8

M1 D G gnd gnd CMOSN W={width_N} L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.dc VGS 0 1.8 0.1

.control
*set hcopypscolor = 1 *White background for saving plots
*set color0=white
*set color1=black

run

let x = (-VDS#branch)
set curplottitle="id vs vgs"
plot x deriv(x)

hardcopy 2.eps (-VDS#branch)
.endc
~
```

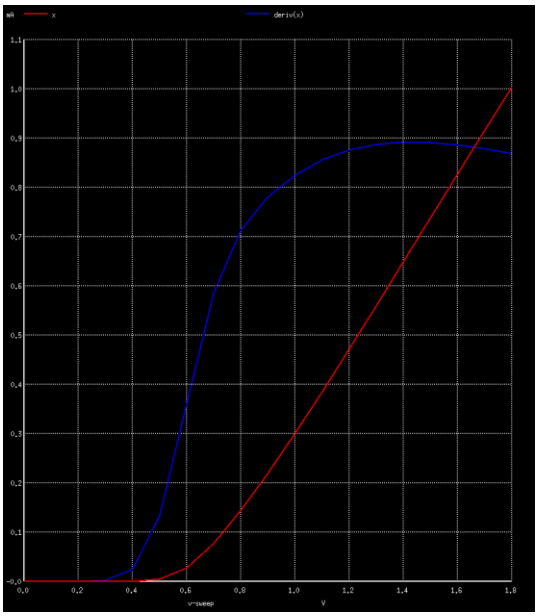
Netlists for both subparts are same except for $\mathbf{V_{DS}}$ values. This code uses the snippet given in the tutorial for an n- MOSFET. Deriv(x) returns the derivative of vector x.

Plots:

For a)



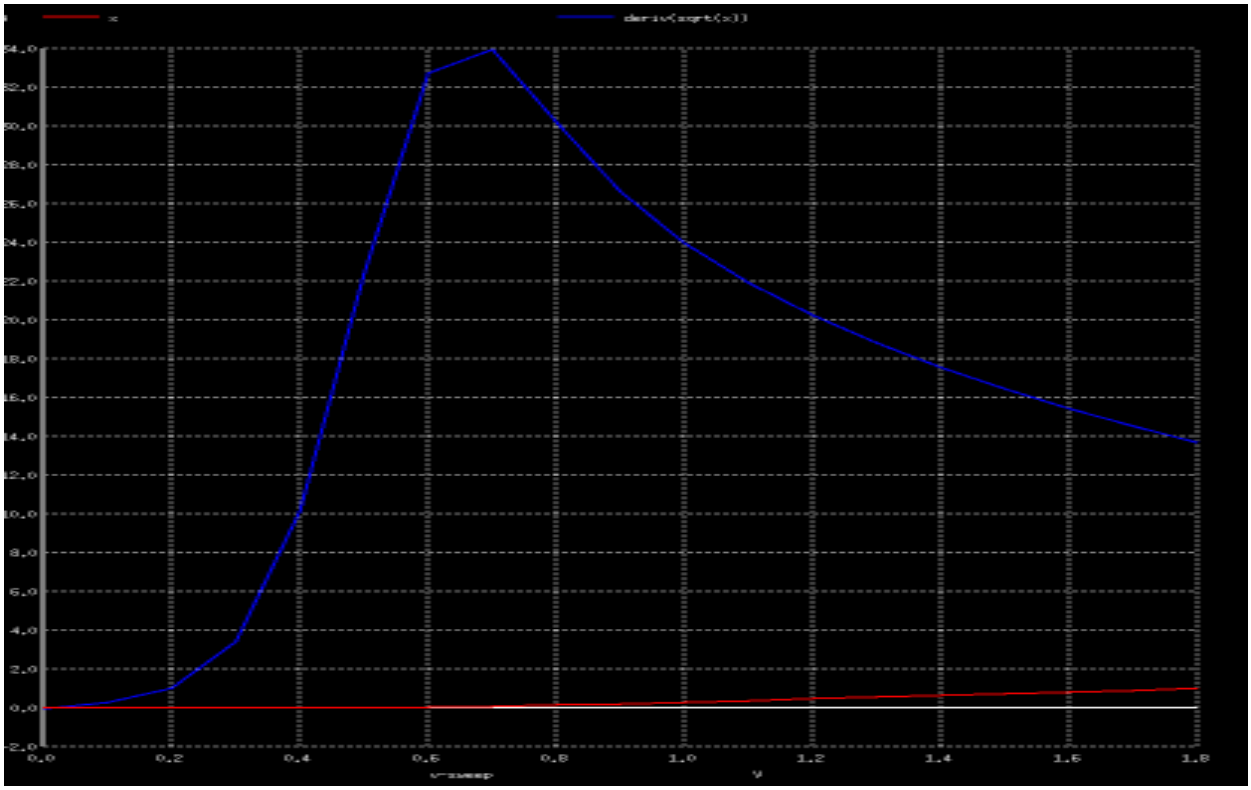
For b)



Legend: ----ID -----Derivative (ID)

X-axis: V_{GS} (V) **Y-axis:** I_D (uA)

For (b) :



Legend: ----ID -----Derivative (square root (I_D))

X-axis: V_{GS} (V) **Y-axis:** I_D (uA)

Calculations:

For 1st case, $V_{ds} = 0.05\ V$. Here we have the device in linear region. ie $I_d \propto (V_{GS} - V_{TH}) + C$

Now from the graphs, we find maximum derivative at $x_0 = 0.7\ V$. Corresponding $y_0 = 7.23 \times 10^{-5}\ A$ and slope $m = 0.0339$

now for V_{th}, $y_1 = 0$ ie $(x_1, y_1) = (V_{TH}, 0)$

now, $y_1 - y_0 = m(x_1 - x_0)$

$$\Rightarrow V_{TH} = x_0 - \frac{y_0}{m}$$

$$\Rightarrow V_{TH} = 0.7 - \frac{7.23 \times 10^{-5}}{3.39 \times 10^{-2}}$$

$$= \underline{\underline{0.697\ V}}$$

For 2nd case, $V_{ds} = 1.8\ V$. ie NMOS is in saturation region. From the graphs, maximum derivative is found sqrt (I_D) as $I_D \propto (V_{GS} - V_{TH})^2$

now, $x_0 = 0.64$, $y_0 = 4.45 \times 10^{-5}$, $m_0 = 0.034$

$$\Rightarrow \sqrt{y_0} = 0.00861$$

now $V_{TH} = x_0 - \frac{y_0}{m}$

$$= 0.64 - \frac{86.1 \times 10^{-4}}{340 \times 10^{-4}}$$

$$= \underline{\underline{0.446V}}$$

Explanations:

When V_{DS} is low (0.05V), ID is proportional to (V_{GS}-V_{TH}) + const as the device is in linear region . So we find out the linear equation governing this by finding a point (x,y) and slope m and then proceed to find V_{TH} as y =0 when x= V_{TH}.

Similarly when V_{DS} is high (1.8V) , MOS is in saturation region, hence I_D is proportional to $(V_{GS} - V_{TH})^2$.

So we consider sqrt(I) and (V_{GS} - V_{TH}) as before and proceed to find V_{TH} from linear equation.

From the above calculations we observe that values are not the same for both the cases. This can be attributed to a second order effect - Drain Induced Barrier Lowering effect. This occurs in short channel devices with high drain voltages, where Drain which is close to gate forces the transistor to turn on before than expected resulting in decrease in V_{TH} from the expected value.

Question 3) From the simple MOS models discussed in class, find out the technology parameter µC ox and V T for NMOS and PMOS devices with the help of simulations for

i) **Body to source voltage (V BS) of 0V ,**
ii) **V BS = 900mV**
iii) **V BS = −900mV .**

Do you observe any difference in V T for the three cases? Explain.

Netlist:

(For NMOS)

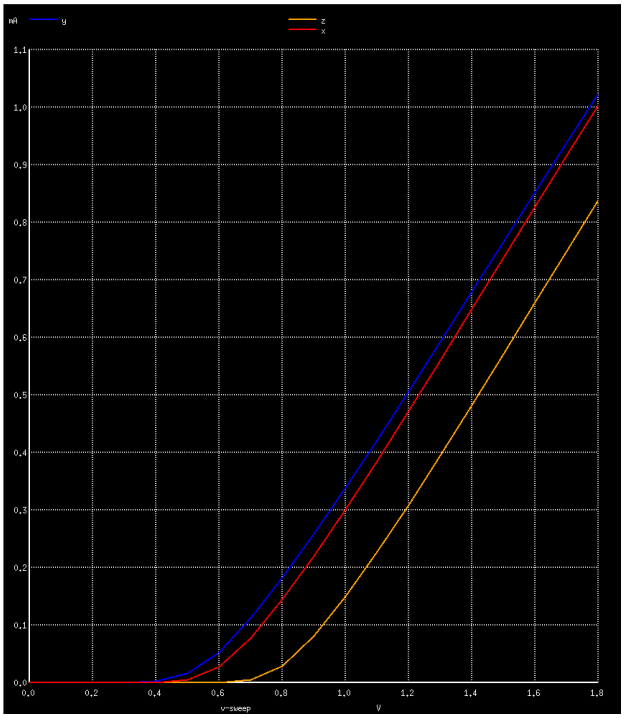
```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 'SUPPLY'
VDS D gnd 1.8
VDS1 D1 gnd 1.8 $ different Drains for each MOS
VDS2 D2 gnd 1.8
VBS1 B1 gnd 0.9
VBS2 B2 gnd -0.9

M1 D G gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_
N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2 D1 G gnd B1  CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width
_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M3 D2 G gnd B2 CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_
N*LAMBDA} PD={10*LAMBDA+2*width_N}

.dc VGS 0 1.8 0.1

.control

run

let x = (-VDS#branch)
let Y = (-VDS1#branch)
let z = (-VDS2#branch)
print  x y z
set curplottitle="id vs vgs"
plot x Y z

hardcopy 3_n.eps (-VDS#branch)
.endc
```

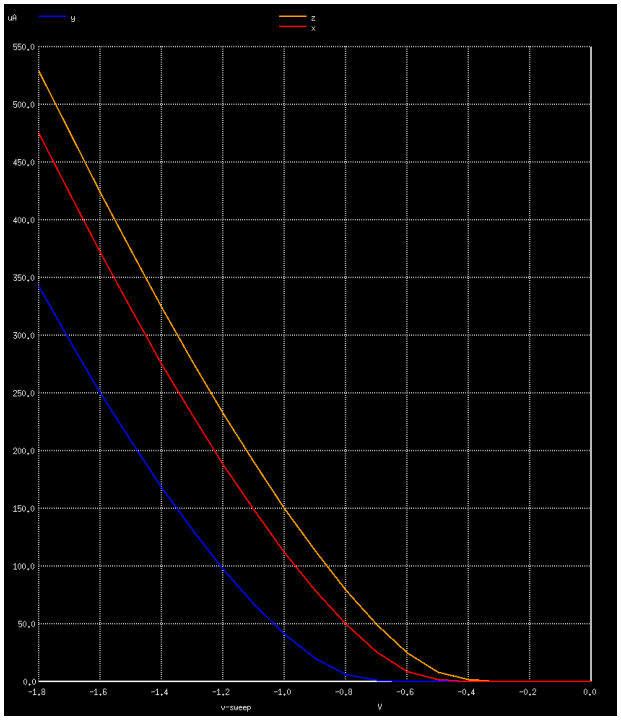
(For PMOS)

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY= -1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA} $ PMOS
.global gnd vdd

VGS G gnd 'SUPPLY'
VDS D gnd -1.8
VDS1 D1 gnd -1.8 $different Drains for each MOS
VDS2 D2 gnd -1.8
VBS1 B1 gnd 0.9
VBS2 B2 gnd -0.9

M1 gnd G D gnd CMOSP W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_
N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2 gnd G D1 B1  CMOSP W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width
_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M3 gnd G D2 B2 CMOSP W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_
N*LAMBDA} PD={10*LAMBDA+2*width_N}

.dc VGS -1.8 0 0.1

.control
run

let x = (VDS#branch)
let Y = (VDS1#branch)
let z = (VDS2#branch)
print  x y z
set curplottitle="id vs vgs"
plot x Y z

hardcopy 3_p.eps (-VDS#branch)
.endc
```

Plots:

(For NMOS) (For PMOS)





Legend : ----(V_{BS}=0) ----(V_{BS}=0.9V) ----(V_{BS}=-0.9V)

X-Axis: V_{GS} (in V) **Y-Axis** = I_{DS} (mA and uA)

Explanations:

For finding V_{TH} in the above plots, we follow the approach similar to the previous question. We find the linear equation and find the V_{TH} from the equation . If the device is in saturation region then we take square root of I_D_and construct the linear equation. (V_{TH} values are found below)

(I) When $V_{BS} = 0$, from the drain plots, slope is maximum at $x = 0.7V$. Here $m = 3.39 \times 10^{-2}$

The cordinates of this point is $(0.7, 0.0086) \Rightarrow (V_{GS}, \sqrt{I_D})$

now we know another point is $(V_{TH}, 0)$

$$\Rightarrow V_{TH} = x_0 - \frac{y_0}{m}$$

$$= 0.7 - \frac{0.0086}{0.039}$$

$$= 0.7 - 0.2536$$

$$= 0.4463V$$

II When $V_{BS} = 900mV$, now the graph appears shifted but the slopes almost remain same.

Here, $m = 3.36 \times 10^{-2}$ with point $(0.6, 0.0076)$

$$V_T = x_0 - \frac{y_0}{m}$$

$$= 0.6 - \frac{0.0076}{0.036}$$

$$= 0.6 - 0.211$$

$$= 0.389\ V$$

III When $V_{BS} = -900mV$, now graphs shifts to the opposite side where when V_{BS} is '+' got shifted.

Here from the plots, $\max(m) = 3.39 \times 10^{-2}$, $x_0 = 0.9V$

Corresponding $y_0 = 0.0091$

$$\text{now } V_T = x_0 - \frac{y_0}{m}$$

$$= 0.9 - \frac{0.0091}{0.0339}$$

$$= 0.9 - 0.2684$$

$$= 0.631\ V$$

Same as NMOS, we proceed to calculate V_{TH} for PMOS.

- When $V_{BS} = 0$, we get maximum slope of -0.02 {we'll get negative as V_{GS} is negative}
  now corresponding $(x_0, y_0) = (0.7, 0.0051)$
  now for finding another point $(V_{TH}, 0)$,

$$V_{TH} = -0.7 - \frac{0.0051}{-(0.02)}$$
$$= -0.7 + 0.225$$
$$= -0.445$$
$$|V_{TH}| = 0.445\,V$$

- When $V_{BS} = 900mV$, we get max slope $m = -0.02$ and correspondingly $(x_0, y_0) = (0.9, 0.0044)$

$$\text{now, } V_{TH} = -0.9 - \frac{(0.0044)}{(-0.02)}$$
$$= -0.9 + 0.22$$
$$= -0.68V$$

- When $V_{BS} = -900mV$, we get max slope at $m = -0.023$ and corresponding coordinates $(x_0 y_0) = (-0.6, 0.0051)$

$$\text{now, } V_{TH} = -0.6 - \frac{(0.0051)}{(-0.023)}$$
$$= -0.6 + 0.221$$
$$= -0.3782\,V$$

Theoretically verifying the values of V_{BS} , we know that when V_{BS} is positive , electrons are attracted towards the body leaving behind the hole pairs near the Drain-source region thereby increasing the Threshold voltage. Similarly when V_{BS} is negative, holes are attracted and electrons remain in the Drain-source region thereby easily forming the inversion region and decreasing the V_{TH} value.

Since we got the values of V_{TH}, we can find $\mu_n C_{ox}$ by selecting a point (say saturation region) and then apply the values of (x,y) = (V_{GS}, I_D) and obtained value of V_{TH} in the equation to obtain $\mu_n C_{ox}$

We have the relation:

$$I_D = 0.5\ \mu_n C_{ox} (V_{GS} - V_{TH})^2$$

Since $\mu_n C_{ox}$ is intrinsic to a MOSFET and since we are not considering second order effects in calculations , we'll calculate it for the case when NMOS($V_{BS=0}$) and is (~) **1.78×10^{-4}** and for PMOS it turns out to be **8.24×10^{-5}**

Question 4) Plot I D – V DS for the two cases shown in figures 1(a) and (b). Explain why a W/2L transistor does not behave in the same way as a series combination of two W/L transistors for small values of L.

Netlist:

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 'SUPPLY'
VDS D gnd 1.8
VJX J X 0

M1 D G J gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*
LAMBDA} PD={10*LAMBDA+2*width_N}

M2 X G gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_
N*LAMBDA} PD={10*LAMBDA+2*width_N}

M3 D G gnd gnd CMOSN W={width_N} L={2*2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*widt
h_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.dc VDS 0 1.8 0.1

.control
*set hcopypscolor = 1 *White background for saving plots
*set color0=white
*set color1=black

run

let x = VJX#branch $ series connnection
let y = -VDS#branch
set curplottitle="id vs vgs"
print x y
plot x y-x

hardcopy 4.eps (-VDS#branch)
.endc
```

It can be noted that I've used a common Drain, Gate and source for both type of circuits. Hence I've declared a redundant voltage node to get current through 1st circuit and hence subtract it with total current from Drain to get the current through the 2nd circuit arrangement,

Plots:

Legend : ----W/L + W/L ----W/2L

X-axis: V_{DS} (nS) Y-axis: I_{DS} (uA)

Explanations:

Here we have two circuits where 1st circuit has 2 MOSFETs (say M1 and M2) connected in series. And let the other MOSFET be M3 with twice the length of other MOSFETs. While running the plots, we've used transient analysis as the effect of **parasitic capacitances** play a major role and rest all factors are mostly same while comparing.

Since the length of M3 is double, its capacitances between various regions infact decrease resulting in a decrease of drain current through it. Also we should note that Drain current I_D decreases as L increases as they are inversly proportional. These factors together result in a low drain current through M3 when compared to (M1+M2).

Question 5) Consider the circuits shown in figures 2(a) and (b). Find the peak I ON and average I OF F for W= 1.8µm, W= 3.6µm, W= 18µm, W= 36µm. (Give plot snapshots and a table of I ON and I OF F for different W.) Do I ON and I OF F scale linearly with respect to W, comment.

Netlist:

(For I_{ON})

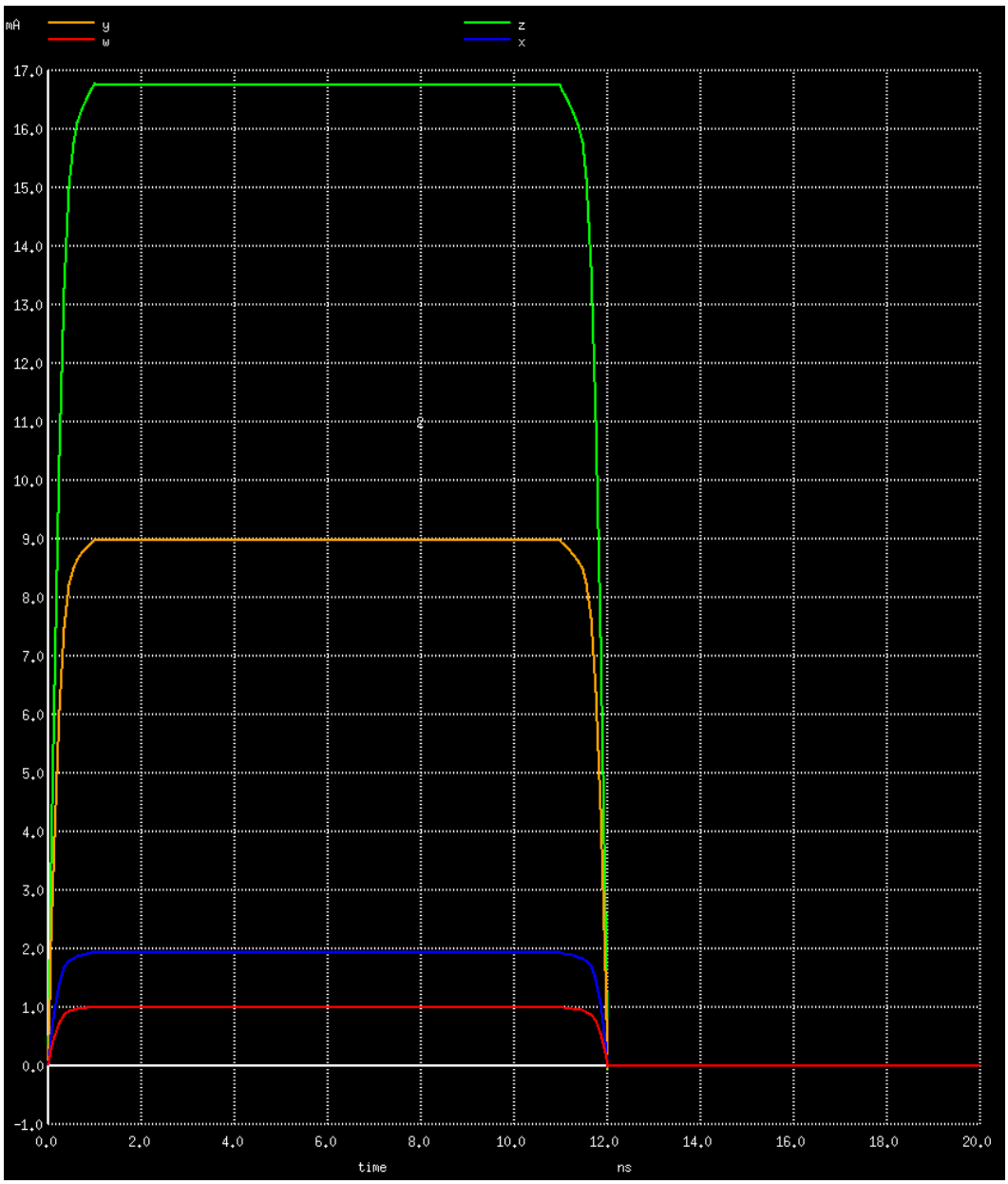
```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 1.8
VDS1 D1 gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns $ initV finalV delay rise fall half full
VDS2 D2 gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
VDS3 D3 gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
VDS4 D4 gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
*VDS D gnd 1.8

M1 D1 G gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width
_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2 D2 G gnd gnd CMOSN W={2*width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*wid
th_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M3 D3 G gnd gnd CMOSN W={10*width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*wi
dth_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4 D4 G gnd gnd CMOSN W={20*width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*wi
dth_N*LAMBDA} PD={10*LAMBDA+2*width_N}

*.dc VGS 0 1.8 0.1
.tran 0.1n 20n

.control
*set hcopypscolor = 1 *White background for saving plots
*set color0=white
*set color1=black

run

let w = (-VDS1#branch)
let x = (-VDS2#branch)
let y = (-VDS3#branch)
let z = (-VDS4#branch)
set curplottitle="id vs vgs"
plot w x y z

*hardcopy fig_mos_id_vgs.eps (-VDS#branch)
.endc
```

(For I_{OFF})

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 0
VDS1 D1 gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns $ initV finalV delay rise fall half full
VDS2 D2 gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
VDS3 D3 gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
VDS4 D4 gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
*VDS D gnd 1.8

M1 D1 G gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width
_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2 D2 G gnd gnd CMOSN W={2*width_N} L={2*LAMBDA} AS={5*2*width_N*LAMBDA} PS={10*LAMBDA+2*2*width_N} AD={5
*2*width_N*LAMBDA} PD={10*LAMBDA+2*2*width_N}

M3 D3 G gnd gnd CMOSN W={10*width_N} L={2*LAMBDA} AS={5*10*width_N*LAMBDA} PS={10*LAMBDA+2*10*width_N} AD
={5*10*width_N*LAMBDA} PD={10*LAMBDA+2*10*width_N}

M4 D4 G gnd gnd CMOSN W={20*width_N} L={2*LAMBDA} AS={5*20*width_N*LAMBDA} PS={10*LAMBDA+2*20*width_N} AD
={5*20*width_N*LAMBDA} PD={10*LAMBDA+2*20*width_N}

*.dc VGS 0 1.8 0.1
.tran 0.01n 1n

.control
*set hcopypscolor = 1 *White background for saving plots
*set color0=white
*set color1=black

run

let w = (-VDS1#branch)
let x = (-VDS2#branch)
let y = (-VDS3#branch)
let z = (-VDS4#branch)
set curplottitle="id vs vgs"
plot w x y z
plot avg(w) avg(x) avg(y) avg(z)

*hardcopy fig_mos_id_vgs.eps (-VDS#branch)
.endc
```

Plots:

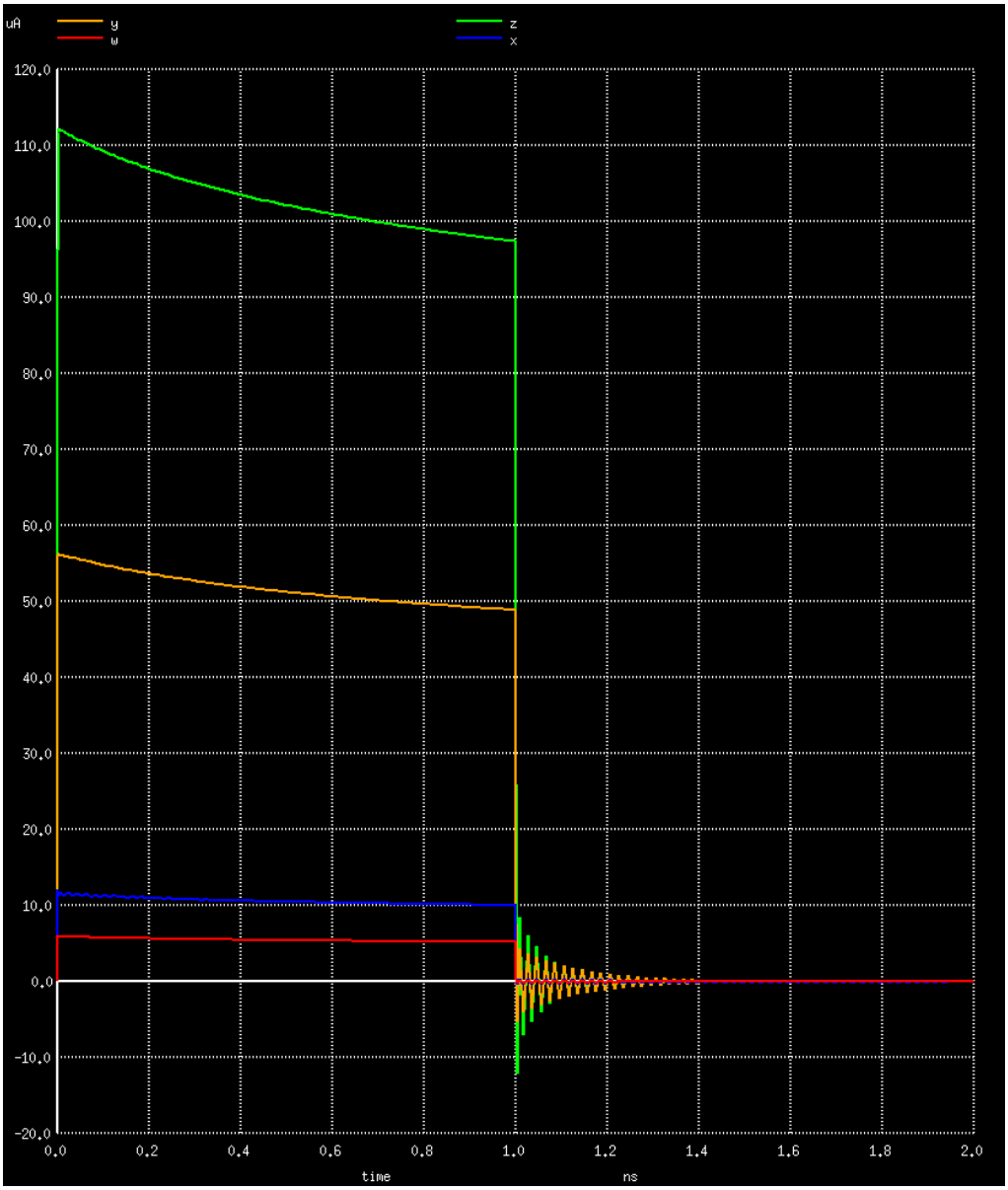
(For I_{ON})



Legend : ----W=36 ----W=18 ----W=3.6 ----W=1.8 (uM)

X-axis: time (nS) Y-axis: I_{DS} (uA)

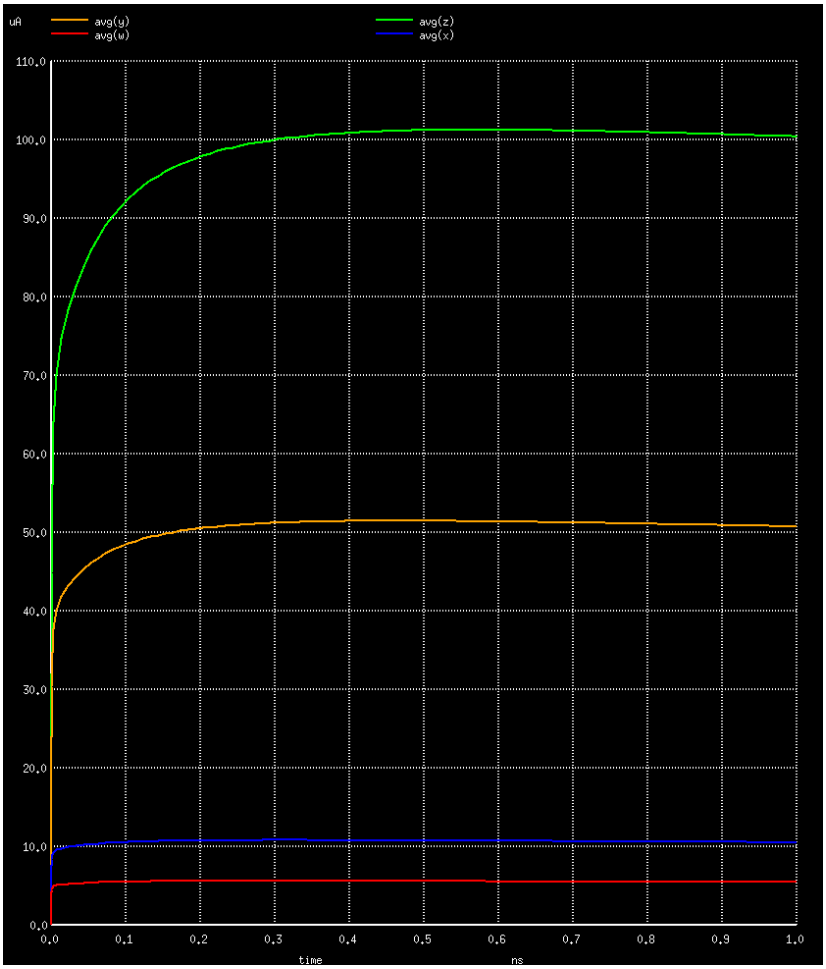
(For I_{OFF})



Legend : ----W=36 ----W=18 ----W=3.6 ----W=1.8 (uM)

X-axis: time (nS) Y-axis: I_{DS} (uA)

(I_{OFF} avg)



Legend : ----W=36 ----W=18 ----W=3.6 ----W=1.8 (uM)

X-axis: time (nS) Y-axis: I_{DS} (µA)

Table:

Width (W in µM)	Peak I_{ON} (in mA)	Average I_{OFF} (in µA)
1.8	1	5.468
3.6	1.935	10.510
18	9.003	50.729
36	16.798	100.426

Explanations:

In case of I_{ON} values, we can observe that Peak values increasing linearly (approximately) but we can notice that there's slight deviation (getting lesser values) . From the equations of drain current we get that I_{ON} should increase linearly but due to **second order effects** which effectively decreases the drain current by a bit than expected.

In case of I_{OFF} values, we can observe that average values increasing linearly but we can notice that not much deviation as observed before .

Question 6) Consider the schematic shown in figure 3. Switch 'SW' is closed at time t=0.1.8µ .

(a) Replace the switch 'SW' by an NMOS (W/L = 0.18µ) and plot v(out), when i) v c (0 –) = 0V and v(in) = 1.8V, ii) v c (0 –) = 1.8V and v(in) = 0V. Do you get exact same voltage at output as at input in steady state for both the cases. Comment for both the cases with reasons for difference (if any).

(b) Replace the switch 'SW' by an PMOS (W/L = 0.18µ) and plot v(out), when i) v c (0 –) = 0V and v(in) = 1.8V, ii) v c (0 –) = 1.8V and v(in) = 0V. Do you get exact same voltage at output as at input in steady state for both the cases. Comment for both the cases with reasons for difference (if any).

Netlist:

A) (For NMOS)

I) Vin= 1.8 and V(c⁻) = 0

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 1.8
VDS D gnd 1.8 $ VIN
VSC S C 0
C1 C gnd 0.1p
 .ic v(s) = 0 $ VOUT
M1 D G S gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*
LAMBDA} PD={10*LAMBDA+2*width_N}

*.dc VGS 0 1.8 0.1
.tran 0.1 200n
.control

run

let x = C
let y = VSC#branch
set curplottitle="id vs vgs"
plot x

*hardcopy fig_mos_id_vgs.eps (-VDS#branch)
.endc
```

II) Vin= 0V and V(c$^-$) = 1.8V

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 0.45
VDS D gnd 0 $ VIN
VSC S C 0
C1 C gnd 0.1p
 .ic v(s) = 1.8 $ VOUT
M1 D G S gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*
LAMBDA} PD={10*LAMBDA+2*width_N}

*.dc VGS 0 1.8 0.1
.tran 0.1 200n
.control

run

let x = C
let y = VSC#branch
set curplottitle="id vs vgs"
plot x

*hardcopy fig_mos_id_vgs.eps (-VDS#branch)
.endc
```

B) For PMOS

I) **Vin= 1.8 and V(c$^-$) = 0**

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA} $PMOS
.global gnd vdd

VGS G gnd 0
VDS S gnd 1.8 $ VIN
VSC D C 0
C1 C gnd 0.1p  $ VOUT
 .ic v(d) = 0
M1 D G S S CMOSP W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LA
MBDA} PD={10*LAMBDA+2*width_N}

*.dc VGS 0 1.8 0.1
.tran 0.1 100n
.control
*set hcopypscolor = 1 *White background for saving plots
*set color0=white
*set color1=black

run

let x = C
let y = VSC#branch
set curplottitle="id vs vgs"
plot x

*hardcopy fig_mos_id_vgs.eps (-VDS#branch)
.endc
```

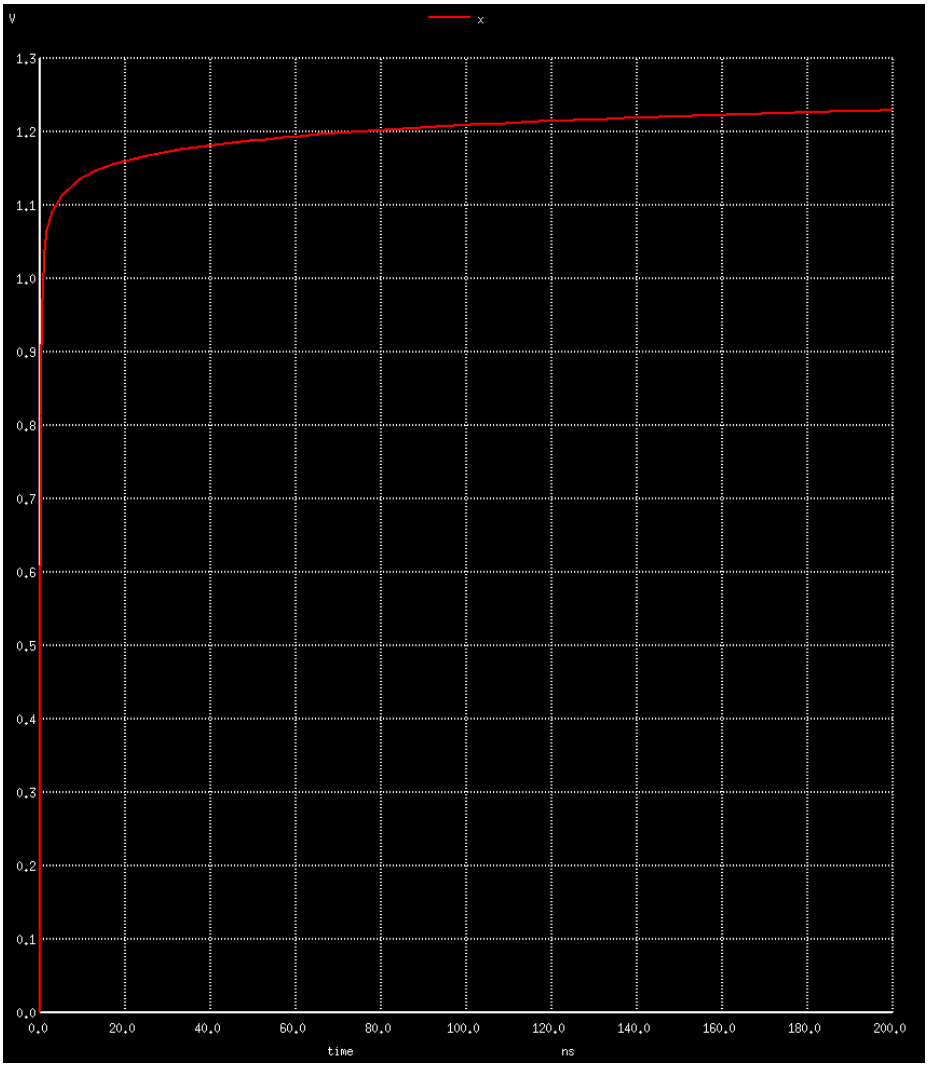
II) **Vin= 0V and V(c^-) = 1.8V**

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA} $PMOS
.global gnd vdd

VGS G gnd 0
VDS S gnd 0 $ VIN
VSC D C 0
C1 C gnd 0.1p  $ VOUT
 .ic v(d) = 1.8
M1 D G S S CMOSP W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LA
MBDA} PD={10*LAMBDA+2*width_N}

*.dc VGS 0 1.8 0.1
.tran 0.1 100n
.control
*set hcopypscolor = 1 *White background for saving plots
*set color0=white
*set color1=black

run

let x = C
let y = VSC#branch
set curplottitle="id vs vgs"
plot x

*hardcopy fig_mos_id_vgs.eps (-VDS#branch)
.endc
```

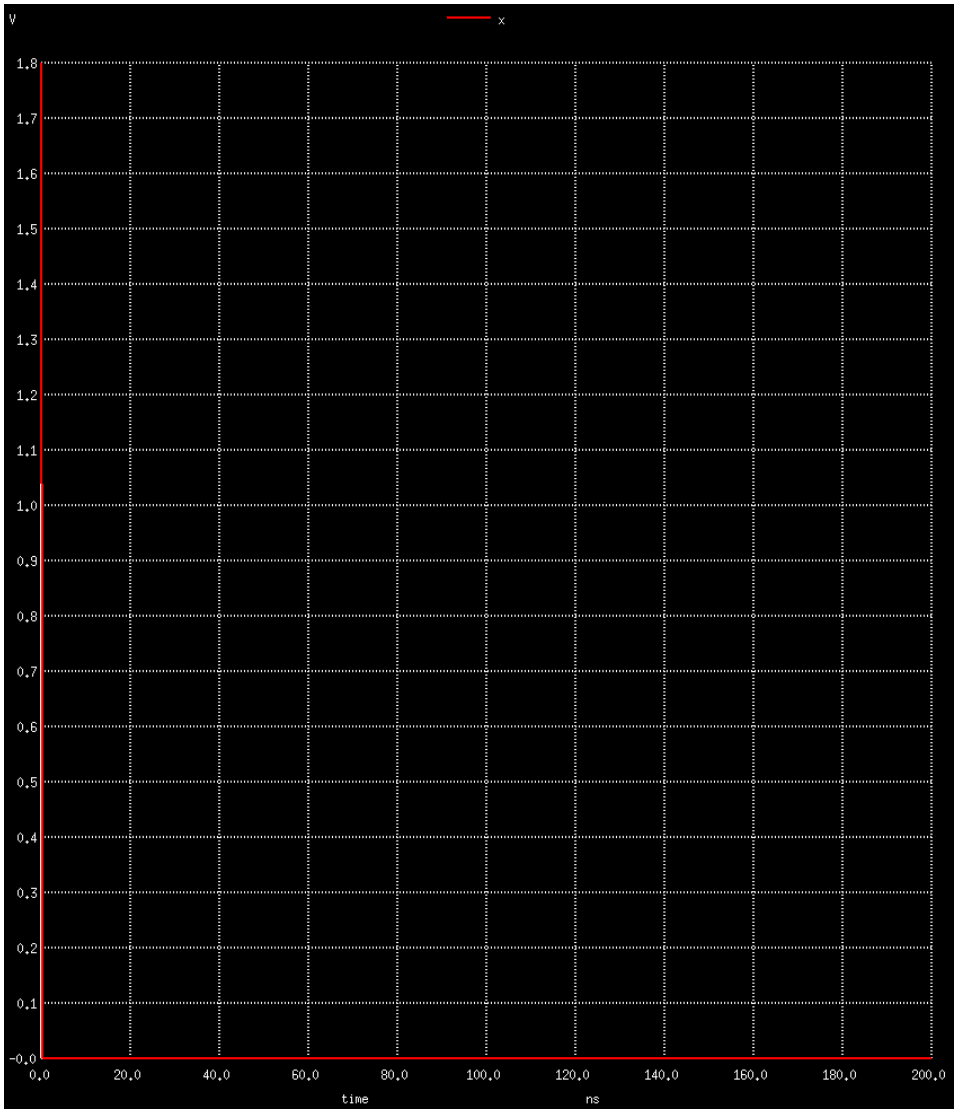
Plots:

A) For NMOS

I) Vin= 1.8 and V(c-) = 0

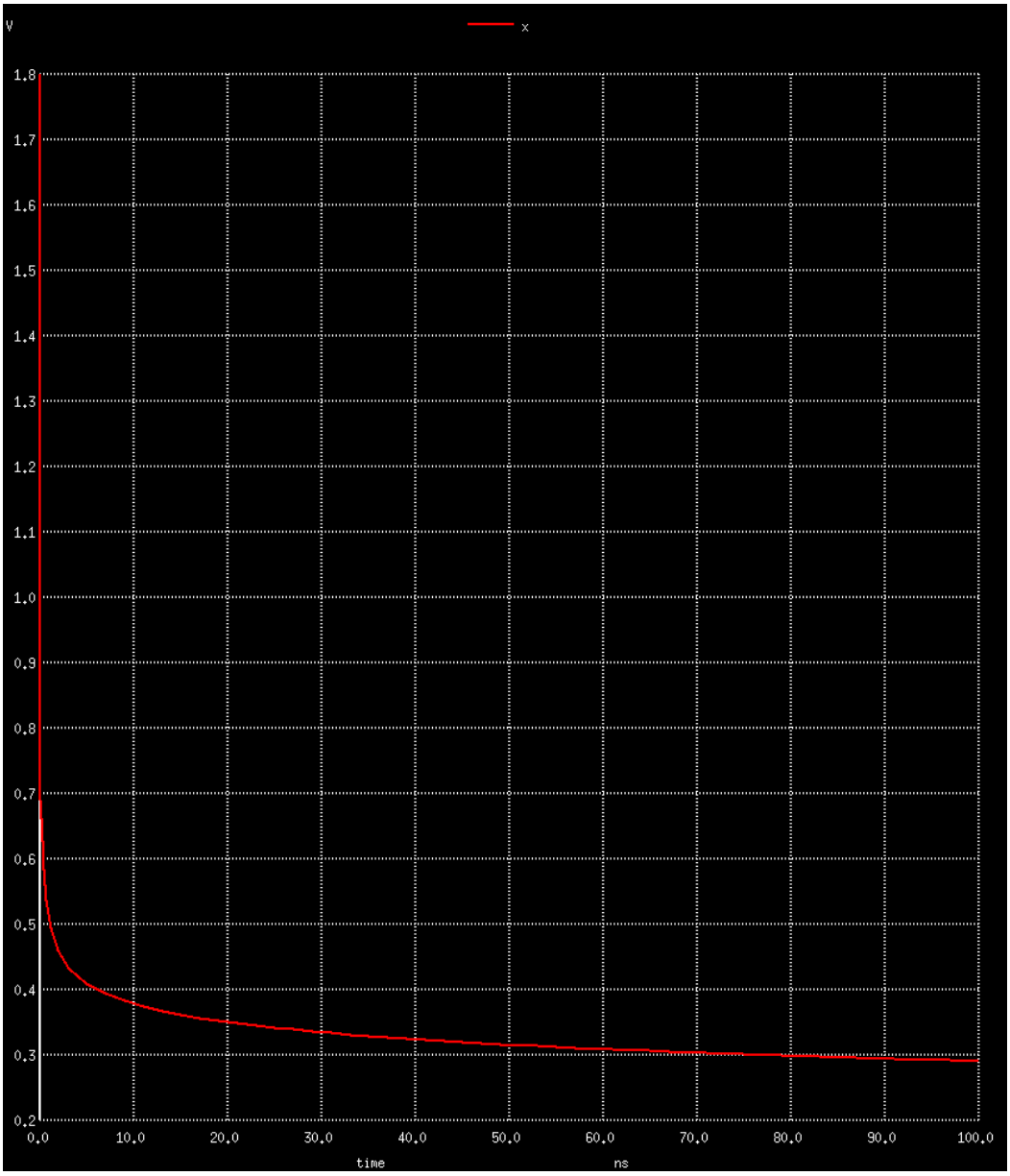


II) Vin= 0 and V(c-) = 1.8V

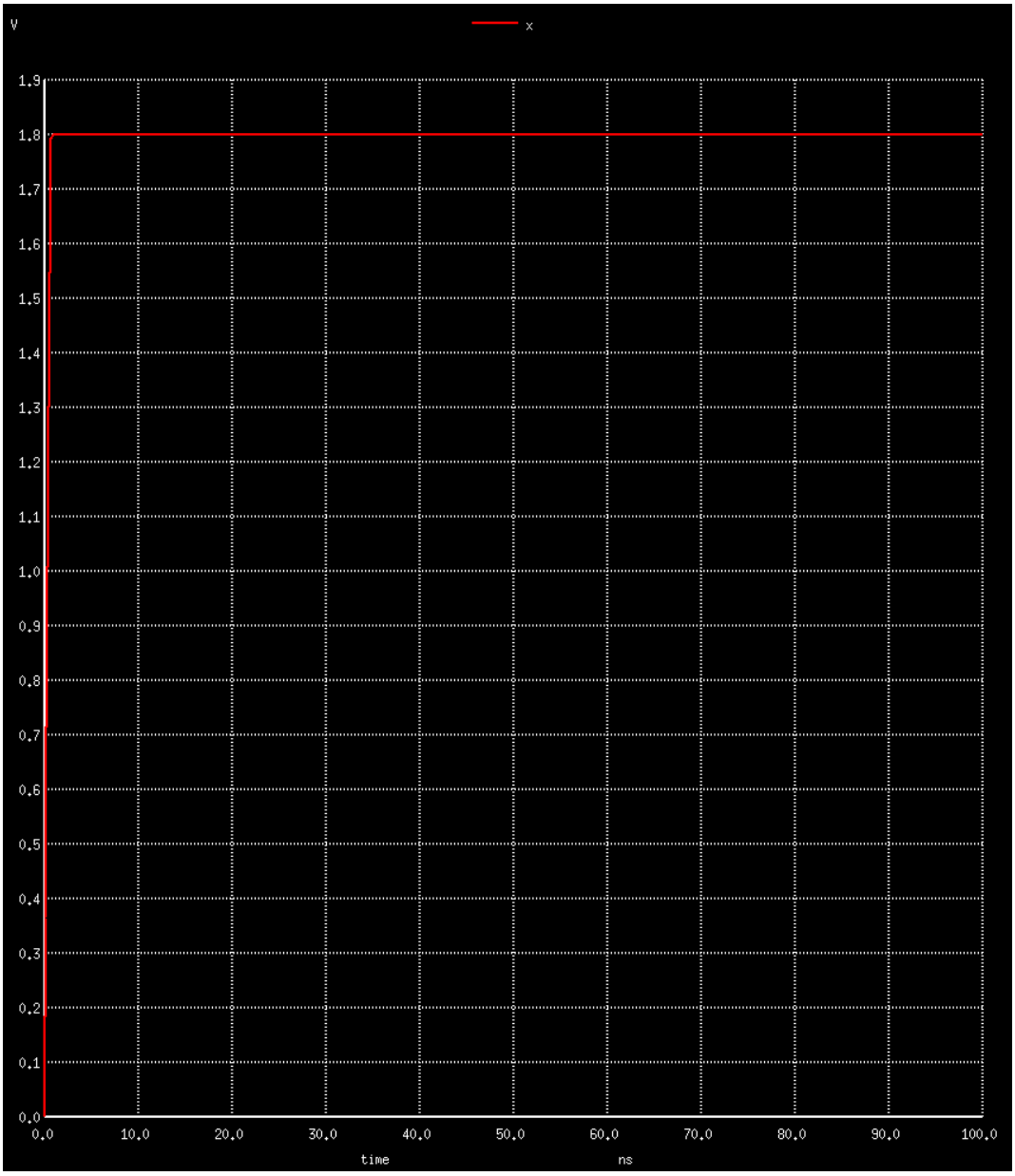


B) For PMOS

I) Vin= 0 and V(c-) = 1.8



I) Vin= 1.8 and V(c-) = 0



Explanations:

We were interchanging Vin and V(c^-) voltages between 0 and 1.8 volts. Firstly the charging/discharging times changes with our capacitance values, so we wouldn't be discussing of the timings but we would consider a reference time period (200 and 100ns) for our observations. Since we are studying voltages on a capacitor, we'll be using transient analysis.

Also since we are using MOSFET as a switch, we connect the Drain-source terminals accordingly to the VIN and V(c-) pins, while V_{GS} can be controlled accordingly to allow/not allow the currents. In my circuits I could find a threshold value for the switch turning on/ off and its 0.45V(~).

So switch remains open for V_{GS} <0.45V and gets closed for V_{GS} > 0.45V.

For the NMOS plots, we could see that the capacitor doesn't charge upto 1.8 V but discharges to 0V in given time period (happens very well before the time period). This also can be attributed to the fact that NMOS are PDN (Pull-down network).This is the reason NMOS is only used to getting a logical LOW (0V) at output in a CMOS inverter. As the capacitor gets charged, source voltage increases which in turn reduces V_{GS} pulling the MOSFET 'OFF' from 'ON' region. So gradually charging of capacitor decreases.

Now considering the PMOS plots, capacitors charges to 1.8 V instantly but doesn't discharge to absolute zero. This leads to the fact of PMOS devices being PUN (pull-up networks). So a PMOS is used to get a logical HIGH (1V) at output of a CMOS inverter. As the capacitor gets charged, source voltage increases which in turn reduces V_{GS} (increases V_{GS}) pulling the MOSFET 'ON' from 'OFF' region. So gradually charging of capacitor increases and this increase is tremendous which is visible from the graphs.

Question 7) Write a netlist for the circuit shown in figure 4. Remember to specify the AS, AD and PS, PD

parameters for the transistors. Plot V out with respect to time and calculate the propagation delay between input and output (t pd) and tabulate them for the following cases:

Given: V in (vin a 0 pulse 0 1.8 0ns 100ps 100ps 9.9ns 20ns)

(a) C L =100 fF, W n = 1.8µm W p = 2.5 × W n

(b) C L =500 fF W n = 1.8µm W p = 2.5 × W n

(c) C L =500 fF W n = 9µm W p = 2.5 × W n .

(d) From the delay table, comment how the scaling up of transistor widths affects the propagation delays.

Note: Delay = (rise-time + fall-time)/2, where rise-time is defined as the delay between rising

output and corresponding falling input when both are at their 50% values. Similarly fall-time

is defined as the delay between falling output and corresponding rising input when both are at

their 50% values.

Netlist:

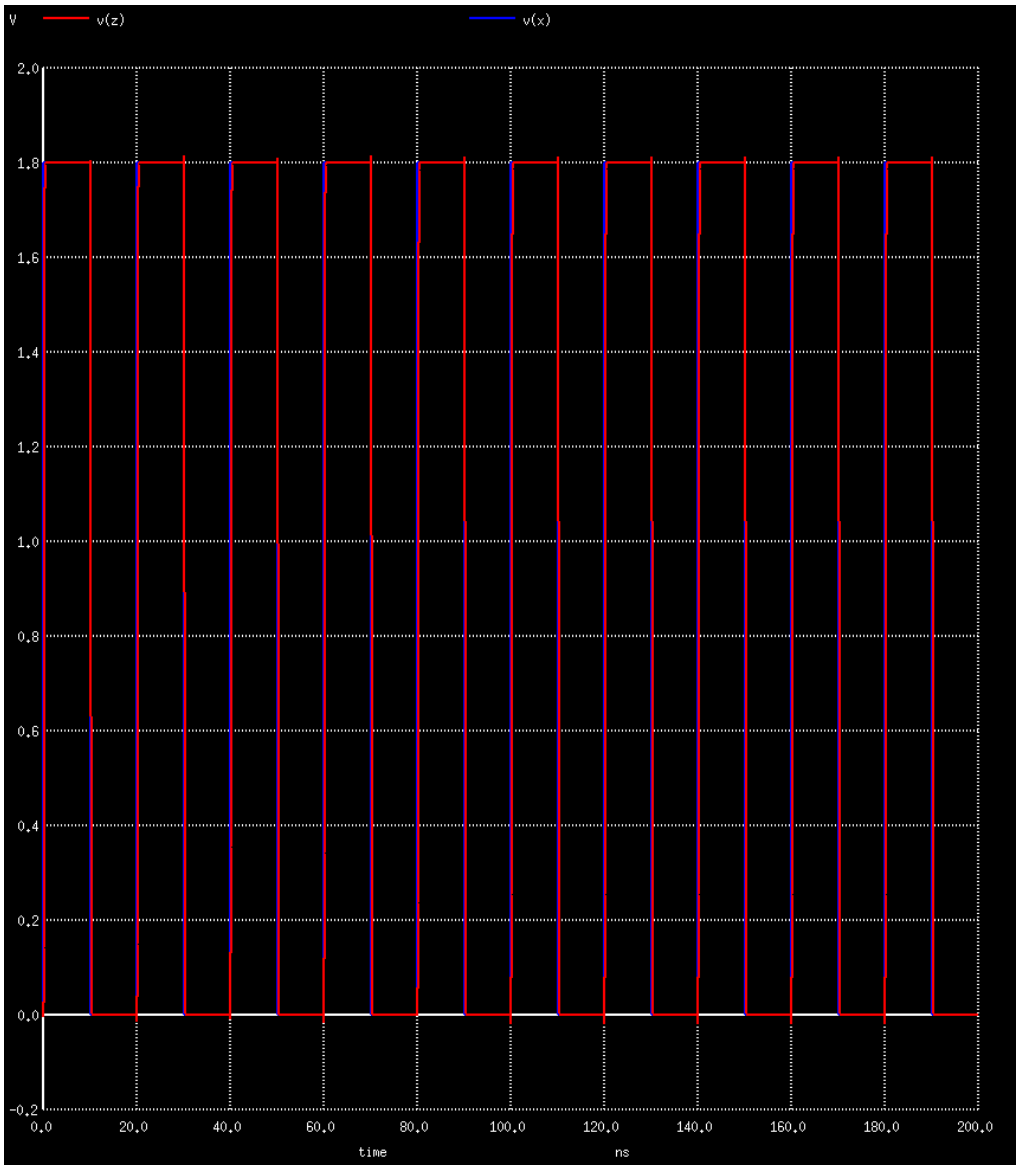
A) B) C)

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N=20*5*LAMBDA
.param width_P=50*5*LAMBDA
.global gnd vdd

VDS vdd gnd 'SUPPLY'
vin x 0 pulse 0 1.8 0ns 100ps 100ps 9.9ns 20ns

M1 y x gnd gnd  CMOSN   W={width_N}   L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*w
idth_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2 y x vdd vdd  CMOSP   W={width_P}   L={2*LAMBDA} AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*w
idth_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3 z y gnd gnd  CMOSN   W={width_N}   L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*w
idth_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4 z y vdd vdd  CMOSP   W={width_P}   L={2*LAMBDA} AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*w
idth_P*LAMBDA} PD={10*LAMBDA+2*width_P}

C1 z gnd 500f $cap

*.dc vin 0 1.8 0.1
.tran 0.1n 200n

** MEASURING DELAYS (Refer manual section 15.4.5)
.measure tran trise
+ TRIG v(z) VAL='SUPPLY/2' RISE=1
+ TARG v(x) VAL='SUPPLY/2' FALL=1
.measure tran tfall
+ TRIG v(x) VAL='SUPPLY/2' RISE=1
+ TARG v(z) VAL='SUPPLY/2' FALL=1

.measure tran tpd param='(trise+tfall)/2' goal = 0

.control
*set hcopypscolor = 1 *White background for saving plots
*set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
*set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))


run
*plot v(a)
*plot v(b)
plot  v(z) v(x)

*hardcopy fig_inv_trans.eps v(b) v(c)
.endc
```

Codes for all 3 parts are similar with just change in C , width_n and width_p values accordingly.

Plots:

A) C L =100 fF, W n = 1.8µm W p = 2.5 × W n

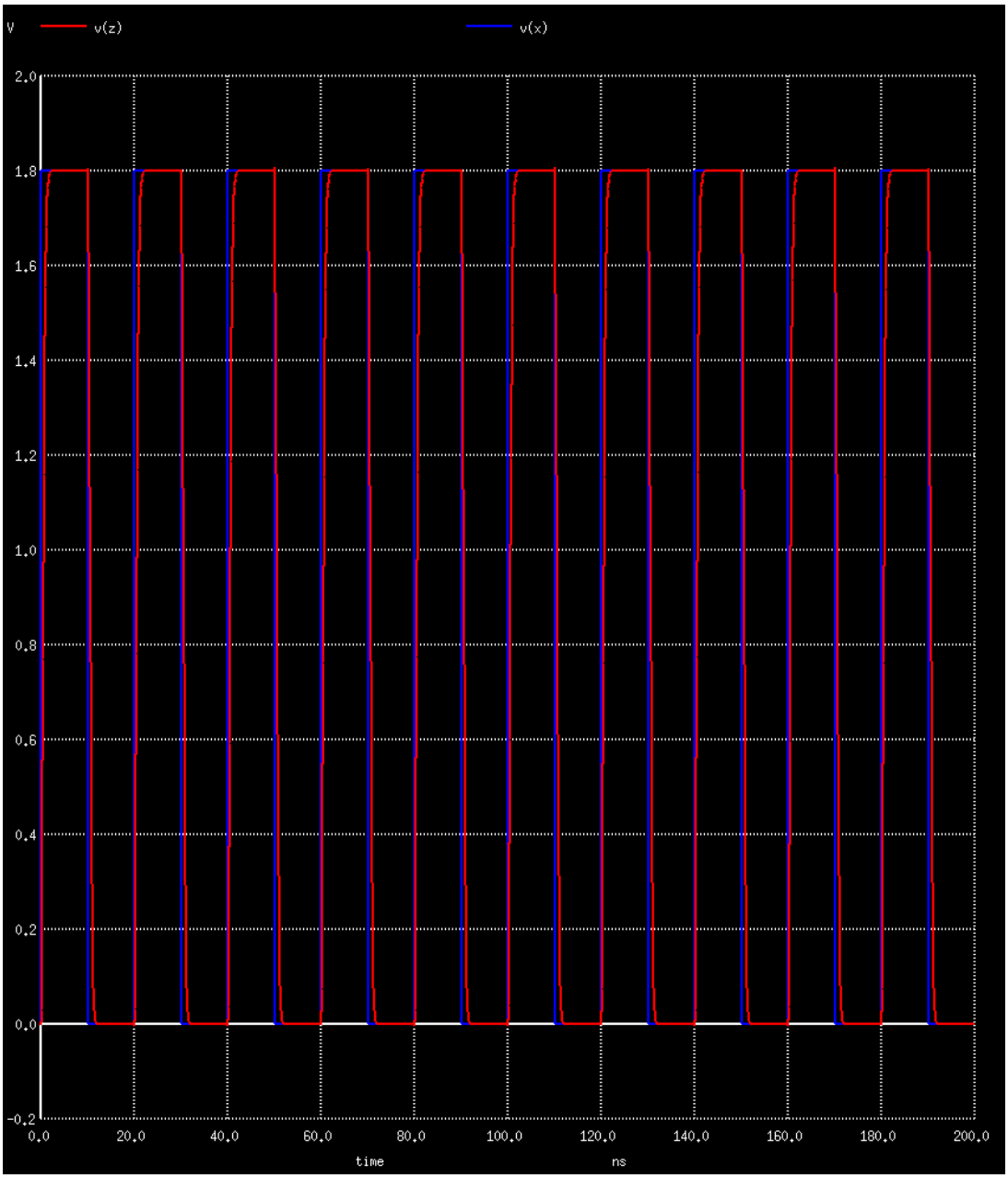


Legend:

----Input Waveform ----Output Waveform

X-Axis: time (in nS) **Y-Axis**: Output Voltage (in V)

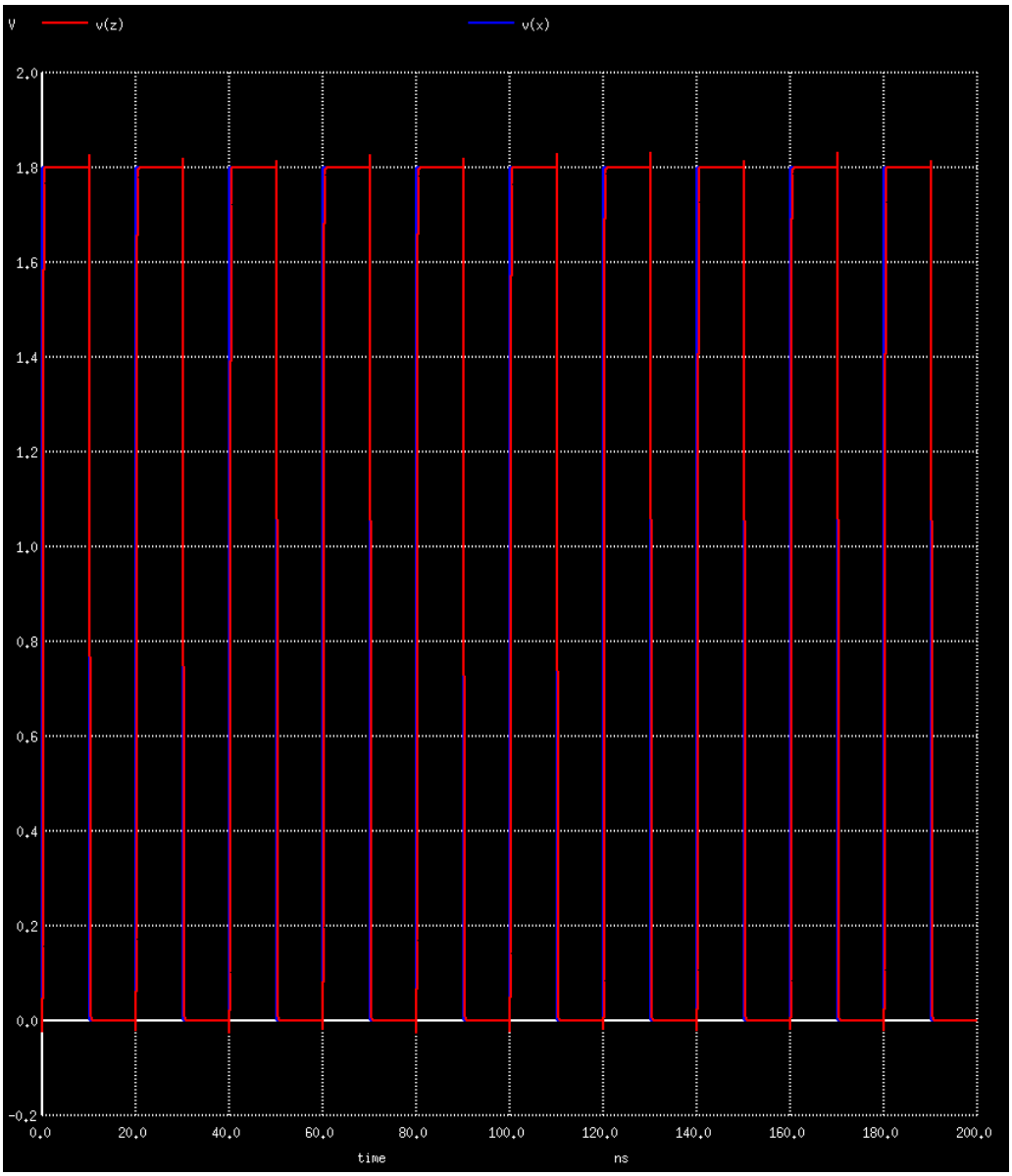
b) C L =500 fF W n = 1.8µm W p = 2.5 × W n



Legend: ----Input Waveform ----Output Waveform

X-Axis: time (in nS) **Y-Axis**: Output Voltage (in V)

c) C L =500 fF W n = 9µm W p = 2.5 × W n .



Legend: ----Input Waveform ----Output Waveform

X-Axis: time (in nS) **Y-Axis**: Output Voltage (in V)

(C(F),W_N (µM))\TIME	**T-RISE**	**T-FALL**	**T.P**
A (100,1.8)	9.843720 nS	10.16937 nS	10.0065 nS
B (500,1.8)	9.519633 nS	10.53750 nS	10.0286 nS
C (500,9)	9.832320 nS	10.18056 nS	10.0064 nS

Explanations:

Here we could observe various propagation delays as (W,L) values are changed. These changes are mainly due to following parameters:

- MOS Capacitance
- Load Capacitance

MOS Capacitance: Here MOS Capacitance (parasitic capacitances) changes as we are changing the Widths of the MOSFETs. This also causes change on delay of the input signal as capacitance changes.

LOAD Capacitance: Here LOAD Capacitance (capacitance connected as load) changes as we are directly changing it in each case. Hence the effective time Constant of the system changes thus varying the propagation delay.

So, we'll use two relations for explaining the 3 cases, I.e.

- propagation delay increases with capacitance.
- Capacitance decreases with increasing width {as area of MOSFET increases effectively decreasing capacitance}

From these relations we can say Propagation delay in B > P.D in A. But for C, it's a combined effect of increase and decrease of capacitance, and it turns out that there's decrease in capacitance which is observed from the values of table. This can be attributed to fact that capacitance decreases rapidly with increase in Width of MOSFET.