III-SEM./ETC/AE&IE/CSE/IT/MECHATRONICS/ ELECTRICAL(INST & CTRL/ECE/ 2021(W)
TH-III Digital Electronics

Full Marks: 80 Time- 3 Hrs

Answer any five Questions including Q No.1& 2
Figures in the right hand margin indicates marks

1. Answer **All** questions 2 x 10

a. State De-Morgan's theorems.

b. Convert $(10110101)_2$ from binary to grey code.

c. Find out the number of input lines, output lines and select lines in : (i)1:8 De-Mux (ii)16:1 Mux

d. Write down the truth table of half subtractor.

e. Define race-around condition in flip flop and suggest a method to overcome it.

f. Difference between combination and sequential logic circuit.(any 4)

g. Mention the type of flip flops used in : (i)Ripple Counter (ii)Shift Register

h. Write the excitation table of D-flip flop.

i. List down different types of: (i) Analog to Digital Convertors ,(ii) Digital to Analog Convertors

j. Define Fan In and Fan Out.

2. Answer **Any Six** Questions 6 x 5

a. Simplify the below given expression using Karnaugh's map and draw the logic circuit using logic gates.
$F(a, b, c, d) = \Sigma m (0,2,3,4,7,9,10,11,15) + d (1,6,8)$

b. Explain the function of 4: 1 MUX with neat diagram and truth table.

c. Design the operation of full adder with the help of truth table and circuit diagram.

d. Design a JK flip flop using a RS flip flop.

e. With neat circuit diagram, Explain the working of R-2R ladder type DAC.

f. Write any 5 differences between SRAM and DRAM.

g Draw CMOS logic circuit of NAND and NOR gates.

3 Realize all the logic gates (NOT, AND, OR, NAND, NOR, XOR, XNOR) using NAND gates only. 10

4 Design a 2-bit magnitude comparator using logic gates. 10

5 Sketch the logic diagram of clocked JK Flip - Flop. Explain its working with functional table. 10

6 Explain briefly SISO, SIPO, PISO and PIPO shift register. 10

7 Design a mod-6 synchronous up counter. 10