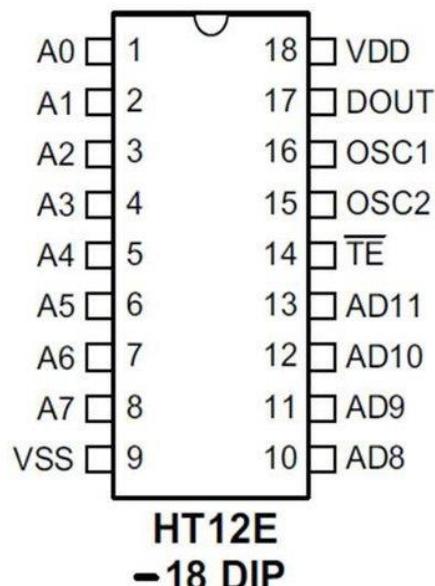


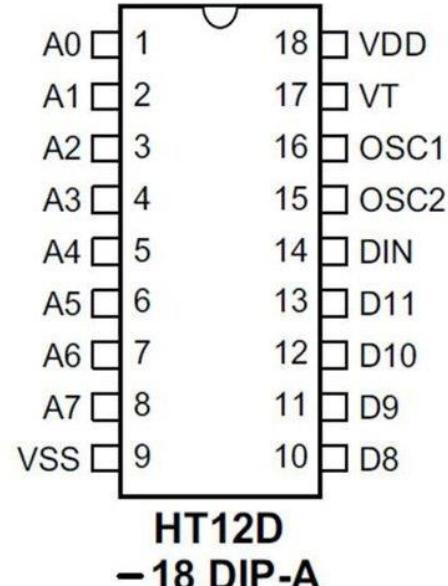
# DT12E & DT12D

**8-Address  
4-Address/Data**



**HT12E  
-18 DIP**

**8-Address  
4-Data**



**HT12D  
-18 DIP-A**

## 1. Introduction

The HT12E and HT12D are **pair of encoder and decoder ICs** used in **wireless remote-control systems**. They provide a reliable method of sending and receiving **parallel data signals** over **RF/infrared (IR) links**.

- **HT12E** → Encoder (Transmitter side)
- **HT12D** → Decoder (Receiver side)

These ICs are designed for **low-power, low-cost wireless communication** and are commonly used in **alarms, remote switches, and wireless control systems**.

## 2. HT12E Encoder IC

### 2.1 Pin Configuration

Pin	Name	Description
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1–8	A0–A7	Address pins – used to set unique address for transmission. Can be HIGH or LOW.
10–13	AD0–AD3	Data input pins – parallel inputs to encode into serial data.
14	TE (Transmit Enable)	Active LOW. When LOW, starts encoding and transmission.
15	DOUT	Serial output pin – connect to RF/IR transmitter.
16	VCC	+5V Supply
9	OSC1	Connect resistor to OSC2 to set oscillator frequency.
5	OSC2	Connect resistor to OSC1 to set oscillator frequency.
7, 6	Not Connected (NC)	Not used internally.
8	GND	Ground

## 2.2 Working Principle

1. **Data Reading:**
  - a. HT12E continuously monitors the **AD0–AD3 input pins**.
2. **Address Matching:**
  - a. HT12E combines the **AD pins** with **address pins (A0–A7)** to create a **12-bit frame**:
    - i. 8 bits → Address
    - ii. 4 bits → Data
3. **Encoding & Serial Output:**
  - a. The 12-bit frame is converted into a **serial pulse stream** (modulated HIGH/LOW) on **DOUT**.
  - b. The **transmit enable (TE)** pin must be LOW for transmission.
  - c. **Oscillator pins (OSC1/OSC2)** control the timing of the pulses.

## 2.3 Encoder Operation Flow

AD0–AD3 Inputs → Read Data

A0–A7 → Append Address

TE = LOW → Enable Transmission

Generate Serial 12-bit Frame → DOUT → RF/IR Transmitter

**Key Feature:** HT12E ensures that the **encoded frame includes address bits** to prevent interference with other transmitters.

## 3. HT12D Decoder IC

### 3.1 Pin Configuration

Pin	Name	Description
1–8	A0–A7	Address pins – must match TX HT12E address pins.
10–13	O0–O3	Data output pins – parallel output corresponding to TX AD0–AD3 pins.
14	VT (Valid Transmission)	Goes HIGH when a valid frame with correct address is received.
16	VCC	+5V Supply
15	DIN	Serial data input – connect to RF/IR receiver output.
9	OSC1	Connect resistor to OSC2 for oscillator frequency.
5	OSC2	Connect resistor to OSC1 for oscillator frequency.
6, 7	NC	Not Connected internally.
8	GND	Ground

### 3.2 Working Principle

1. **Serial Input Reception:**
  - a. HT12D receives **serial pulse stream** at **DIN** from RF or IR module.
2. **Address Verification:**
  - a. Extracts **first 8 bits** of the frame → compares with **local address pins A0–A7**.
  - b. If addresses match → proceeds; if mismatch → ignores signal.
3. **Data Decoding:**
  - a. Extracts **last 4 bits** → sets **O0–O3 outputs** HIGH or LOW depending on TX AD0–AD3 inputs.
4. **Valid Transmission (VT):**
  - a. VT pin goes HIGH → indicates valid data reception
  - b. Can trigger alarms or indicators in external circuitry
5. **Oscillator (OSC1/OSC2):**
  - a. Resistor between OSC1 & OSC2 sets the timing to decode serial data correctly.

### 3.3 Decoder Operation Flow

Serial Data from RF RX → DIN

Extract 12-bit Frame

Check Address Bits (A0–A7)

If Address Match → O0–O3 set according to data bits

VT = HIGH → Valid Transmission Indicated

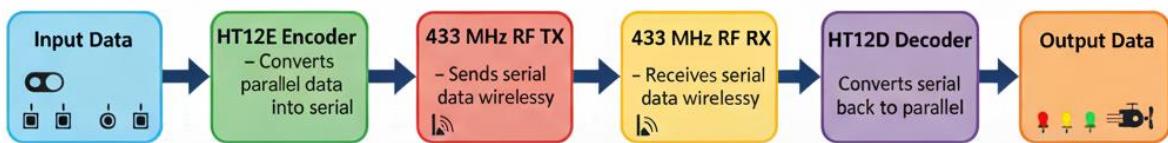
## 4. Key Features of HT12E/HT12D System

- Operates on **5V supply**
- Uses **12-bit frame**: 8-bit address + 4-bit data
- Can support **up to 16 different data signals** (with multiple ICs or pins)
- Hardware-based encoding/decoding → **no microcontroller needed**
- Provides **address matching** → avoids interference
- Easy to interface with **RF/IR modules**

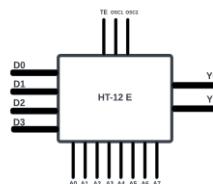
## 5. Summary

Aspect	HT12E	HT12D
Role	Encoder (TX side)	Decoder (RX side)
Input	AD0–AD3 (parallel)	DIN (serial)
Output	DOUT (serial)	O0–O3 (parallel)
Address	A0–A7 (set unique TX address)	A0–A7 (must match TX)
Additional Pin	TE → Transmit Enable	VT → Valid Transmission Indicator
Oscillator	OSC1/OSC2 (sets data rate)	OSC1/OSC2 (sets data rate)

**Operation:** HT12E converts parallel inputs into serial data for RF/IR transmission, HT12D receives the serial stream, checks address, and outputs parallel signals.



## Encoding:



### 1.1) Transmission Side (HT12E – Encoder)

- Inputs (parallel form):
- Data bits (D0–D3): In your case  $\rightarrow \{0,0,0,1\}$
- Address bits (A0–A7): In your case  $\rightarrow \{0,0,0,0,0,0,0,1\}$

- Together: 12 bits total {8 address + 4 data}.

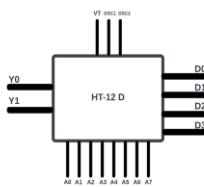
### 1.2) Encoding action:

- When TE (Transmit Enable) is pulled LOW, the HT12E starts serializing the parallel address and data.
- It adds preamble/sync pulses, so the decoder knows when valid data starts.
- Encoded sequence becomes: {0,0,0,0,0,0,0,1,0,0,0,1} which is just address + data concatenated.

### 1.3) Transmission:

- The serialized output is sent out of the DOUT pin.

## Decoding:



### 2.1) Reception Side (HT12D – Decoder)

- Signal reception: The wireless module (RF/IR receiver) captures the serial stream and gives it to DIN pin of HT12D.
- HT12D looks for the preamble and matching address.

### 2.2) Decoding action:

- HT12D extracts the 12 bits.
- Splits them into:
  - Address: {0,0,0,0,0,0,0,1}
  - Data: {0,0,0,1}

### 2.3) Validation:

- If the address matches the one hardwired at the decoder's address pins (A0–A7)  
→  
The VT (Valid Transmission) pin goes HIGH.
- Then the data bits are made available on D0–D3 outputs.

### 2.4) Output:

- Decoded data = {0,0,0,1} → same as transmitted.
- This proves lossless communication (provided address match).

