Anirudh Ramkumar

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PROFILE

With a strong inclination towards silicon chip design, developed practical skills in RTL and FPGA-based System design. Areas of interest include digital VLSI design, computer architecture and embedded processing using FPGAs. Passionate about lifelong learning and innovate with in-depth understanding and develop solutions in the evolving VLSI landscape.

EDUCATION

PSG College of Technology, Coimbatore, India *Oct 2022 – May 2026(Expected)*
Bachelor of Engineering – Electronics and Communication, CGPA: 9.46/10
Courses: Computer Architecture, FPGA-based System Design, System Level Verification Methodologies, Analog VLSI Circuits, Computer Networks

EXPERIENCE

Project Intern – Aviat Networks *May 2025 – Oct 2025(Expected)*
- Working on Port and MAC VLAN based Layer 2 Ethernet switching using Zynq Ultrascale+ MPSoC
- Evaluating performance of ARM Cortex-R5 core for maximum throughput

ACADEMIC PROJECTS

WALLACE TREE MULTIPLIER *[Cadence Virtuoso]*
Implemented 4-bit Wallace tree multiplier in Virtuoso. Calculated delay, power and PDP metrics for different adder architectures (24T and 28T) and supply voltage (1.125V to 1.8V). Analyzed the trade-off between delay and power with respect to supply voltage reduction.

SINGLE STAGE RISC-V CORE *[MakerChip IDE]*
Built a single-stage 32-bit RISC-V core using Transaction-Level Verilog (TL-Verilog), supporting the complete RV32I instruction set. Verified core functionality using an assembly program to compute the sum of the first 9 natural numbers.

DESIGN AND VERIFICATION OF 4-BIT ADDER/SUBTRACTOR *[EDA Playground]*
Implemented a structural-level design of 4-bit Adder/Subtractor in Verilog; Developed a layered SystemVerilog testbench for functional verification against golden reference using EDA Playground.

ROBOTIC SORTING ARM *[Shakti SDK][FPGA Hackathon]*
Developed a Shakti C-Class RISC processor based robotic sorting arm on the Nexys Video FPGA board, designed to classify objects based on colour. Implemented a colour detection algorithm for identification of red, yellow and blue using APDS9960 color sensor.

CONVOLUTIONAL ENCODER *[Xilinx Vivado]*
Designed a (2,1,2) Convolutional Encoder using Mealy FSM with binary state encoding. Simulated and verified the encoder's functionality in Verilog with a custom testbench.

COMPARATIVE STUDY OF CURRENT MIRRORS *[Cadence Virtuoso]*
Implemented simple, source-degenerated, cascode and Wilson current mirror using Cadence Virtuoso. Obtained and analyzed the output resistance and I-V characteristics of the current mirrors. Studied the relation between output current and aspect ratio of the respective transistor.

RSTP IMPLEMENTATION *[Cisco Packet Tracer]*

Implemented Rapid Spanning Tree Protocol in Cisco packet tracer for a ring topology consisting of four switches. Tested the protocol implementation in three different cases: Change of priority, failure of link between designated ports, and addition of switch.

SKILLS

Languages: Python, C, MATLAB
HDLs: Verilog, SystemVerilog (basics)
Tools: Vivado, Vitis, Cadence Virtuoso, EDA Playground
Hardware platform: FPGAs (Artix, Zynq 7000, Zynq Ultrascale+ MPSoC), Microcontrollers (ESP8266, Arduino UNO, 8051), Raspberry Pi
Spoken language: English, Tamil

ACTIVITIES AND ACHIEVEMENTS

- Attended a two-day course on System Level Verification Techniques and Methodologies conducted by Qualcomm and PSG College of Technology.
- Attended a two day course on Embedded processing with FPGAs conducted by NIELIT and PSG College of Technology.
- Completed – Verification Part 1: Fundamentals of SystemVerilog offered by Namaste FPGA.
- Finalist – SHAKTI FPGA Hackathon organized by Shakra Innovations and IIT Madras as part of DIR-V.
- GATE 2025 – AIR 2724.
- Third place – Mathematics Olympiad 2023 organized by PSG College of Technology.