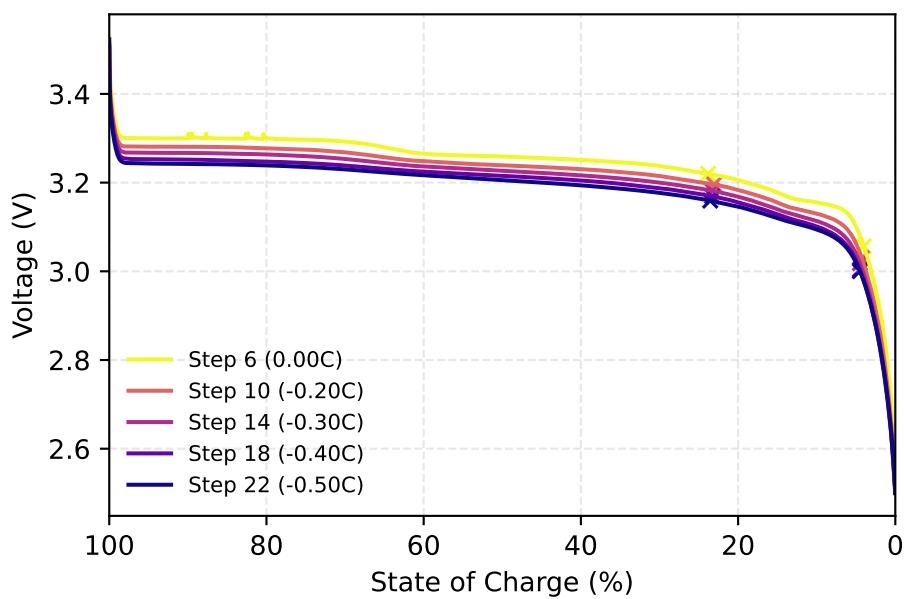
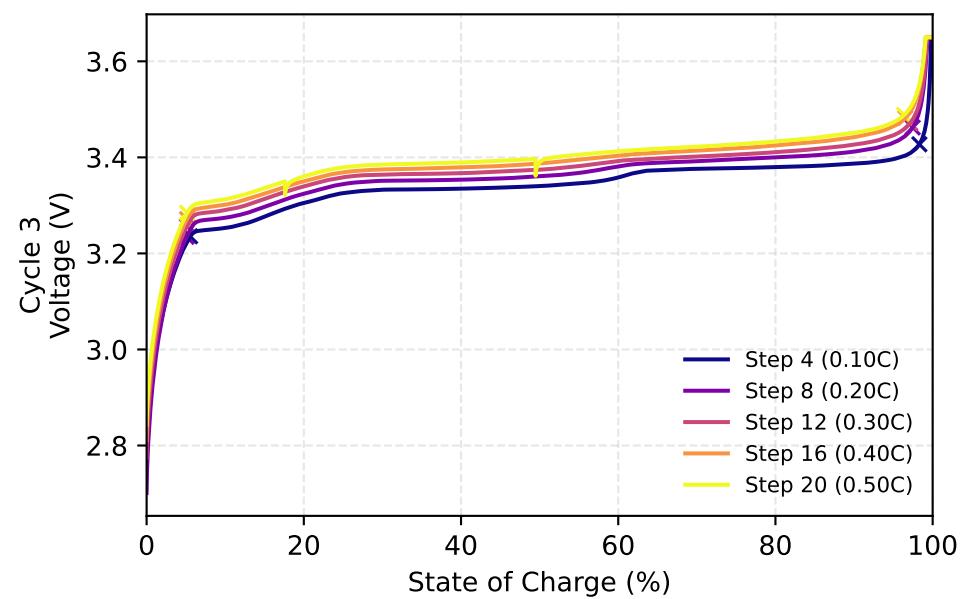
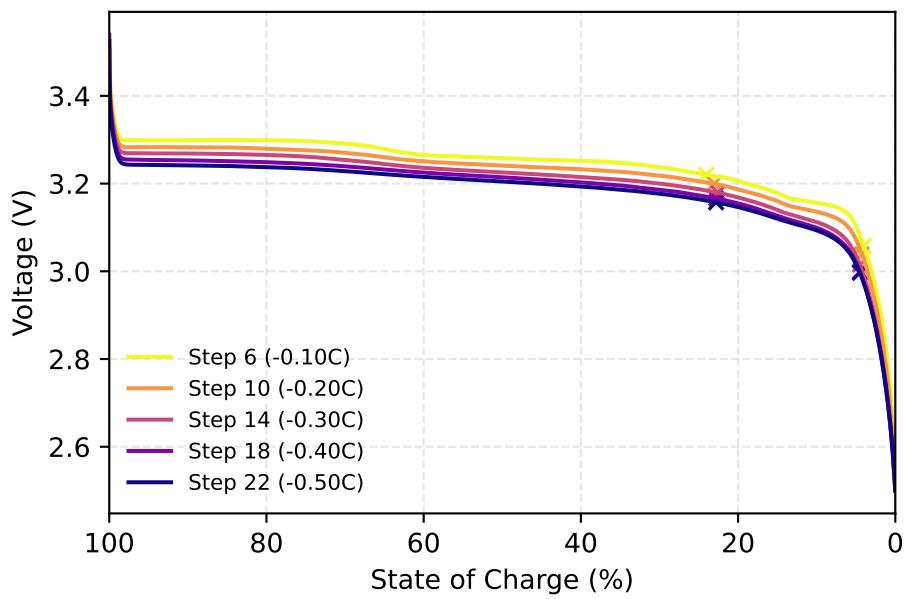
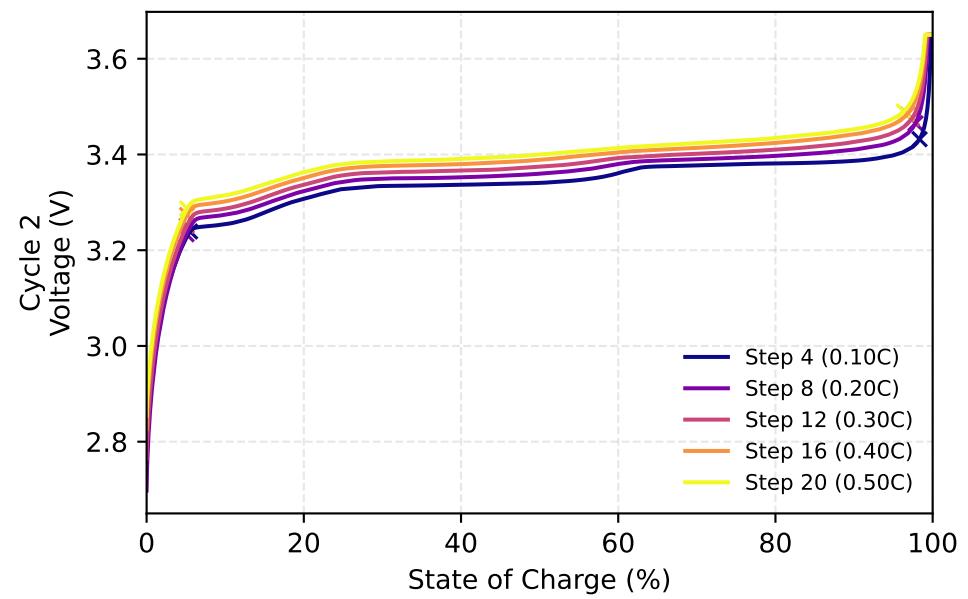
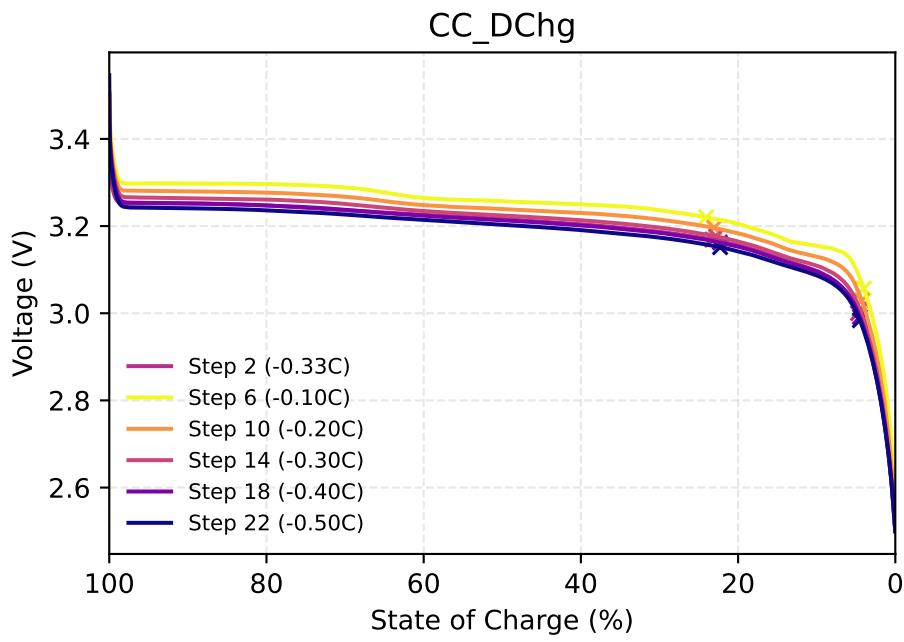
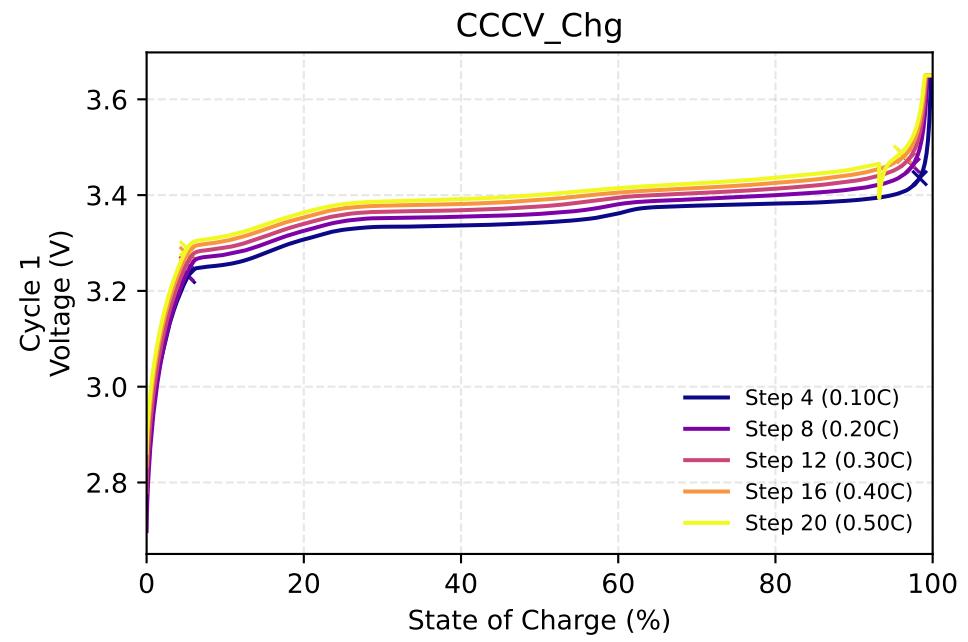
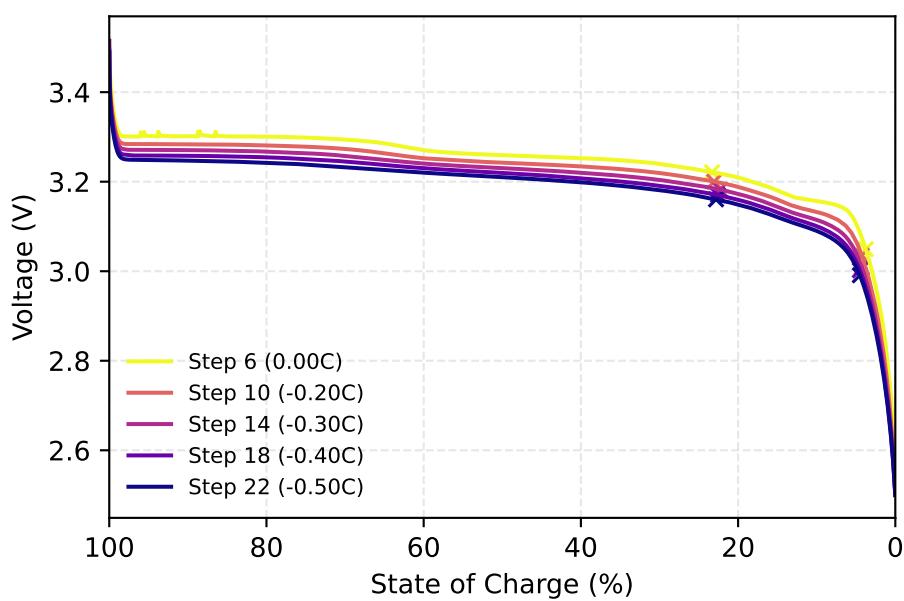
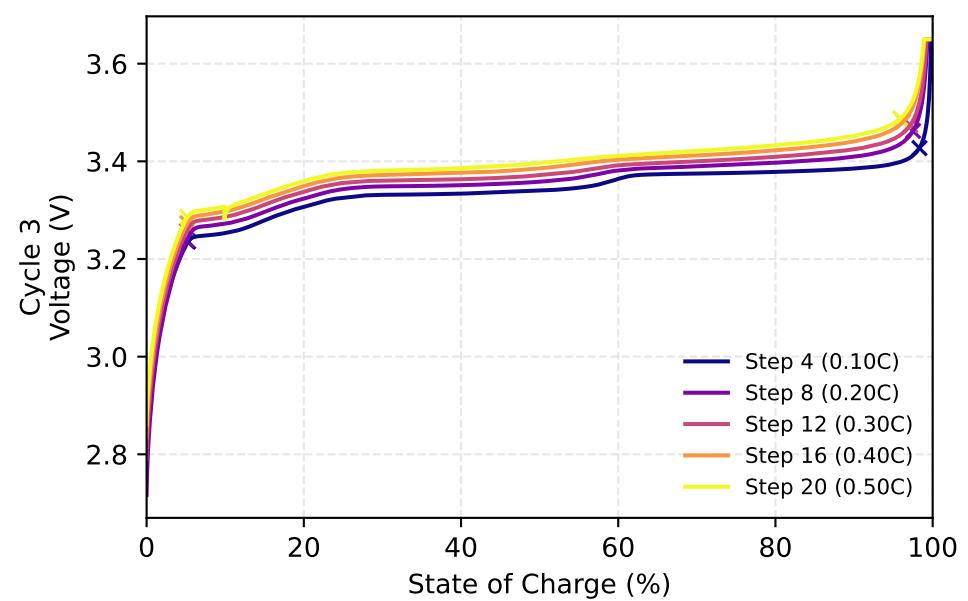
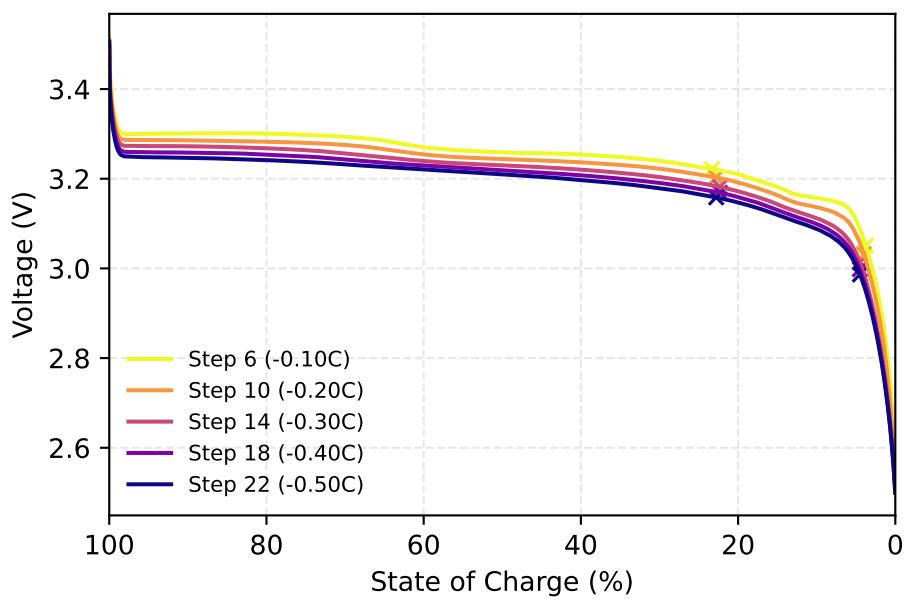
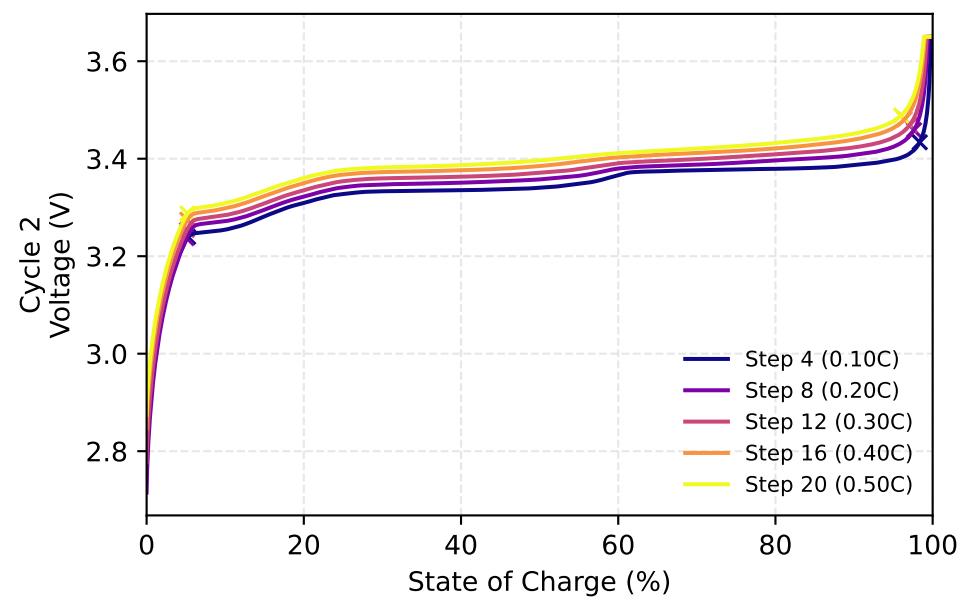
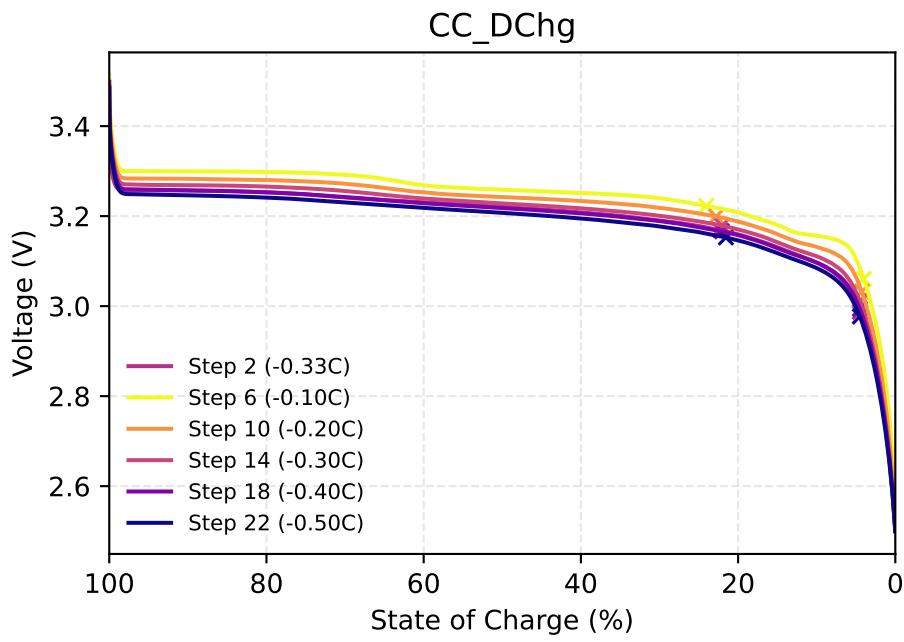
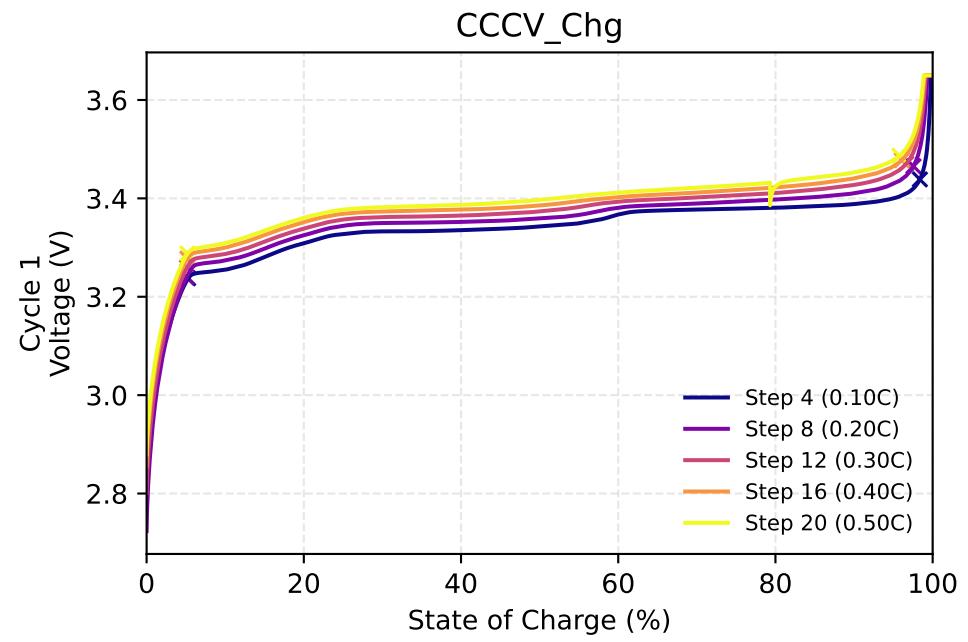


RD_RateCapability_0001 - SoC-V by Cycle and Step Name

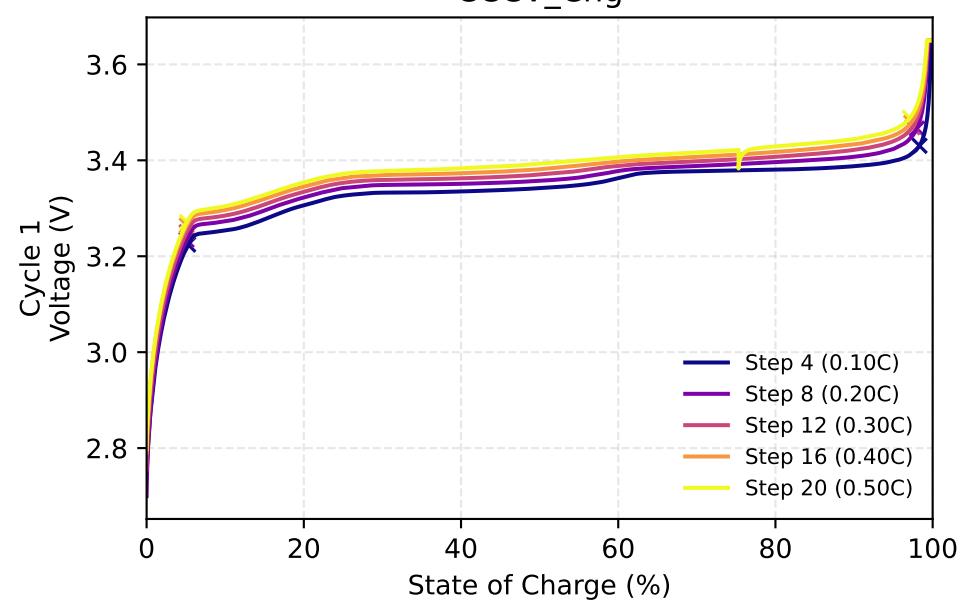


RD_RateCapability_0003 - SoC-V by Cycle and Step Name

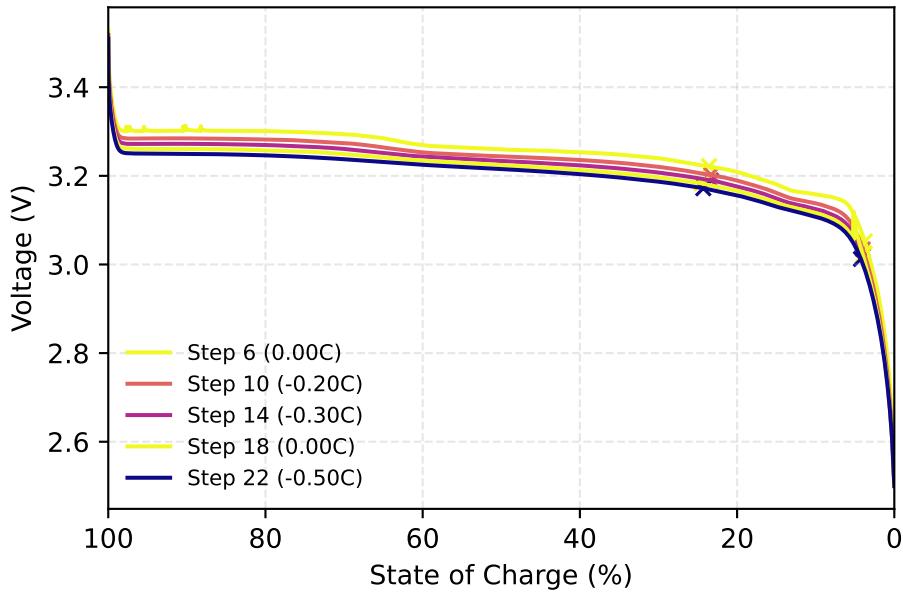
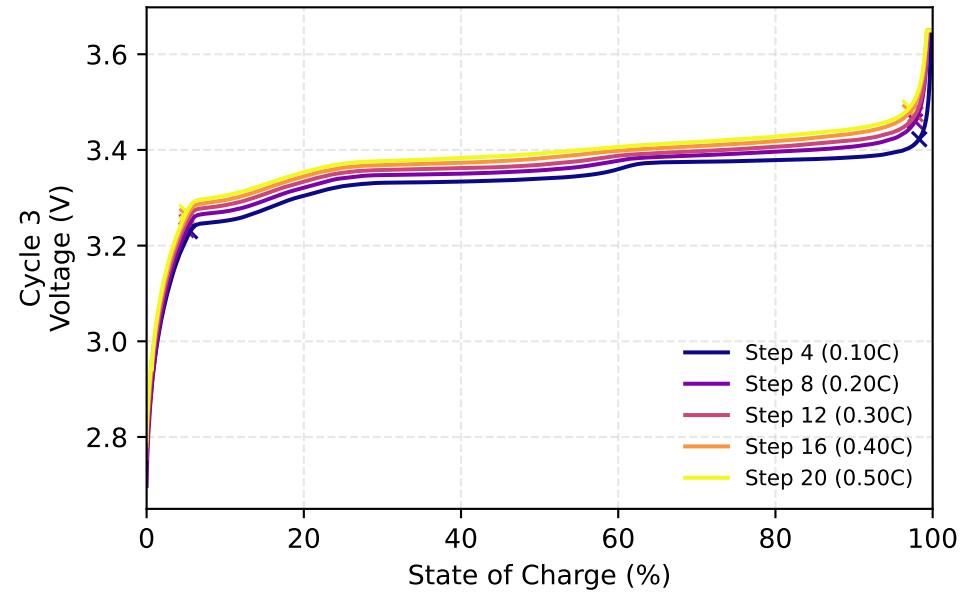
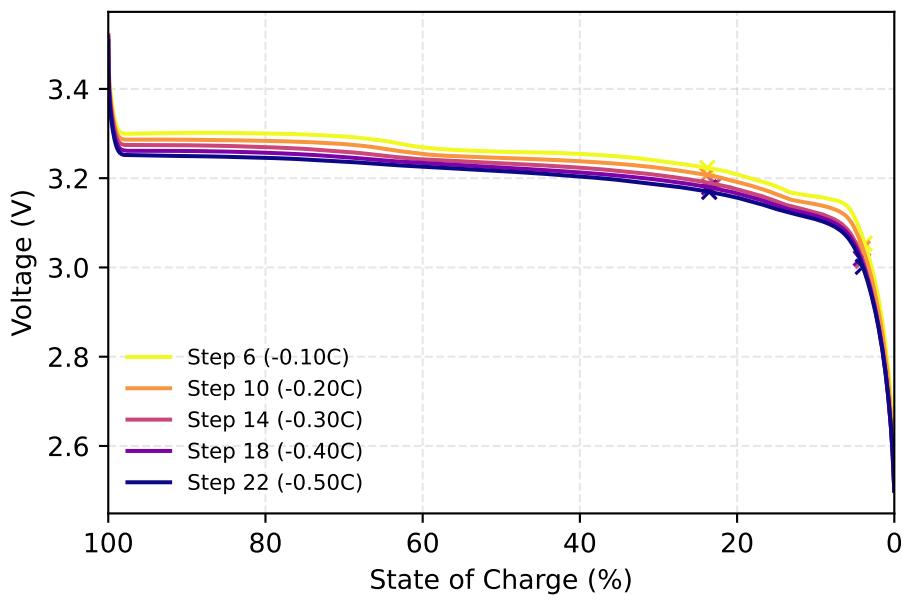
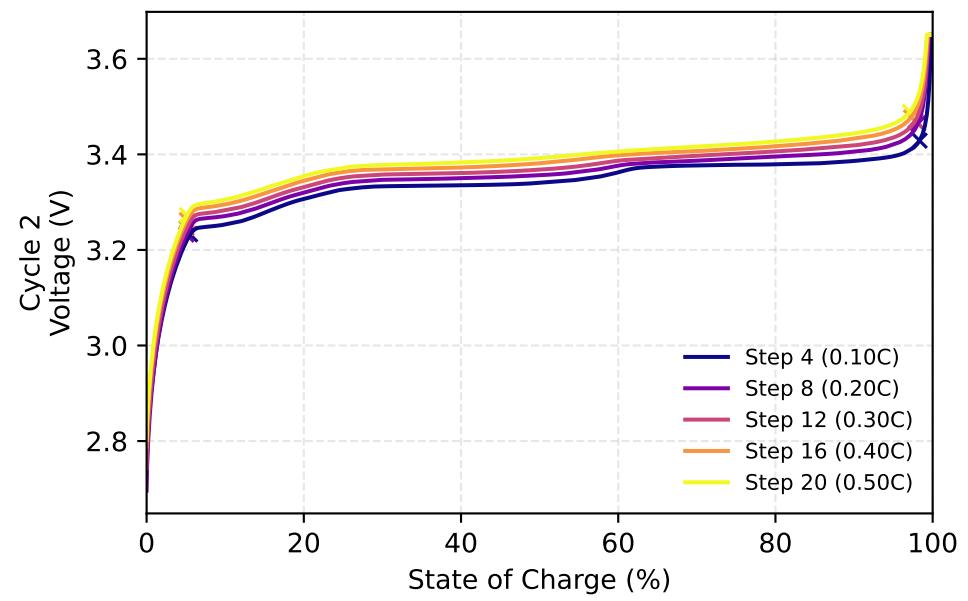
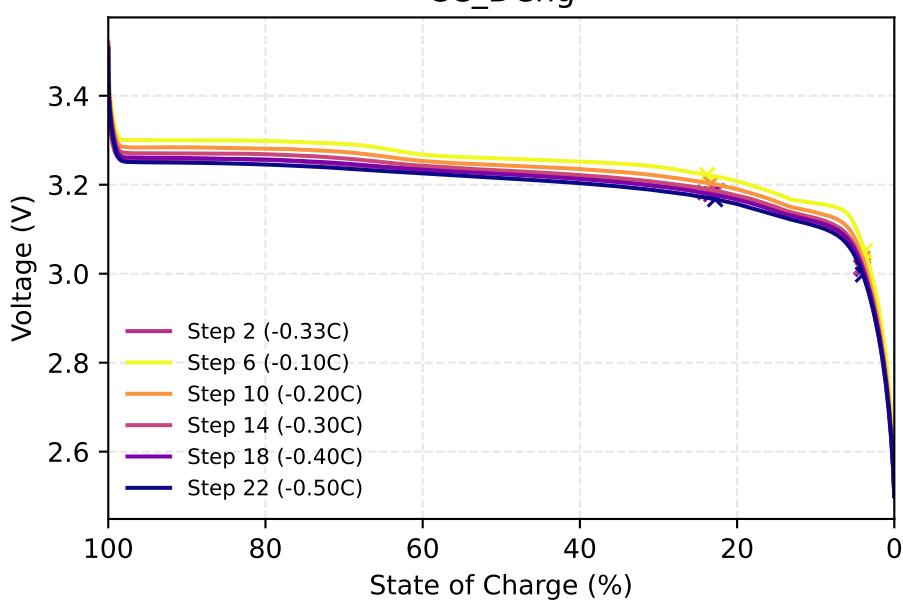


RD_RateCapability_0004 - SoC-V by Cycle and Step Name

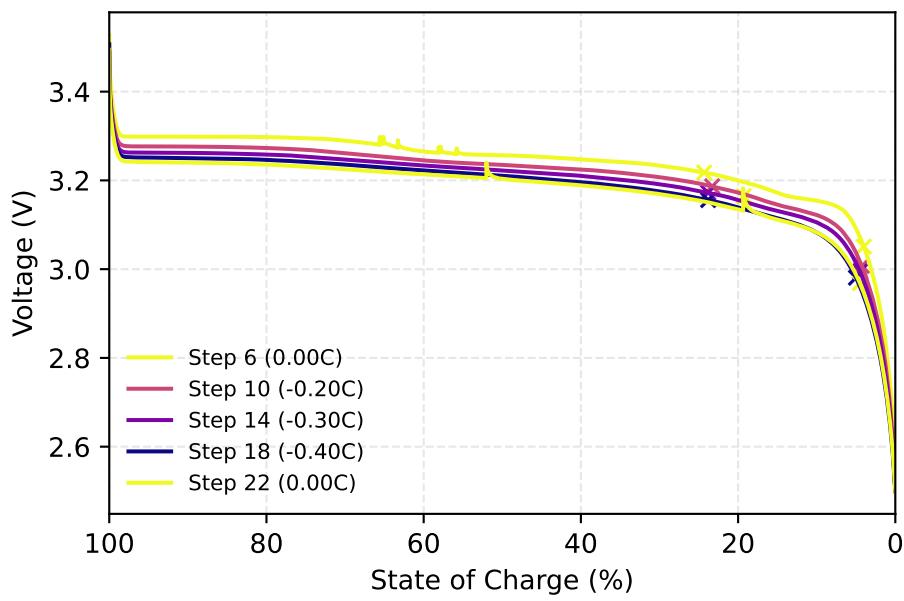
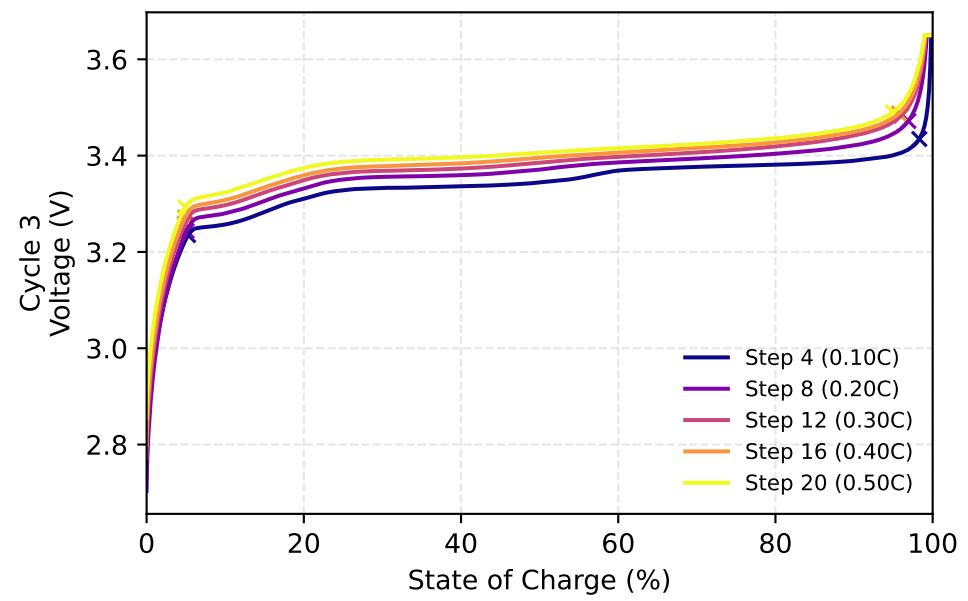
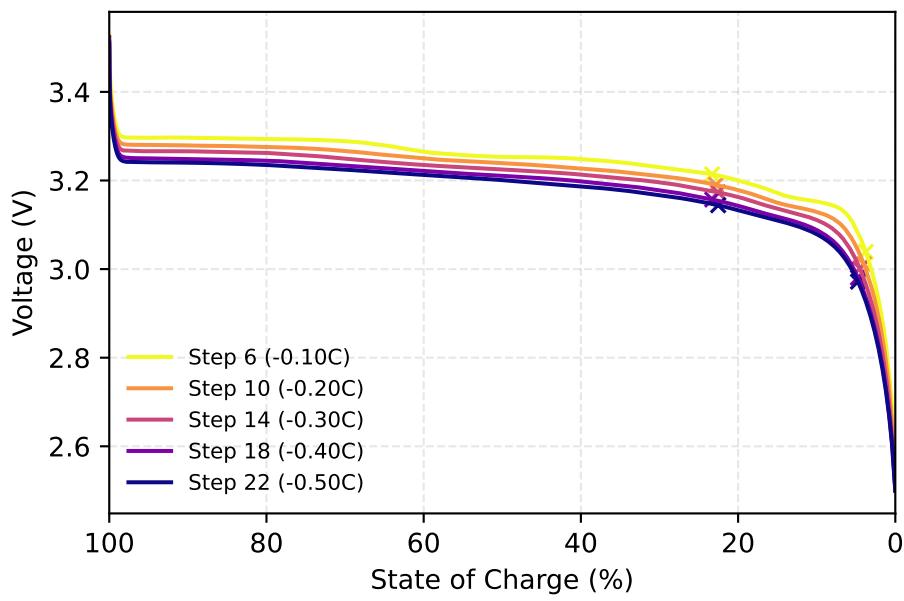
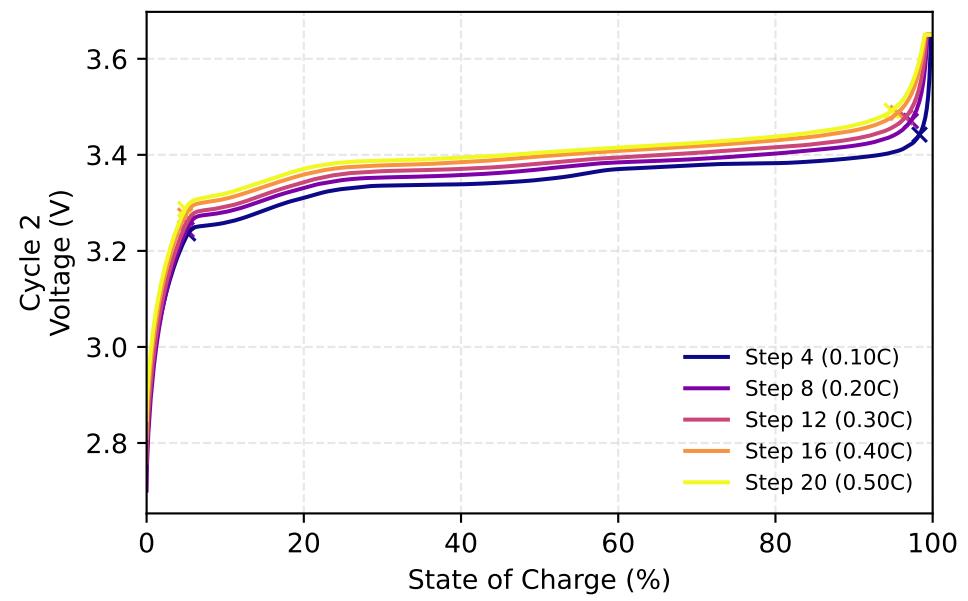
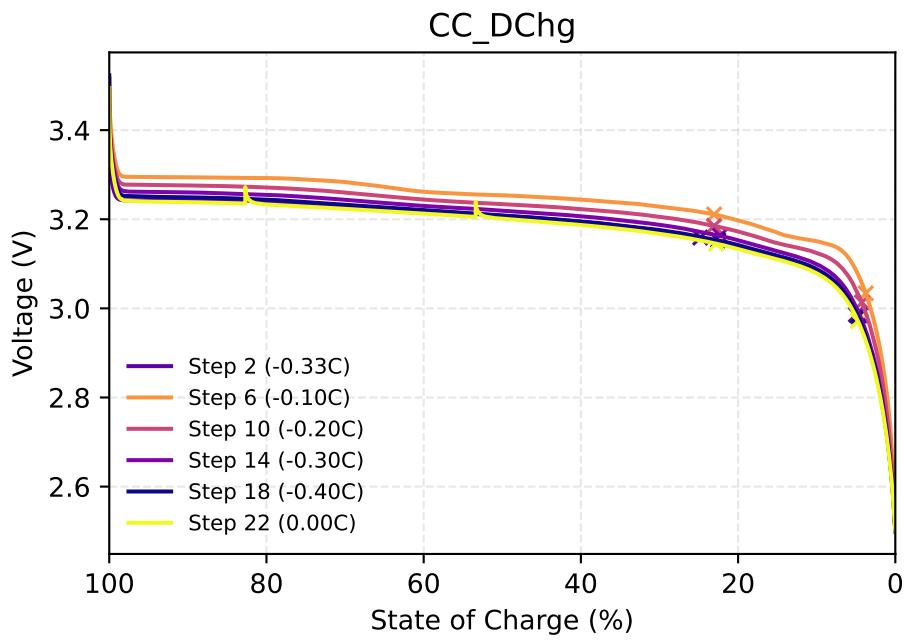
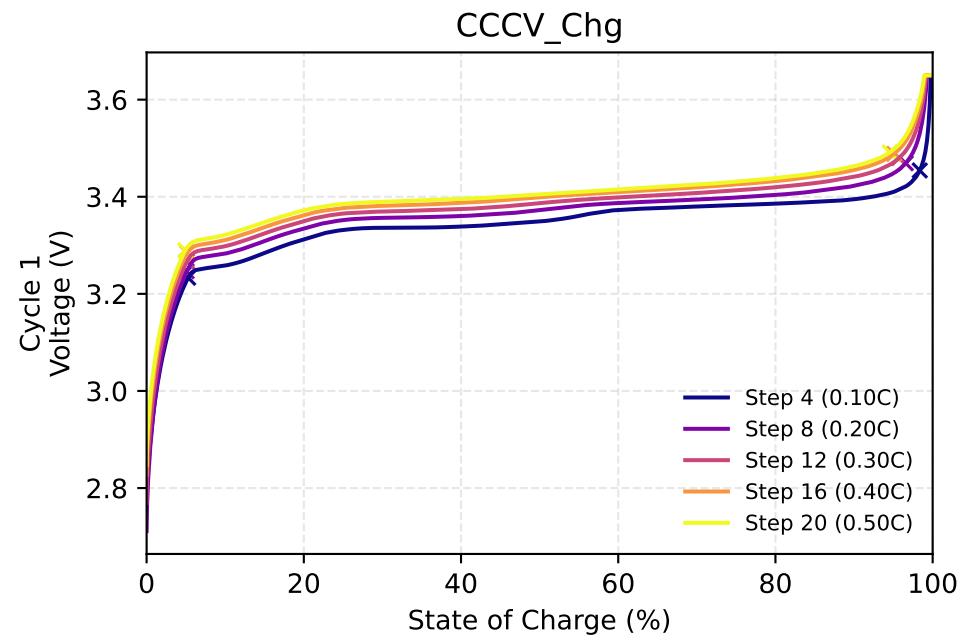
CCCV_Chg



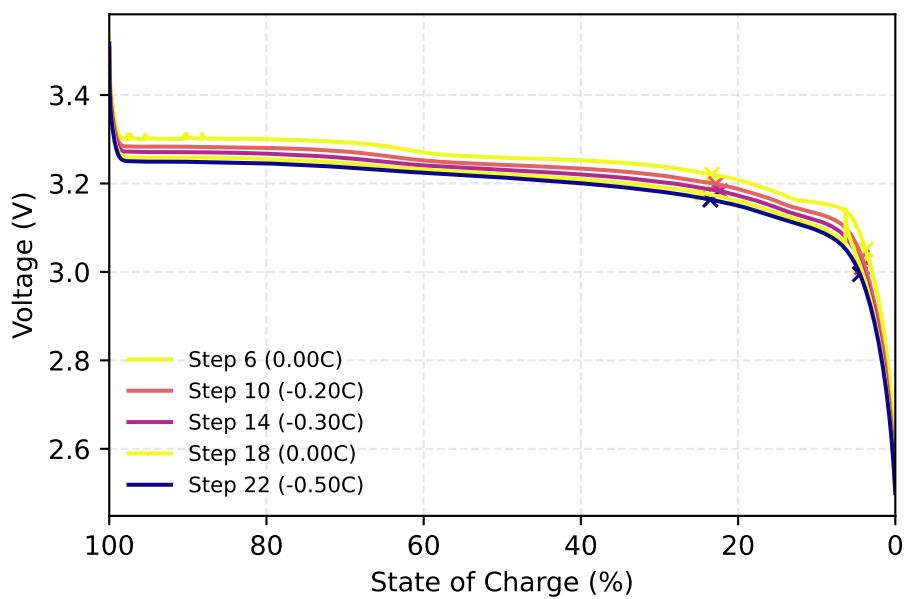
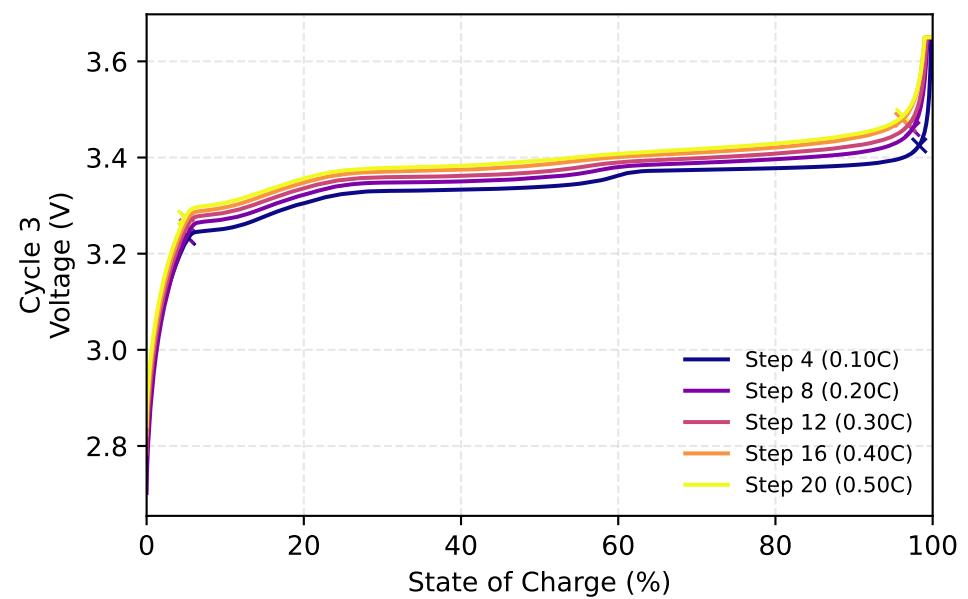
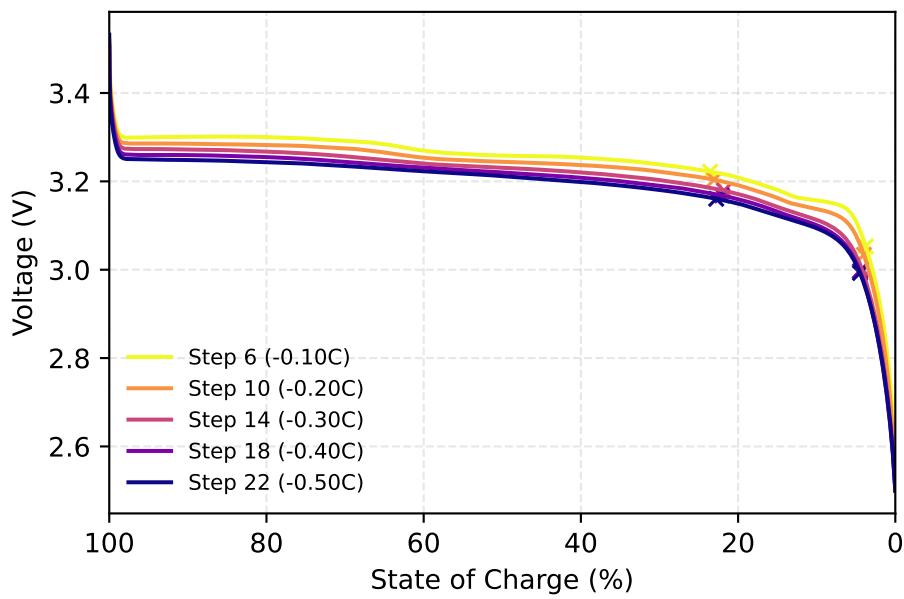
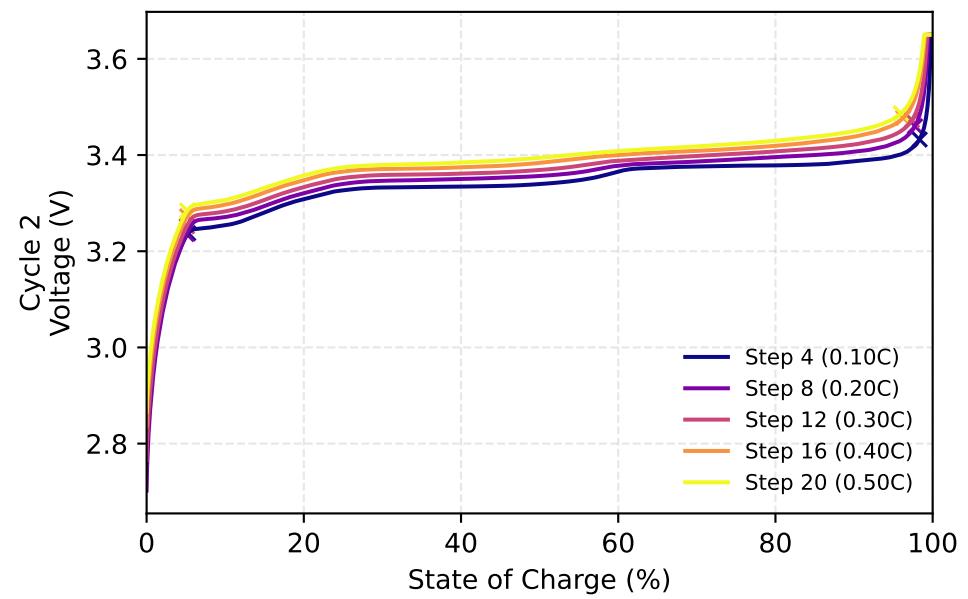
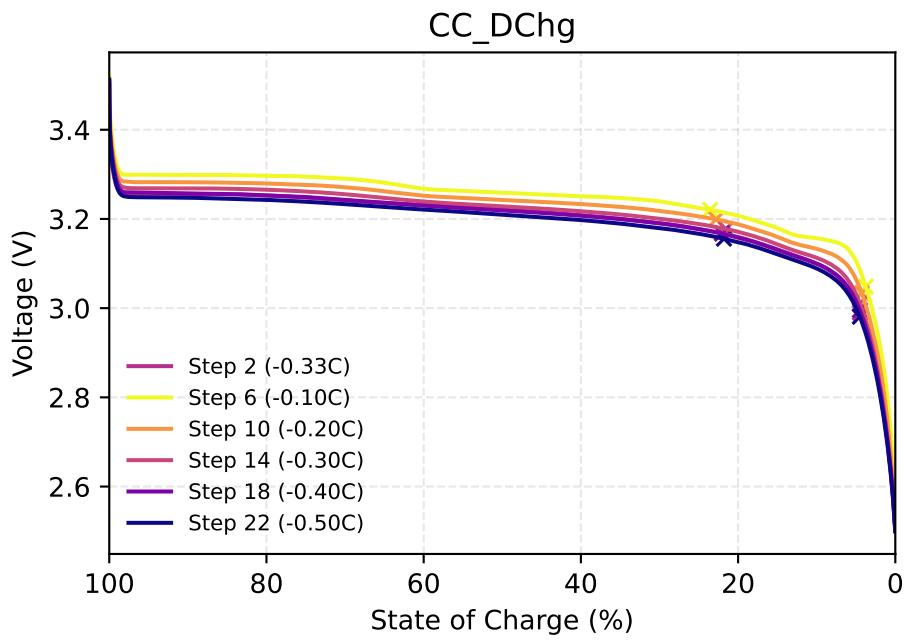
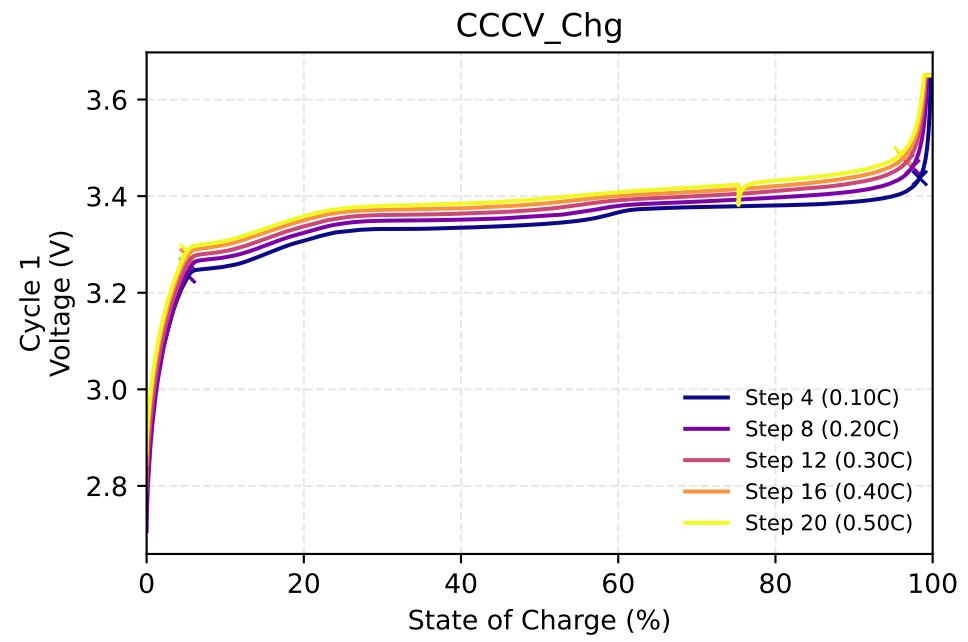
CC_DChg



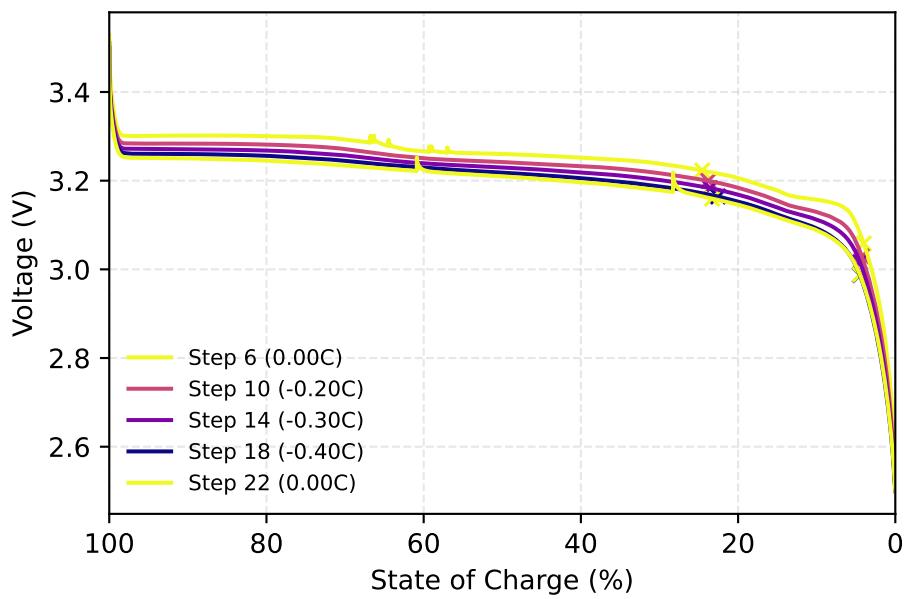
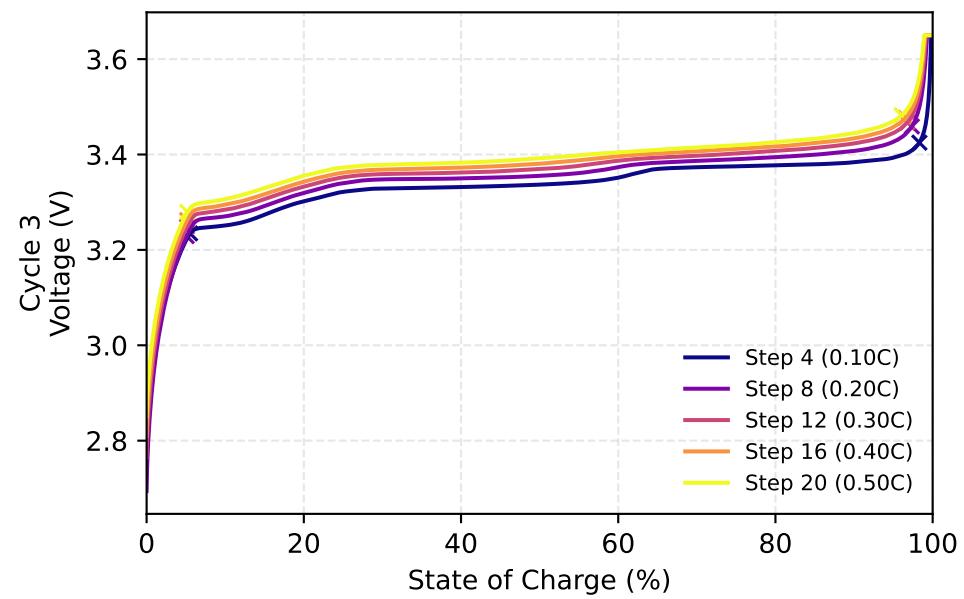
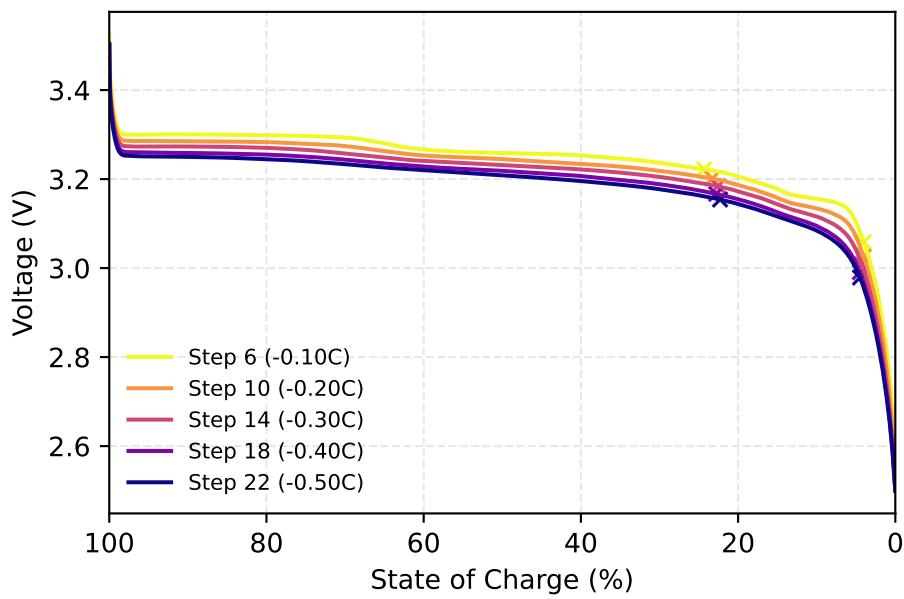
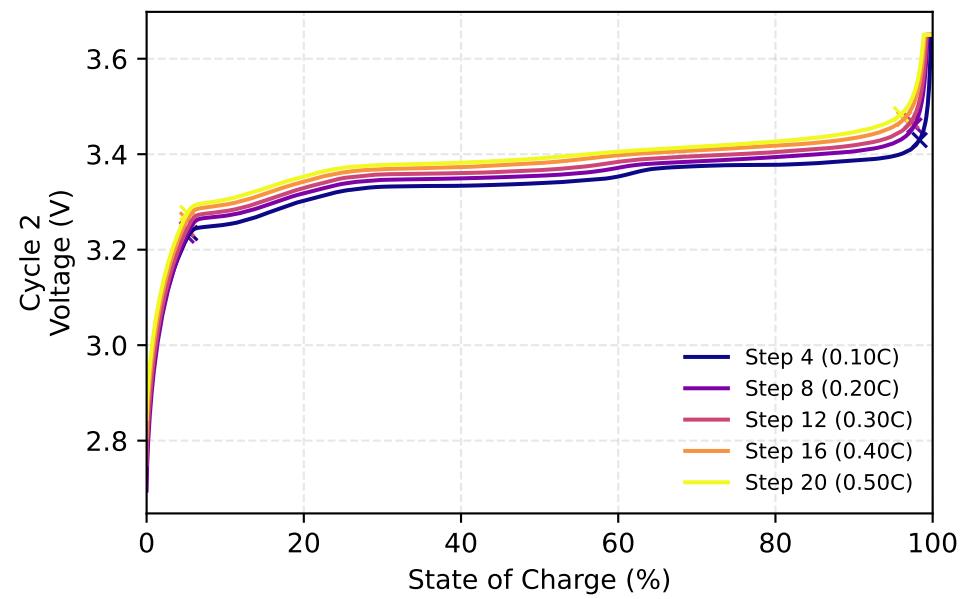
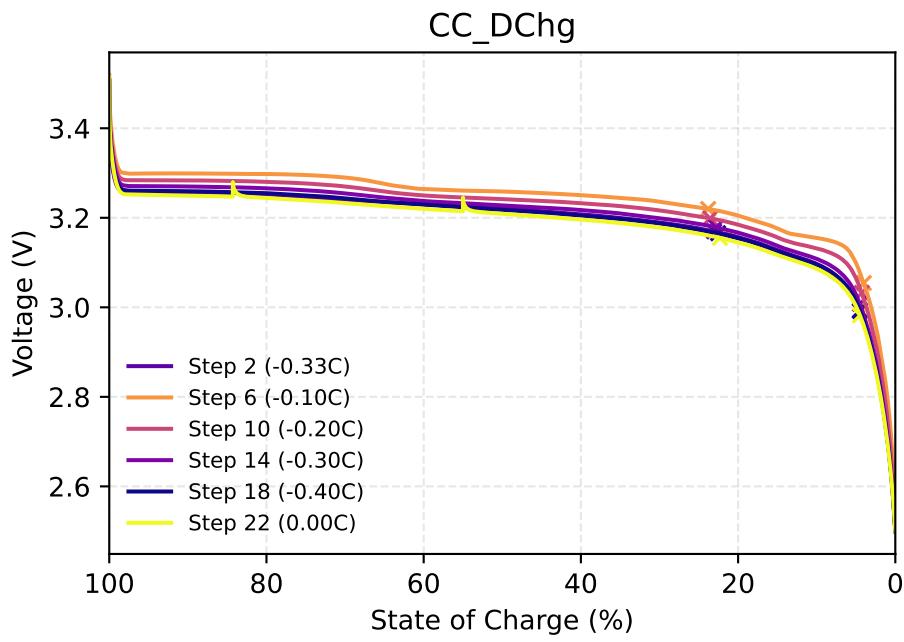
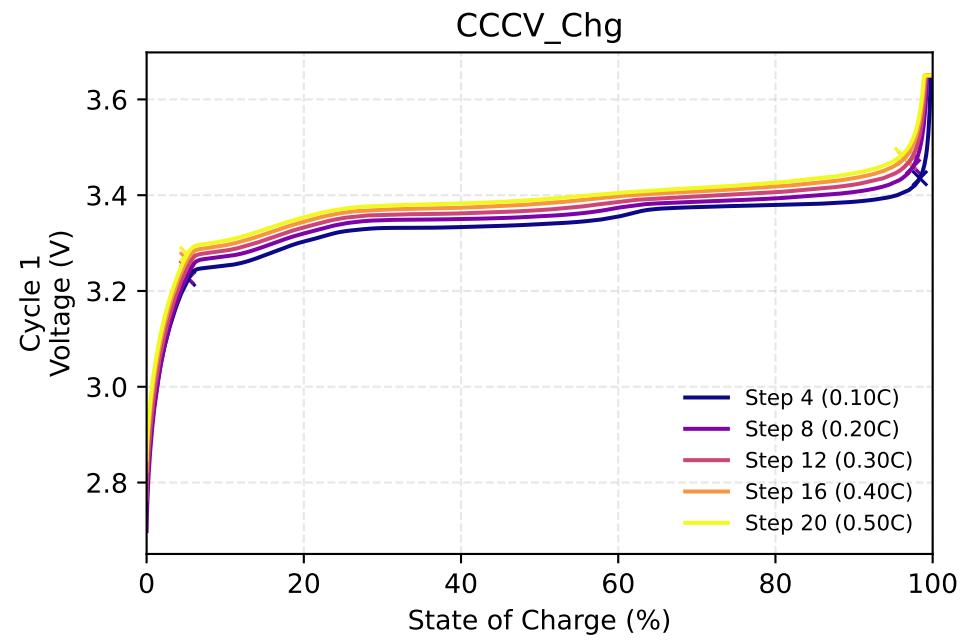
RD_RateCapability_0007 - SoC-V by Cycle and Step Name



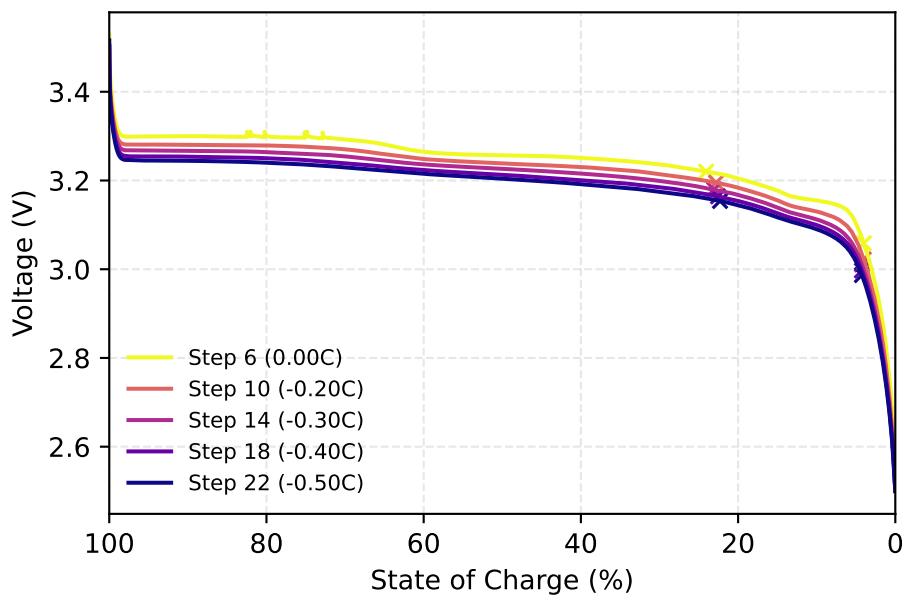
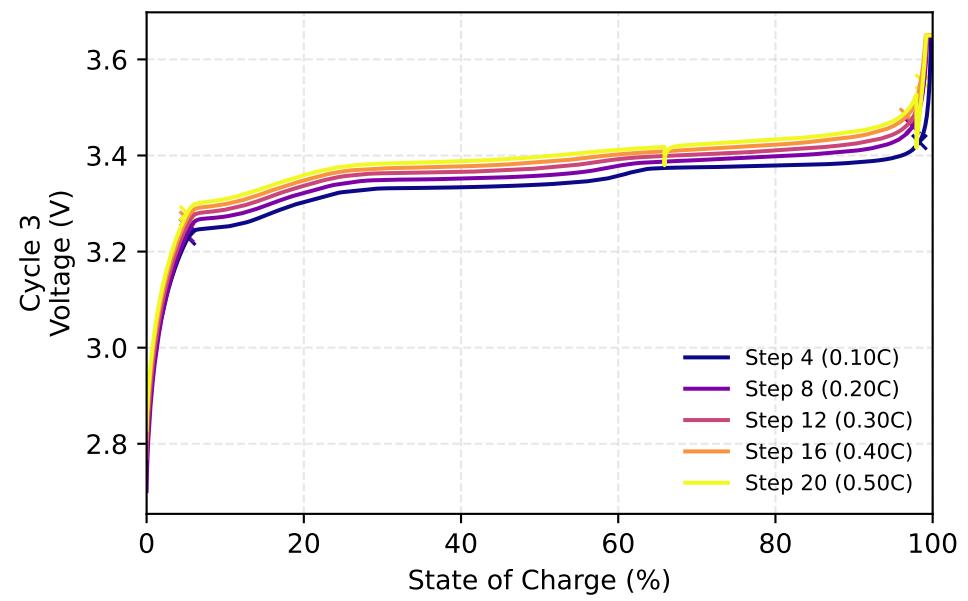
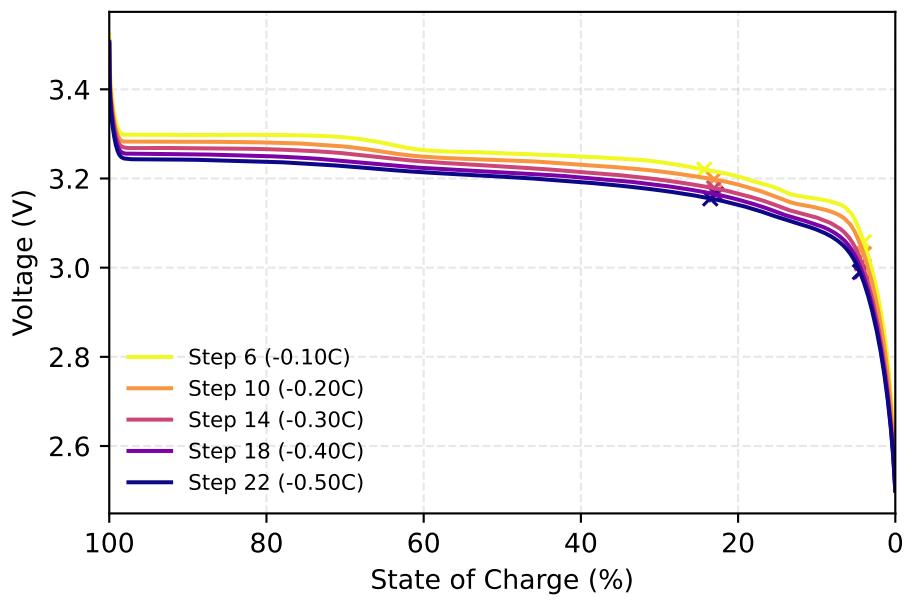
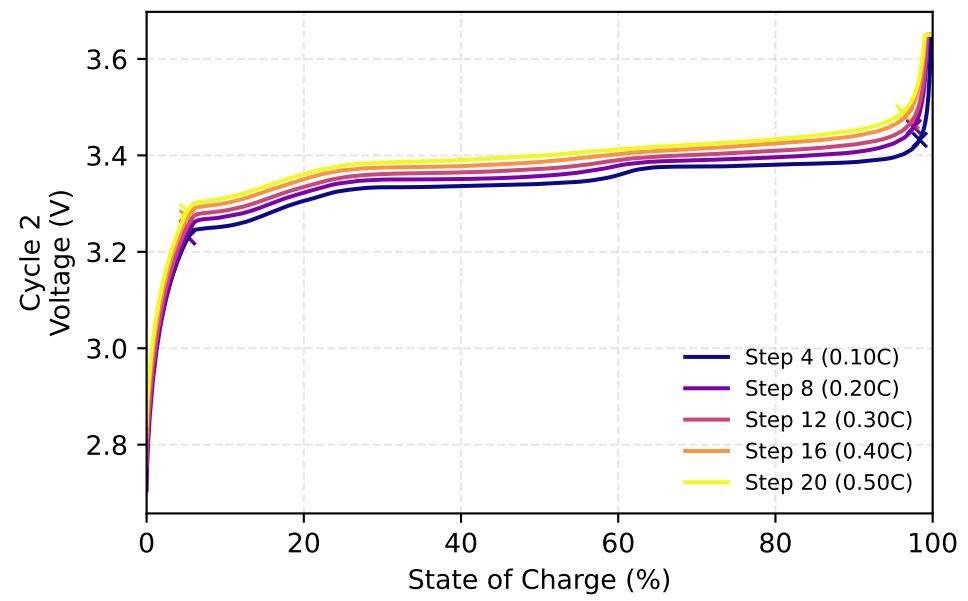
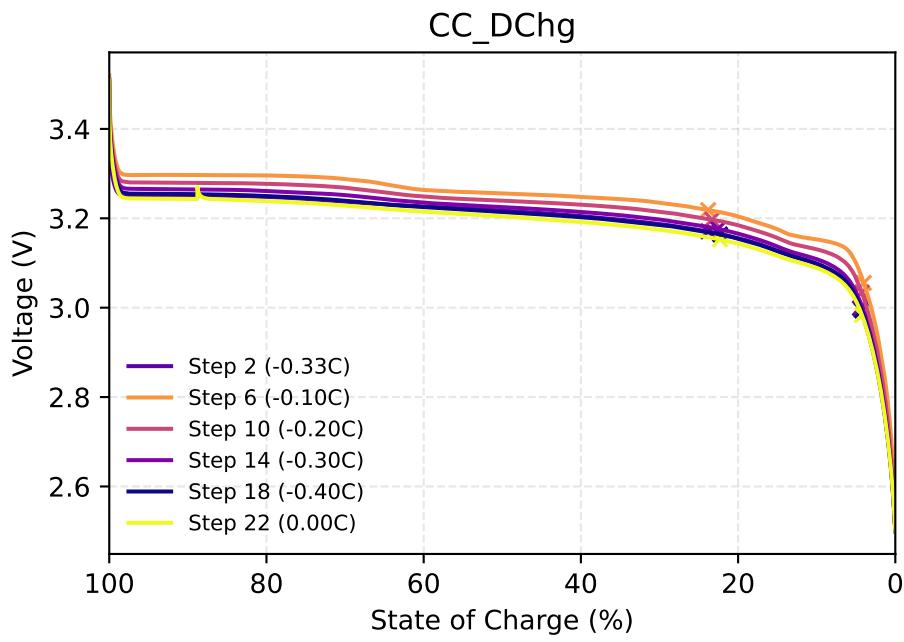
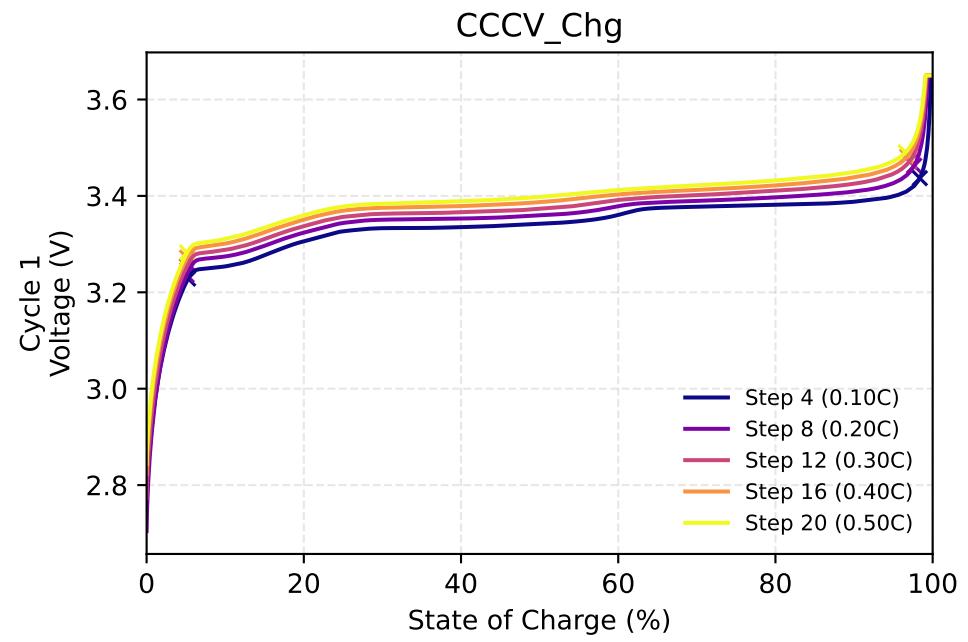
RD_RateCapability_0011 - SoC-V by Cycle and Step Name



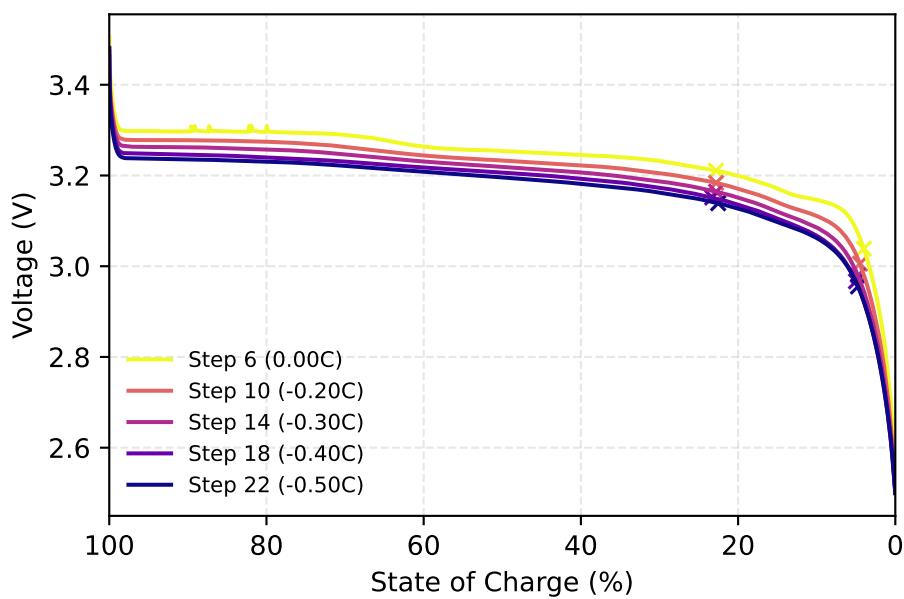
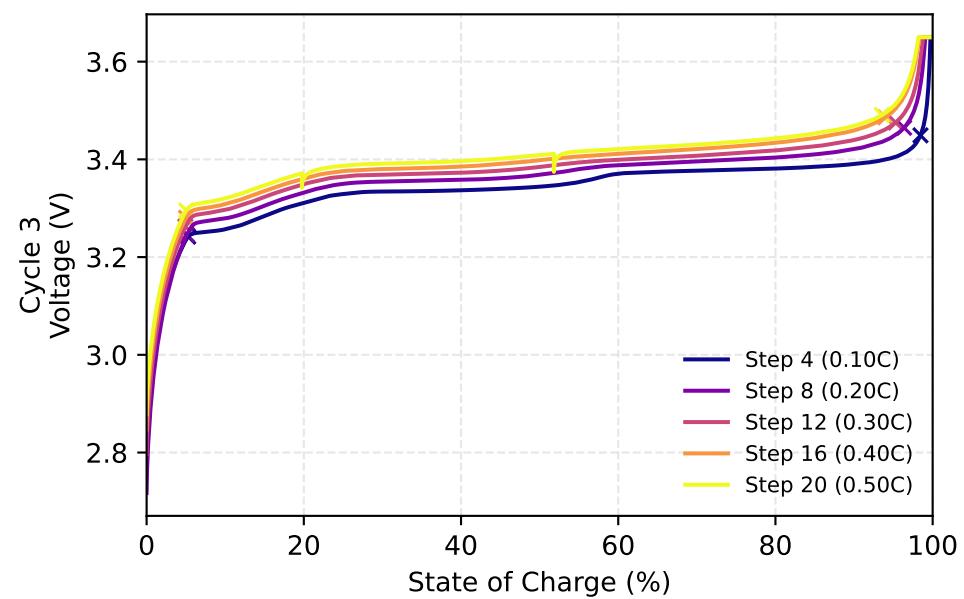
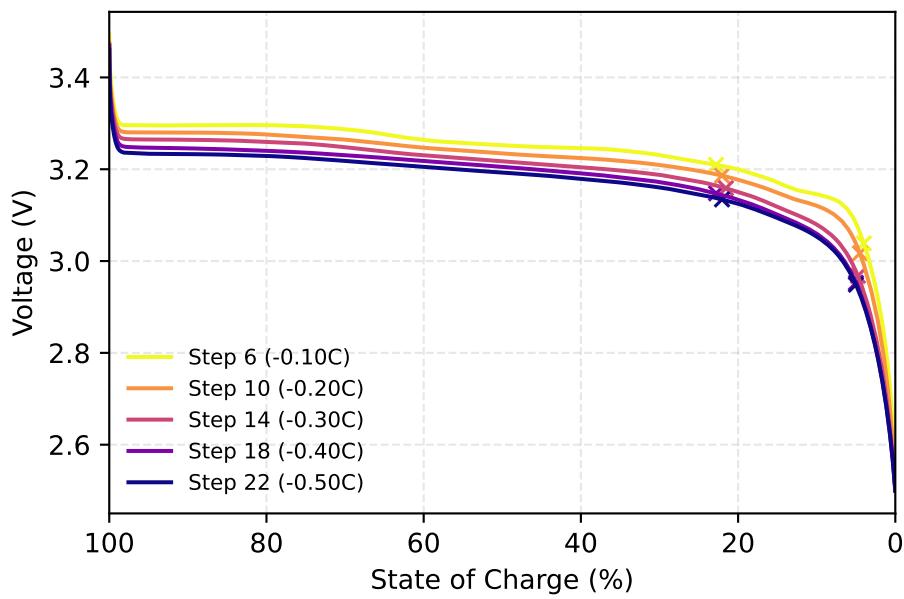
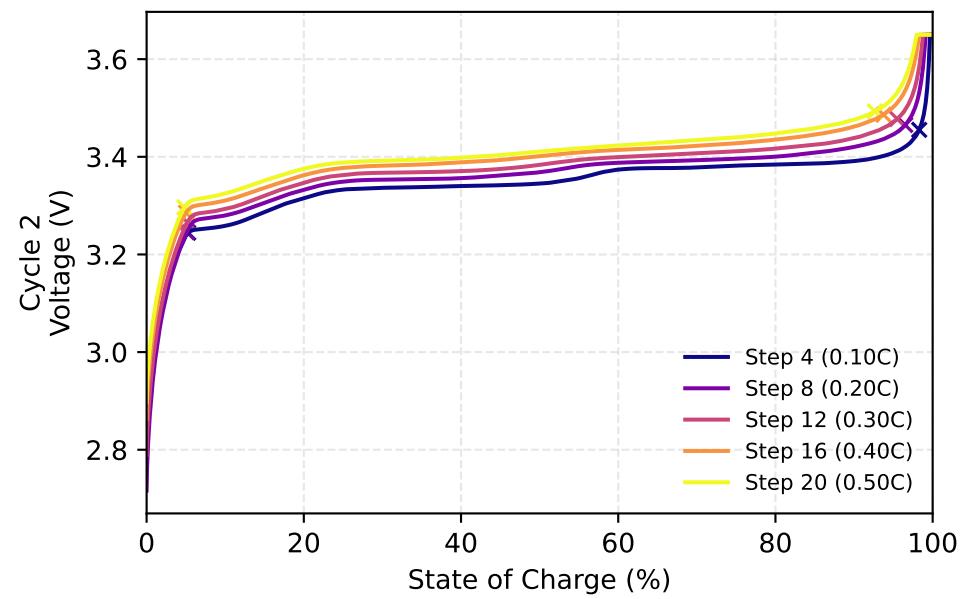
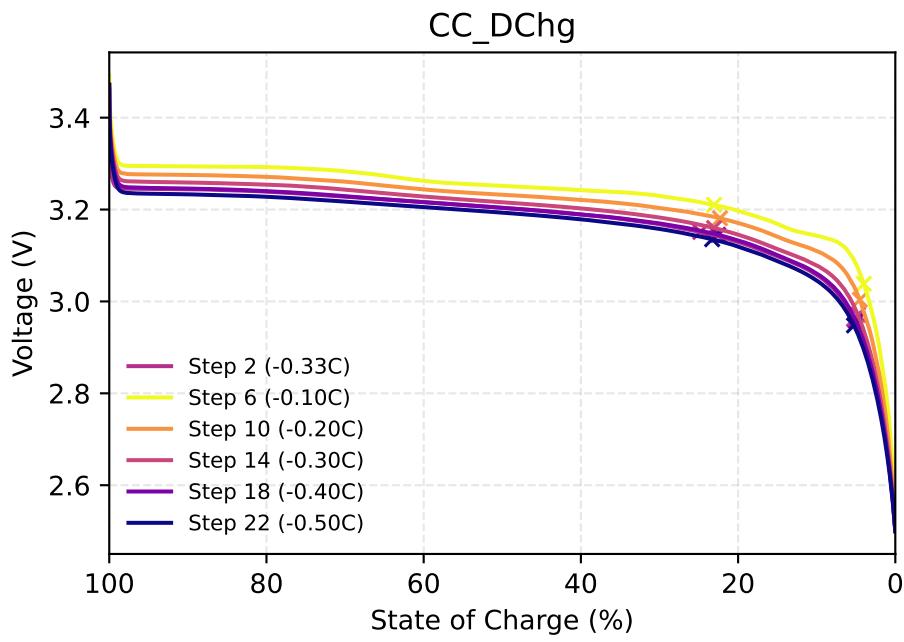
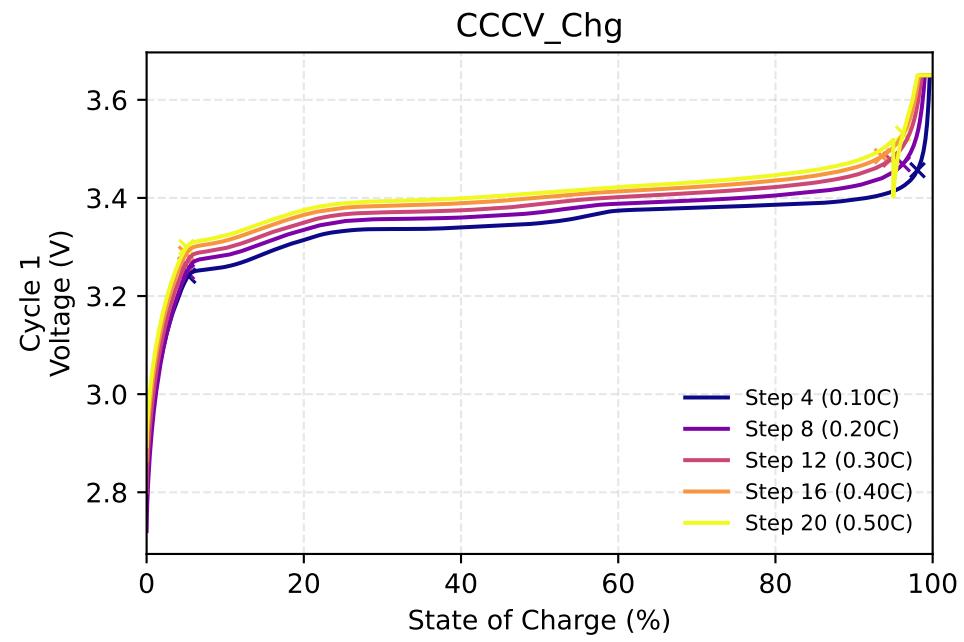
RD_RateCapability_0012 - SoC-V by Cycle and Step Name



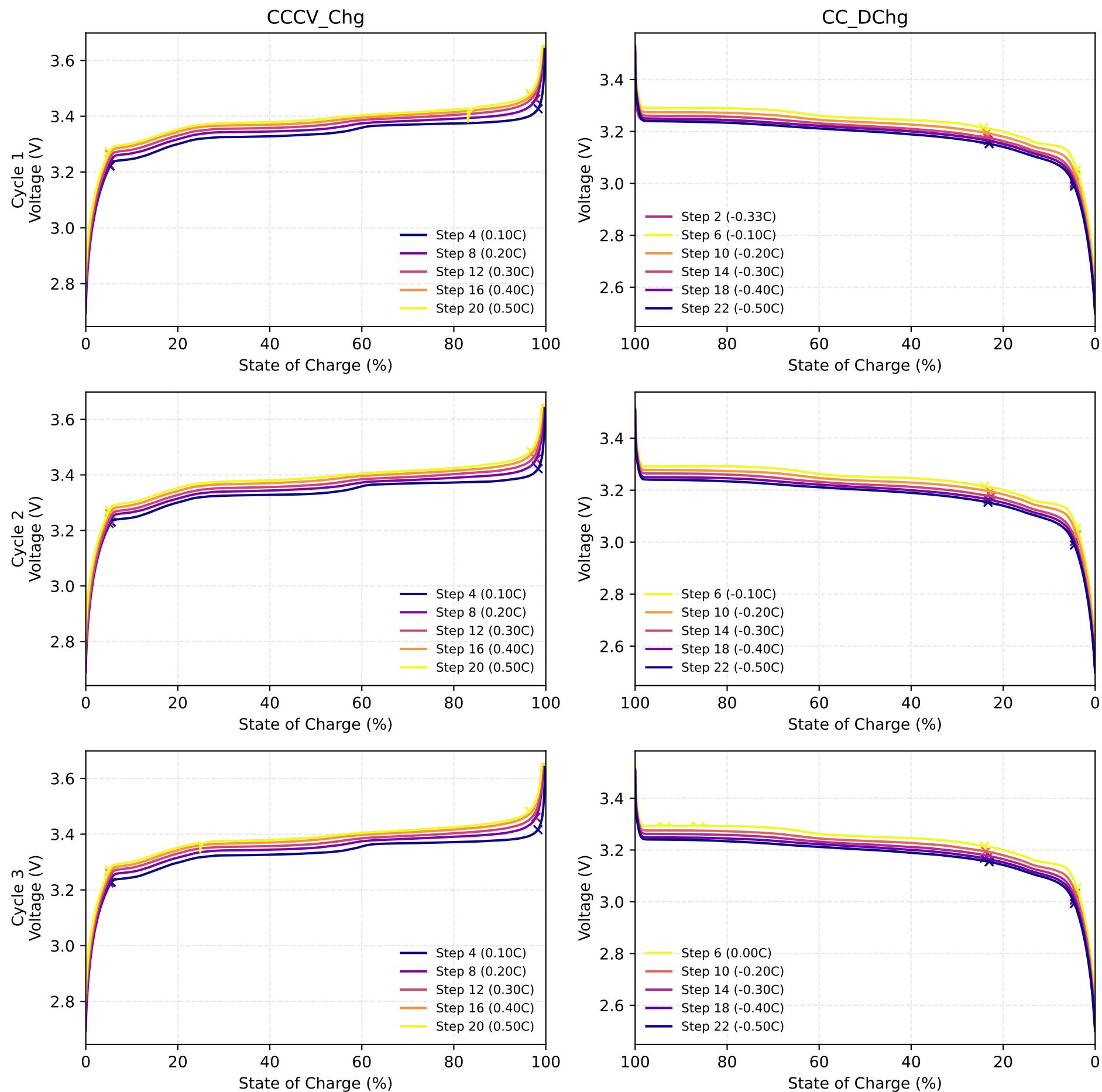
RD_RateCapability_0025 - SoC-V by Cycle and Step Name



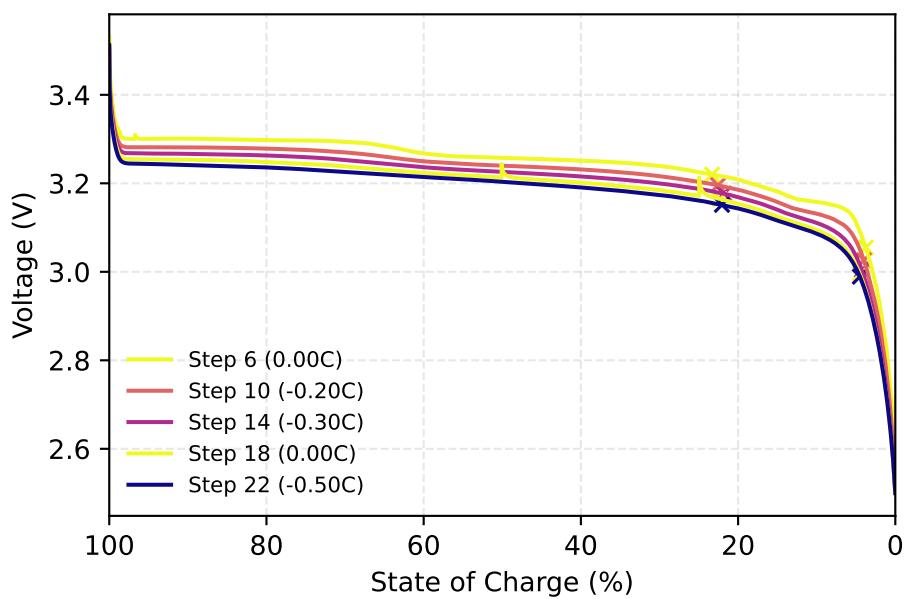
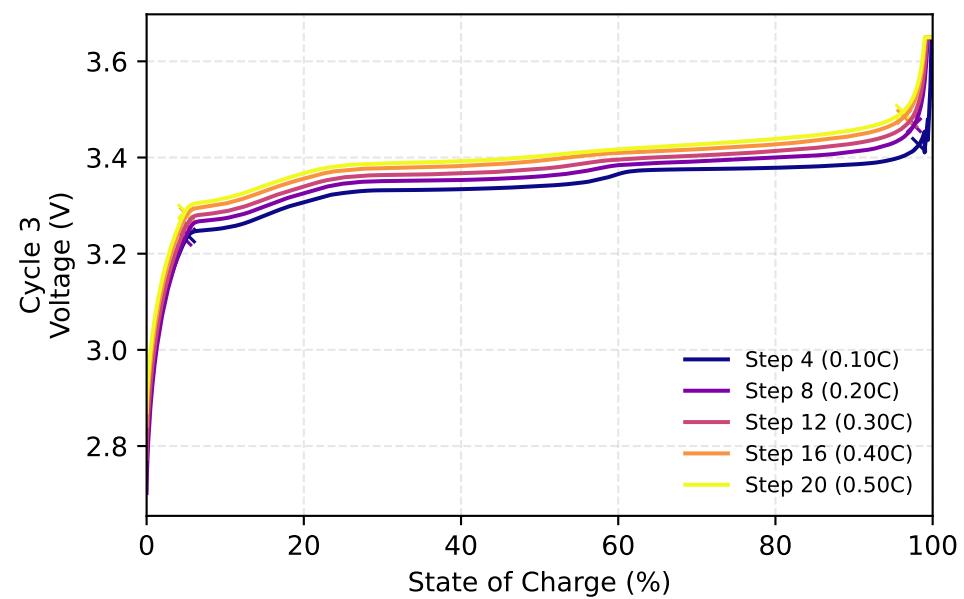
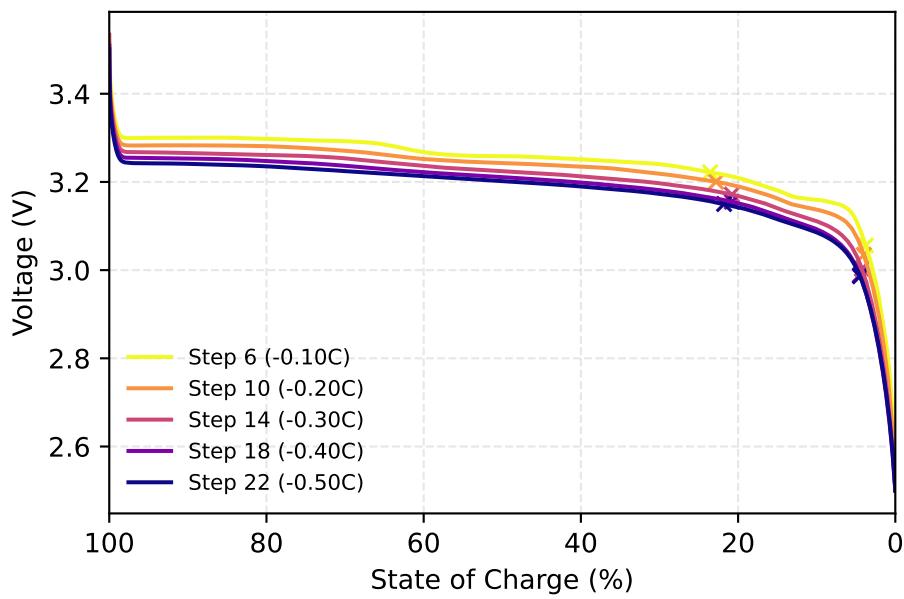
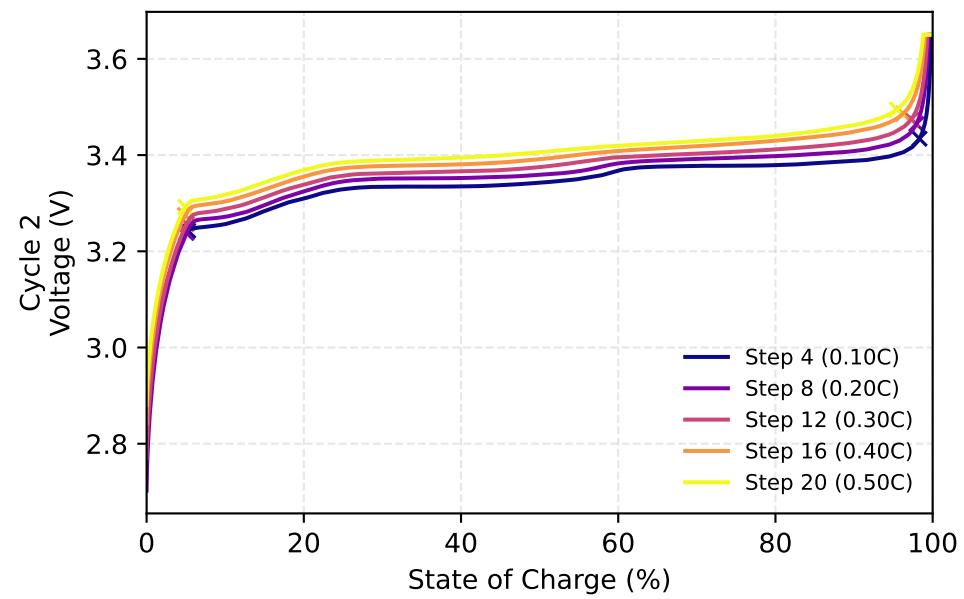
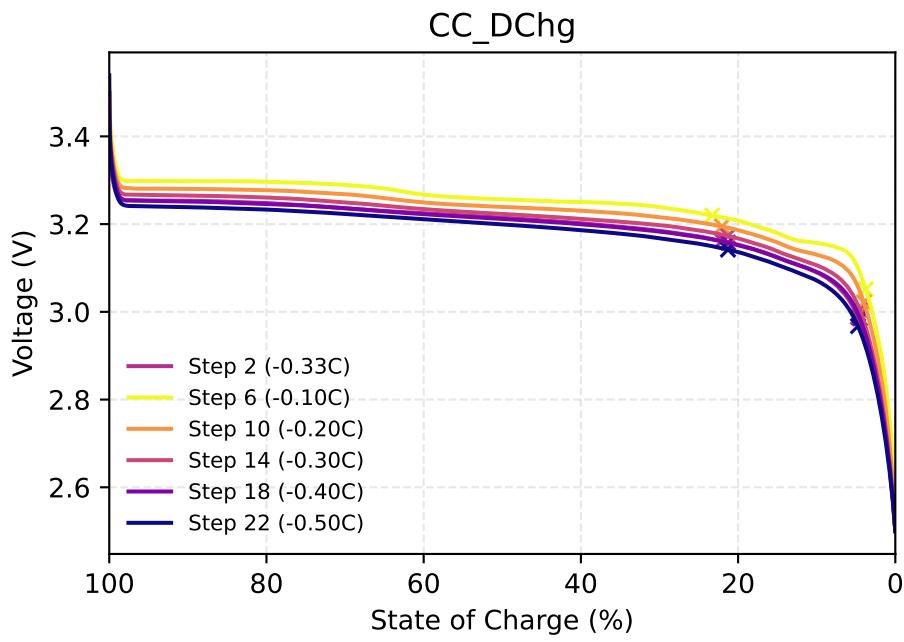
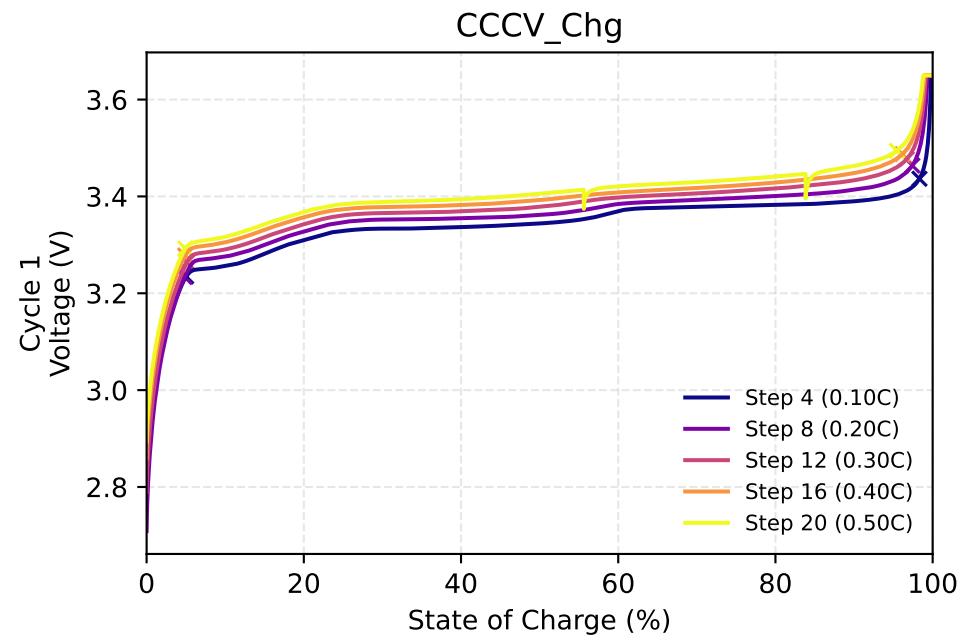
RD_RateCapability_0034 - SoC-V by Cycle and Step Name



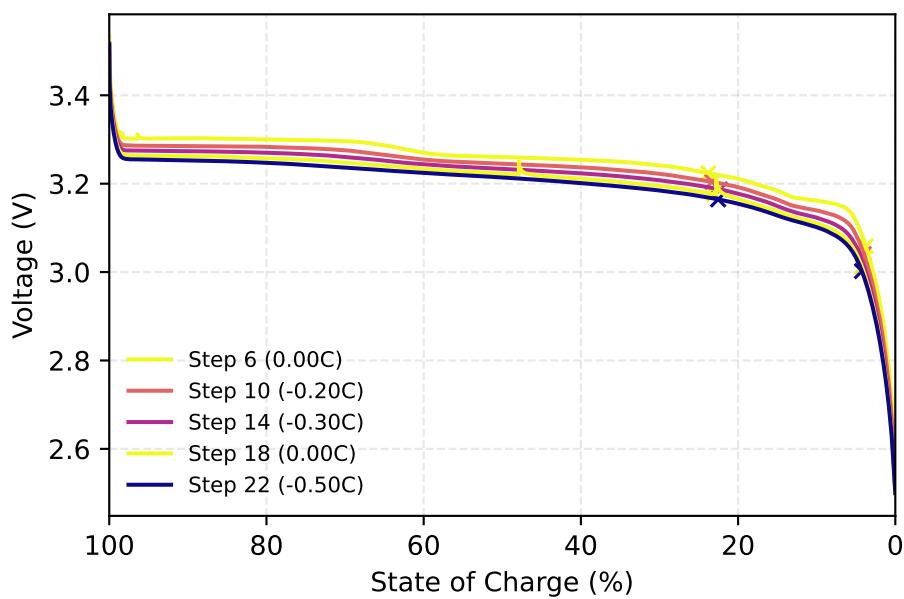
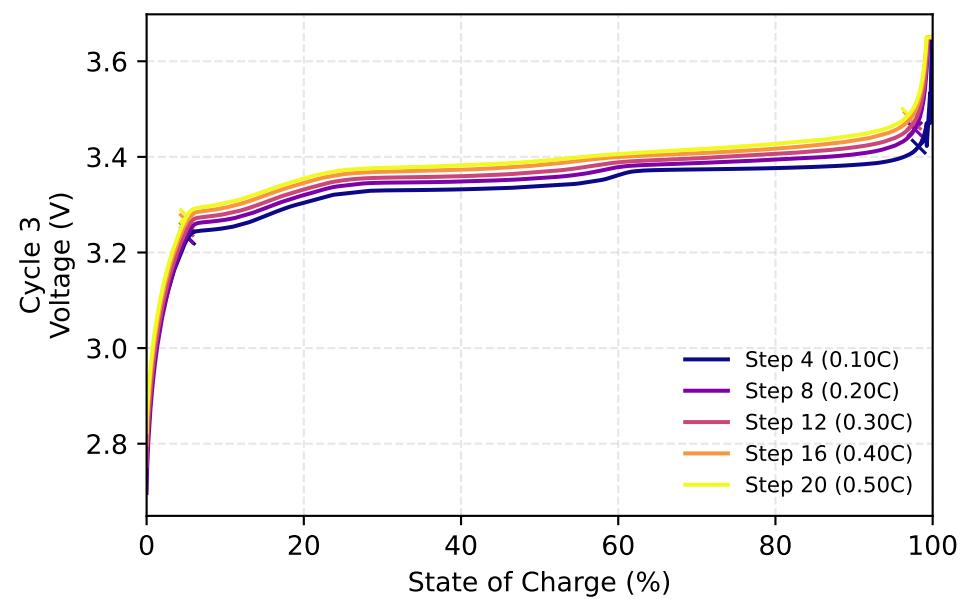
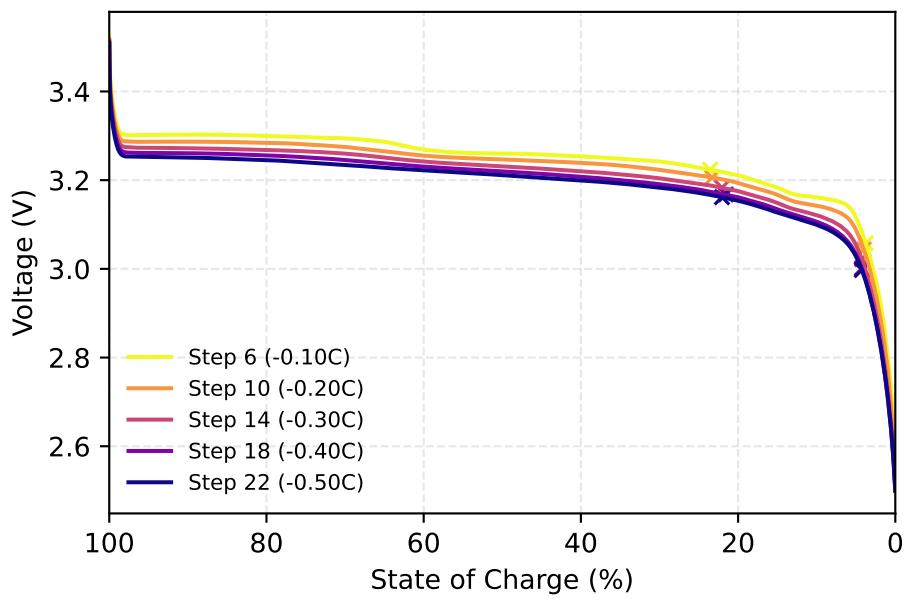
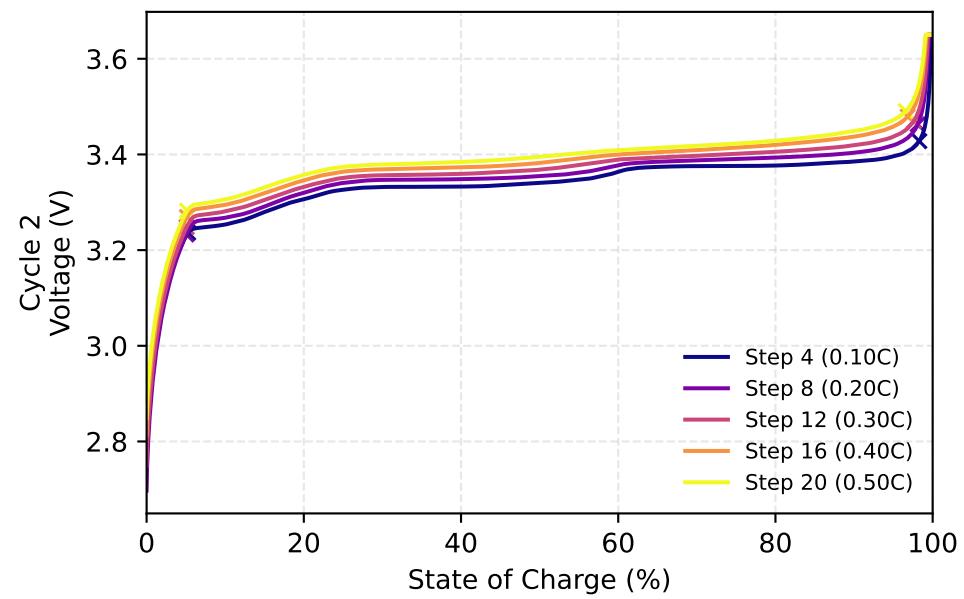
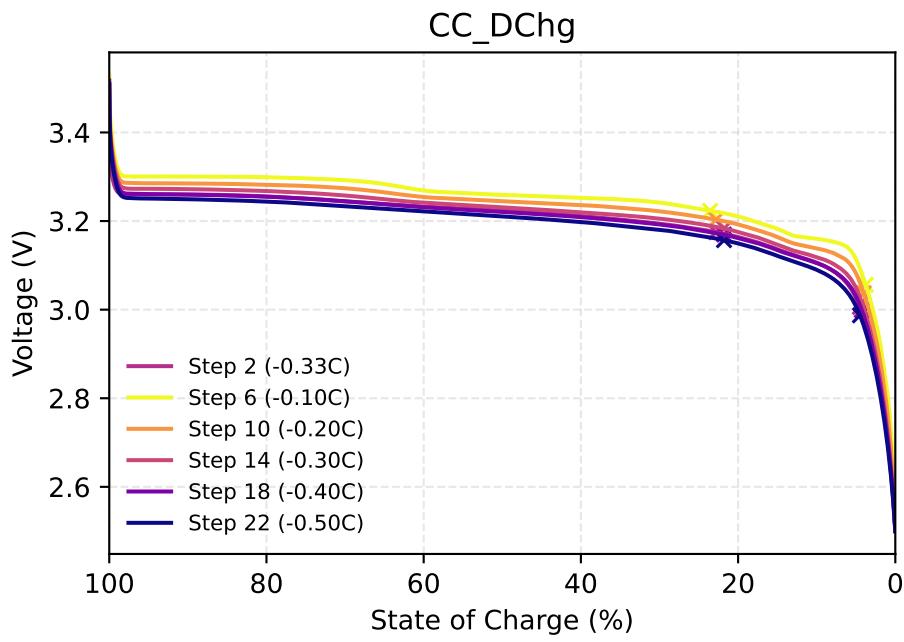
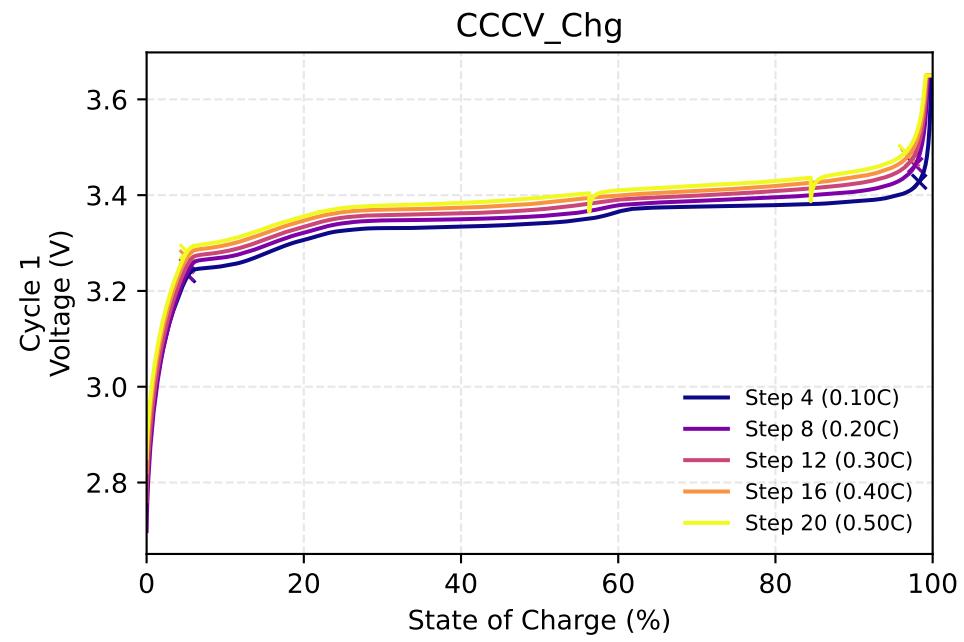
RD_RateCapability_0040 - SoC-V by Cycle and Step Name



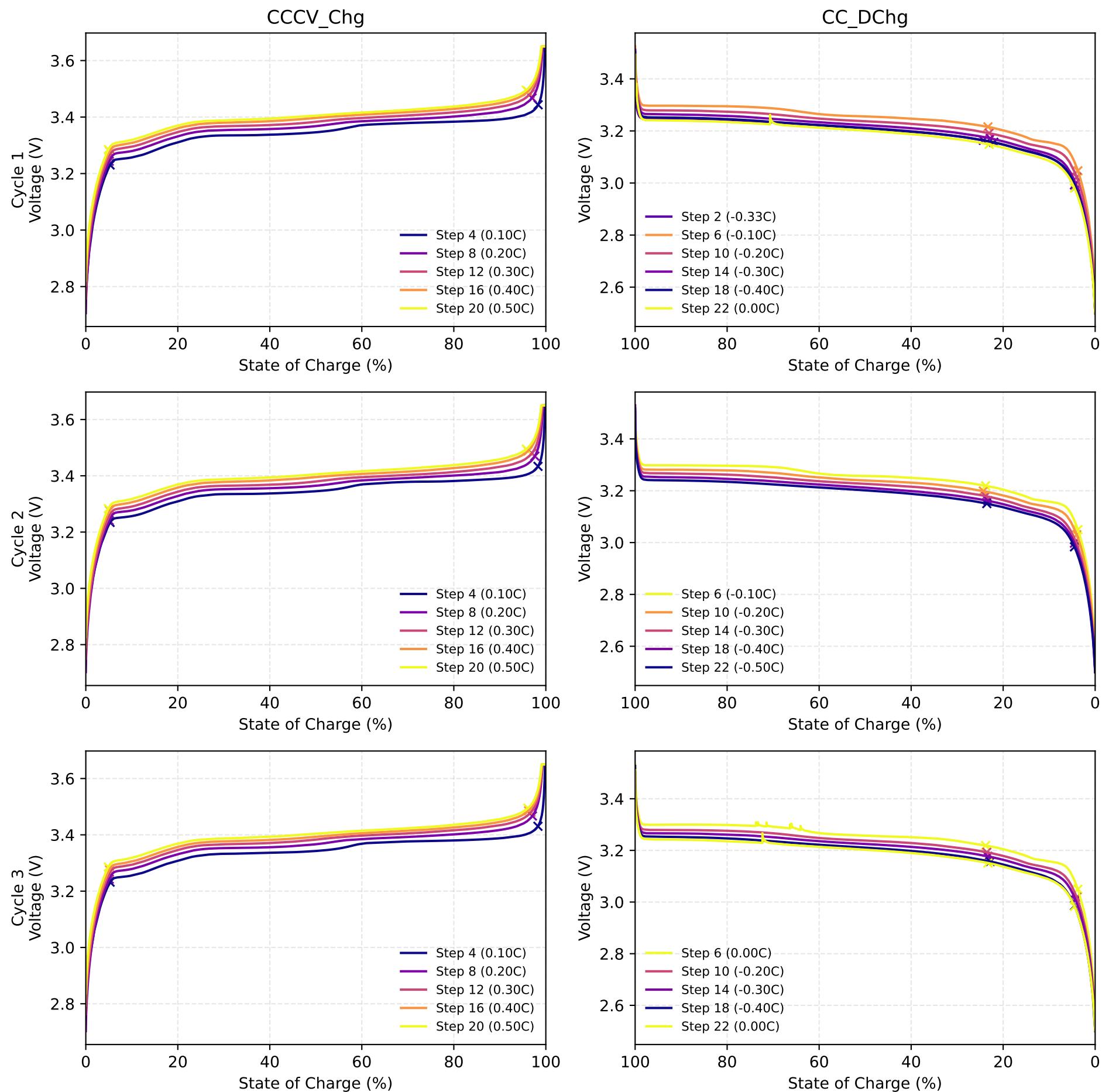
RD_RateCapability_0043 - SoC-V by Cycle and Step Name



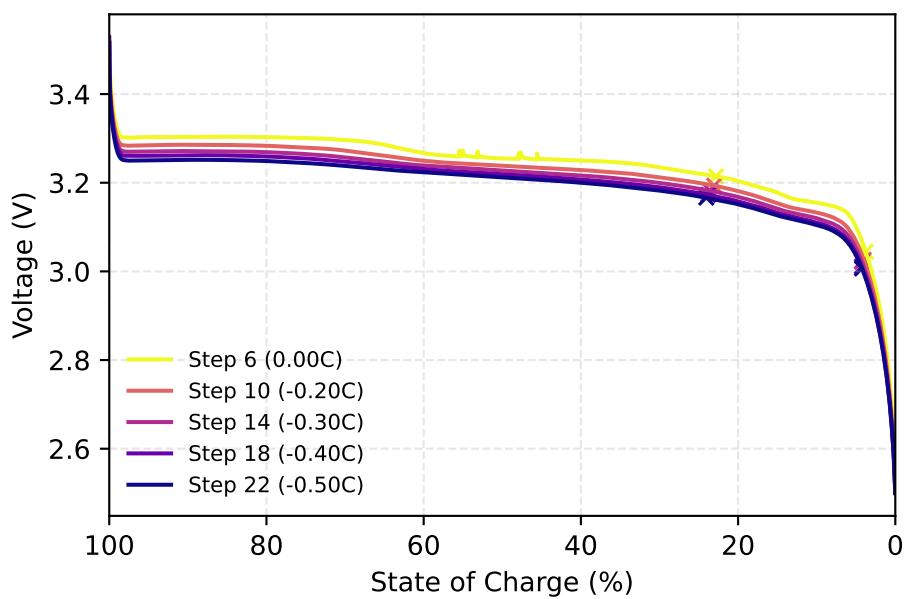
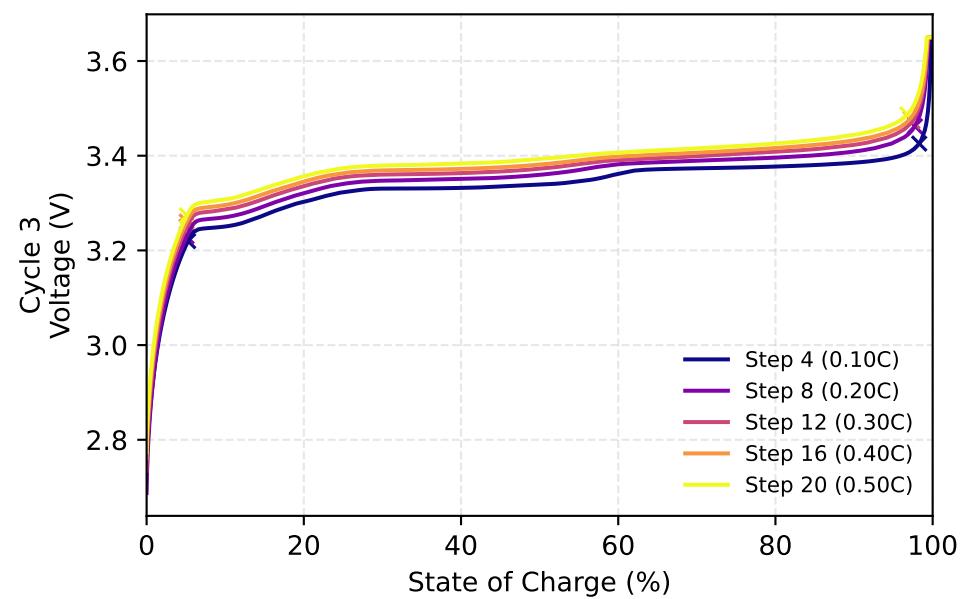
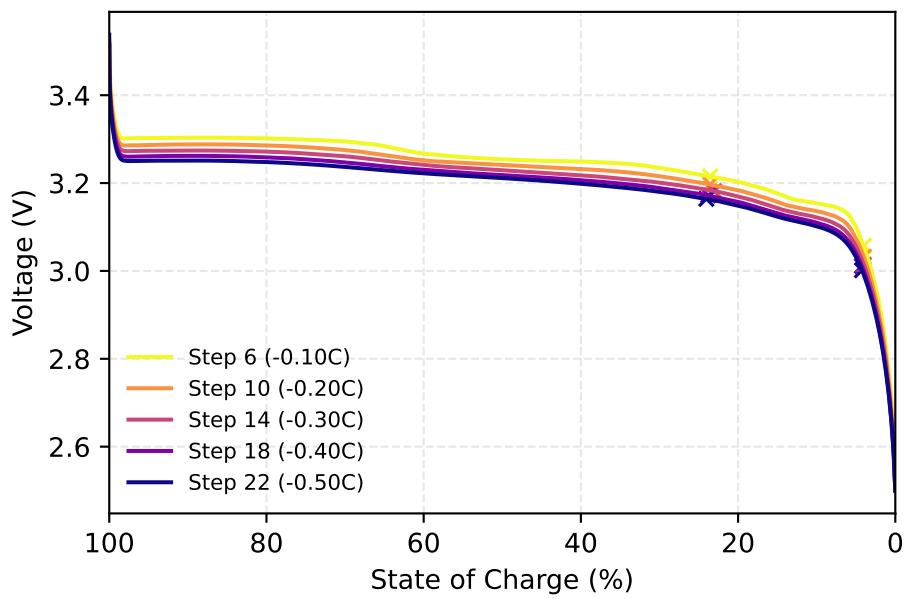
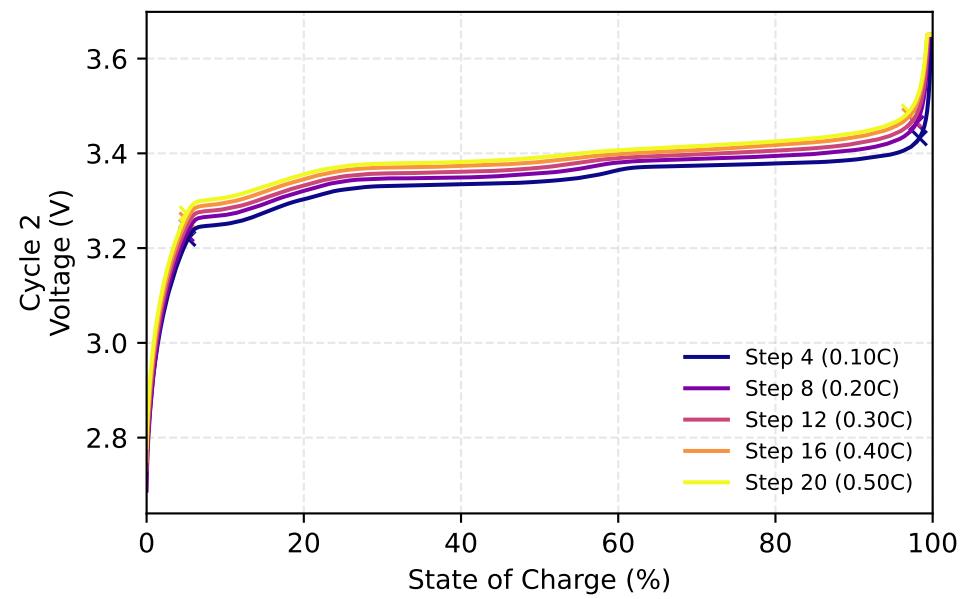
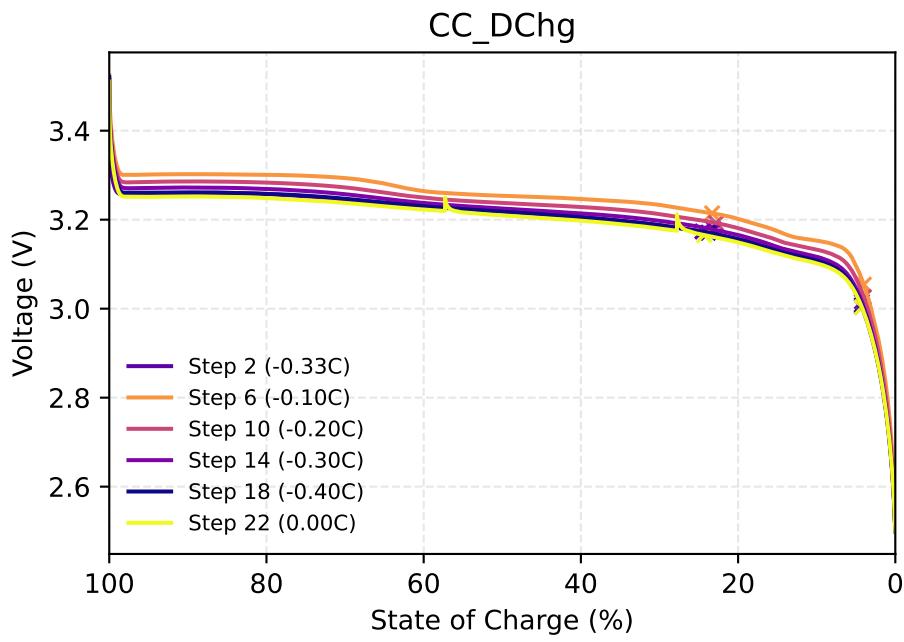
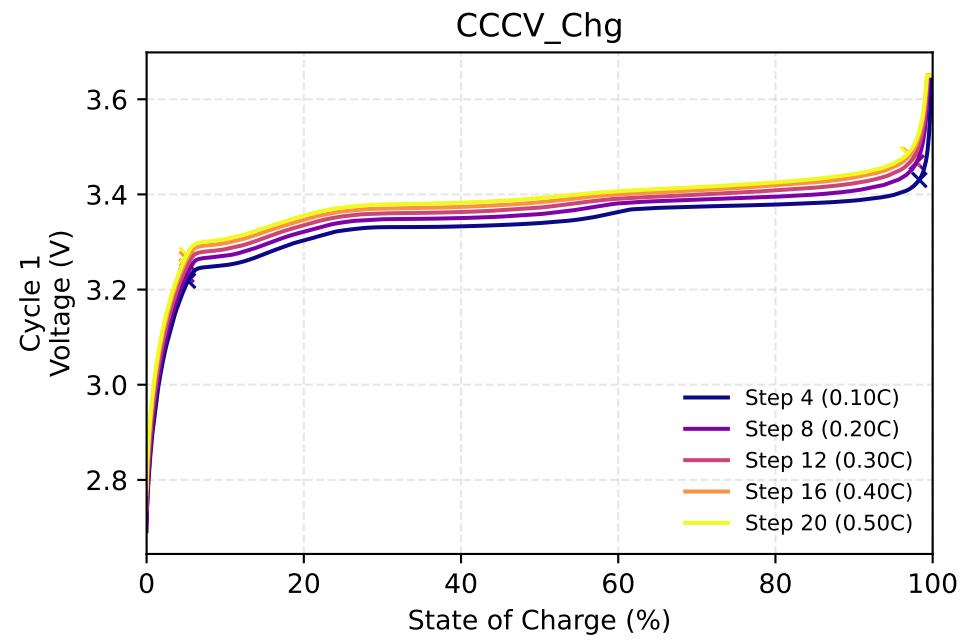
RD_RateCapability_0046 - SoC-V by Cycle and Step Name



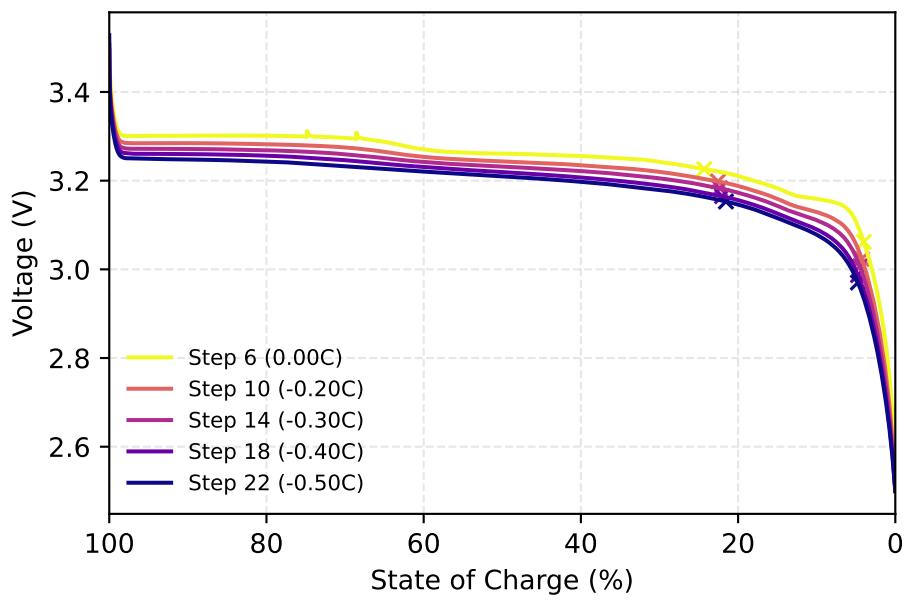
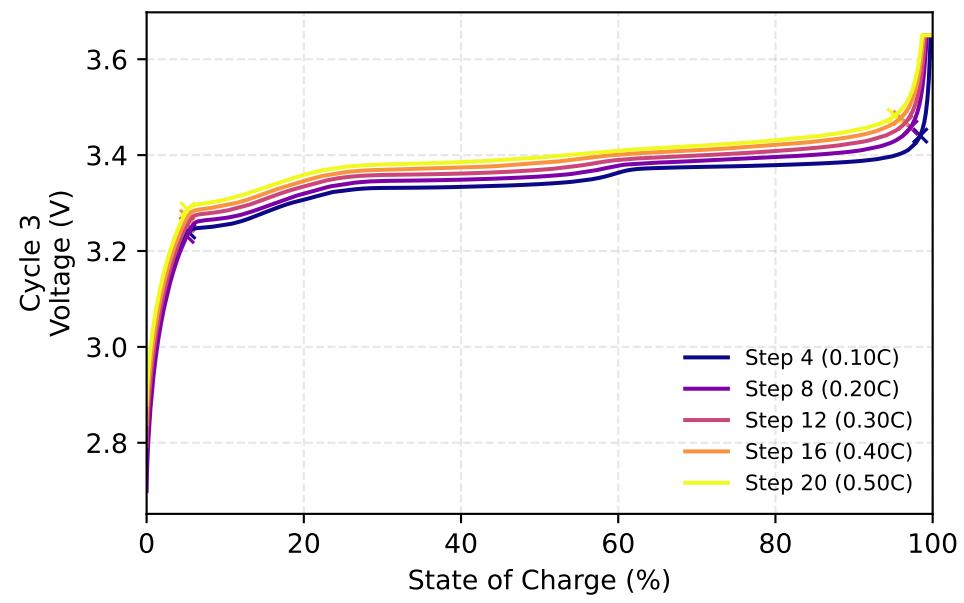
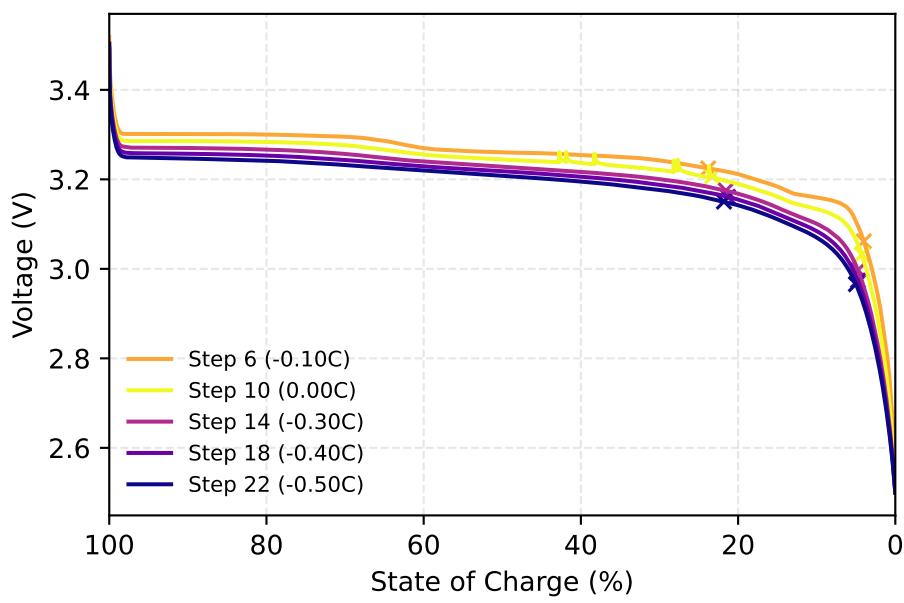
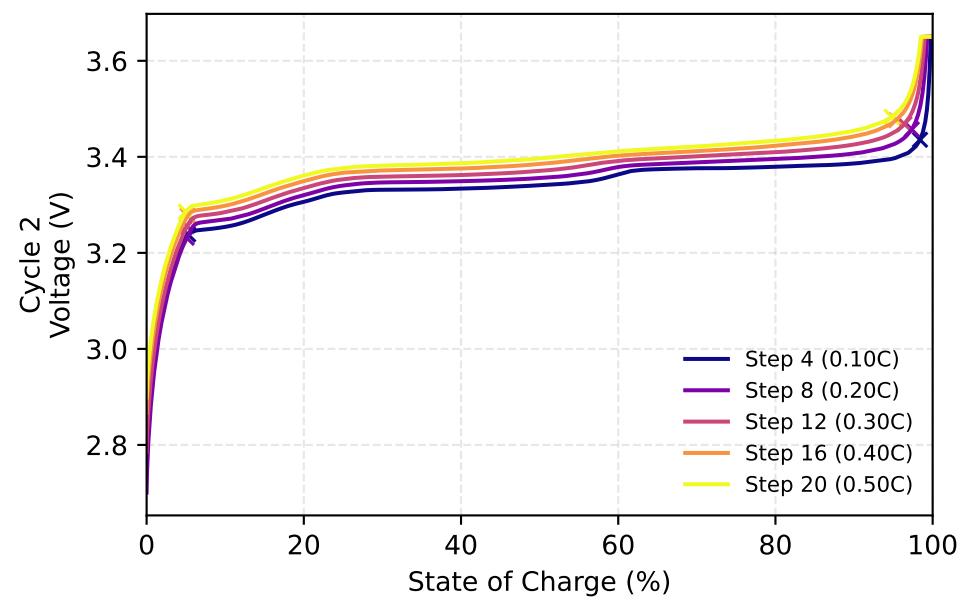
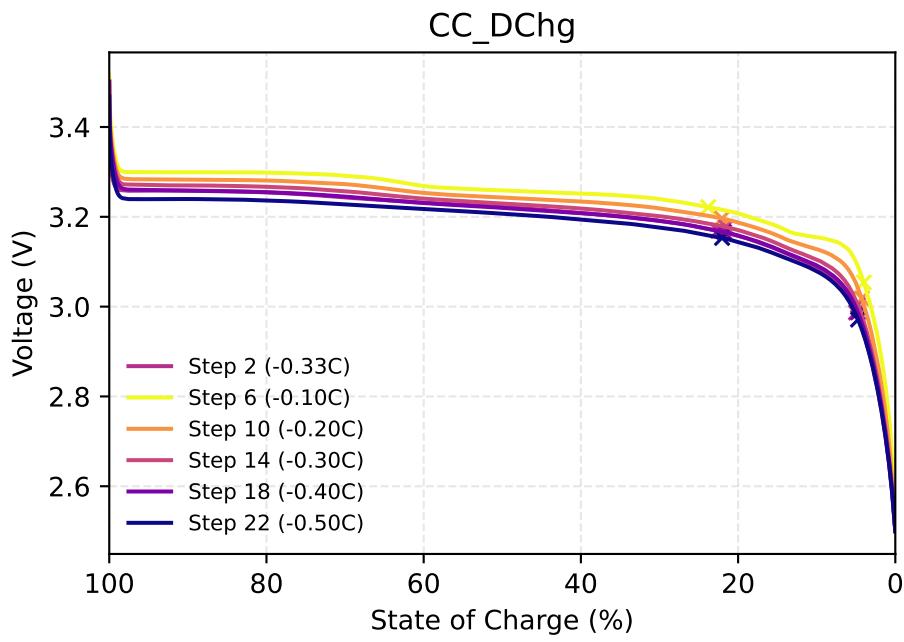
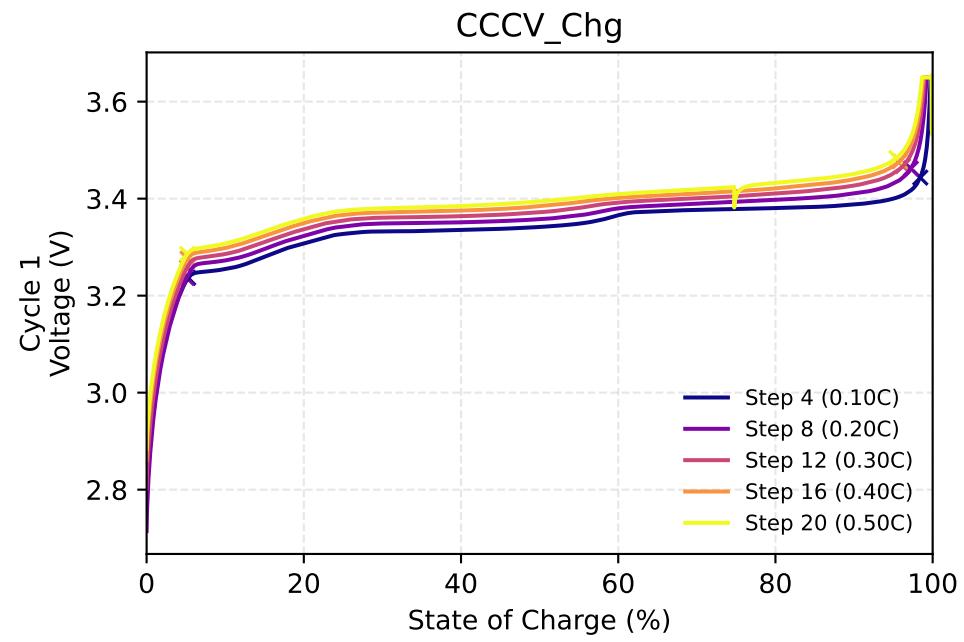
RD_RateCapability_0049 - SoC-V by Cycle and Step Name



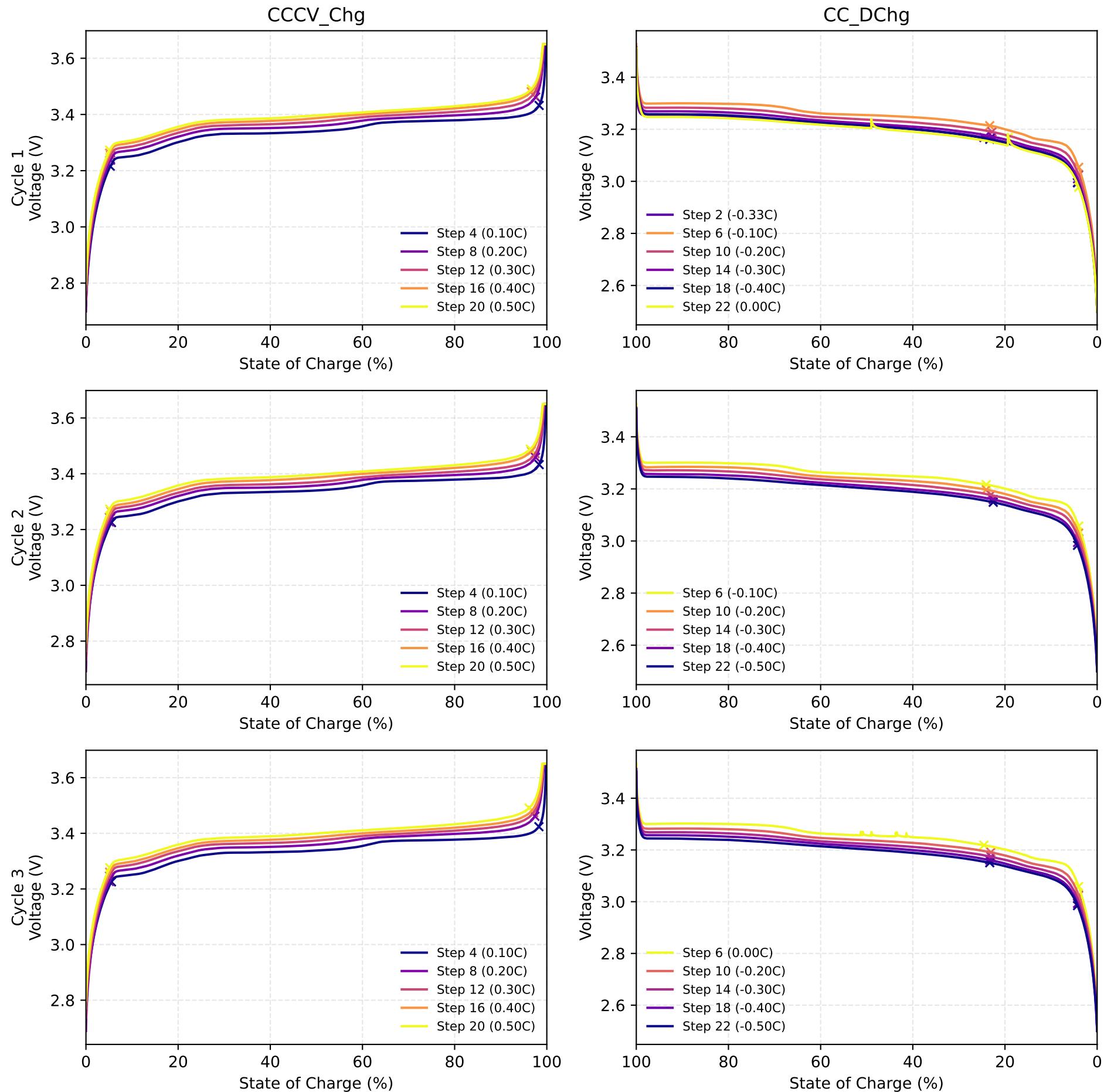
RD_RateCapability_0050 - SoC-V by Cycle and Step Name



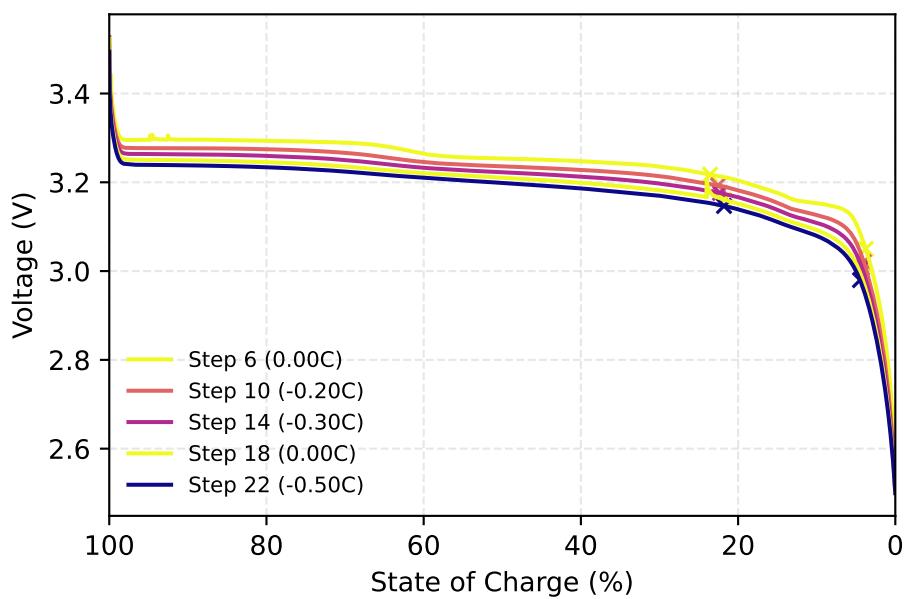
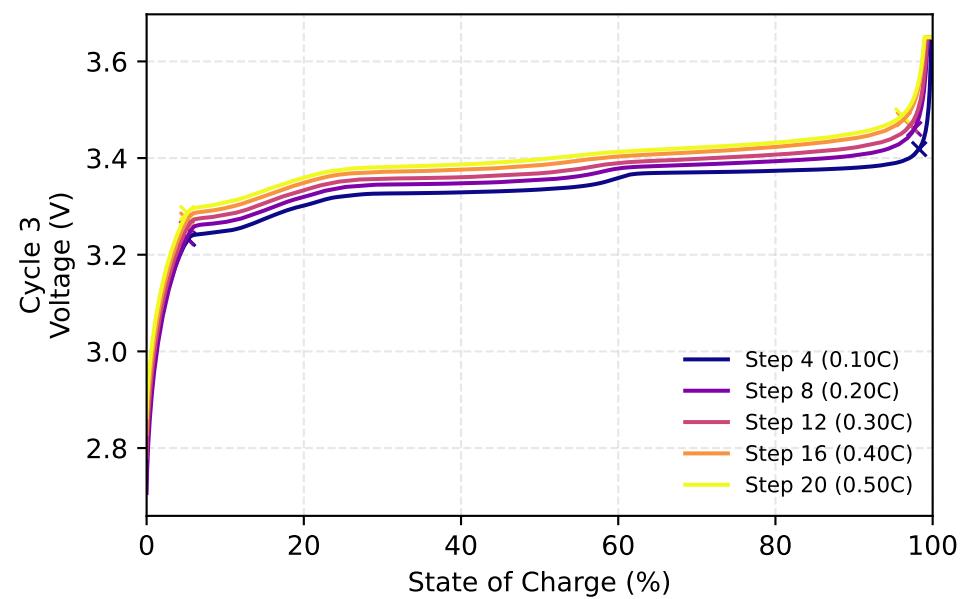
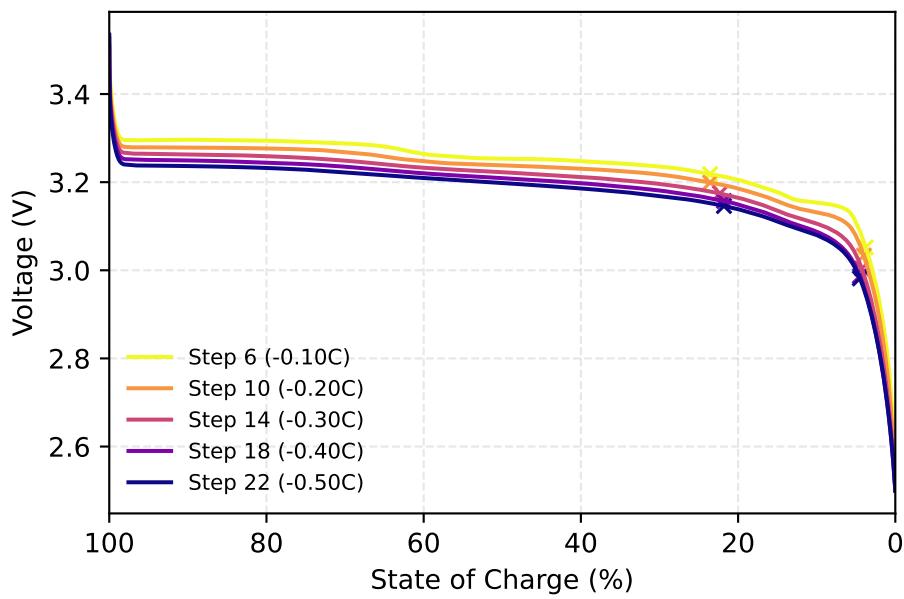
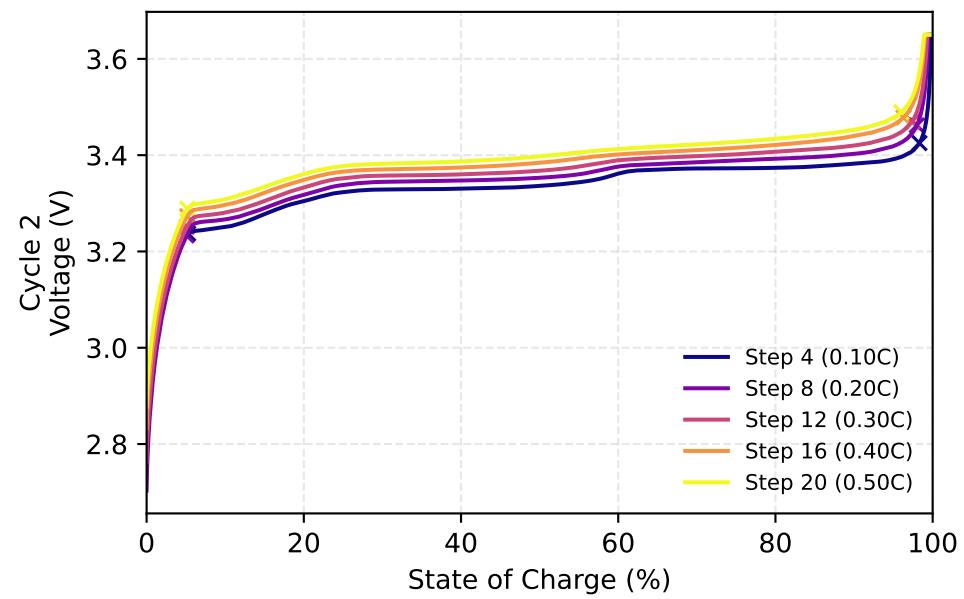
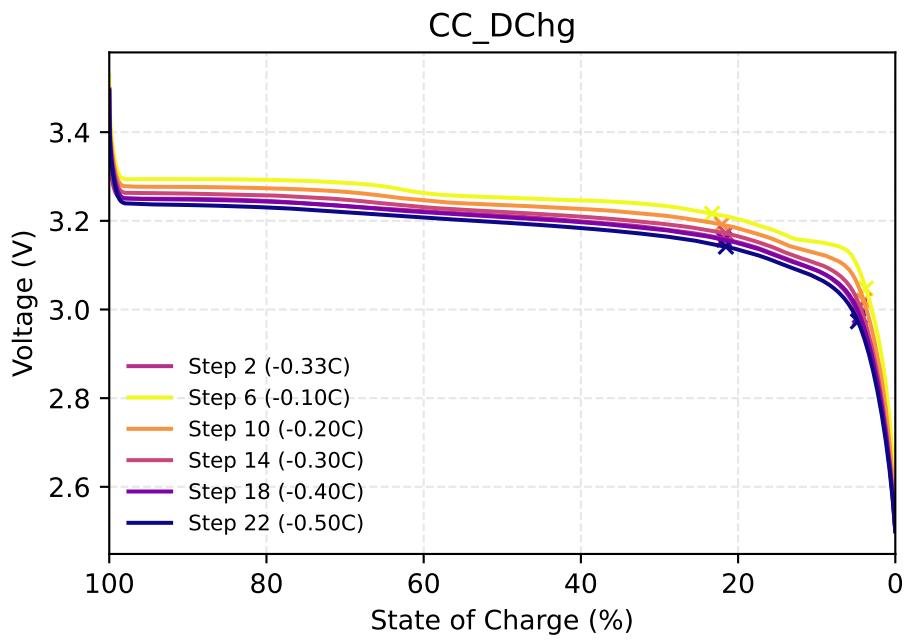
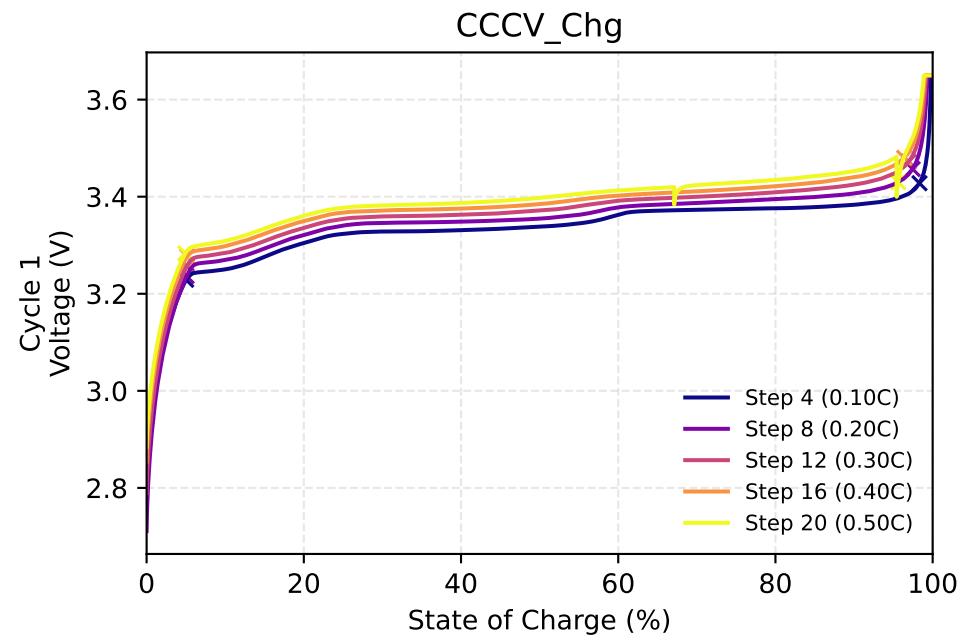
RD_RateCapability_0056 - SoC-V by Cycle and Step Name



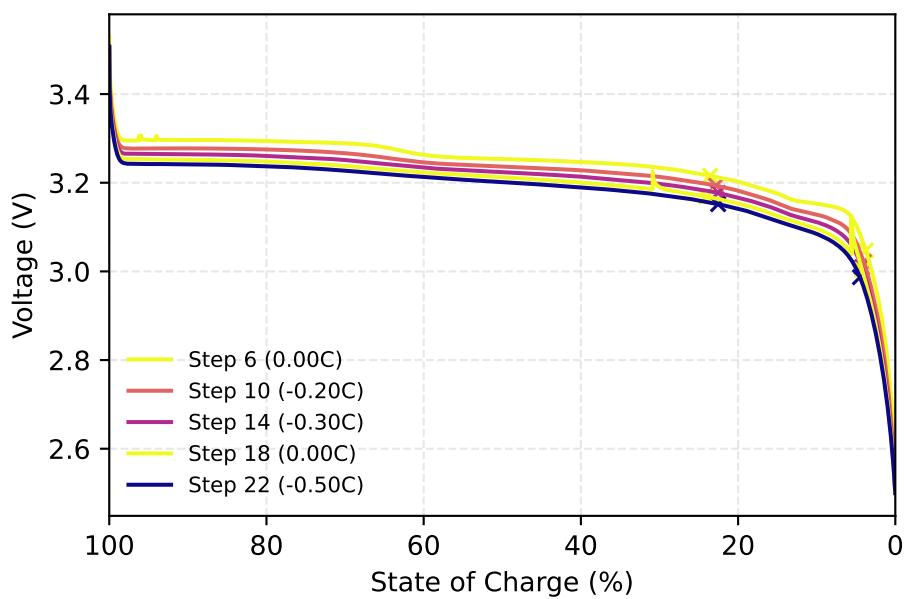
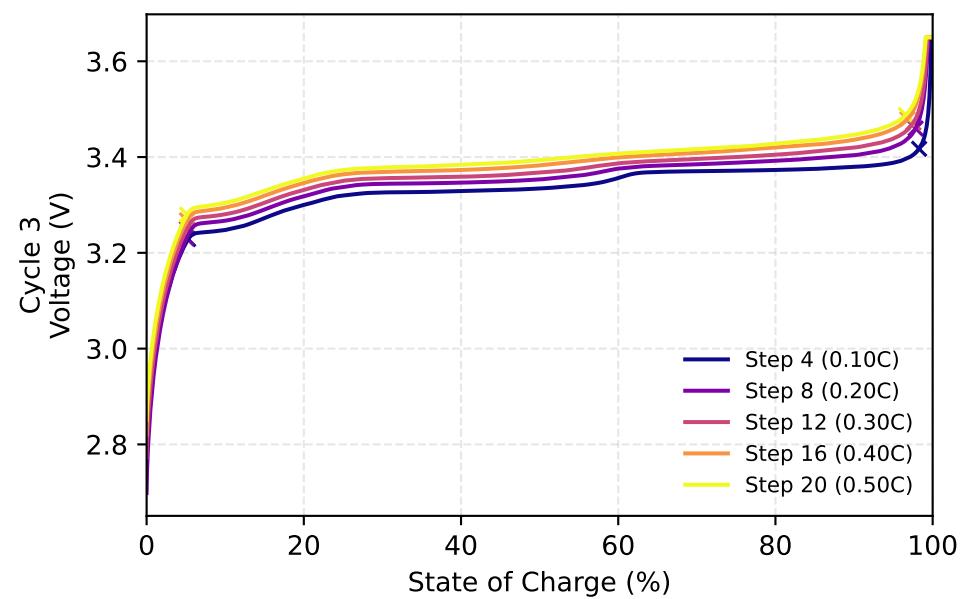
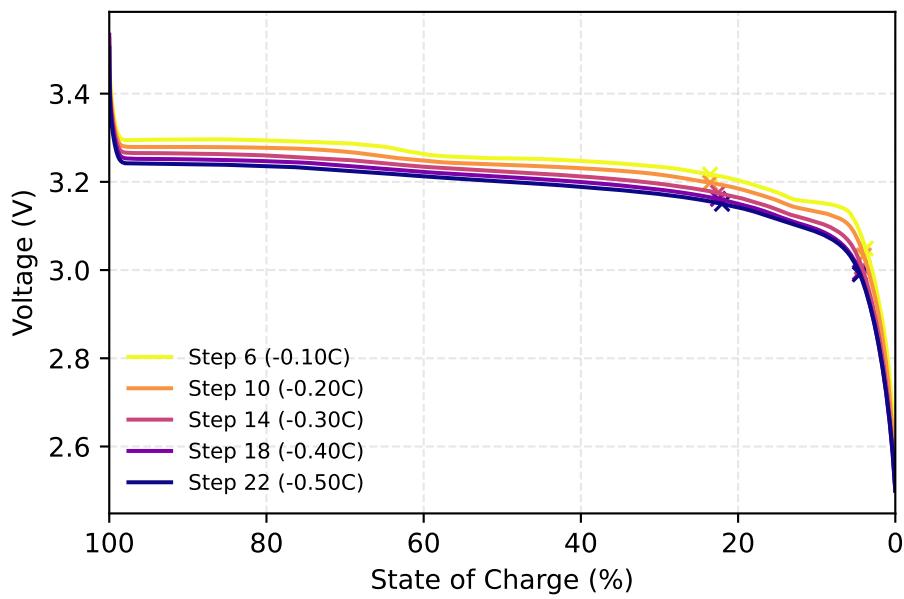
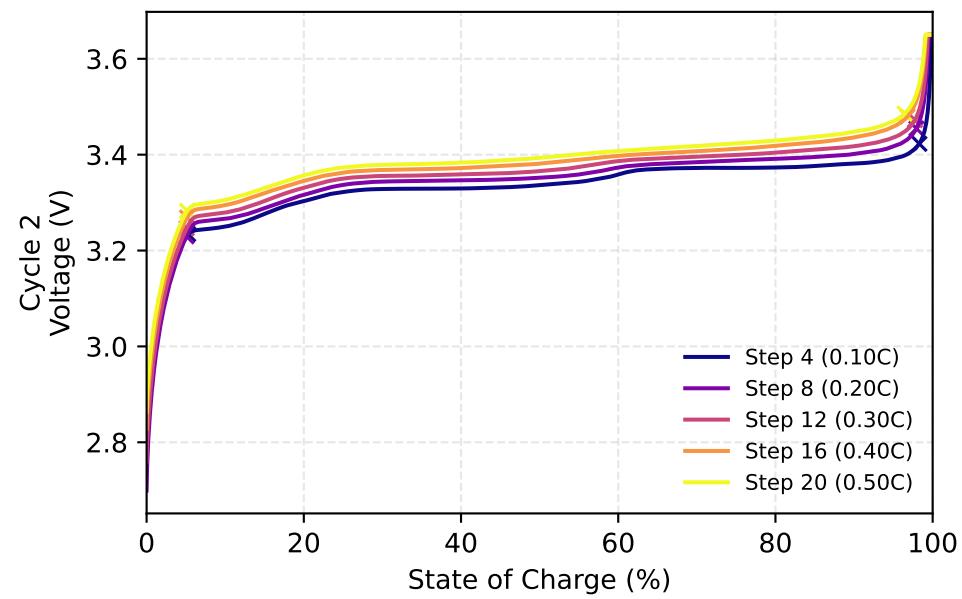
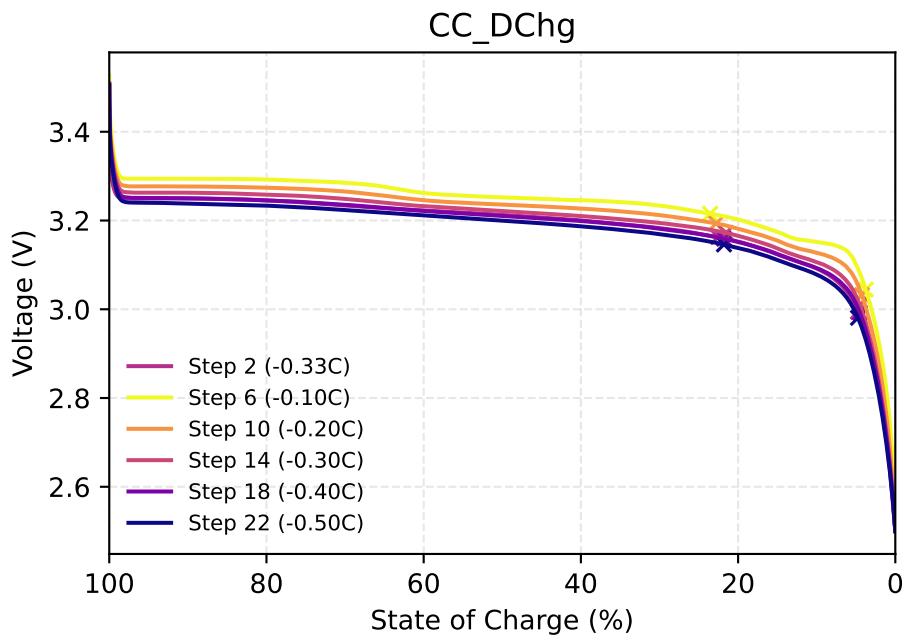
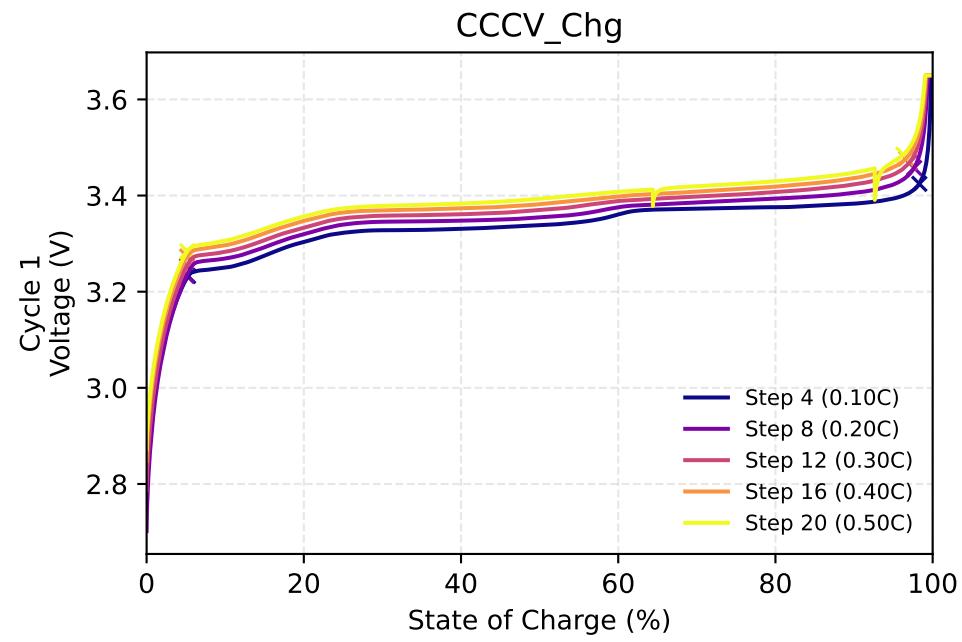
RD_RateCapability_0057 - SoC-V by Cycle and Step Name



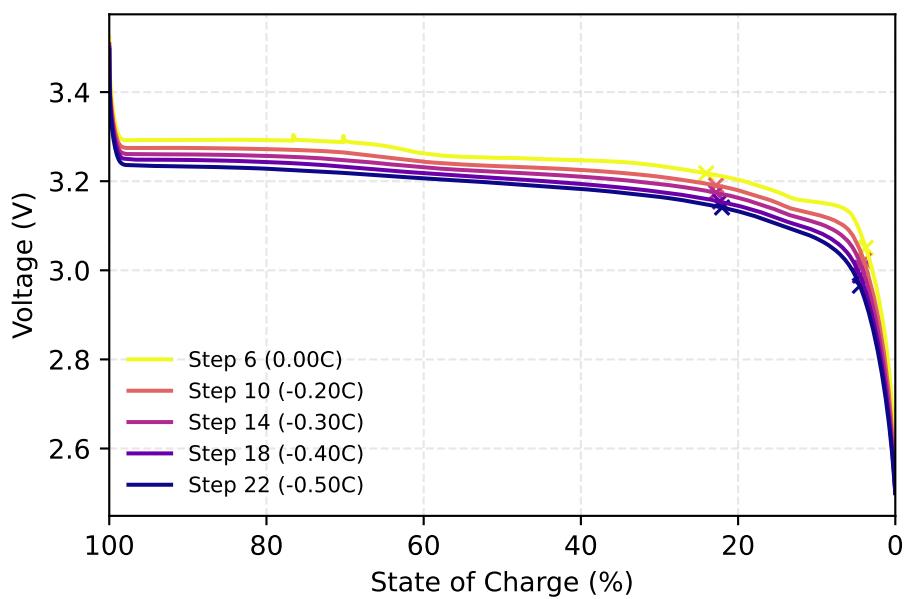
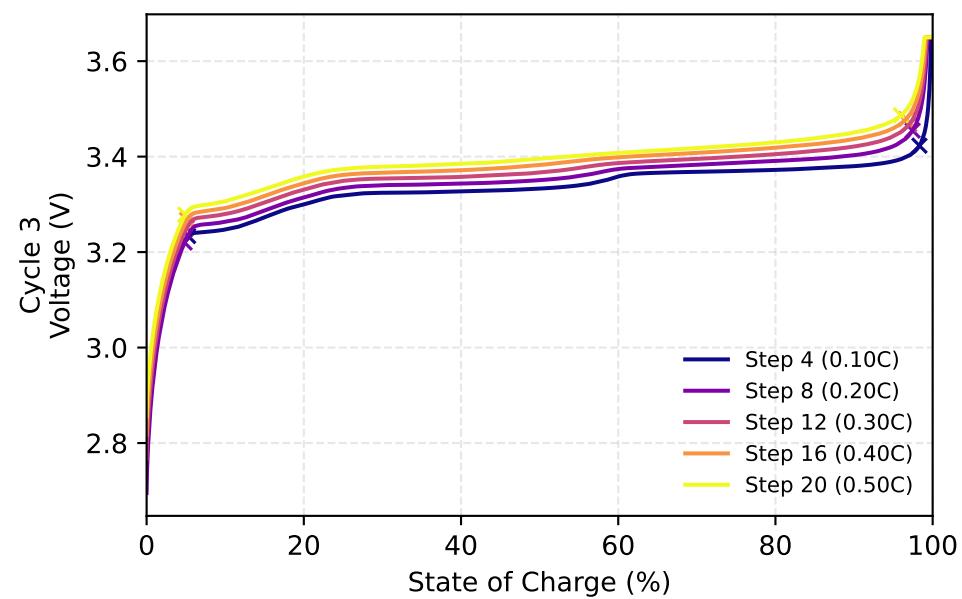
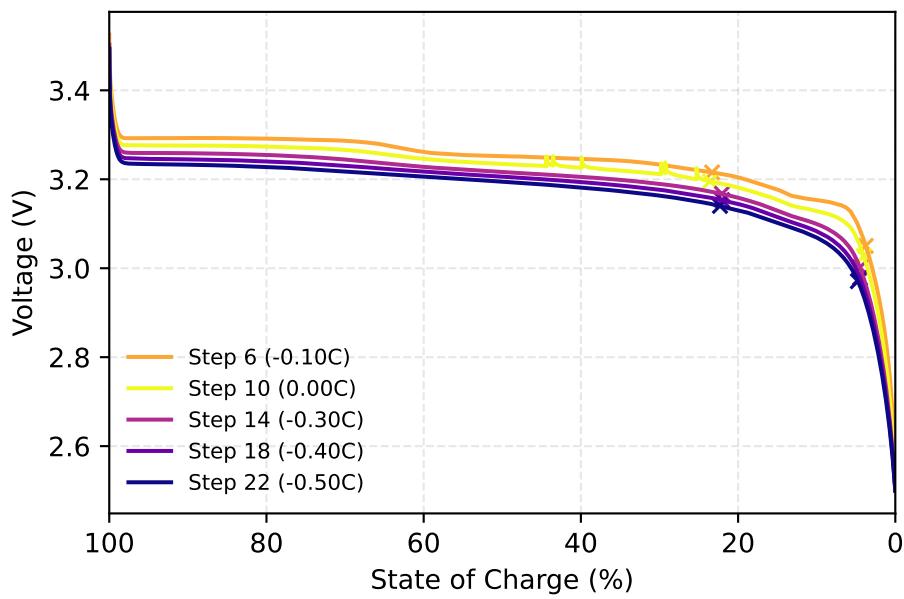
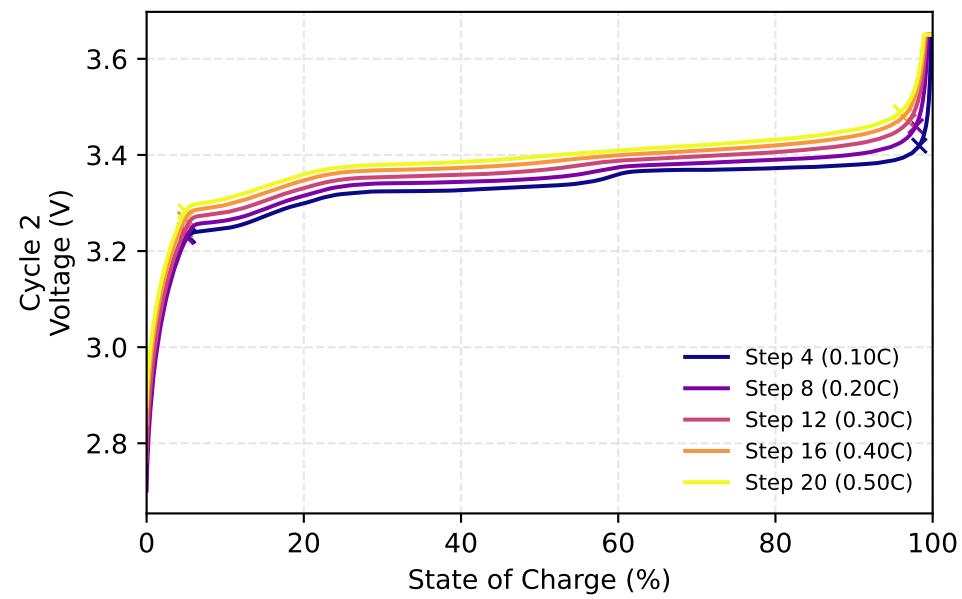
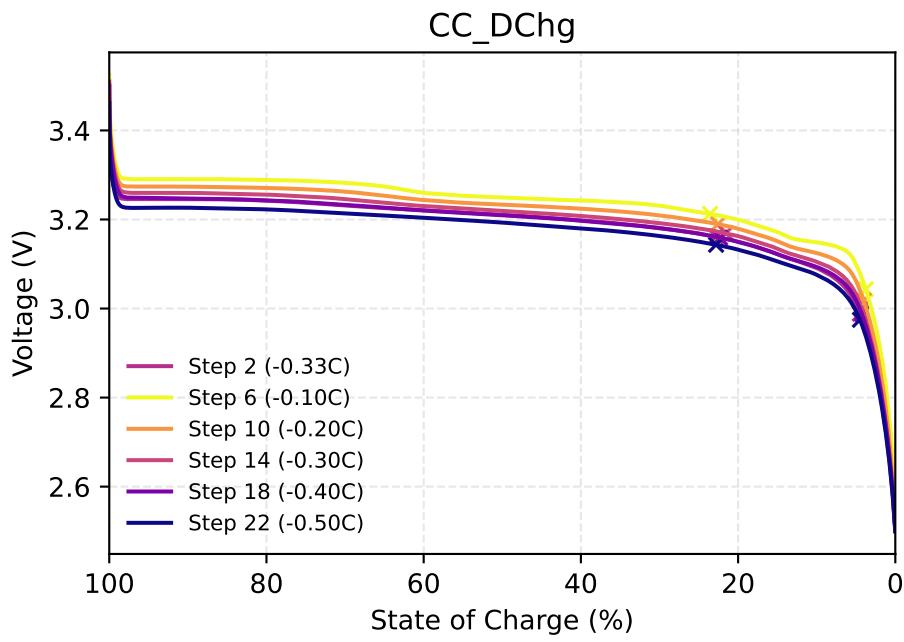
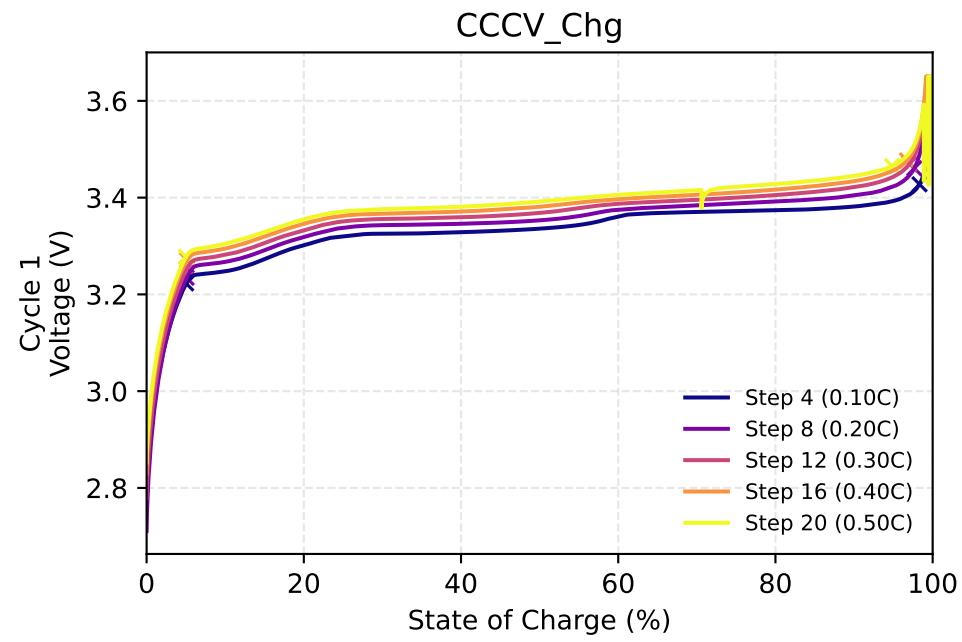
RD_RateCapability_0065 - SoC-V by Cycle and Step Name



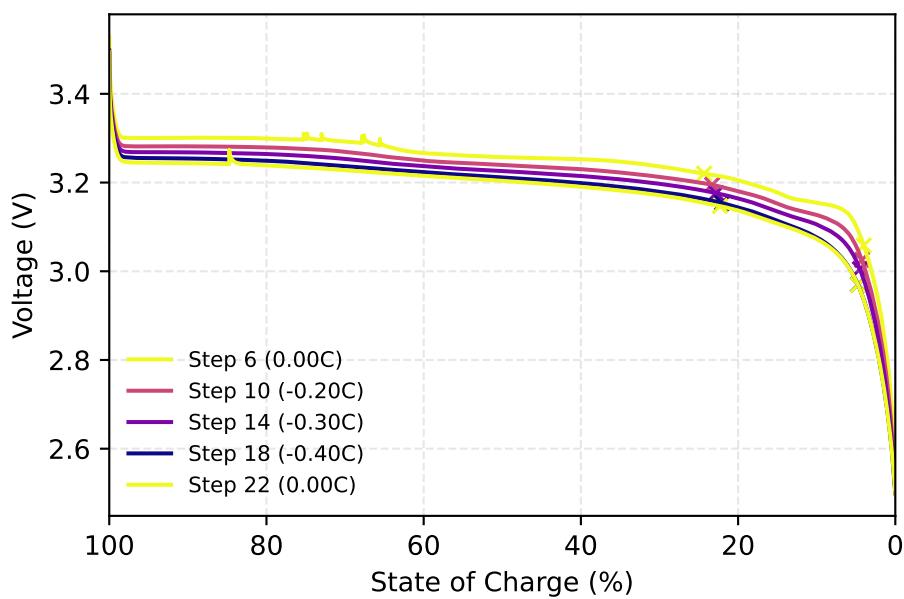
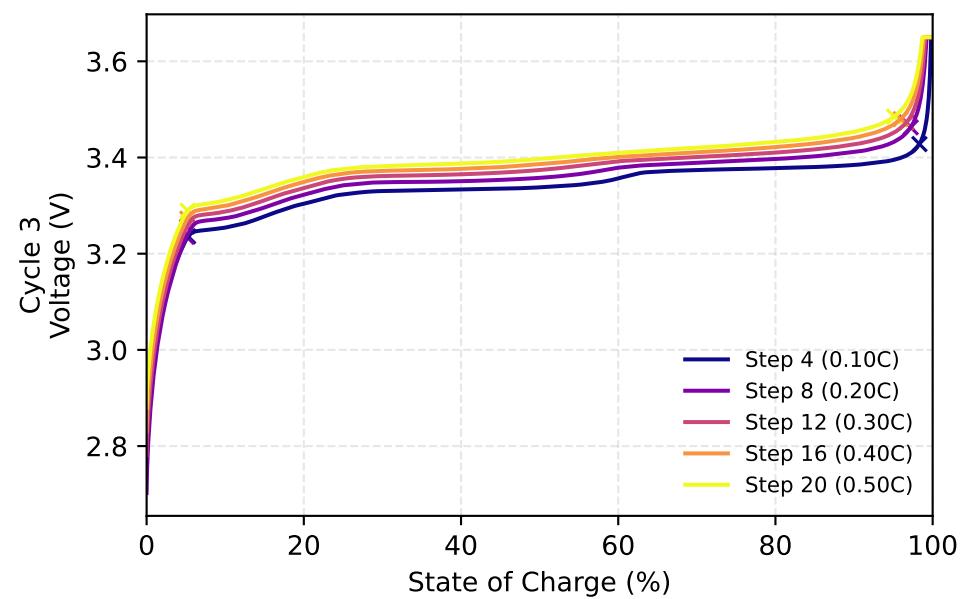
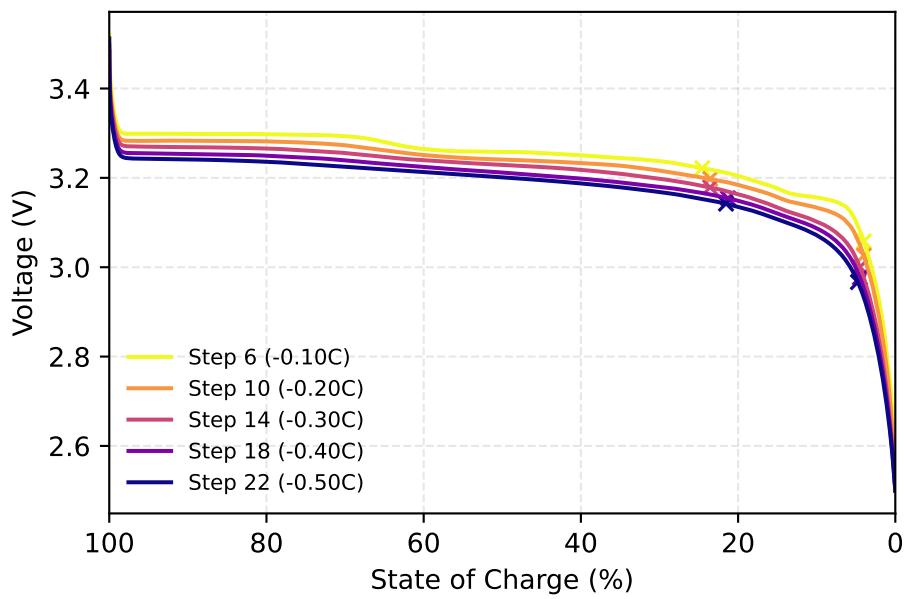
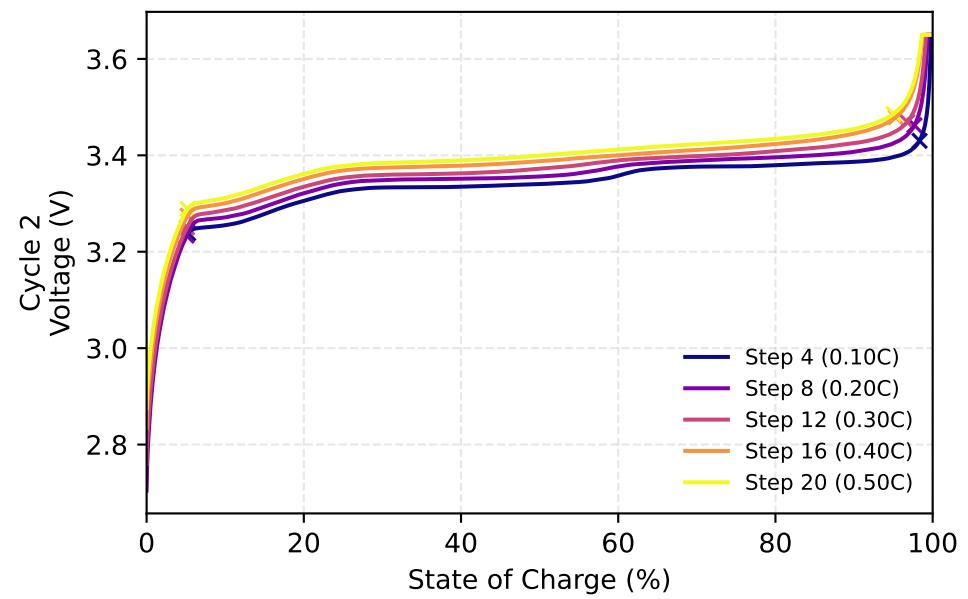
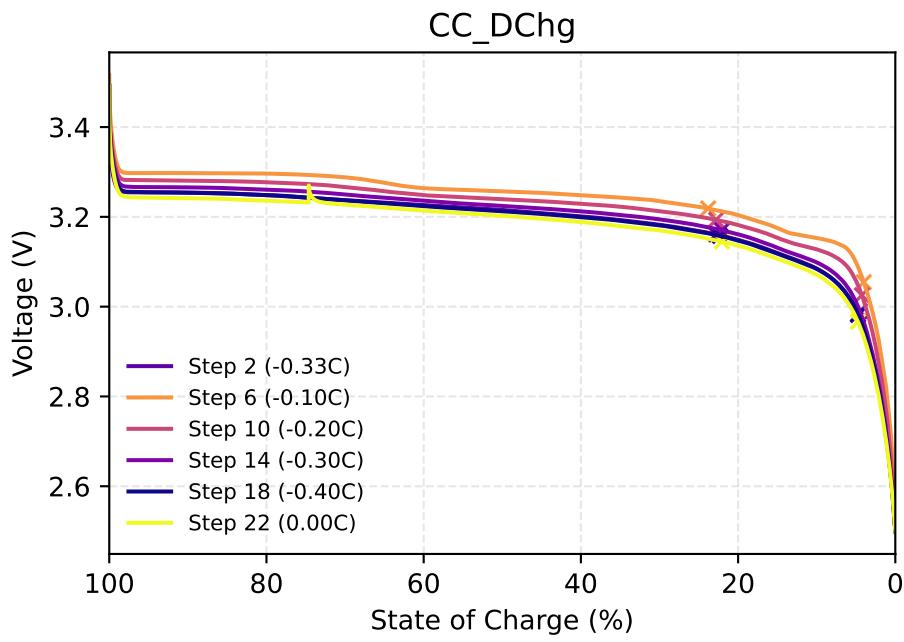
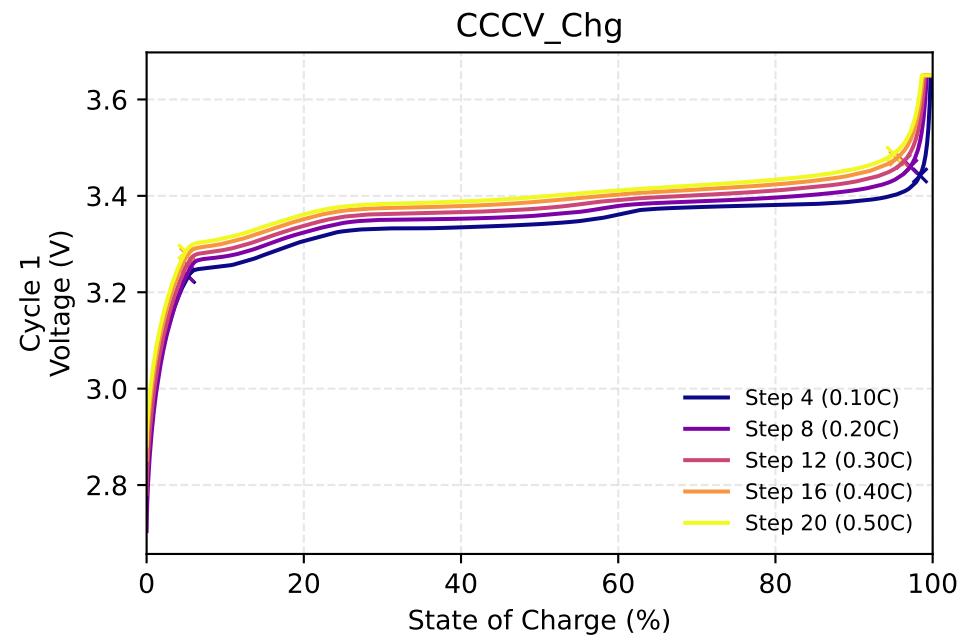
RD_RateCapability_0074 - SoC-V by Cycle and Step Name



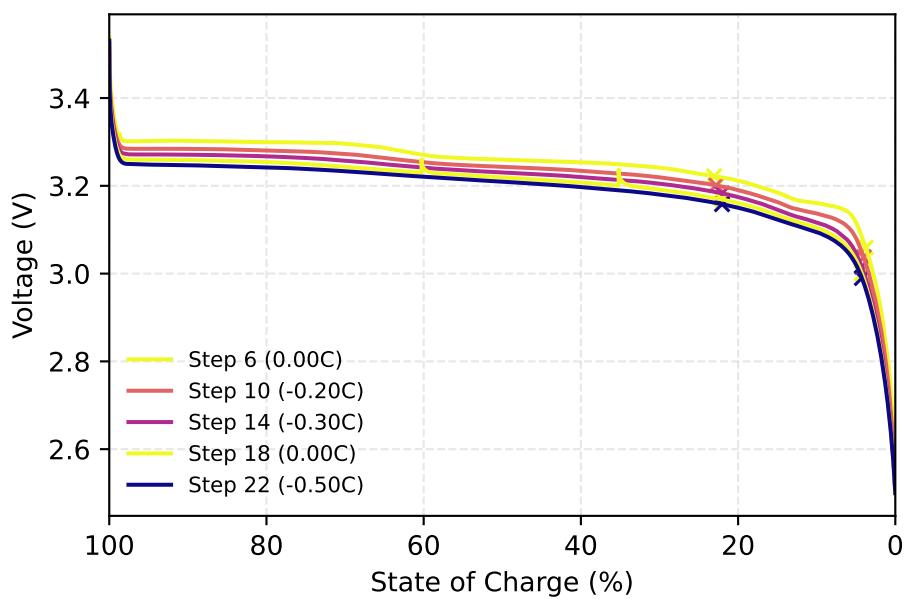
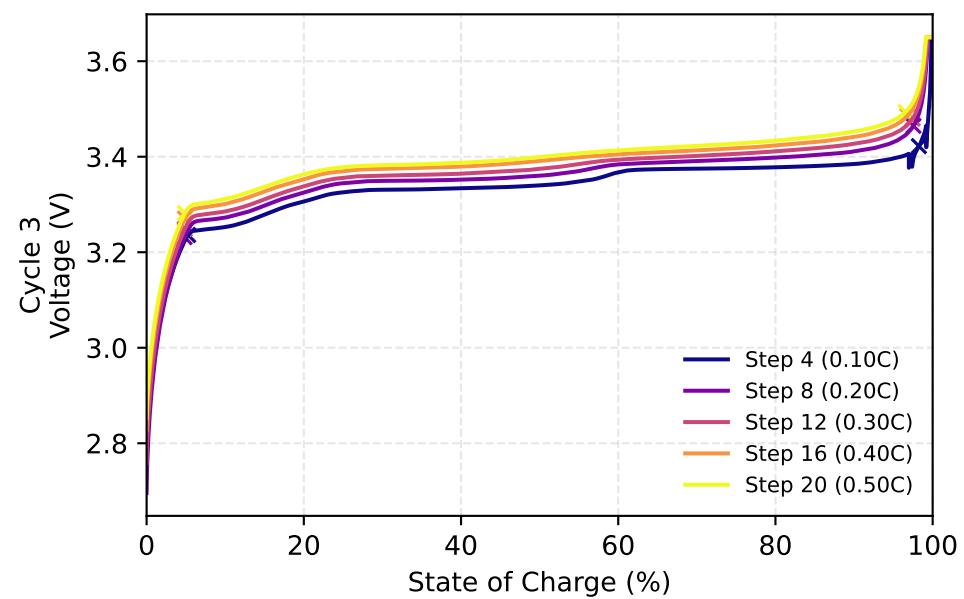
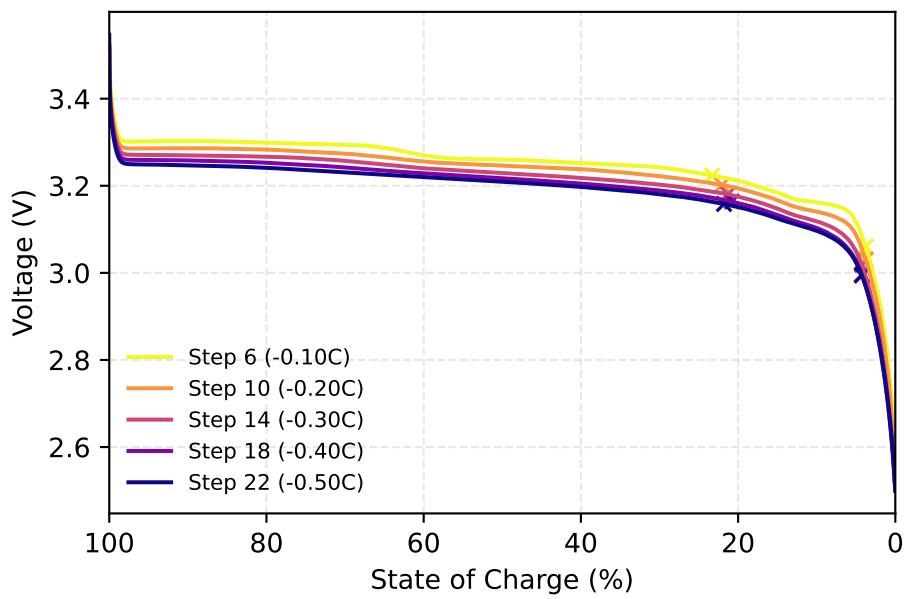
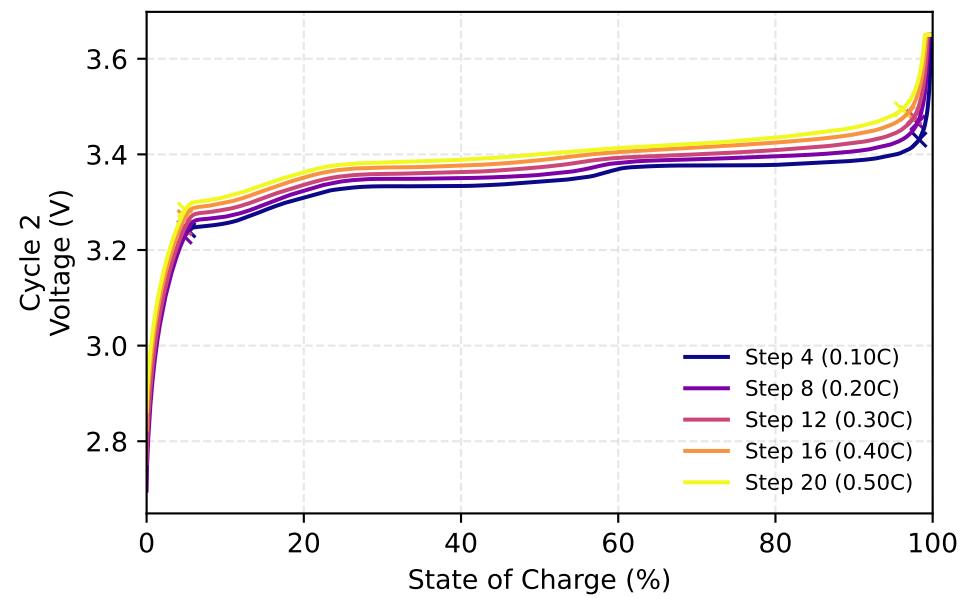
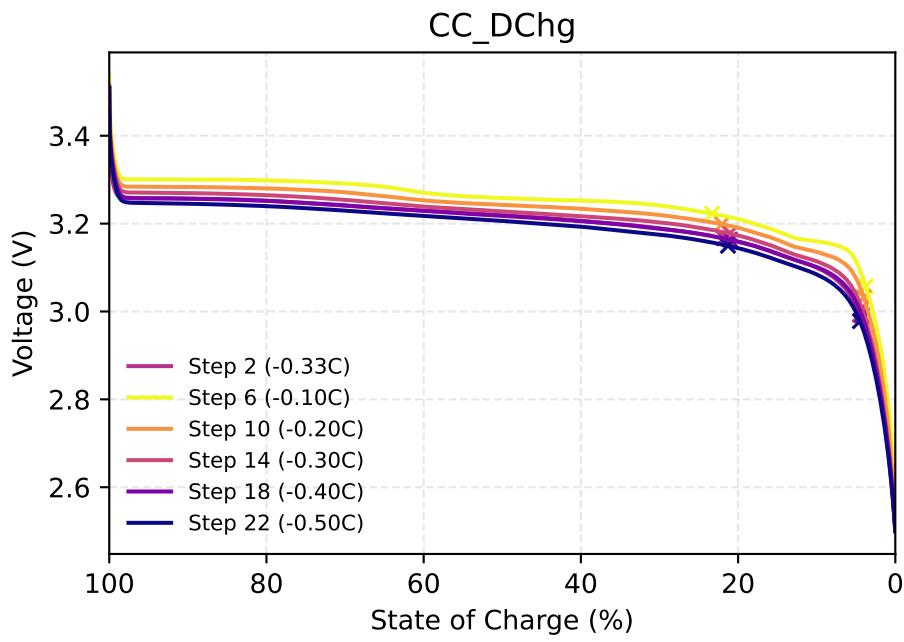
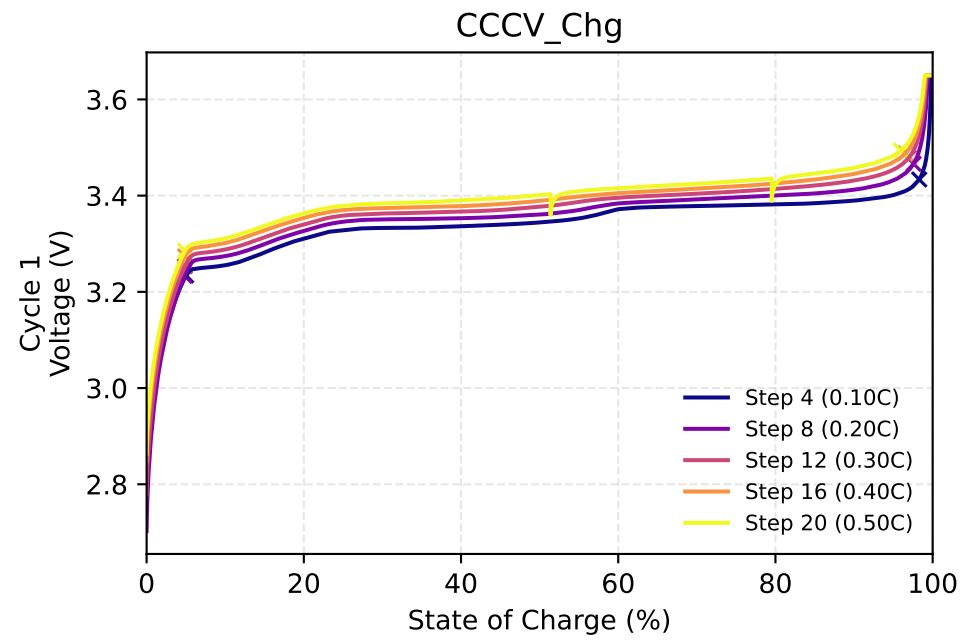
RD_RateCapability_0078 - SoC-V by Cycle and Step Name



RD_RateCapability_0080 - SoC-V by Cycle and Step Name



RD_RateCapability_0087 - SoC-V by Cycle and Step Name



RD_RateCapability_0091 - SoC-V by Cycle and Step Name

