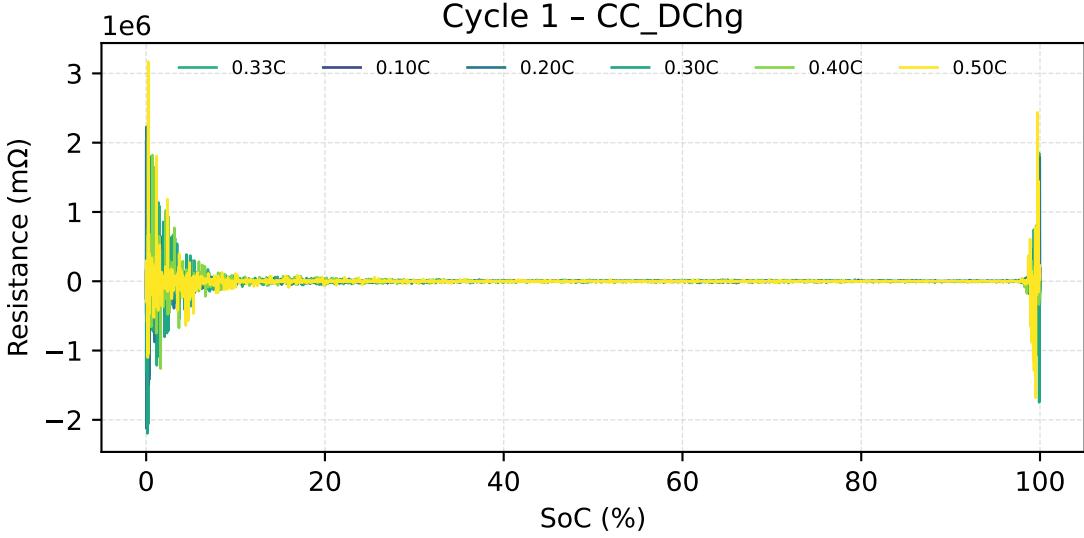
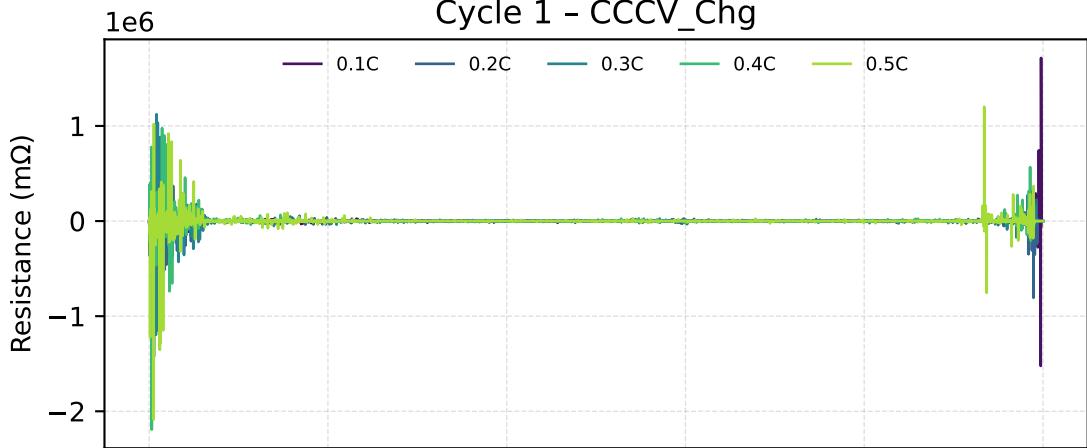


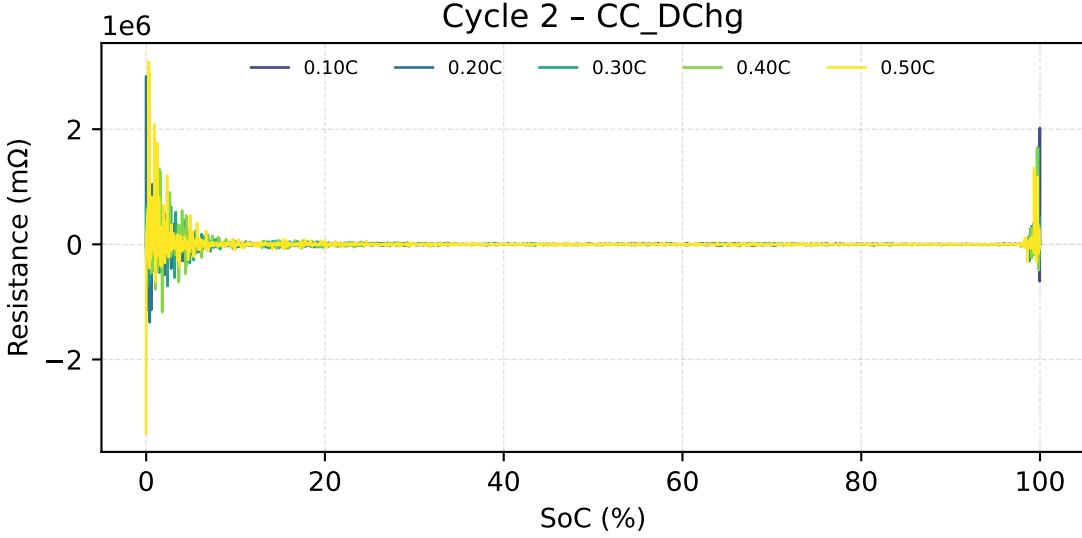
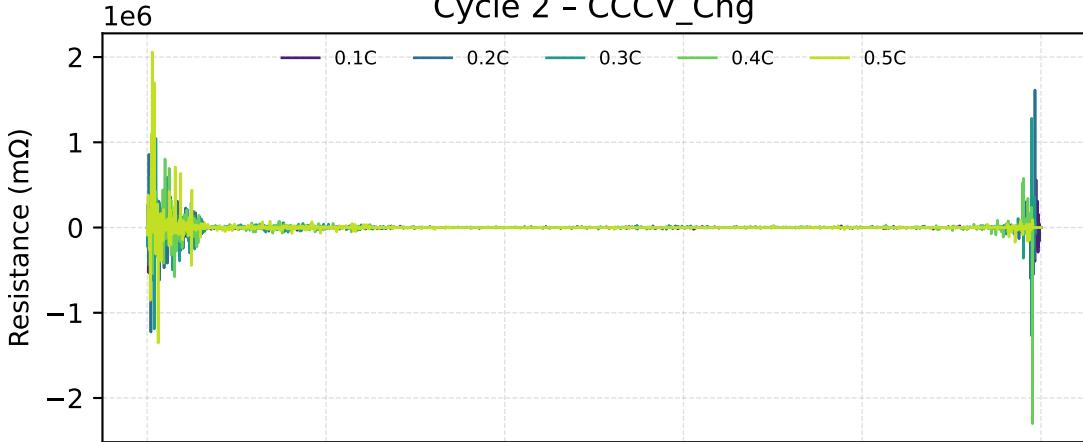
# SoC vs Resistance – RD\_RateCapability\_0001

## Cycle 1 – CCCV\_Chg



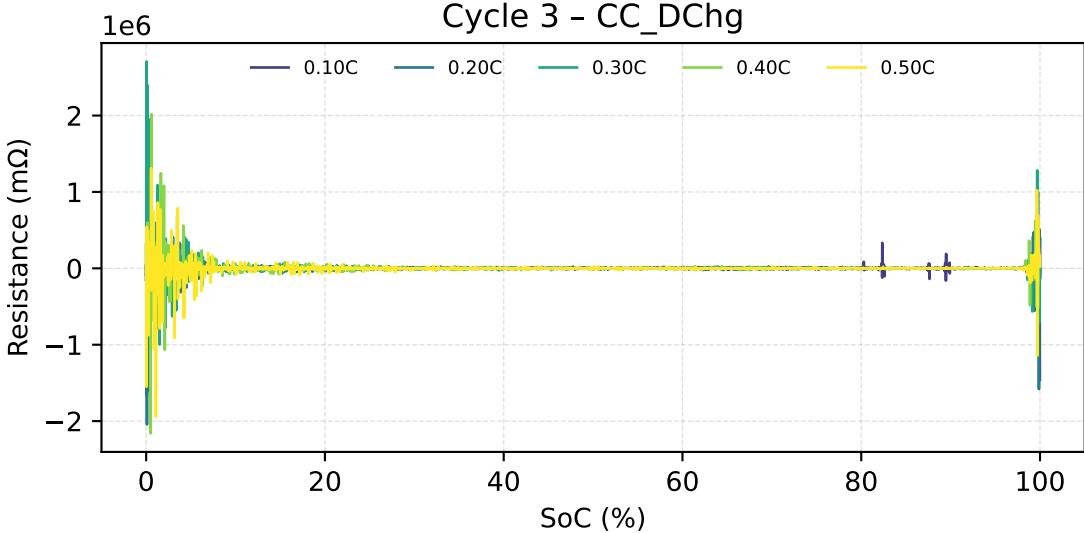
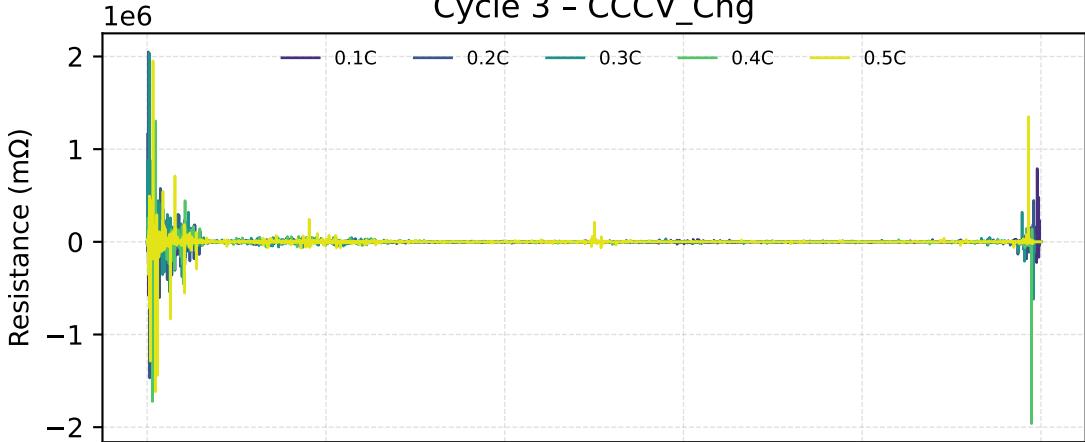
# SoC vs Resistance – RD\_RateCapability\_0001

## Cycle 2 – CCCV\_Chg



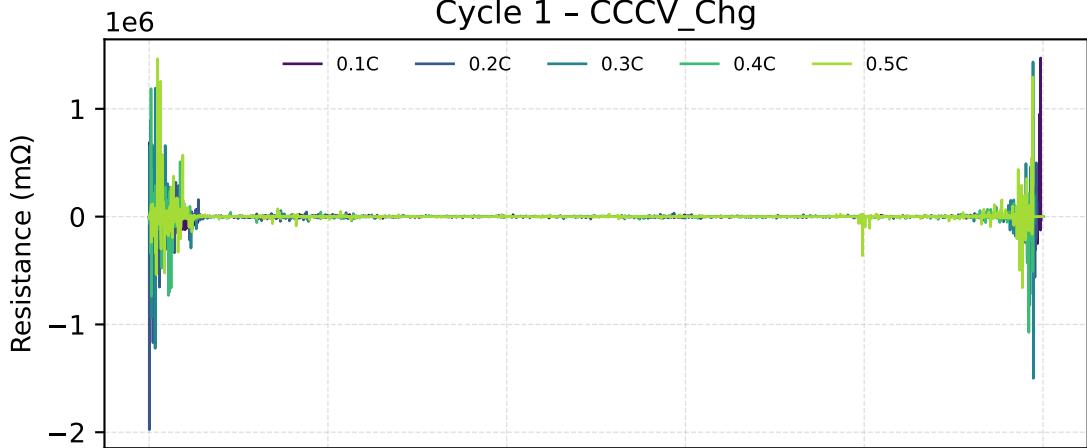
# SoC vs Resistance – RD\_RateCapability\_0001

## Cycle 3 – CCCV\_Chg

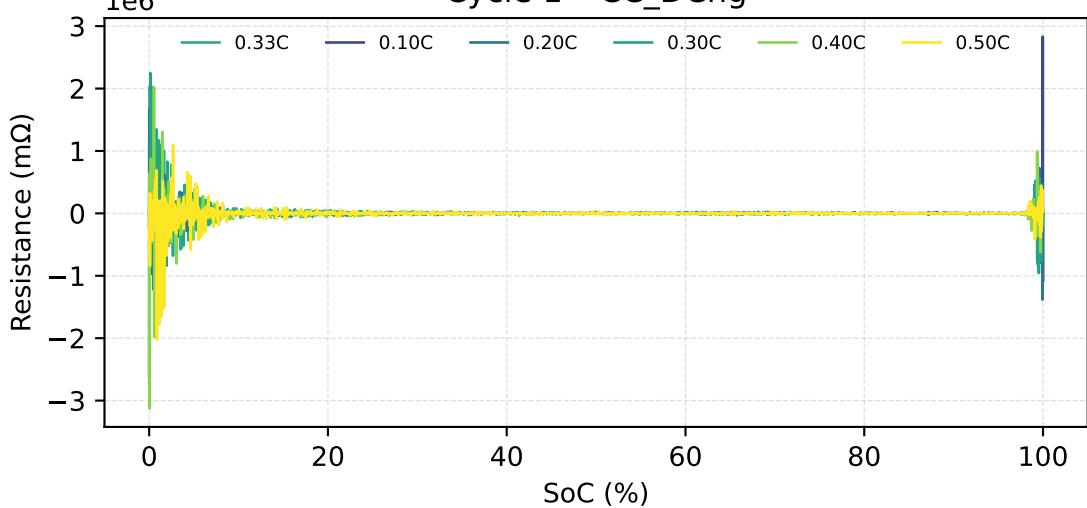


# SoC vs Resistance – RD\_RateCapability\_0003

Cycle 1 - CCCV\_Chg

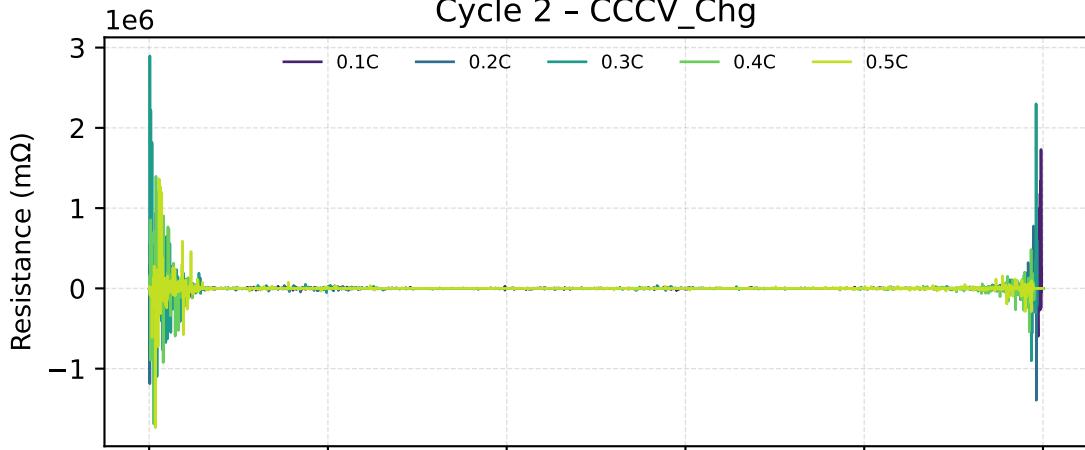


Cycle 1 - CC\_DChg

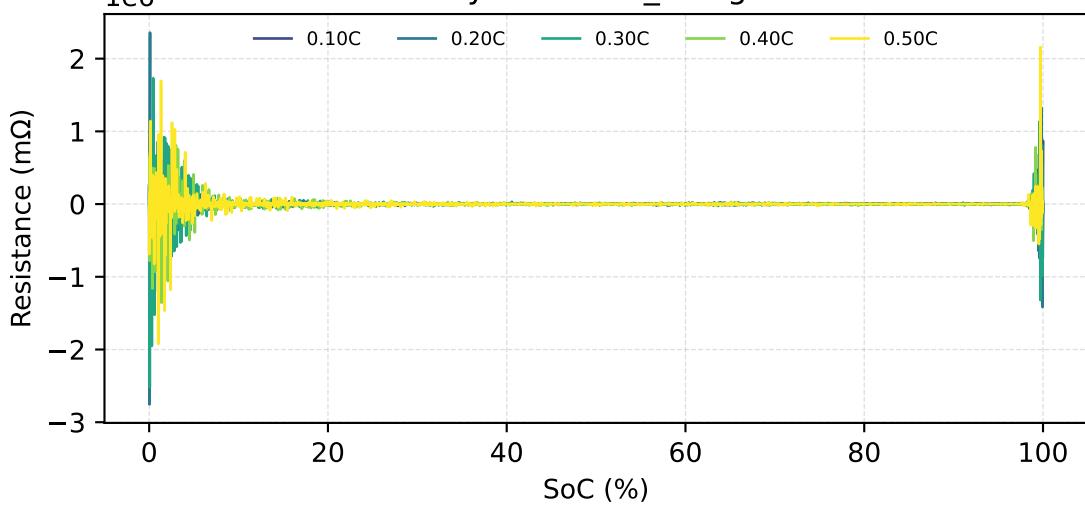


# SoC vs Resistance – RD\_RateCapability\_0003

Cycle 2 – CCCV\_Chg

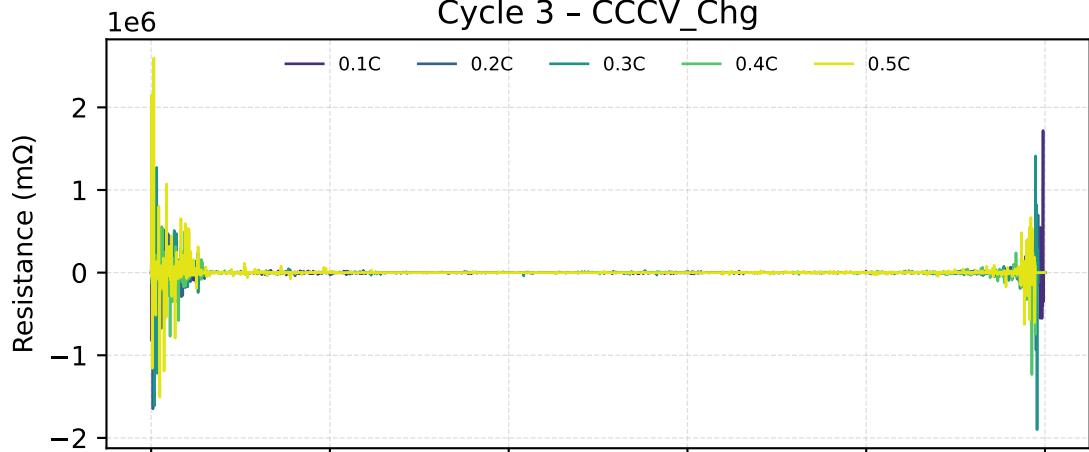


Cycle 2 – CC\_DChg

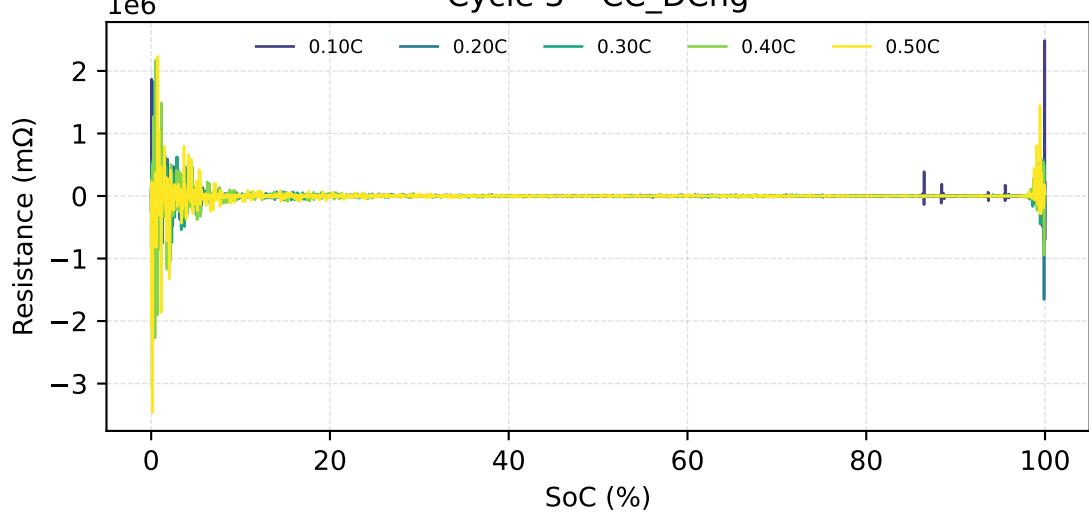


# SoC vs Resistance – RD\_RateCapability\_0003

Cycle 3 – CCCV\_Chg

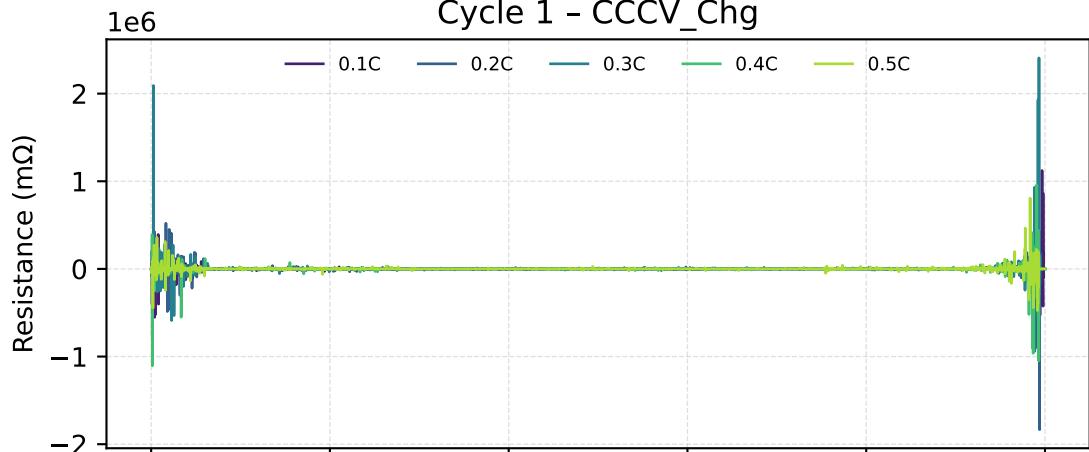


Cycle 3 – CC\_DChg

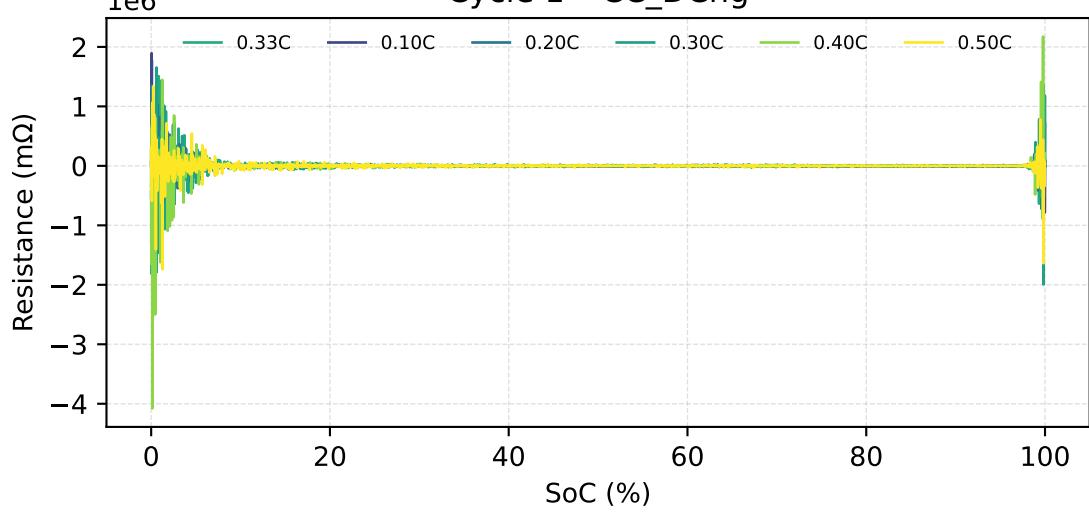


# SoC vs Resistance – RD\_RateCapability\_0004

Cycle 1 - CCCV\_Chg

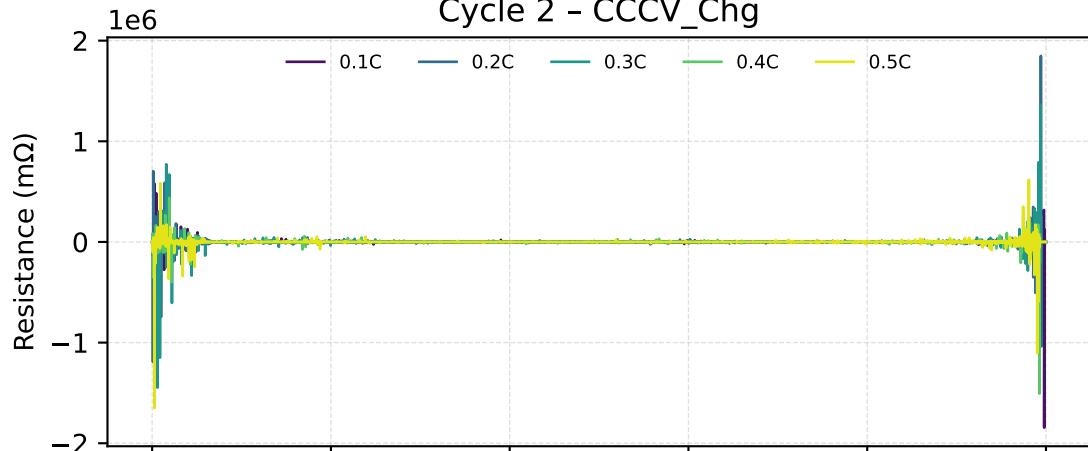


Cycle 1 - CC\_DChg

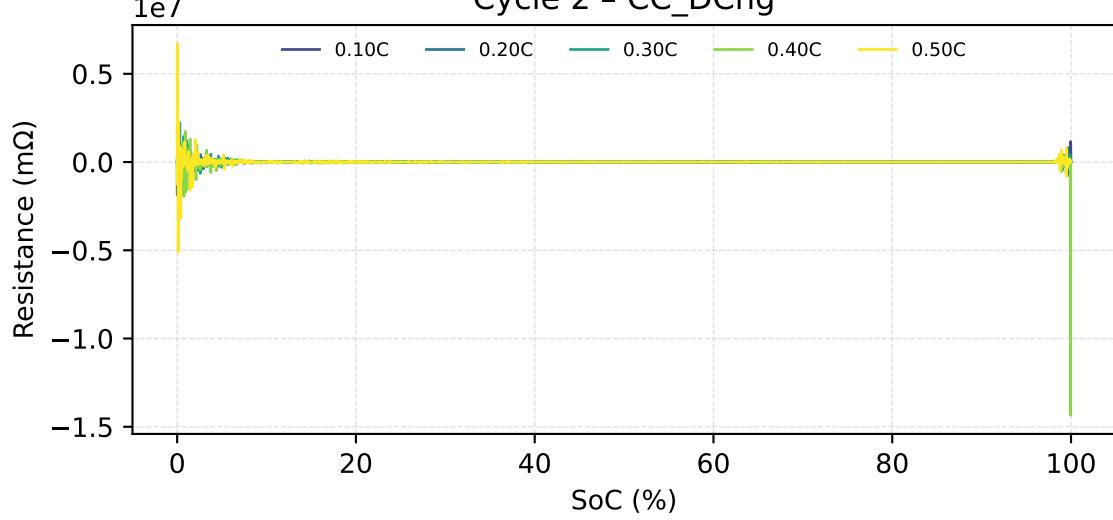


# SoC vs Resistance – RD\_RateCapability\_0004

Cycle 2 – CCCV\_Chg

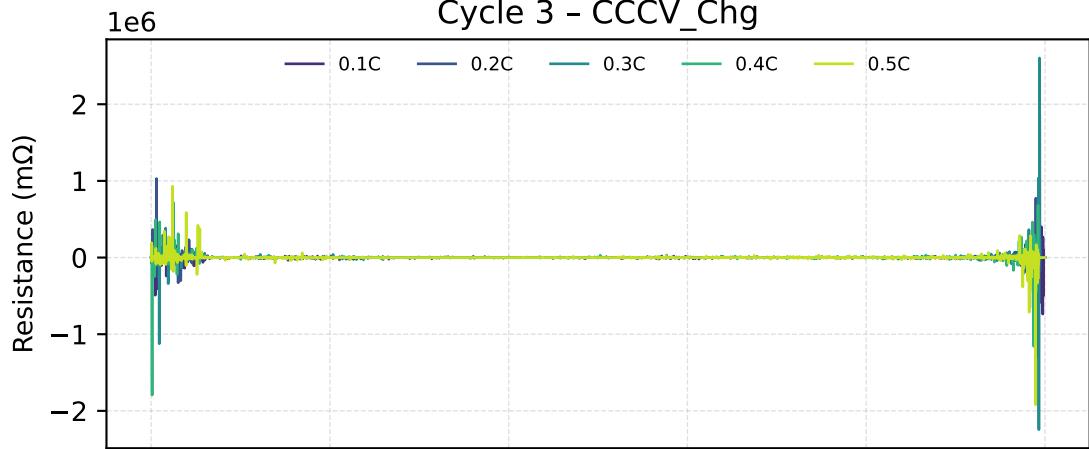


Cycle 2 – CC\_DChg

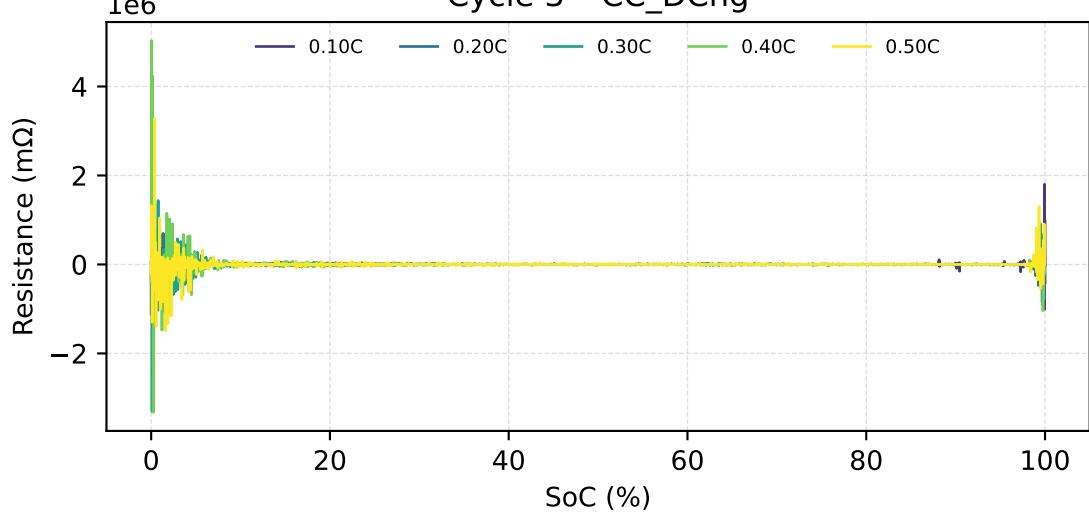


# SoC vs Resistance – RD\_RateCapability\_0004

Cycle 3 – CCCV\_Chg

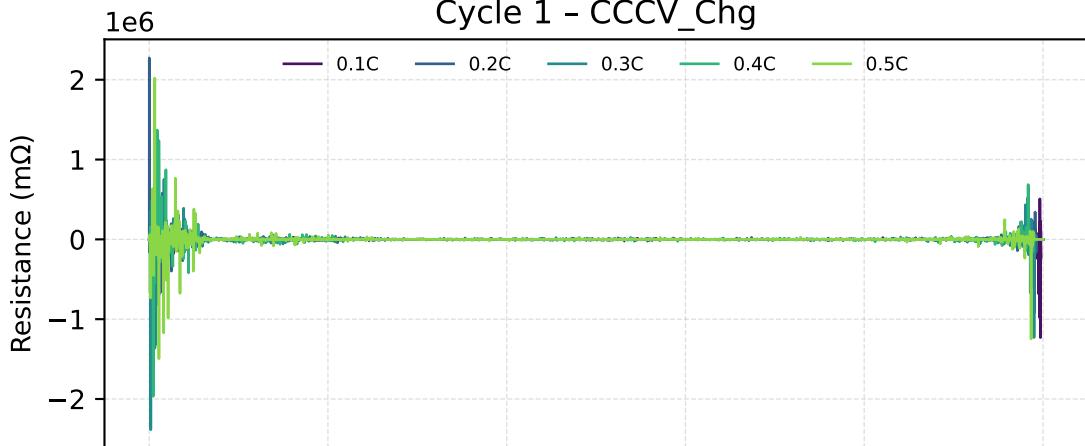


Cycle 3 – CC\_DChg

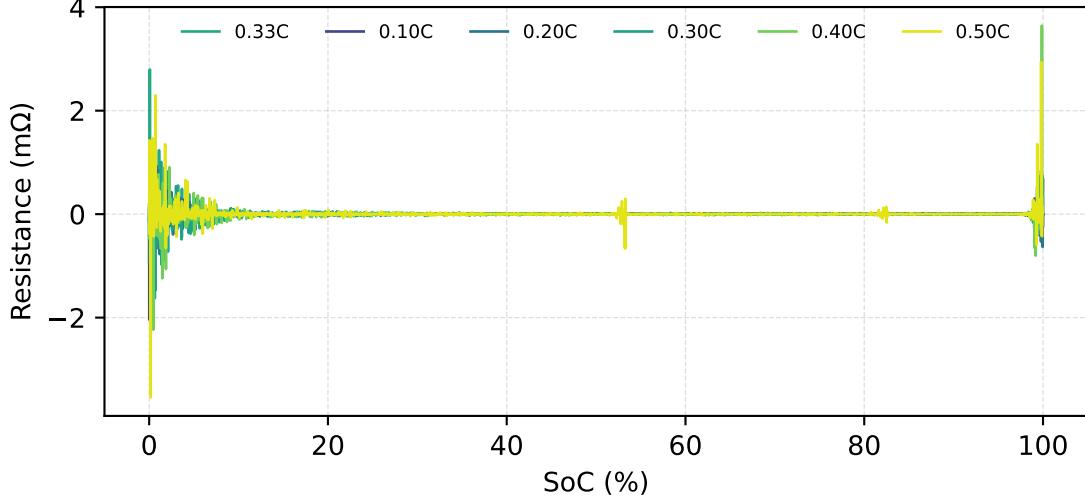


# SoC vs Resistance – RD\_RateCapability\_0007

Cycle 1 - CCCV\_Chg

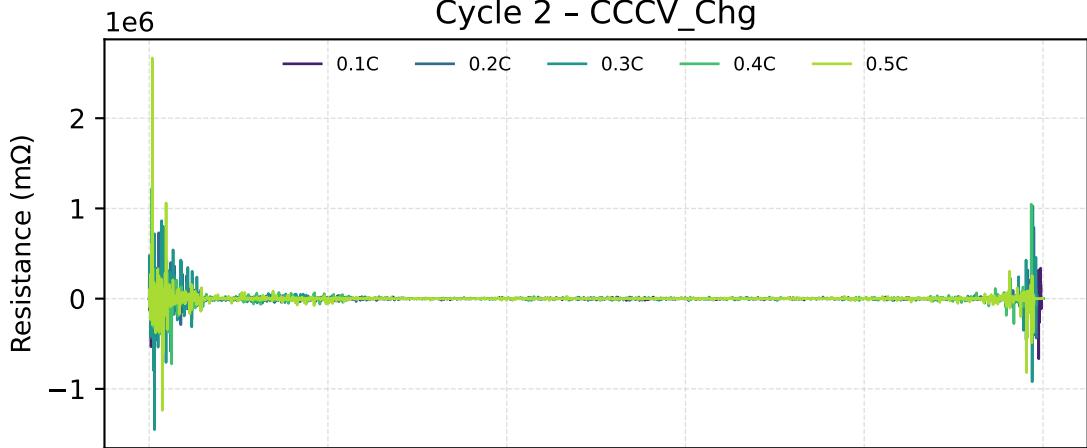


Cycle 1 - CC\_DChg

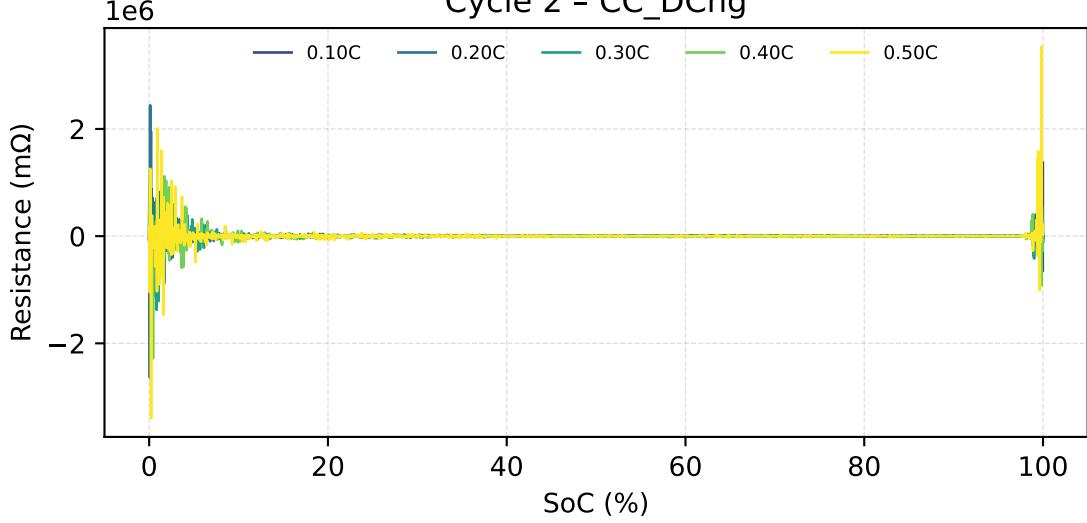


# SoC vs Resistance – RD\_RateCapability\_0007

Cycle 2 – CCCV\_Chg

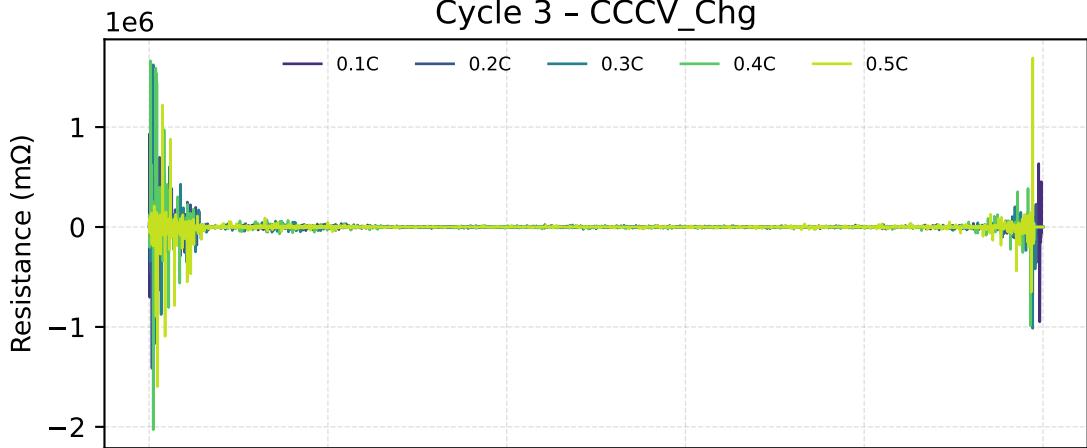


Cycle 2 – CC\_DChg

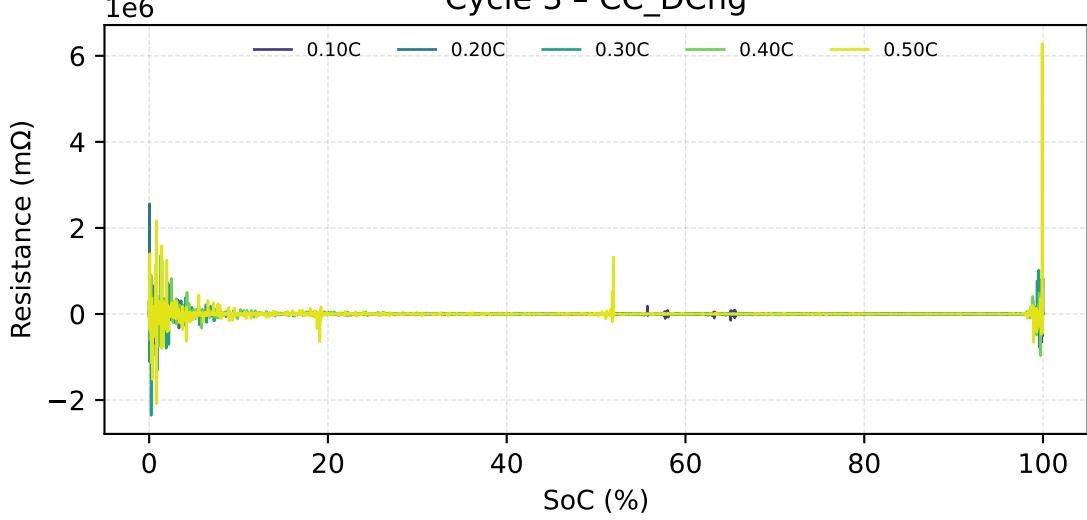


# SoC vs Resistance – RD\_RateCapability\_0007

Cycle 3 – CCCV\_Chg

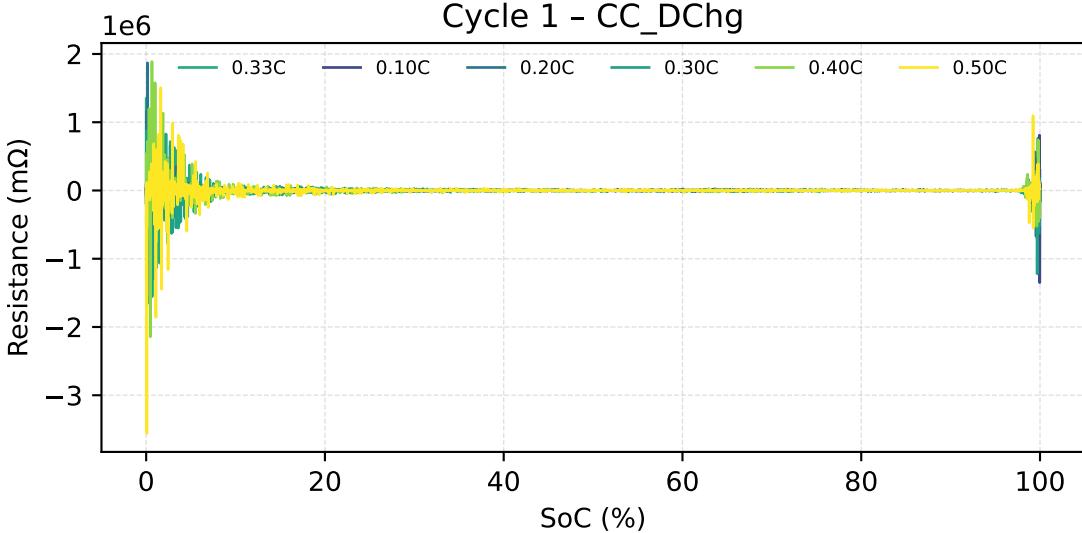
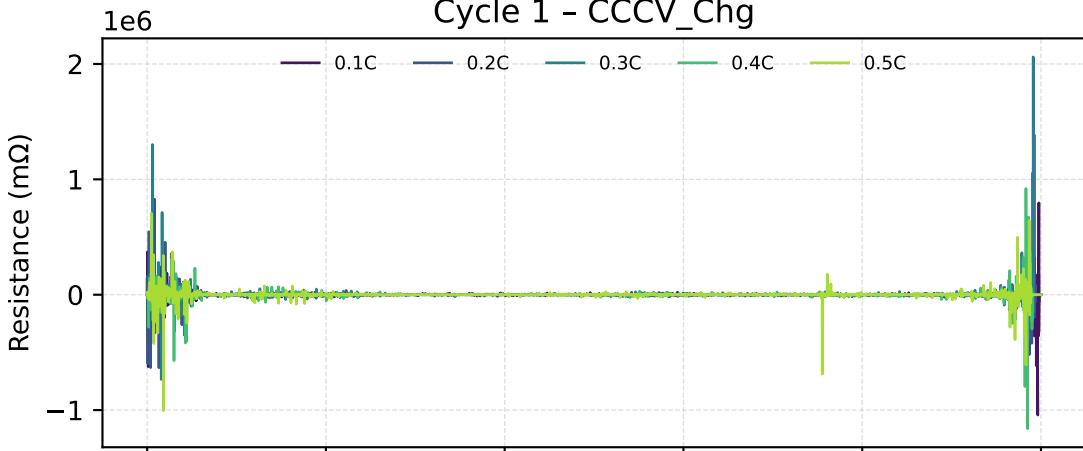


Cycle 3 – CC\_DChg



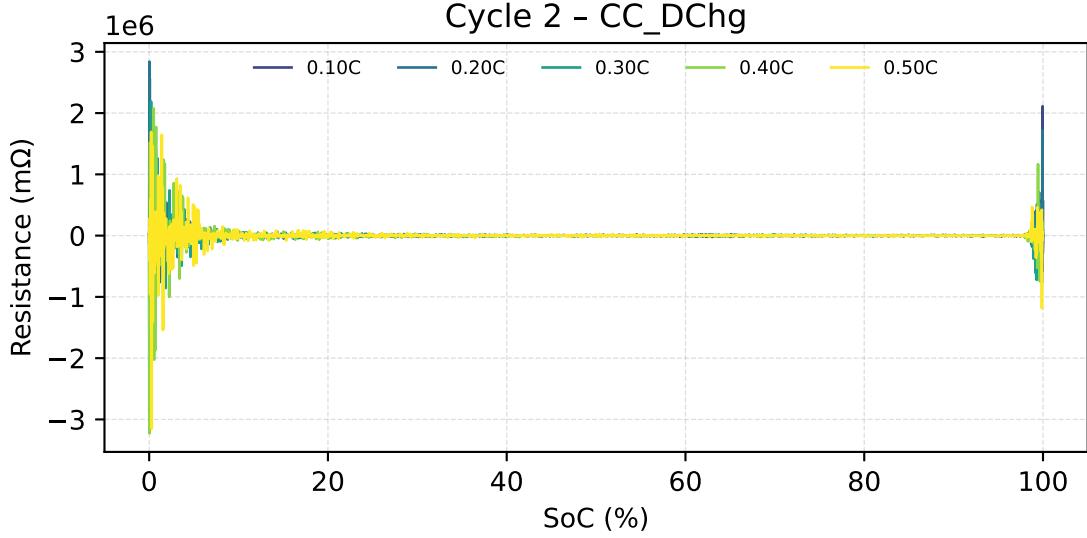
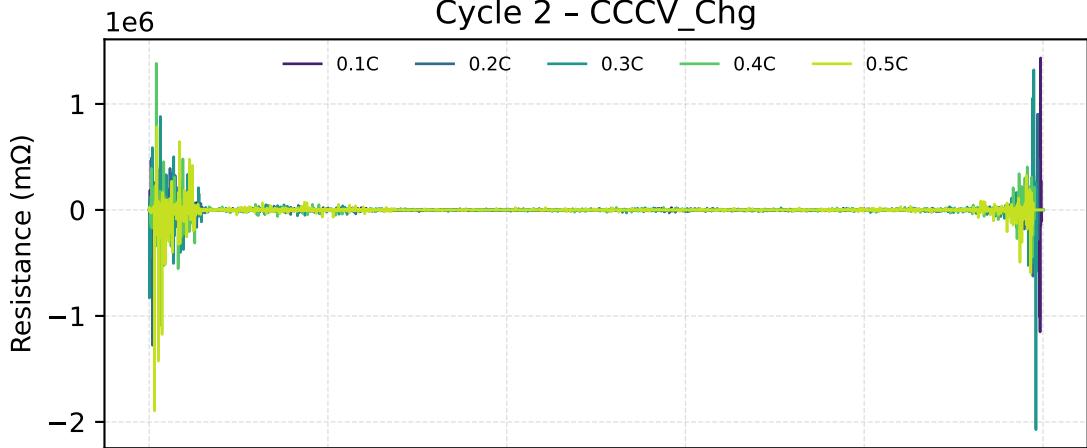
# SoC vs Resistance – RD\_RateCapability\_0011

## Cycle 1 – CCCV\_Chg



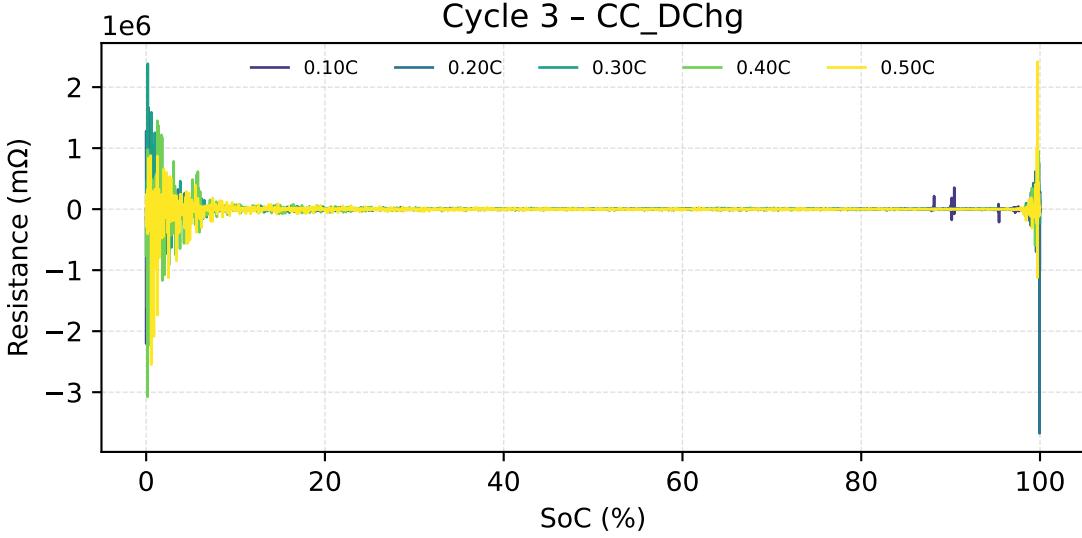
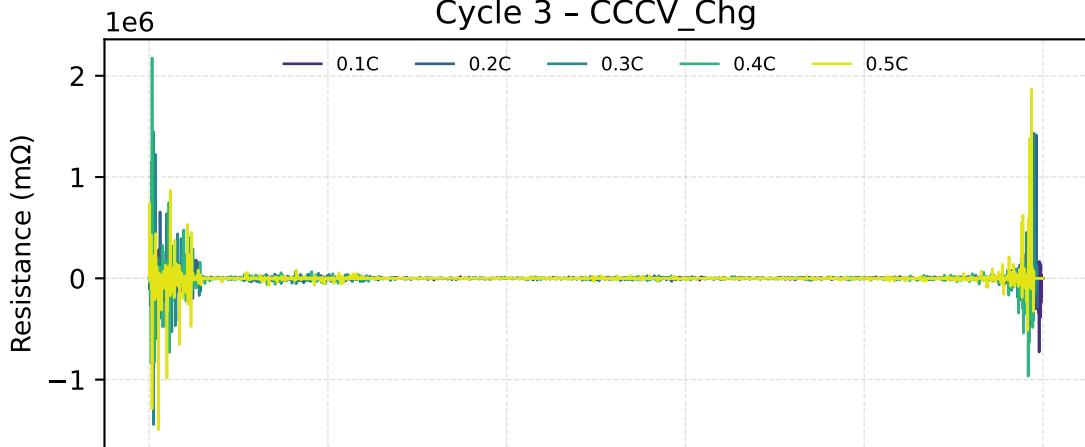
# SoC vs Resistance – RD\_RateCapability\_0011

## Cycle 2 – CCCV\_Chg



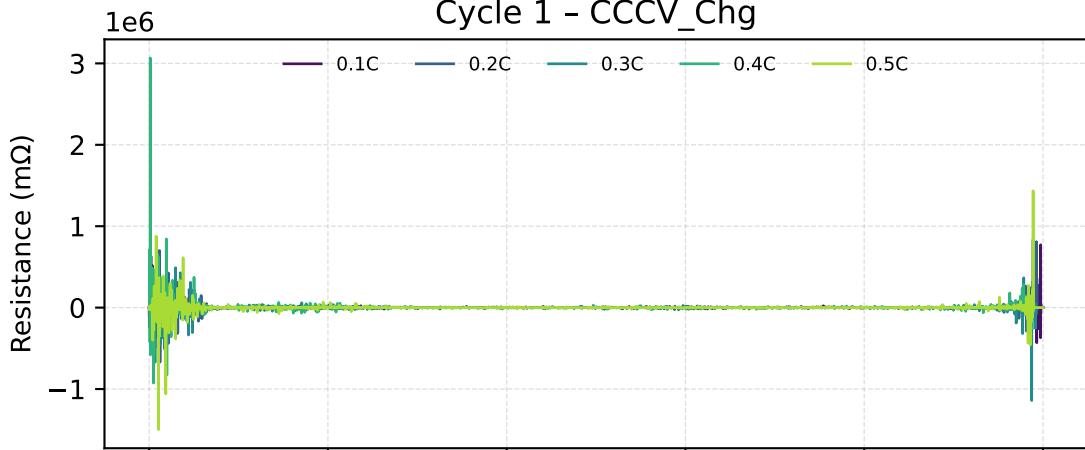
# SoC vs Resistance – RD\_RateCapability\_0011

## Cycle 3 – CCCV\_Chg

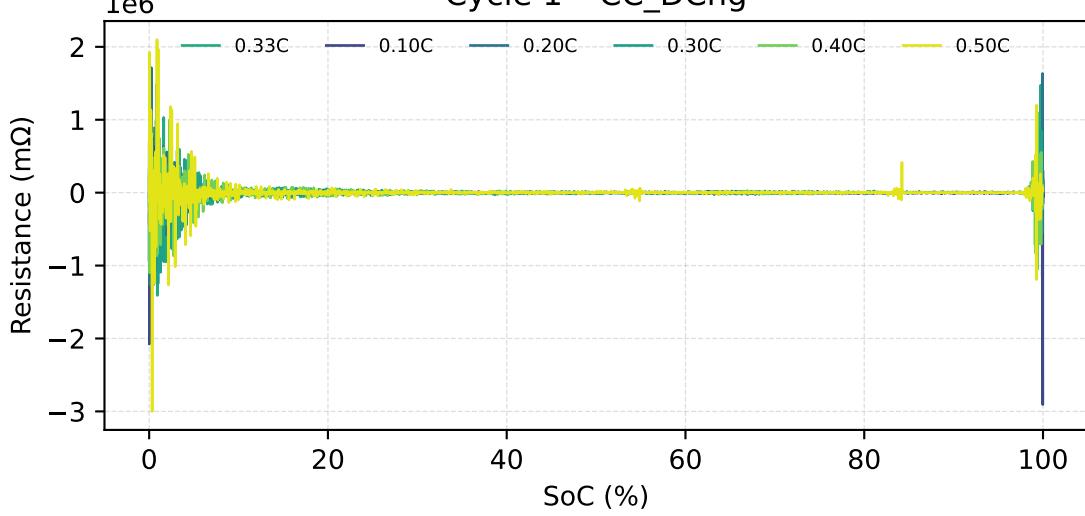


# SoC vs Resistance – RD\_RateCapability\_0012

## Cycle 1 - CCCV\_Chg

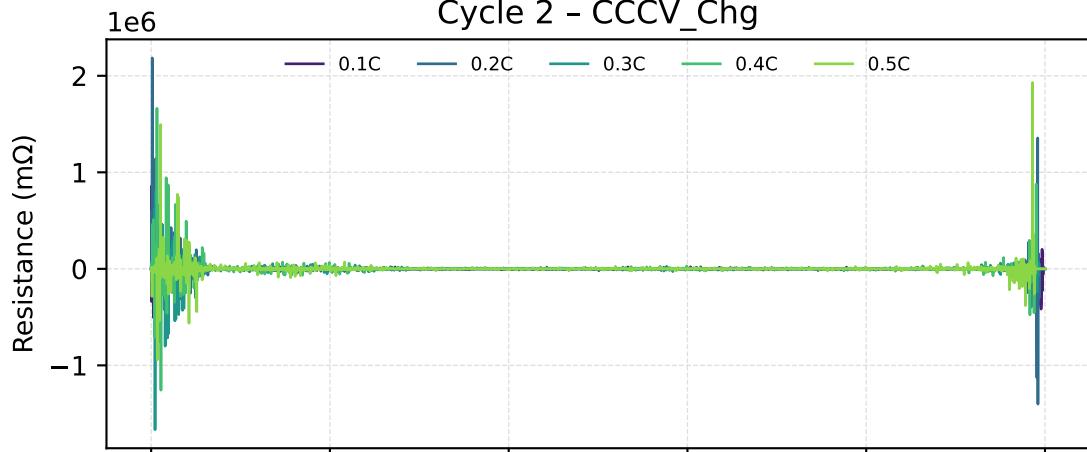


## Cycle 1 - CC\_DChg

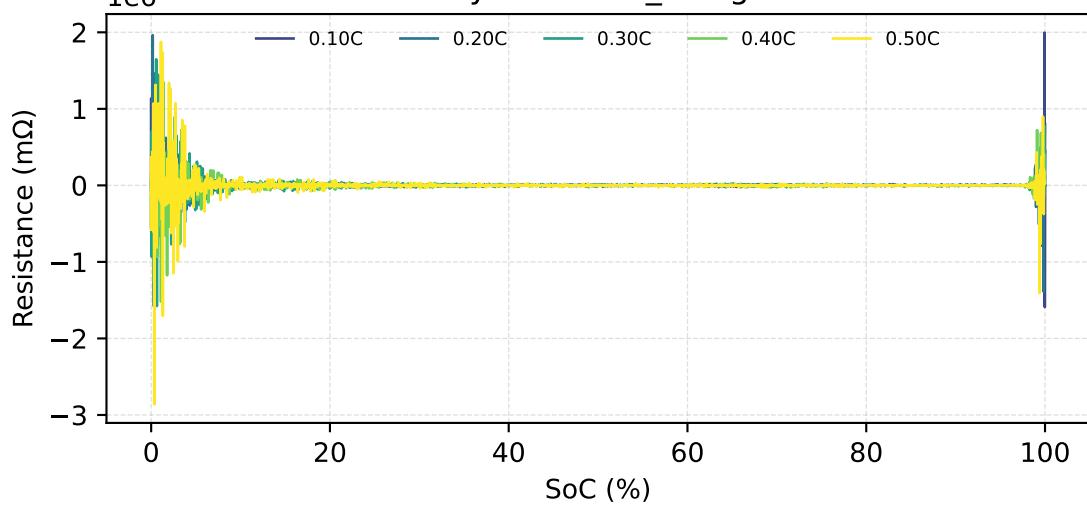


# SoC vs Resistance – RD\_RateCapability\_0012

Cycle 2 – CCCV\_Chg

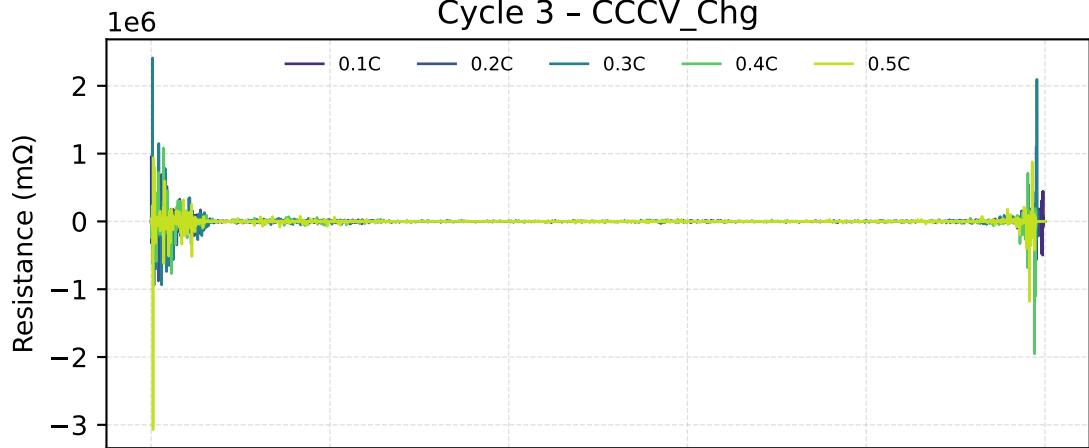


Cycle 2 – CC\_DChg

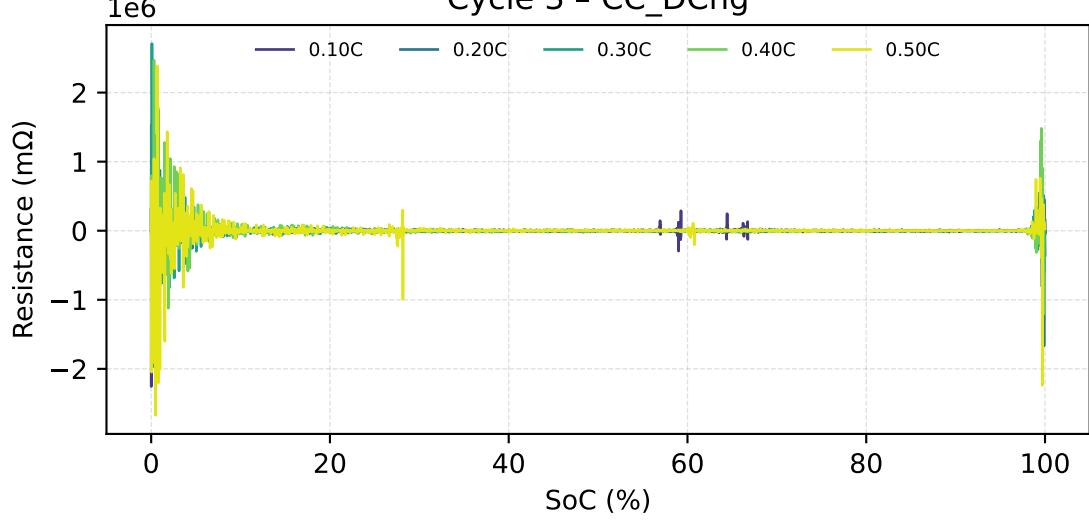


# SoC vs Resistance – RD\_RateCapability\_0012

Cycle 3 – CCCV\_Chg

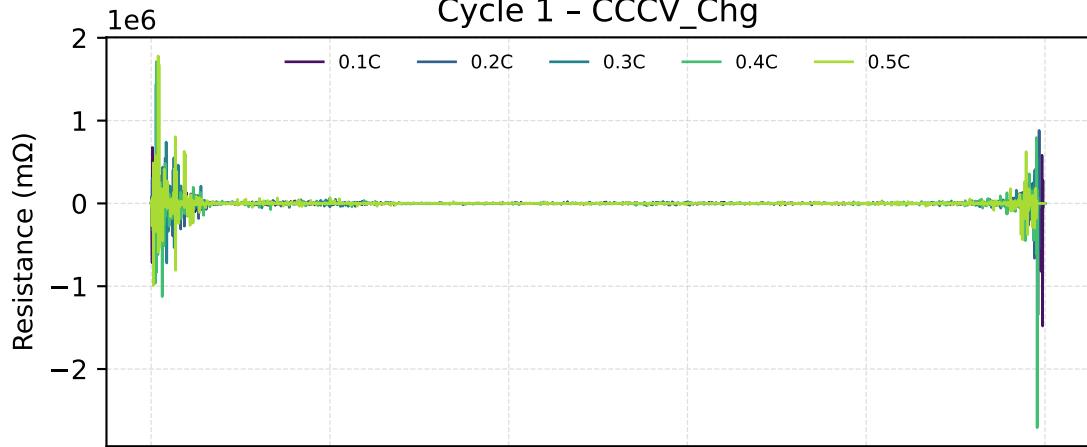


Cycle 3 – CC\_DChg

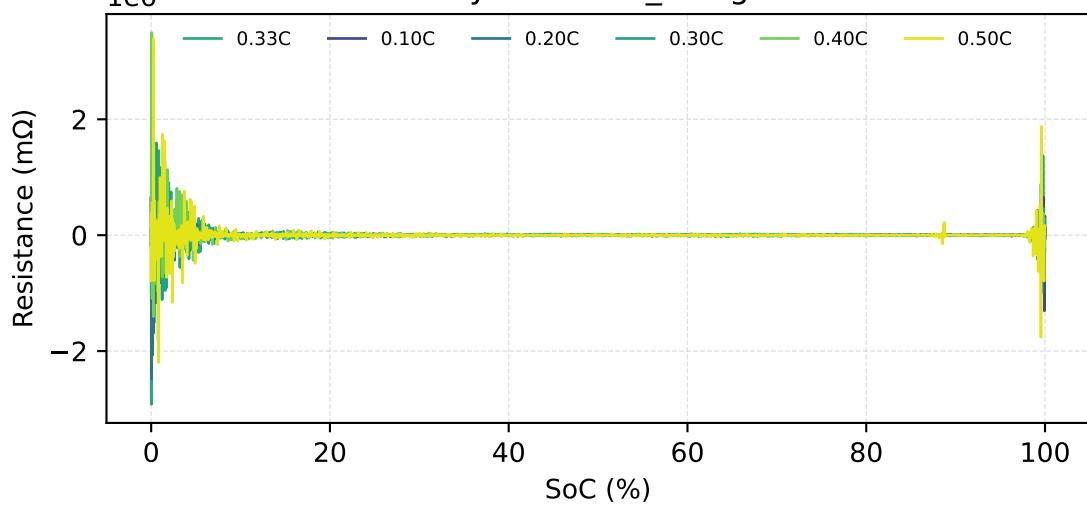


# SoC vs Resistance – RD\_RateCapability\_0025

Cycle 1 - CCCV\_Chg

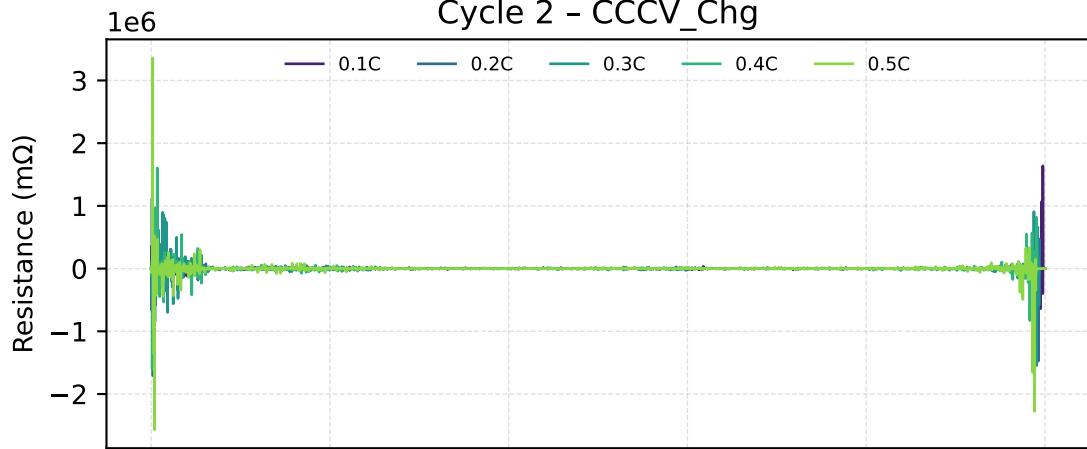


Cycle 1 - CC\_DChg

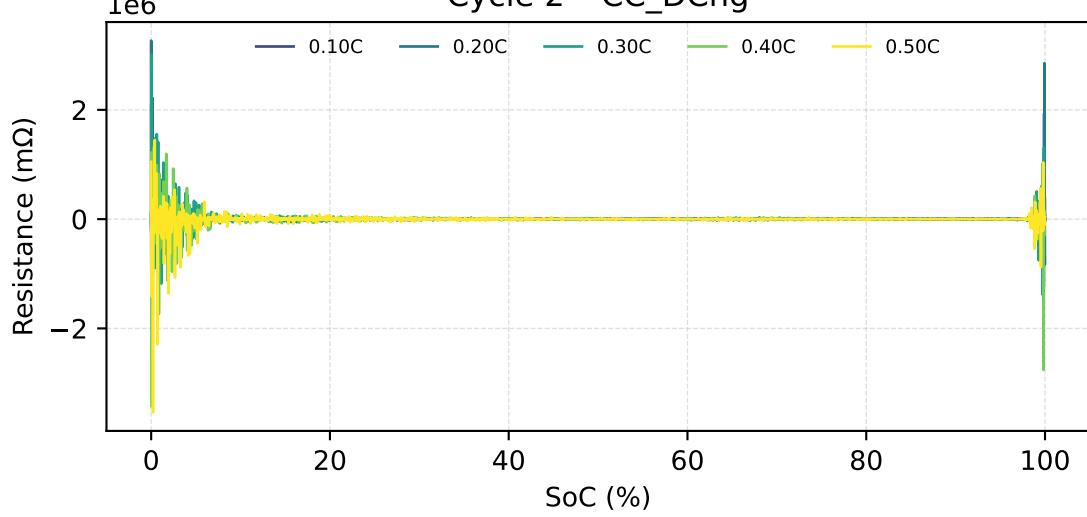


# SoC vs Resistance – RD\_RateCapability\_0025

Cycle 2 – CCCV\_Chg

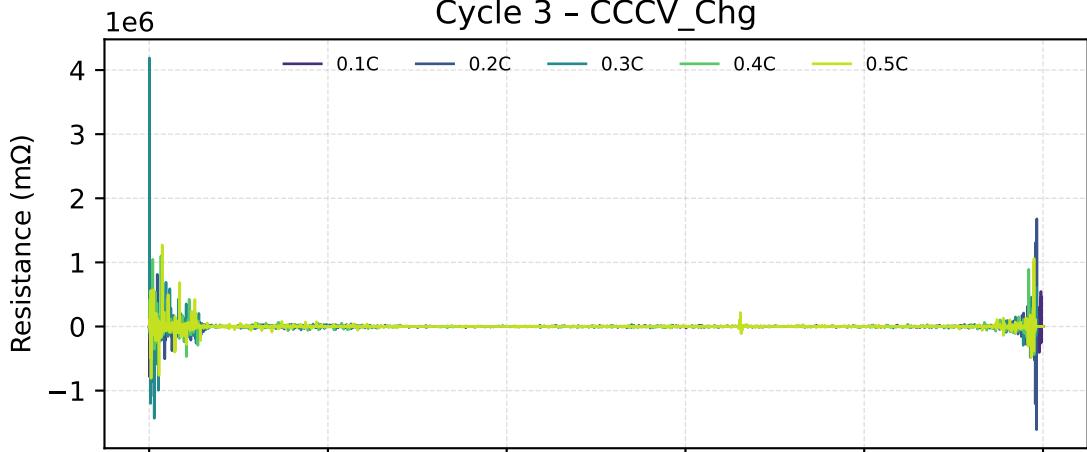


Cycle 2 – CC\_DChg

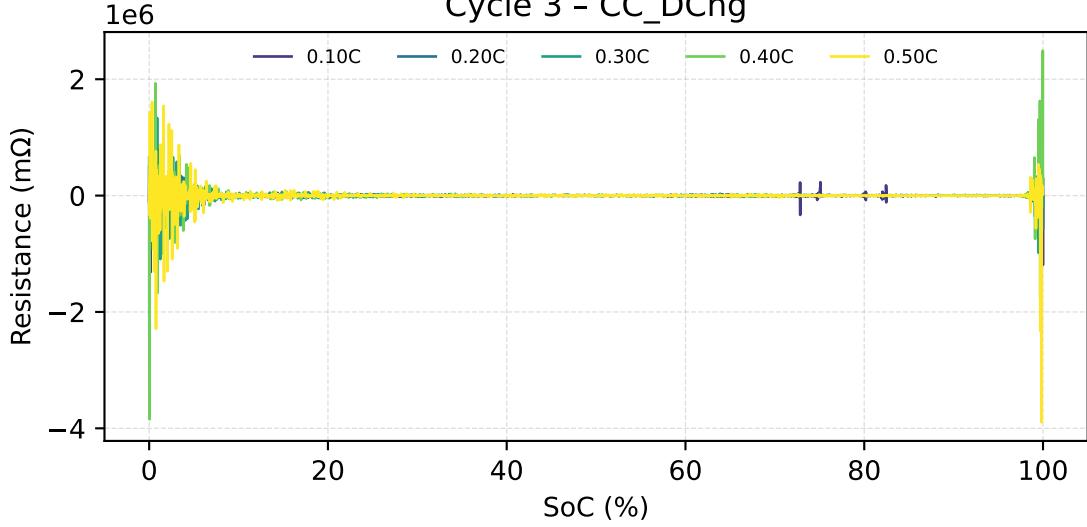


# SoC vs Resistance – RD\_RateCapability\_0025

Cycle 3 – CCCV\_Chg

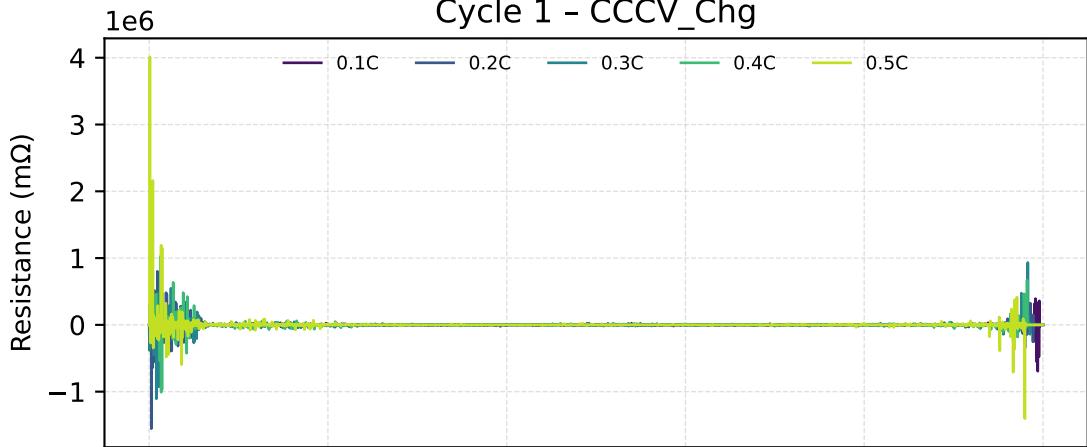


Cycle 3 – CC\_DChg

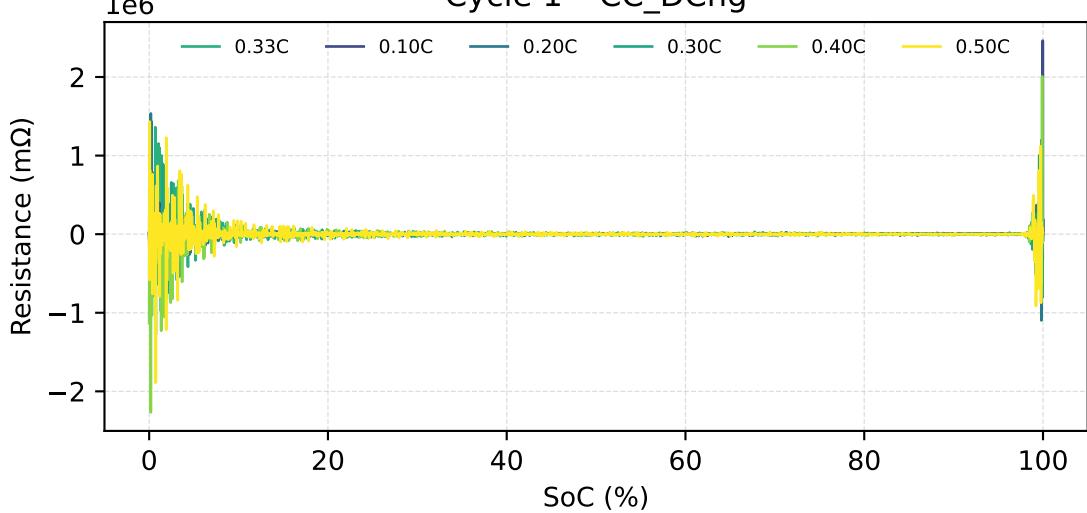


# SoC vs Resistance – RD\_RateCapability\_0034

## Cycle 1 - CCCV\_Chg

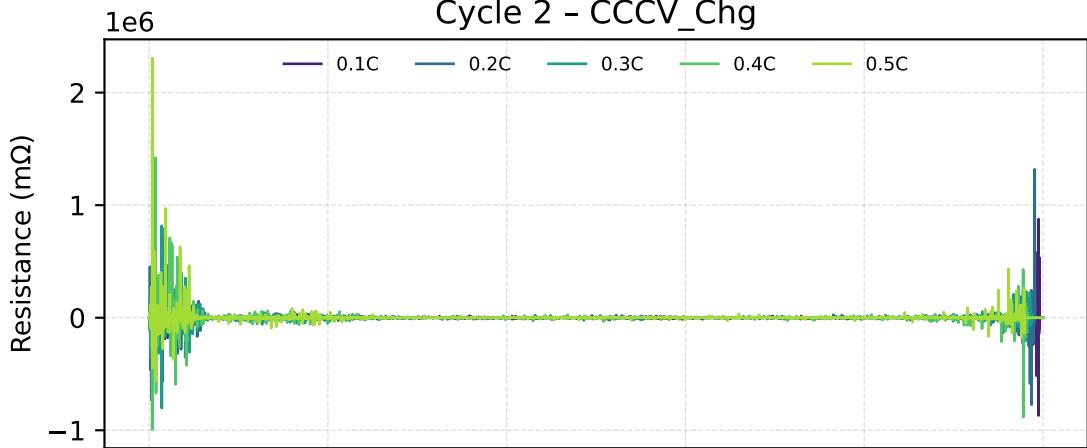


## Cycle 1 - CC\_DChg

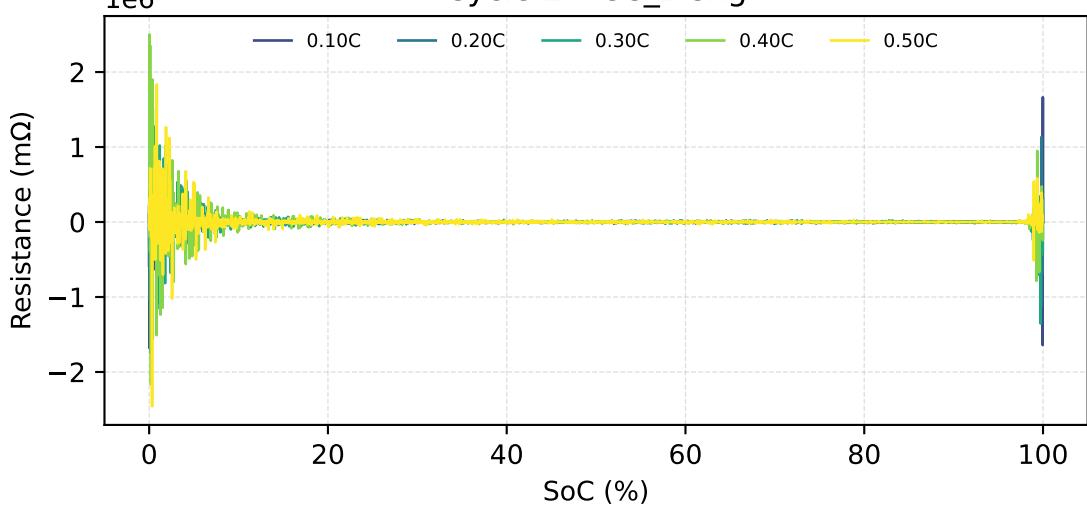


# SoC vs Resistance – RD\_RateCapability\_0034

Cycle 2 – CCCV\_Chg

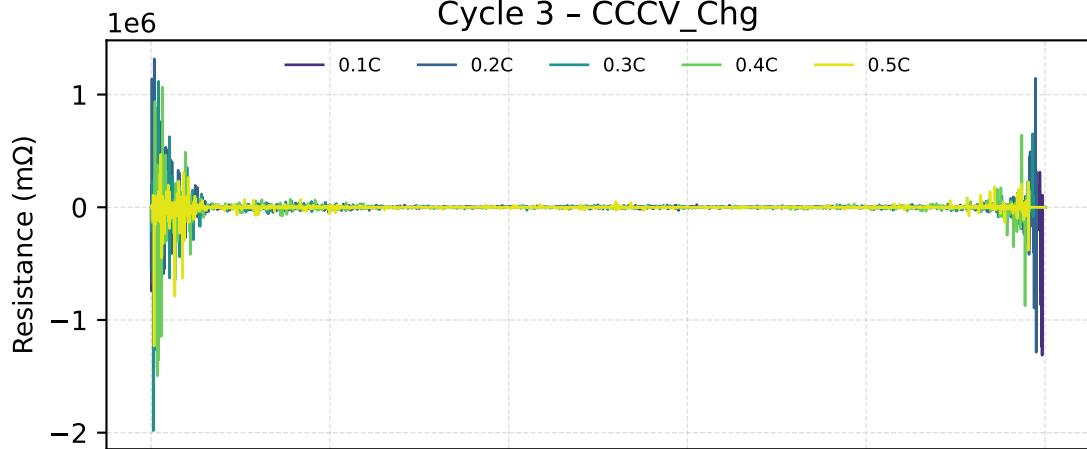


Cycle 2 – CC\_DChg

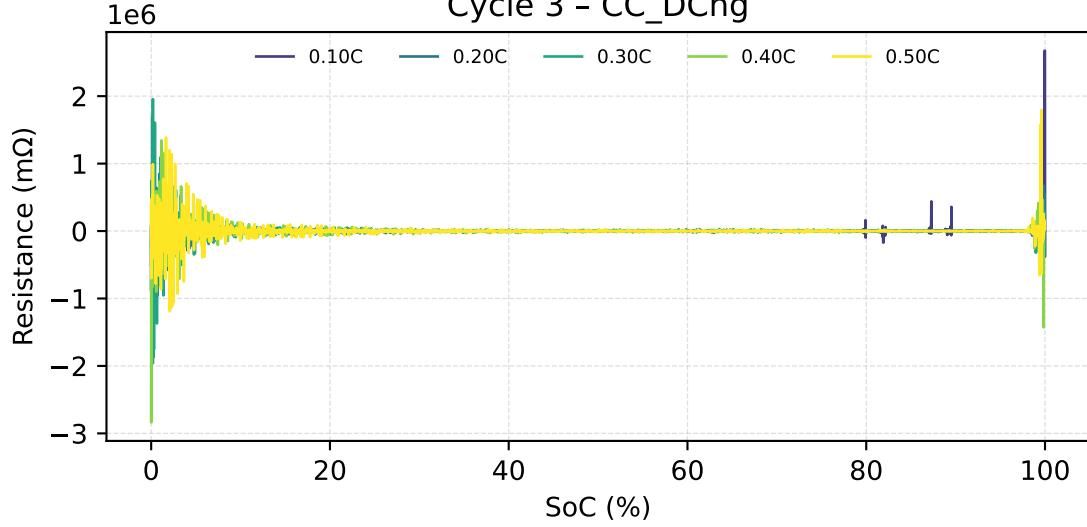


# SoC vs Resistance – RD\_RateCapability\_0034

Cycle 3 – CCCV\_Chg

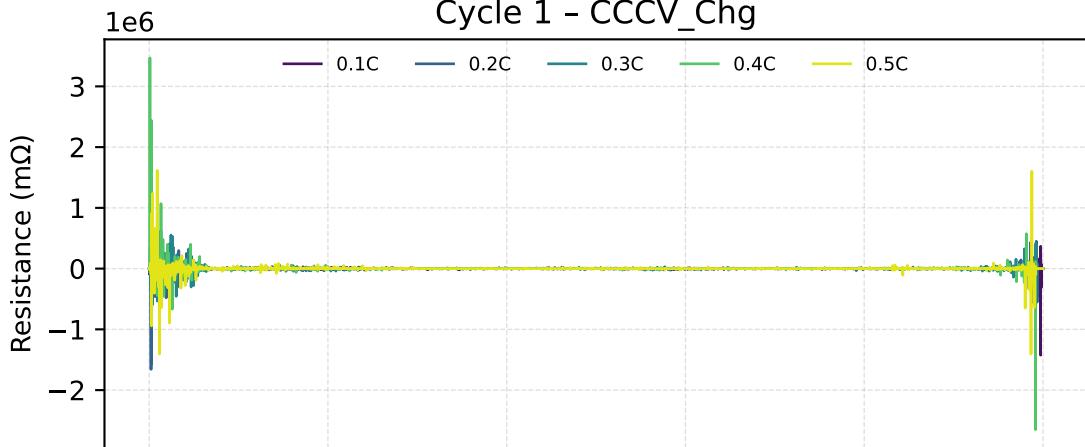


Cycle 3 – CC\_DChg

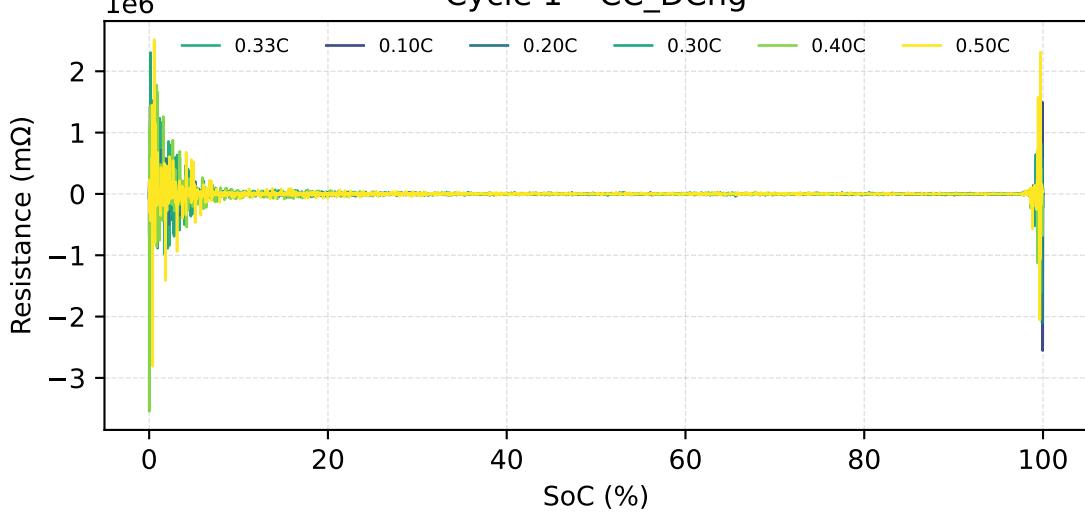


# SoC vs Resistance – RD\_RateCapability\_0040

## Cycle 1 - CCCV\_Chg

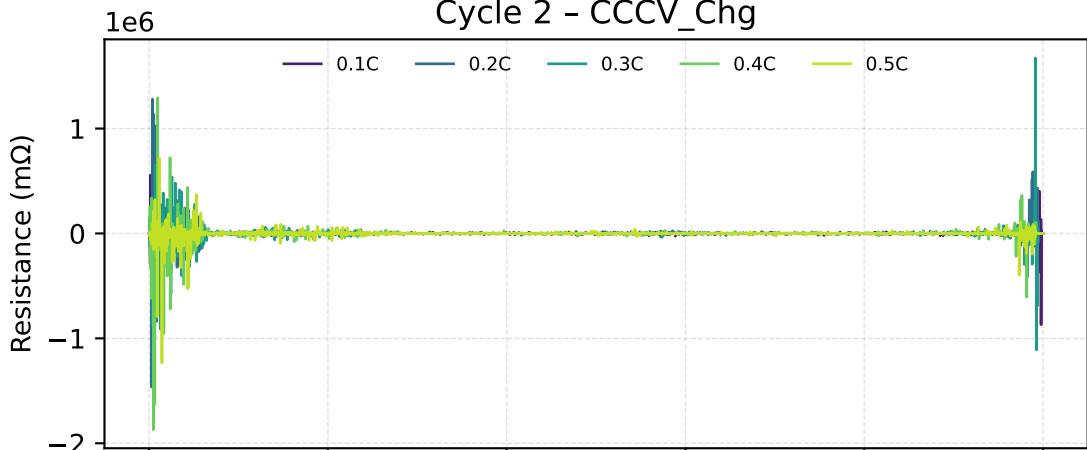


## Cycle 1 - CC\_DChg

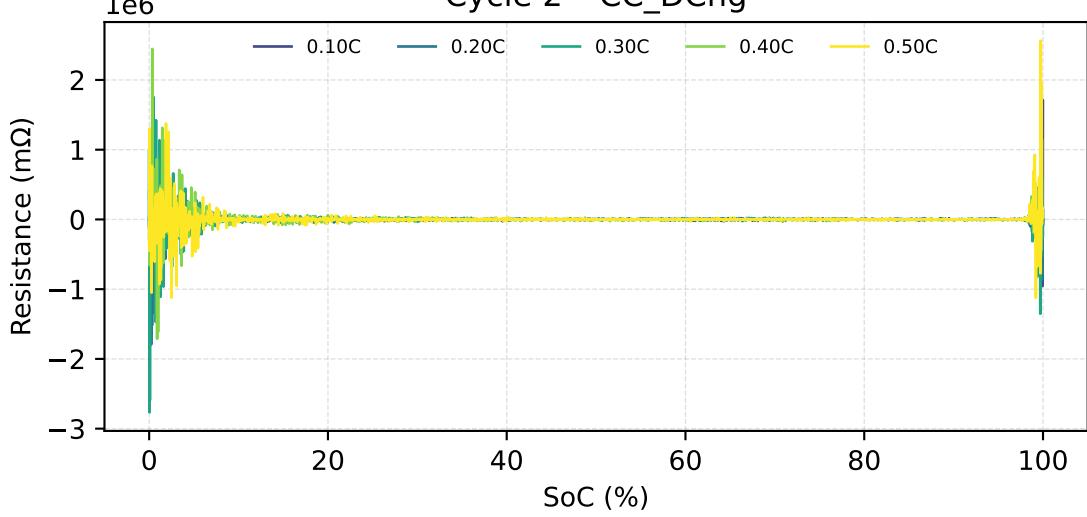


# SoC vs Resistance – RD\_RateCapability\_0040

Cycle 2 – CCCV\_Chg

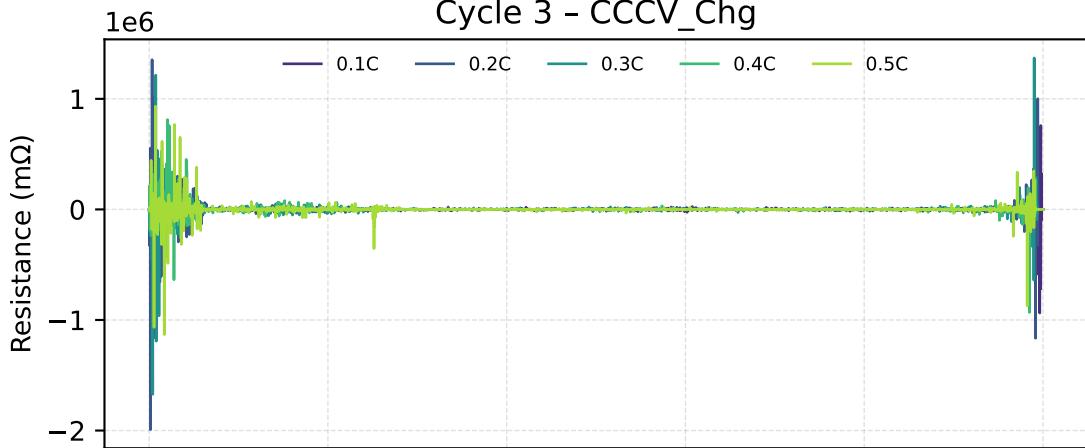


Cycle 2 – CC\_DChg

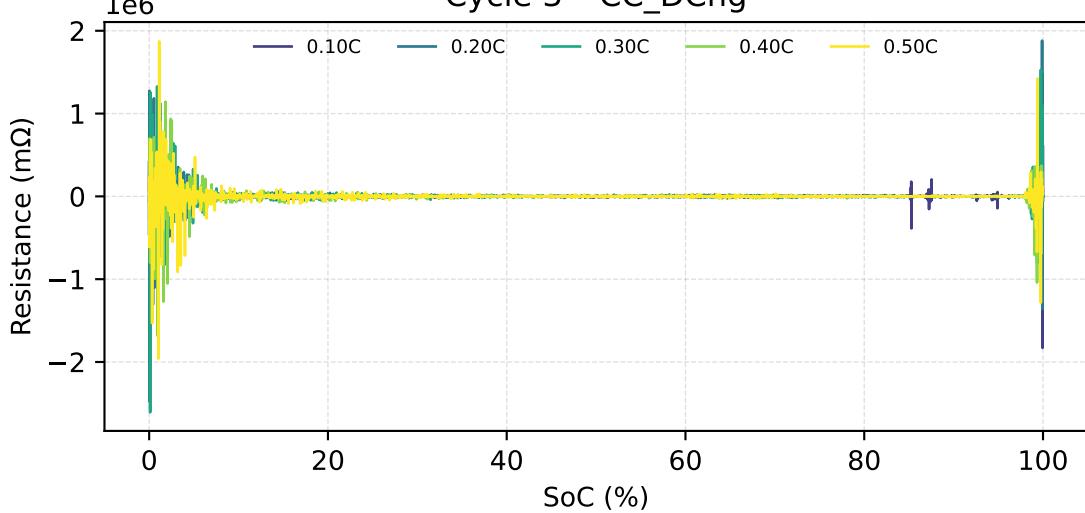


# SoC vs Resistance – RD\_RateCapability\_0040

Cycle 3 – CCCV\_Chg

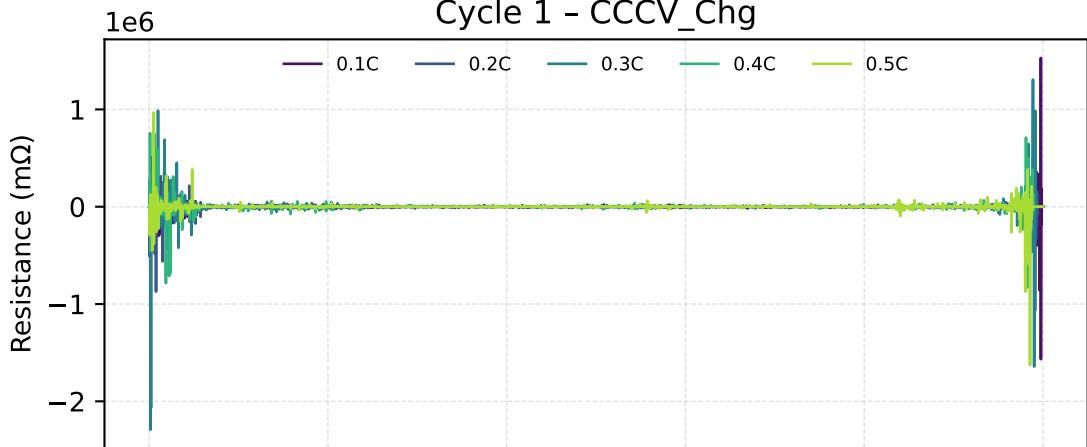


Cycle 3 – CC\_DChg

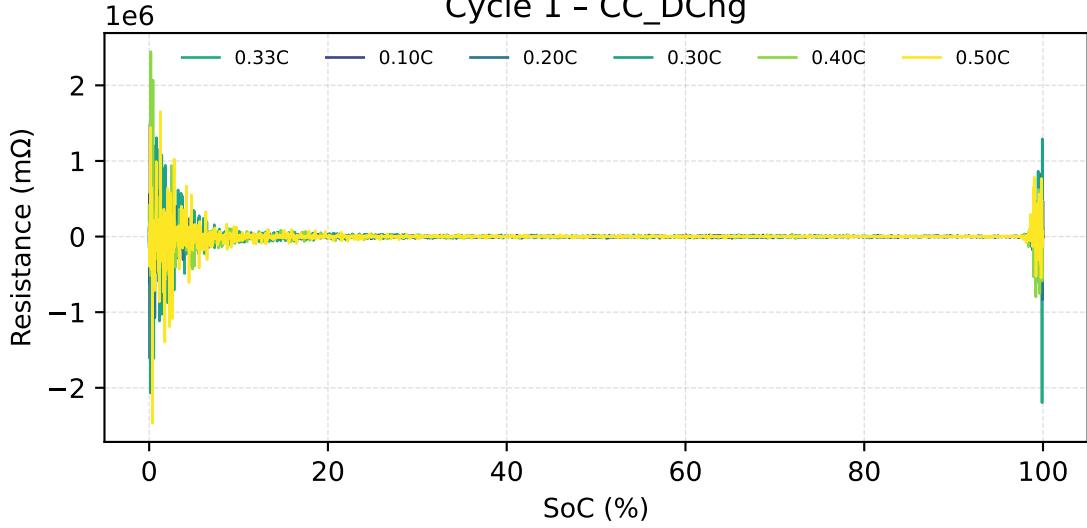


# SoC vs Resistance – RD\_RateCapability\_0043

## Cycle 1 - CCCV\_Chg

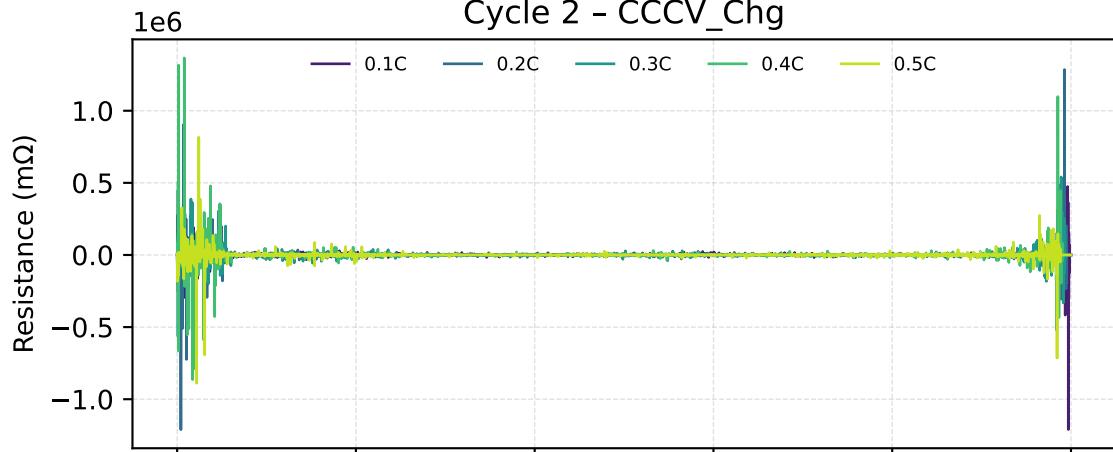


## Cycle 1 - CC\_DChg

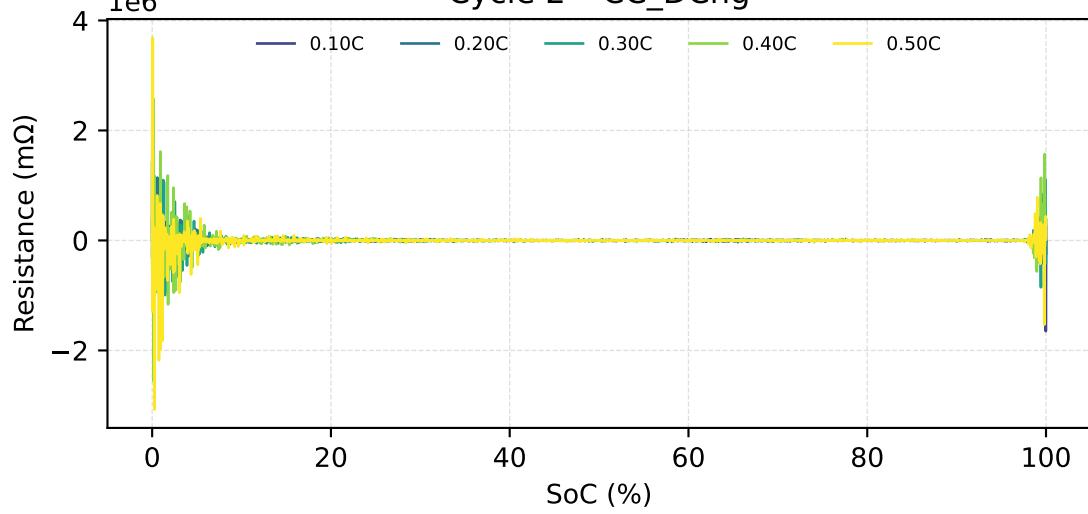


# SoC vs Resistance – RD\_RateCapability\_0043

Cycle 2 – CCCV\_Chg

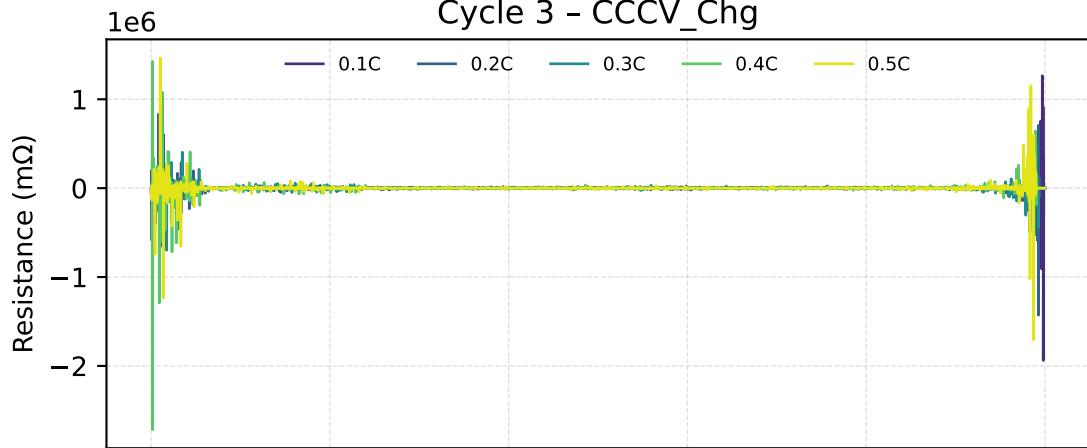


Cycle 2 – CC\_DChg

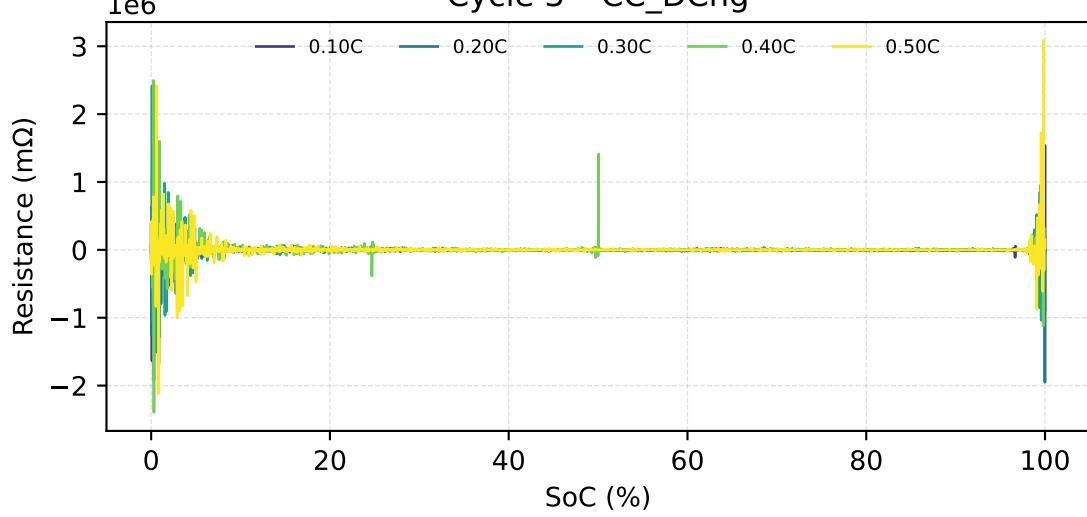


# SoC vs Resistance – RD\_RateCapability\_0043

Cycle 3 – CCCV\_Chg

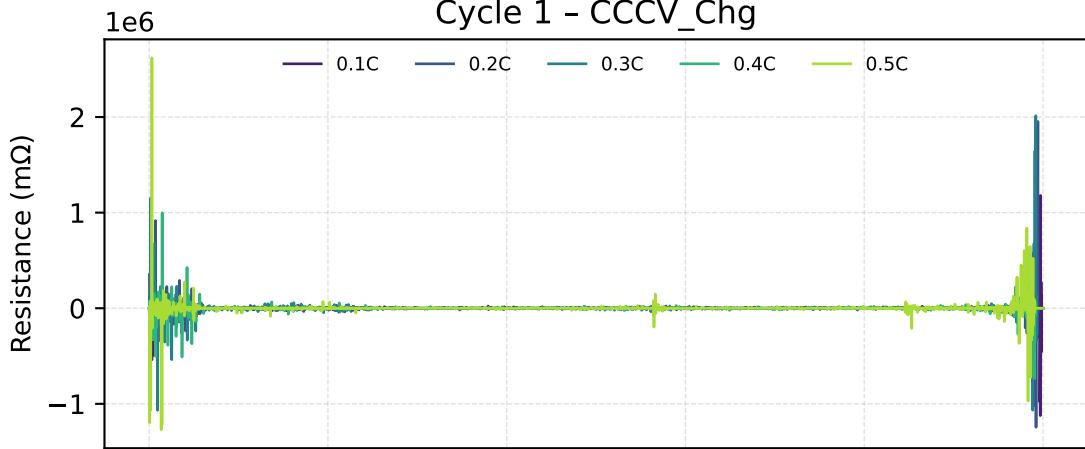


Cycle 3 – CC\_DChg

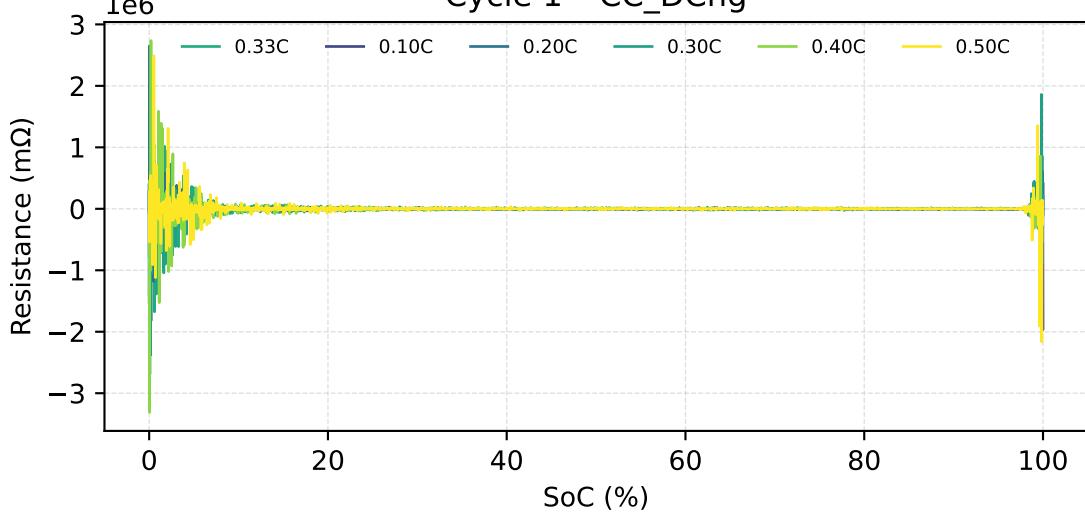


# SoC vs Resistance – RD\_RateCapability\_0046

## Cycle 1 - CCCV\_Chg

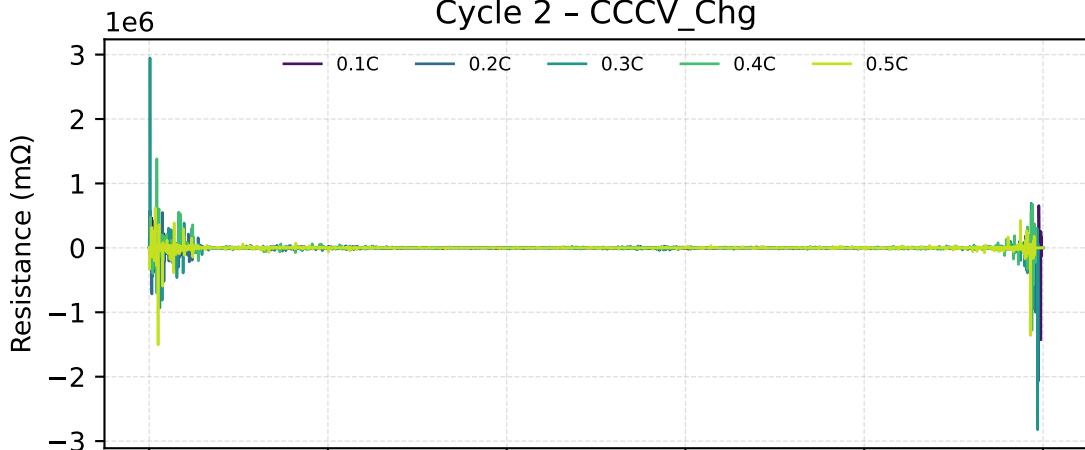


## Cycle 1 - CC\_DChg

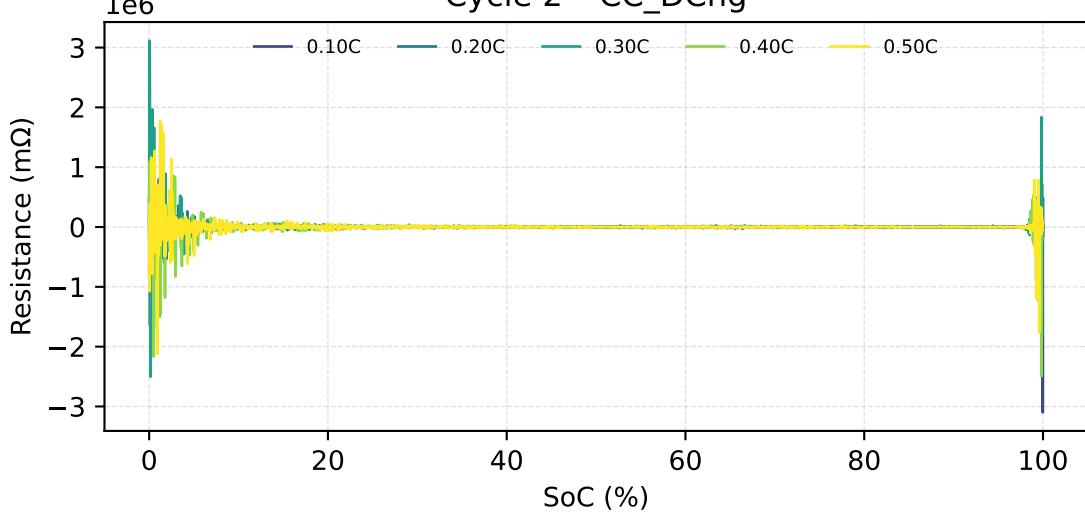


# SoC vs Resistance – RD\_RateCapability\_0046

Cycle 2 - CCCV\_Chg

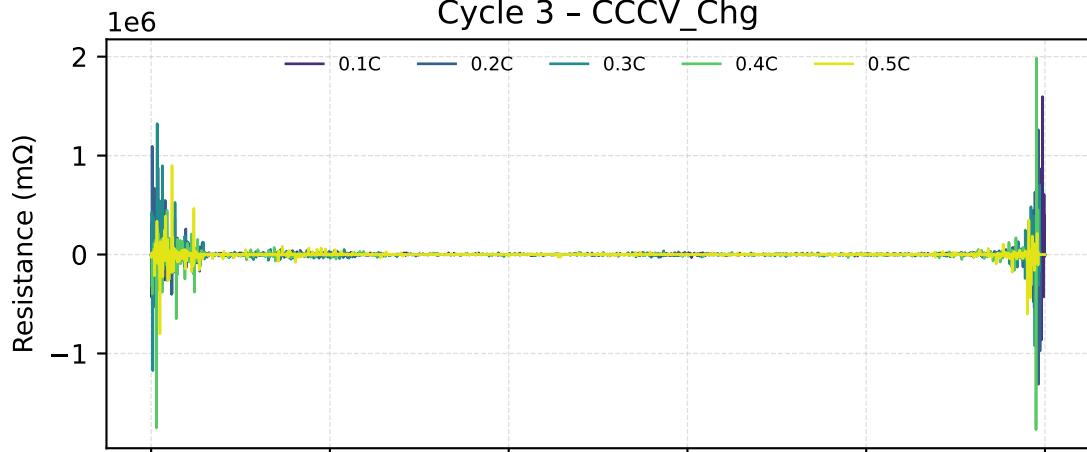


Cycle 2 - CC\_DChg

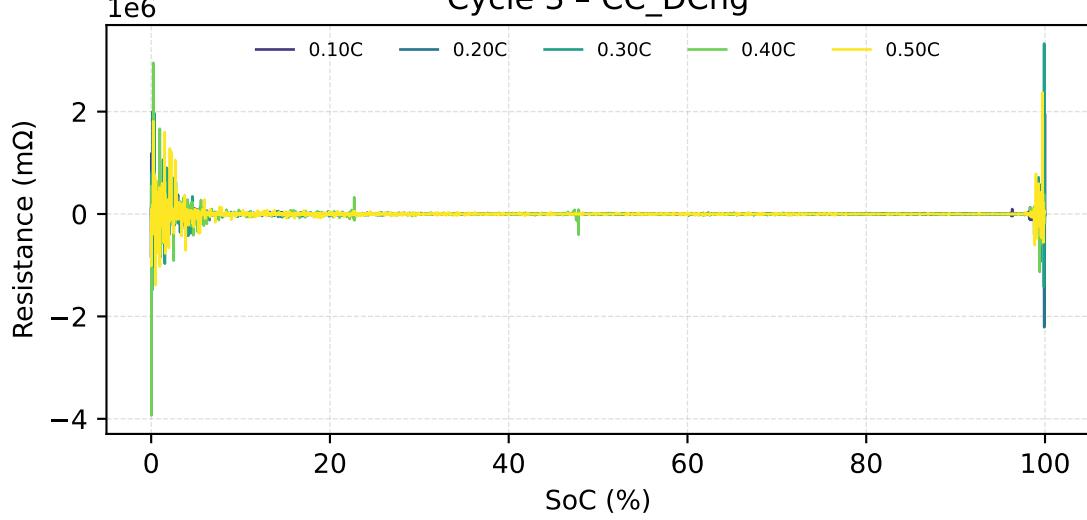


# SoC vs Resistance – RD\_RateCapability\_0046

Cycle 3 – CCCV\_Chg

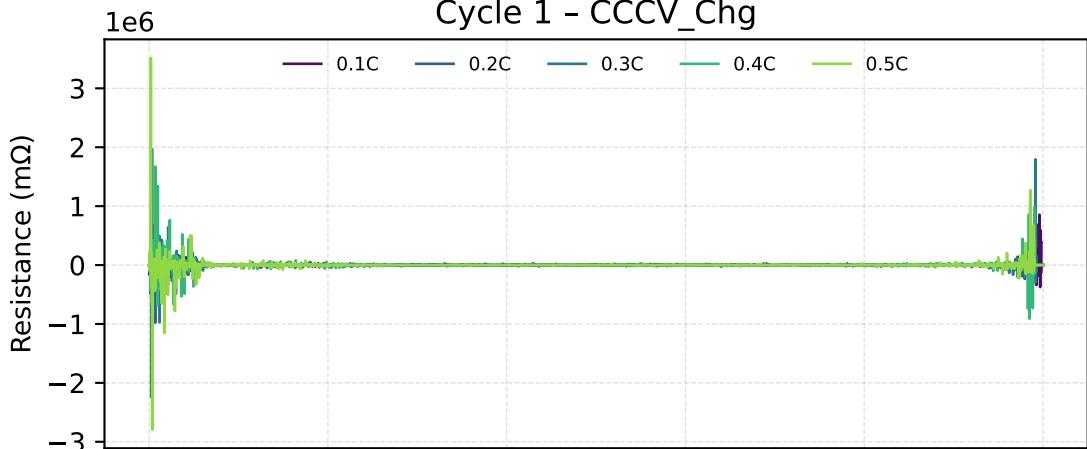


Cycle 3 – CC\_DChg

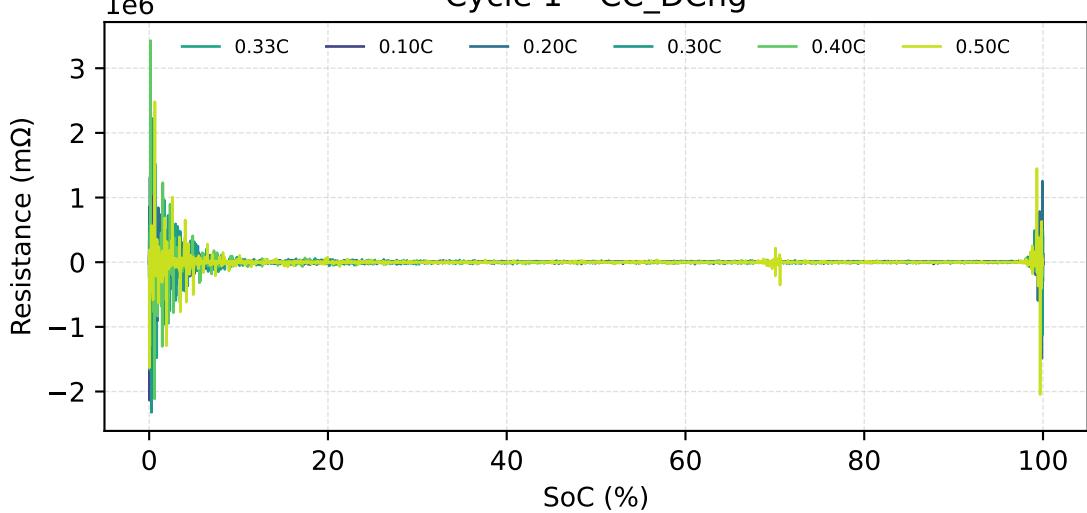


# SoC vs Resistance – RD\_RateCapability\_0049

Cycle 1 - CCCV\_Chg

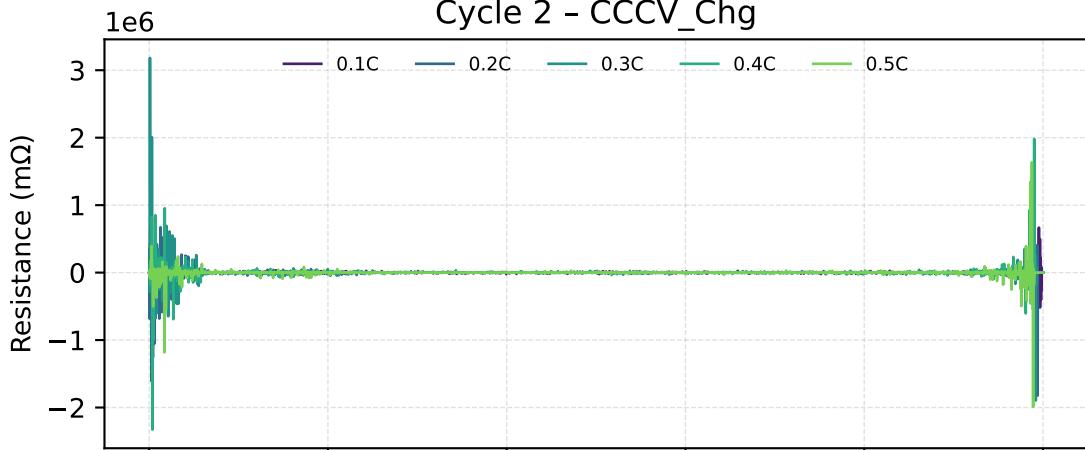


Cycle 1 - CC\_DChg

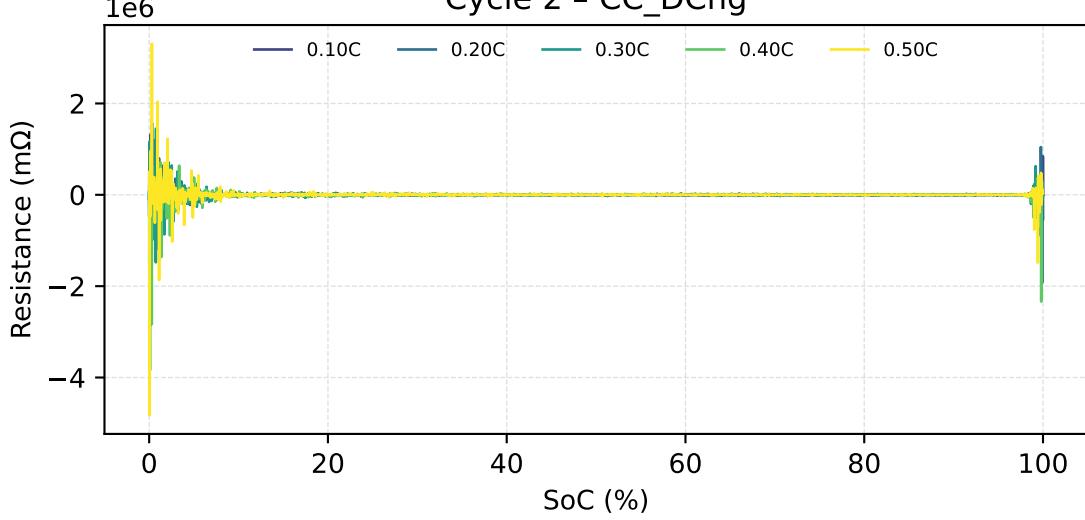


# SoC vs Resistance – RD\_RateCapability\_0049

Cycle 2 – CCCV\_Chg

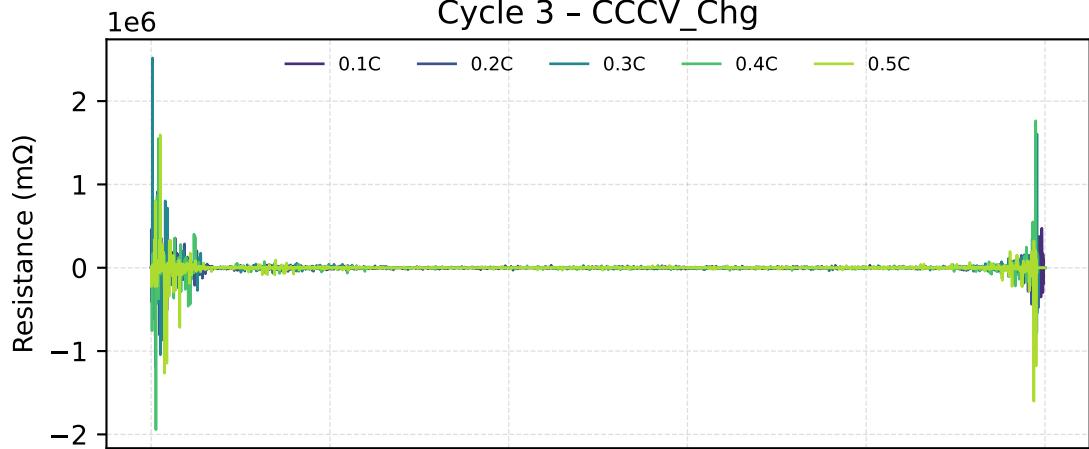


Cycle 2 – CC\_DChg

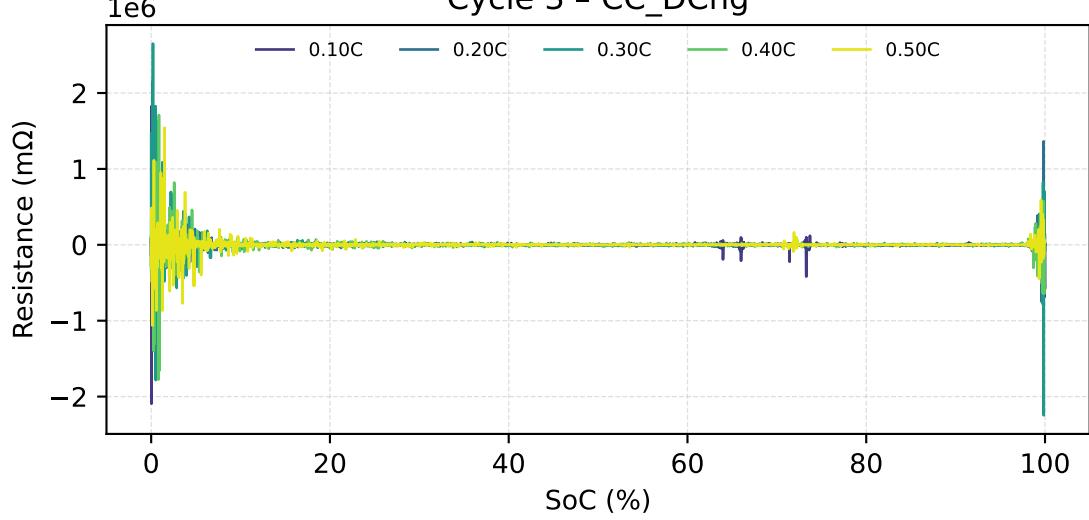


# SoC vs Resistance – RD\_RateCapability\_0049

Cycle 3 – CCCV\_Chg

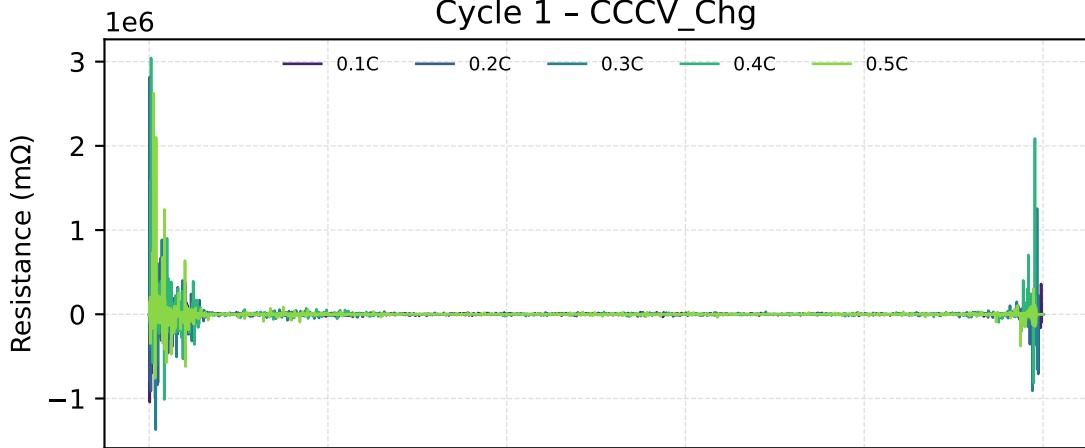


Cycle 3 – CC\_DChg

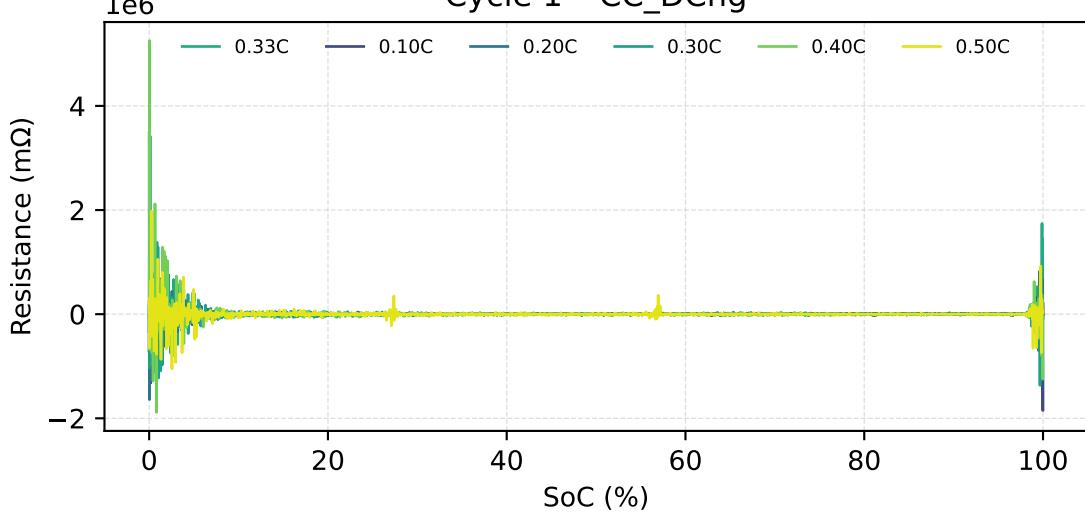


# SoC vs Resistance – RD\_RateCapability\_0050

## Cycle 1 – CCCV\_Chg

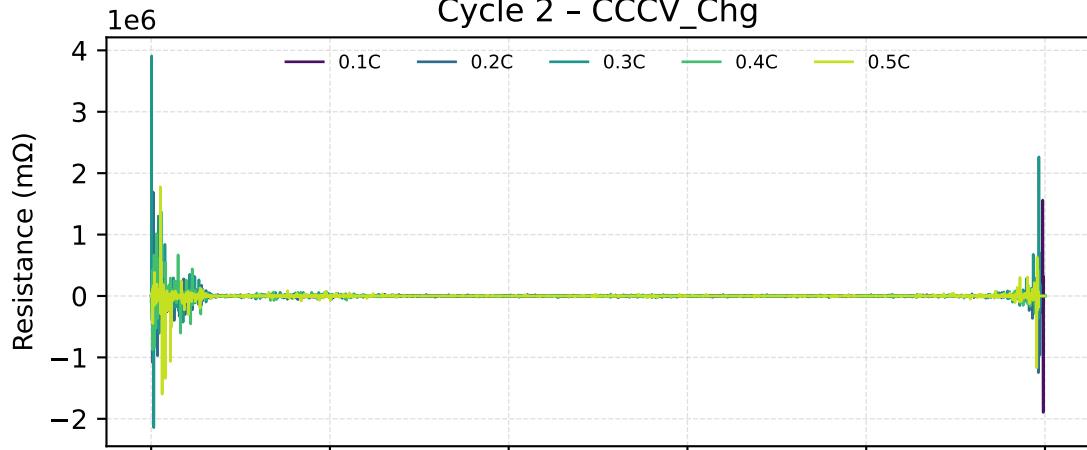


## Cycle 1 – CC\_DChg

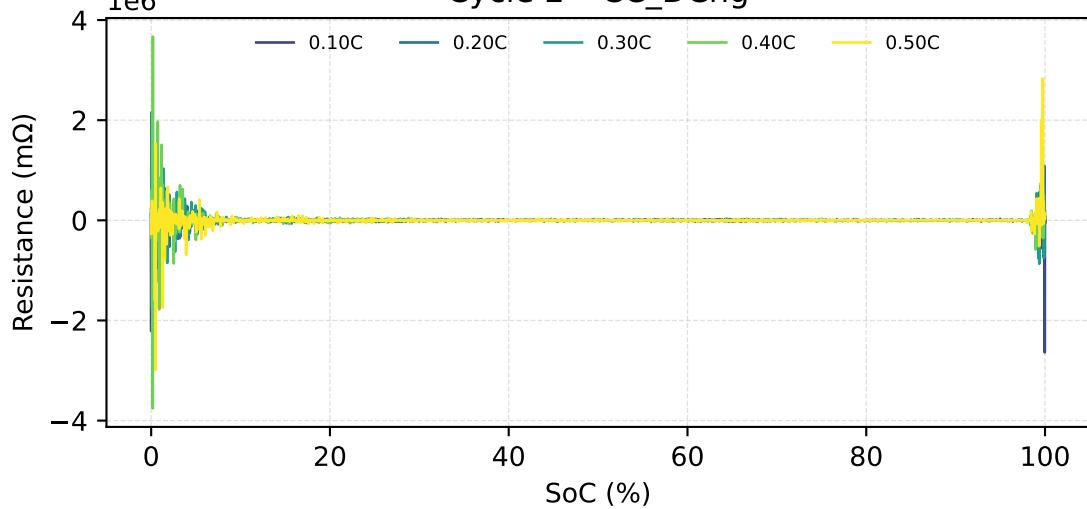


# SoC vs Resistance – RD\_RateCapability\_0050

Cycle 2 – CCCV\_Chg

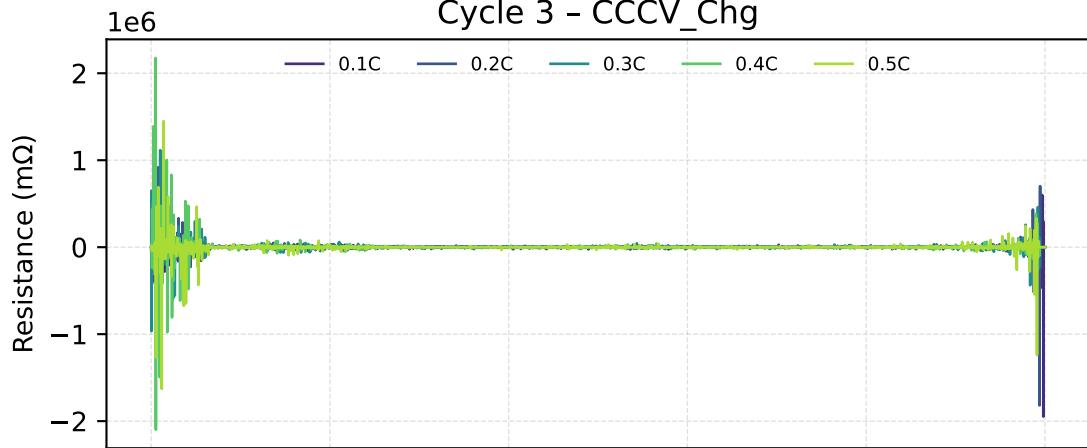


Cycle 2 – CC\_DChg

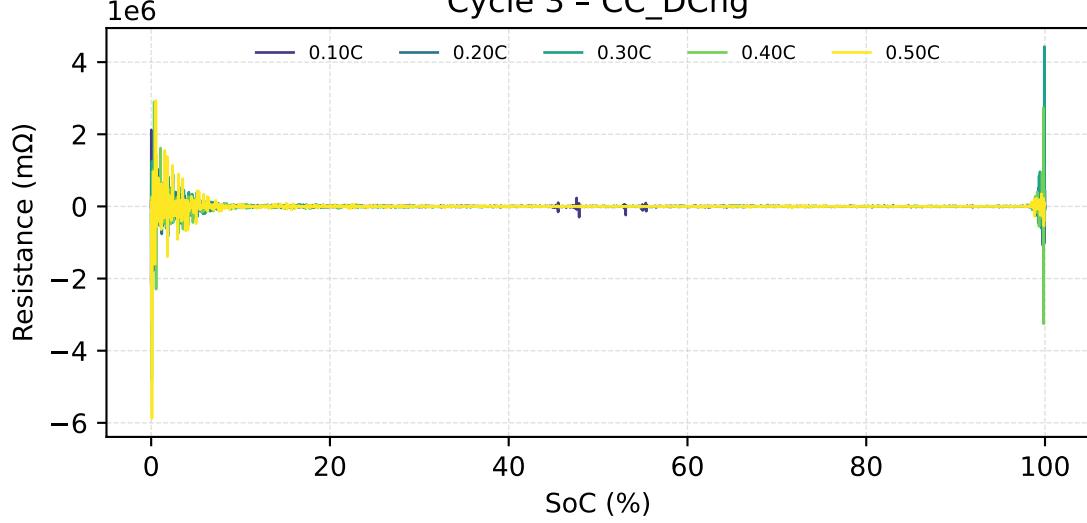


# SoC vs Resistance – RD\_RateCapability\_0050

Cycle 3 – CCCV\_Chg

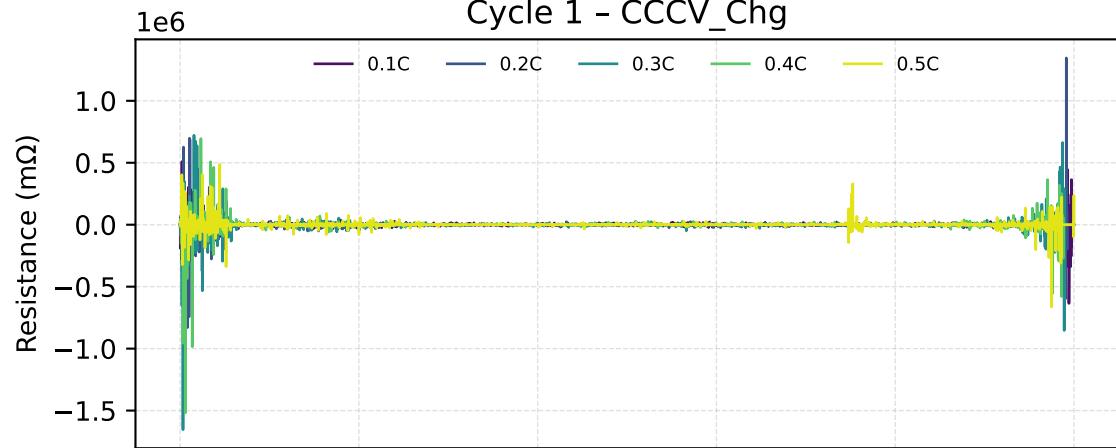


Cycle 3 – CC\_DChg

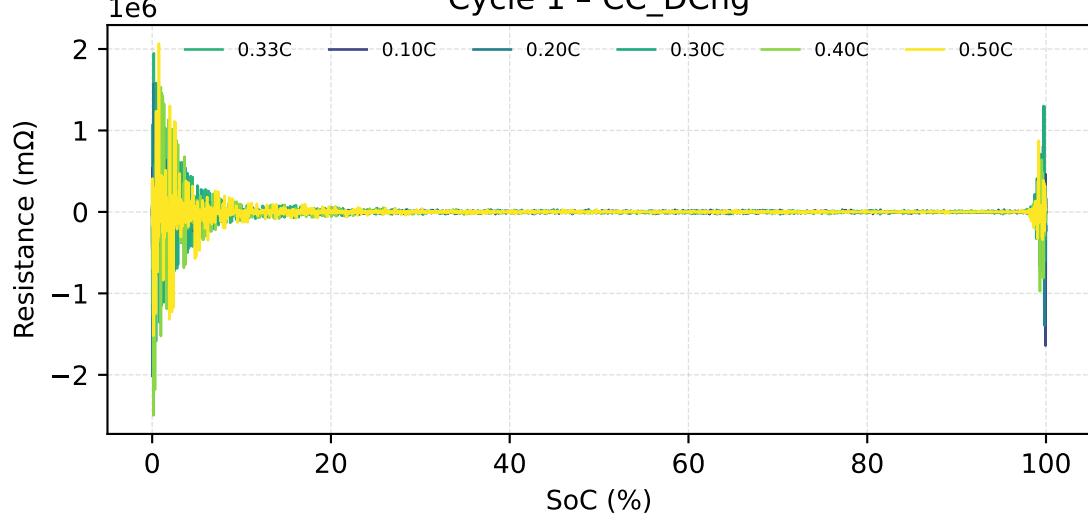


# SoC vs Resistance – RD\_RateCapability\_0056

Cycle 1 – CCCV\_Chg

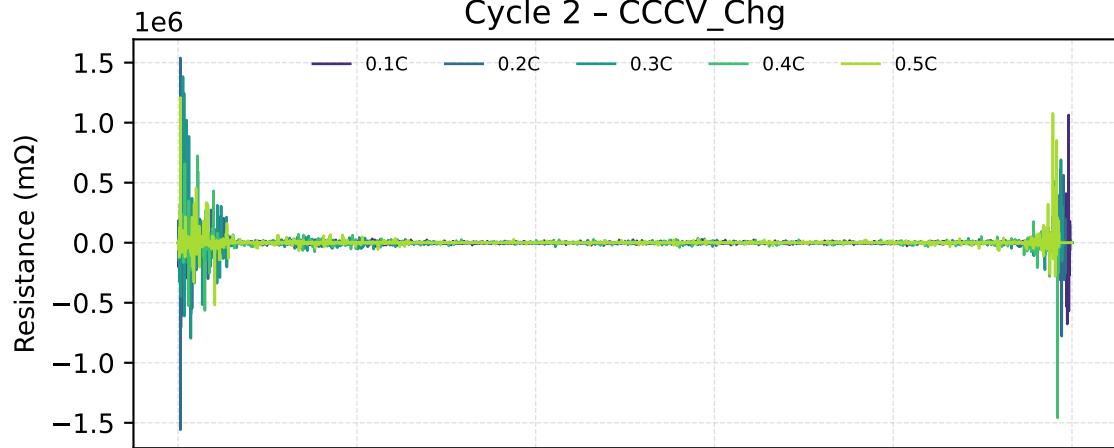


Cycle 1 – CC\_DChg

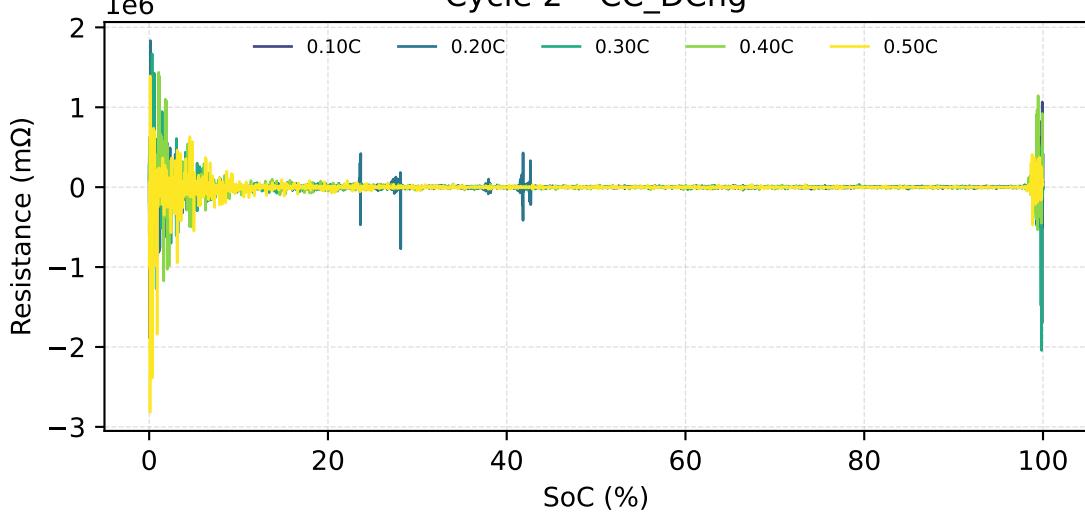


# SoC vs Resistance – RD\_RateCapability\_0056

Cycle 2 – CCCV\_Chg

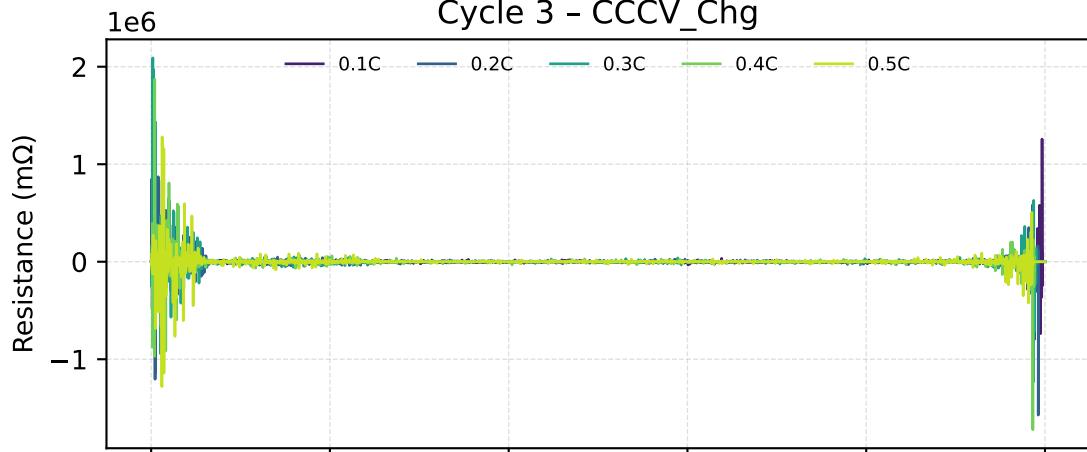


Cycle 2 – CC\_DChg

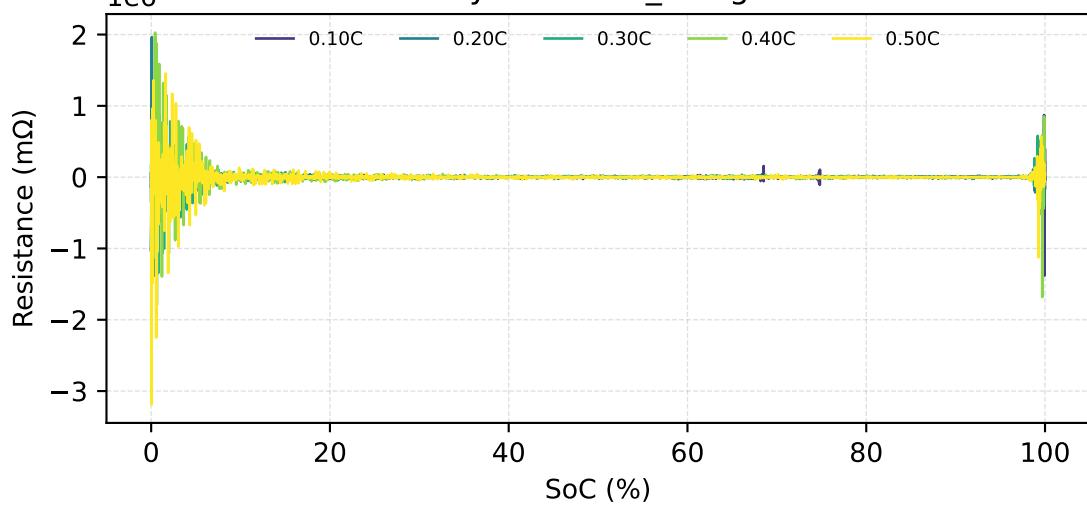


# SoC vs Resistance – RD\_RateCapability\_0056

Cycle 3 – CCCV\_Chg

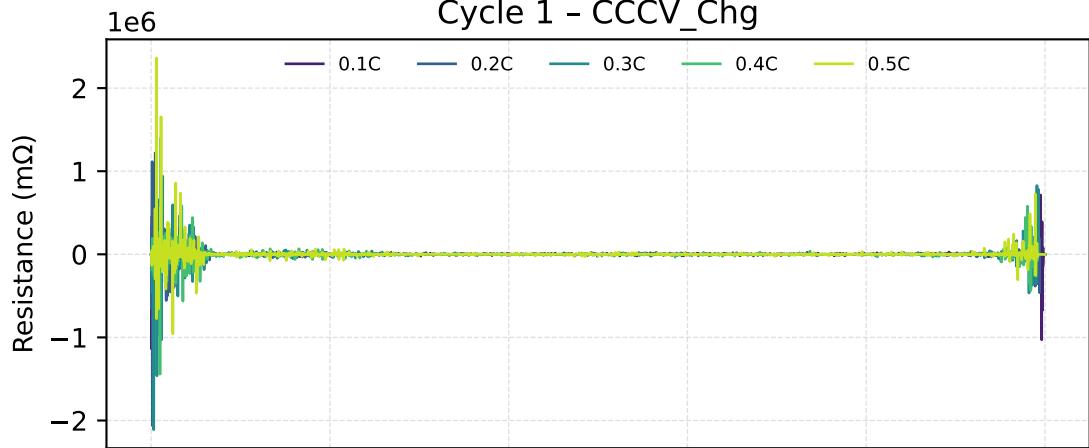


Cycle 3 – CC\_DChg

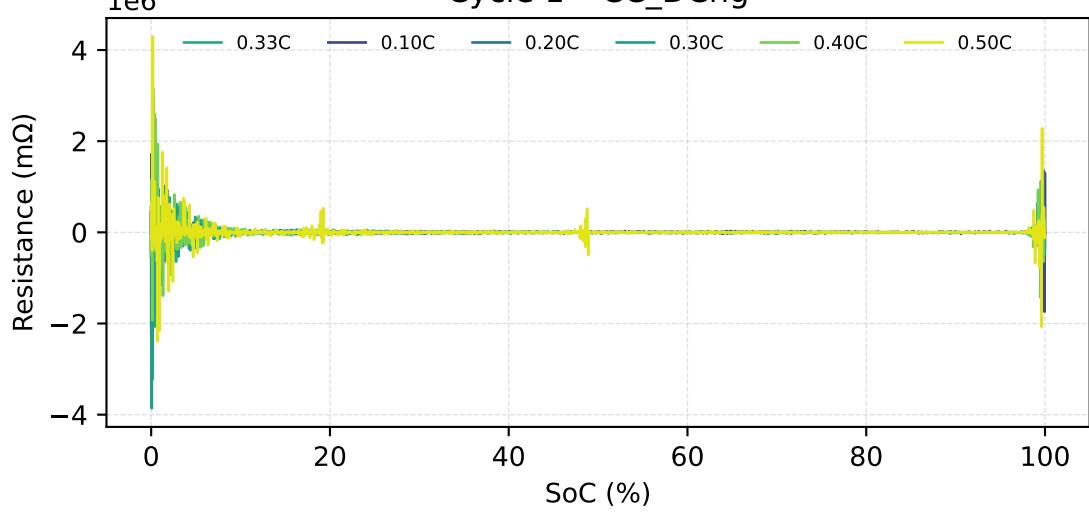


# SoC vs Resistance – RD\_RateCapability\_0057

Cycle 1 - CCCV\_Chg

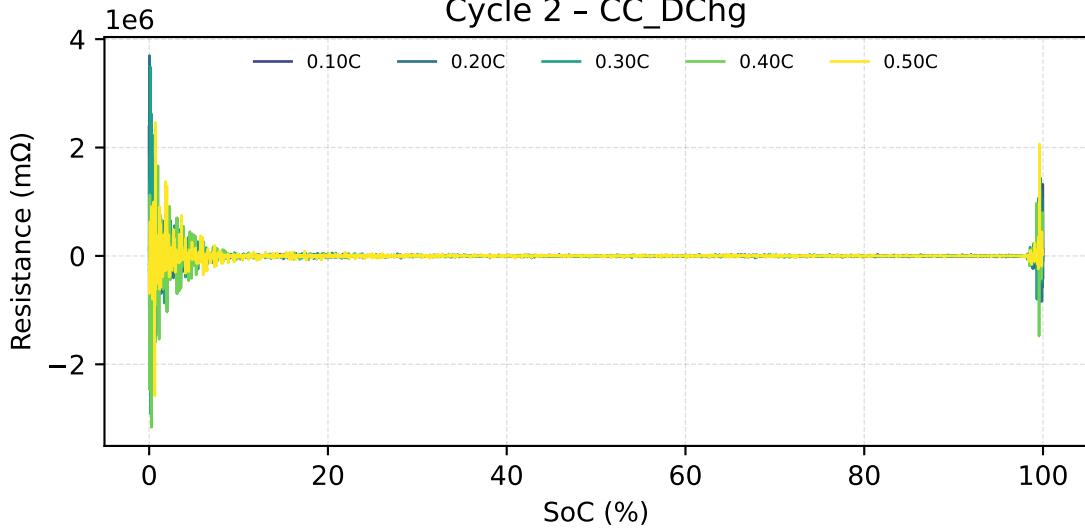
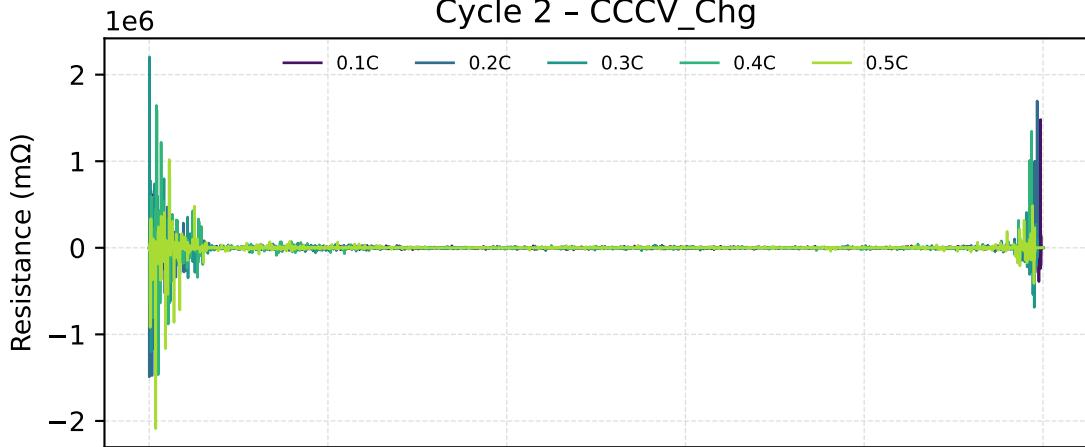


Cycle 1 - CC\_DChg



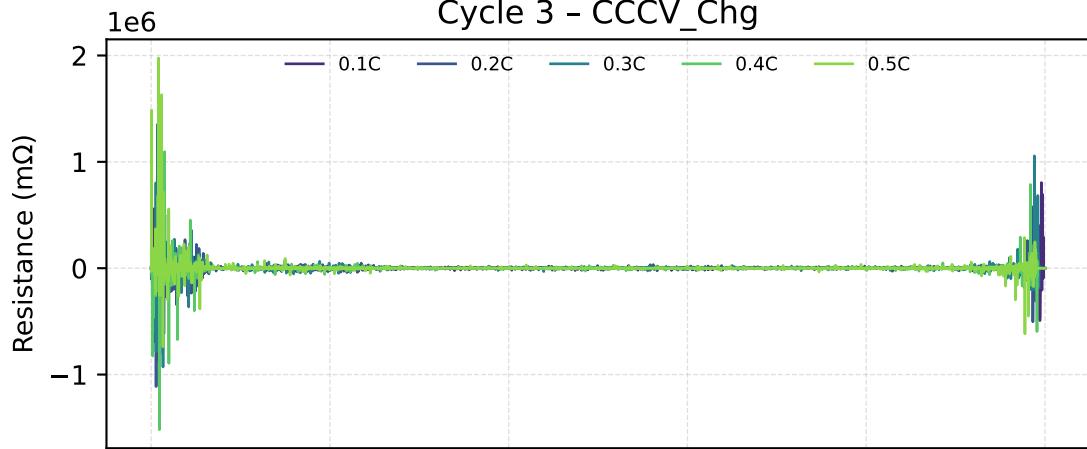
# SoC vs Resistance – RD\_RateCapability\_0057

## Cycle 2 – CCCV\_Chg

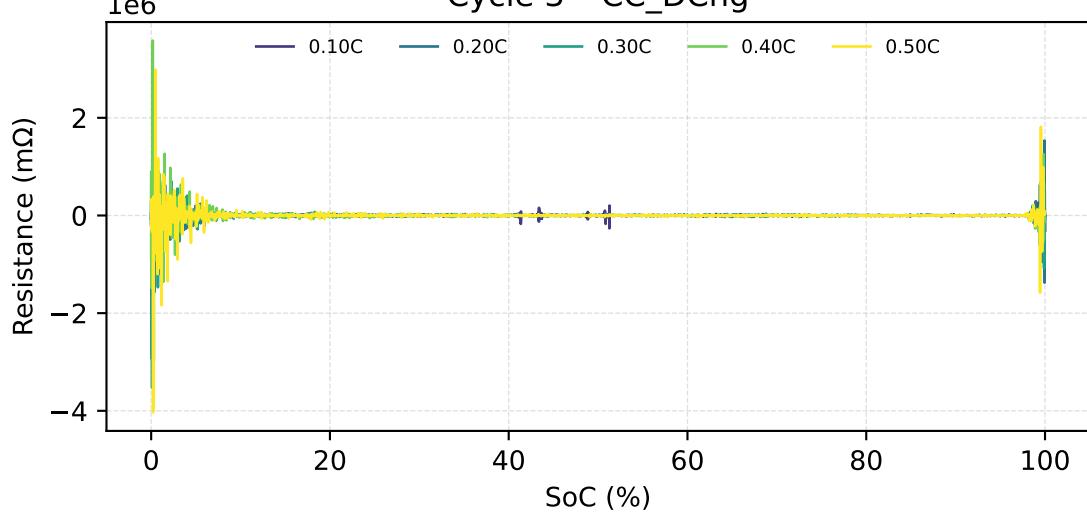


# SoC vs Resistance – RD\_RateCapability\_0057

Cycle 3 – CCCV\_Chg

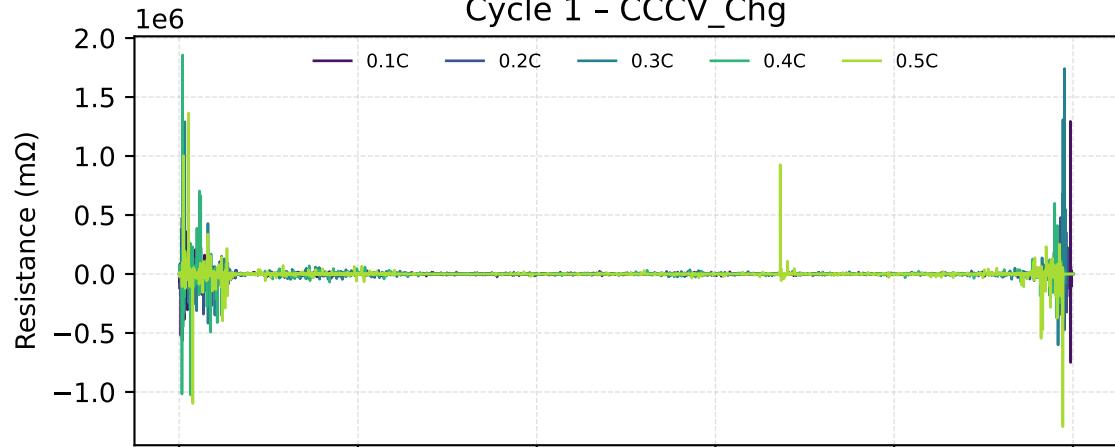


Cycle 3 – CC\_DChg

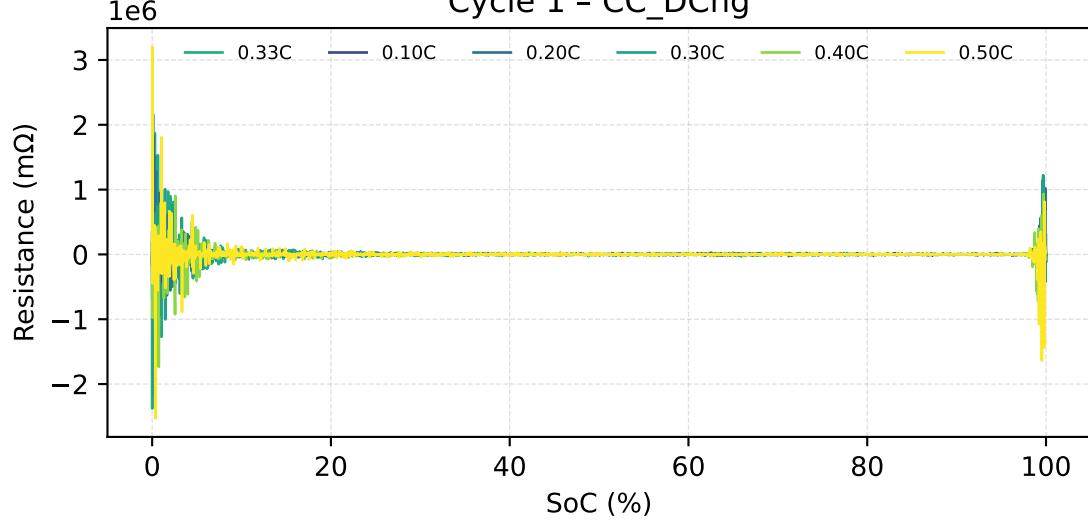


# SoC vs Resistance – RD\_RateCapability\_0065

## Cycle 1 - CCCV\_Chg

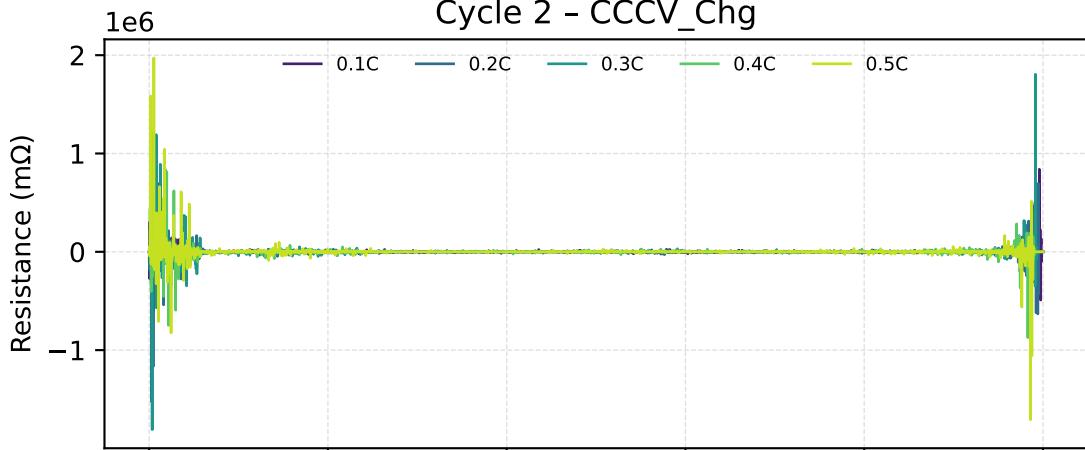


## Cycle 1 - CC\_DChg

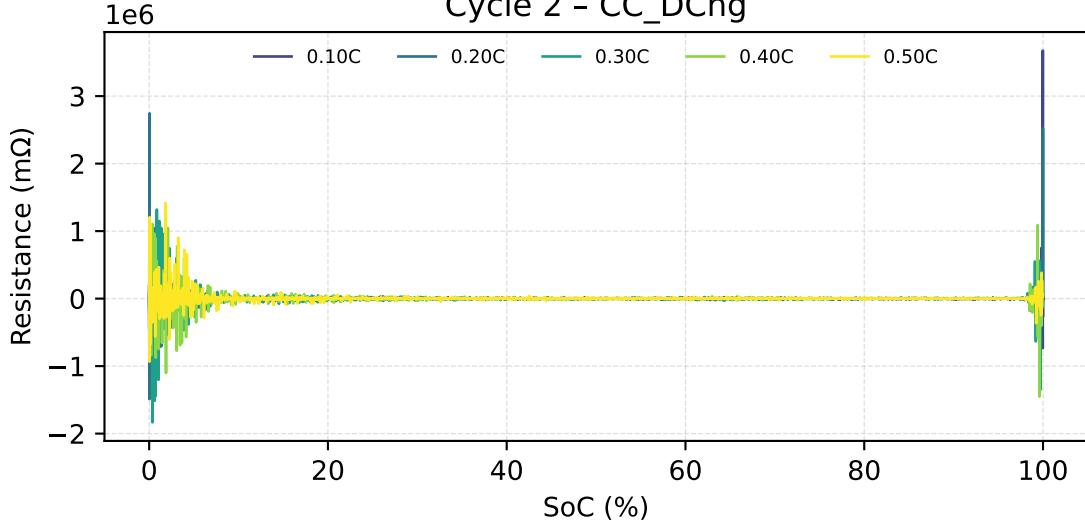


# SoC vs Resistance – RD\_RateCapability\_0065

Cycle 2 – CCCV\_Chg

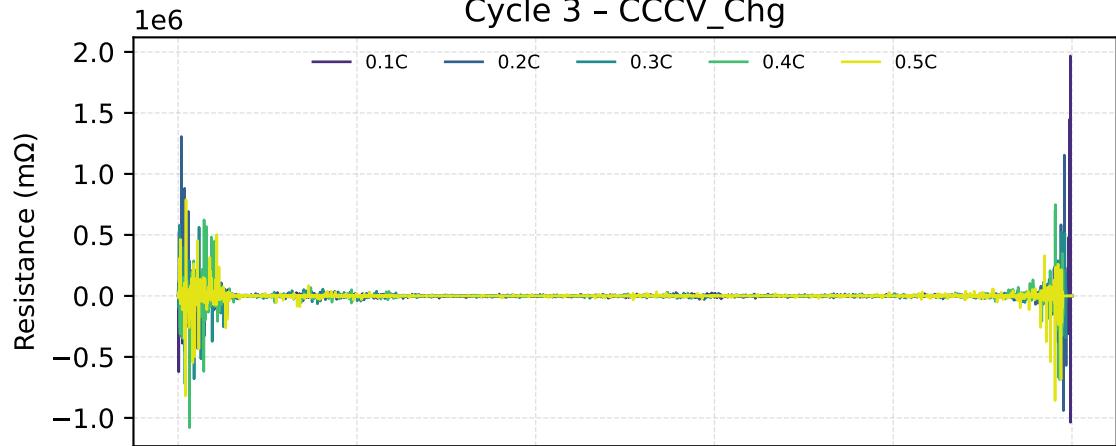


Cycle 2 – CC\_DChg

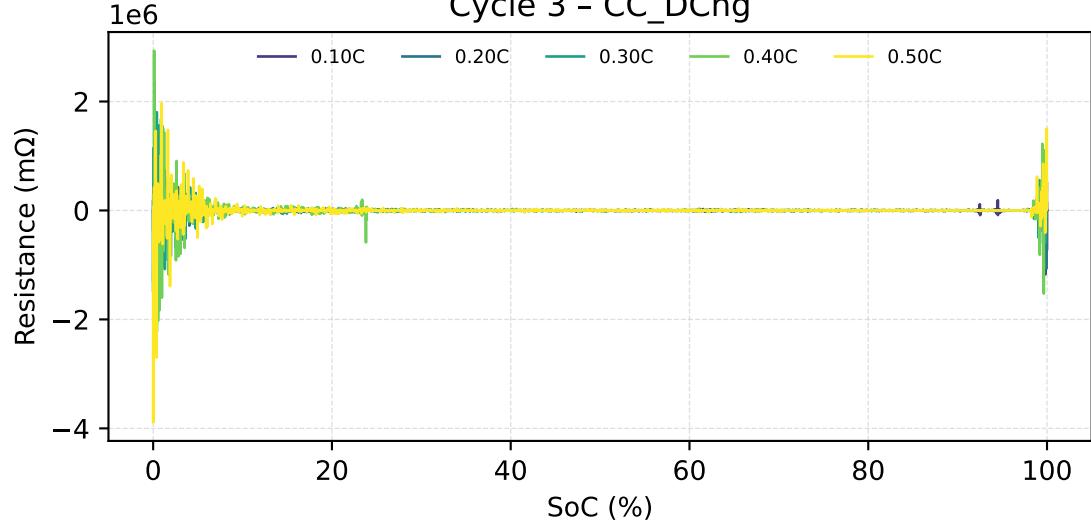


# SoC vs Resistance – RD\_RateCapability\_0065

Cycle 3 – CCCV\_Chg

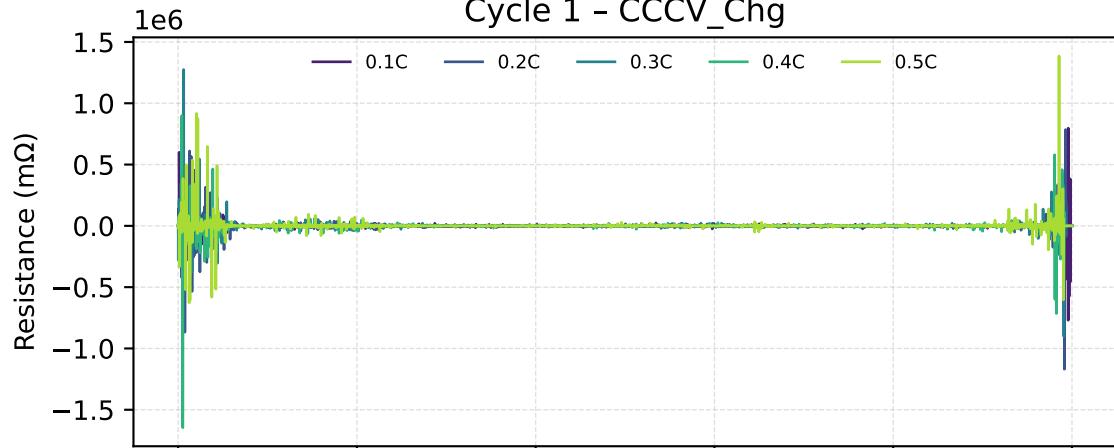


Cycle 3 – CC\_DChg

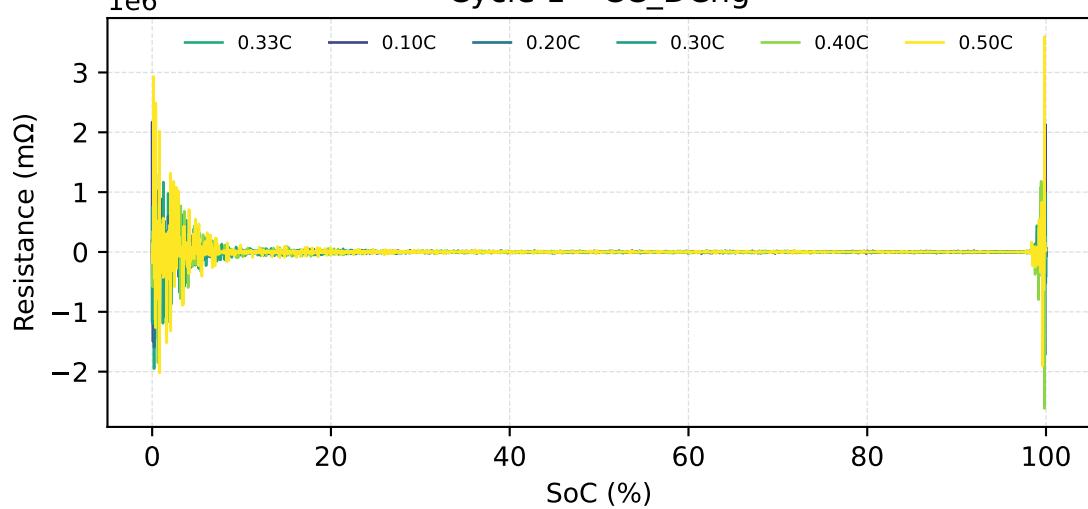


# SoC vs Resistance – RD\_RateCapability\_0074

Cycle 1 - CCCV\_Chg

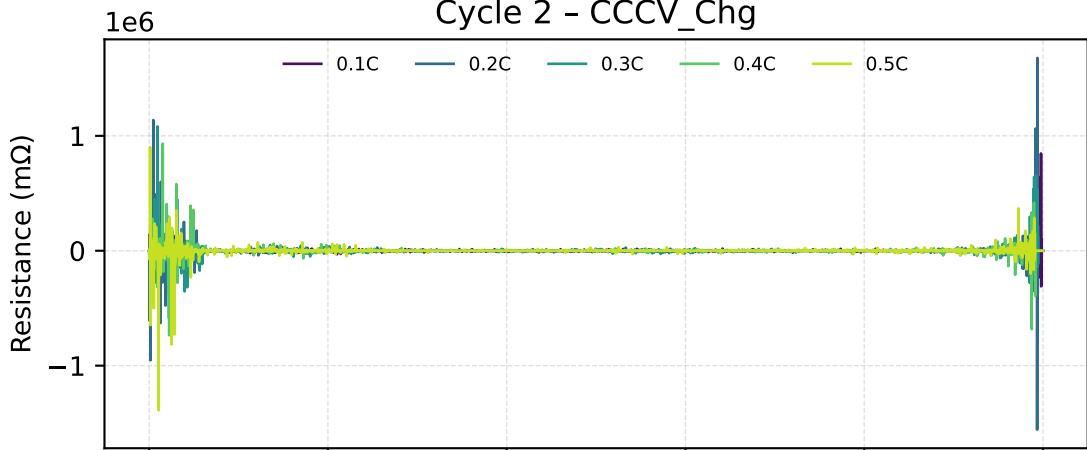


Cycle 1 - CC\_DChg

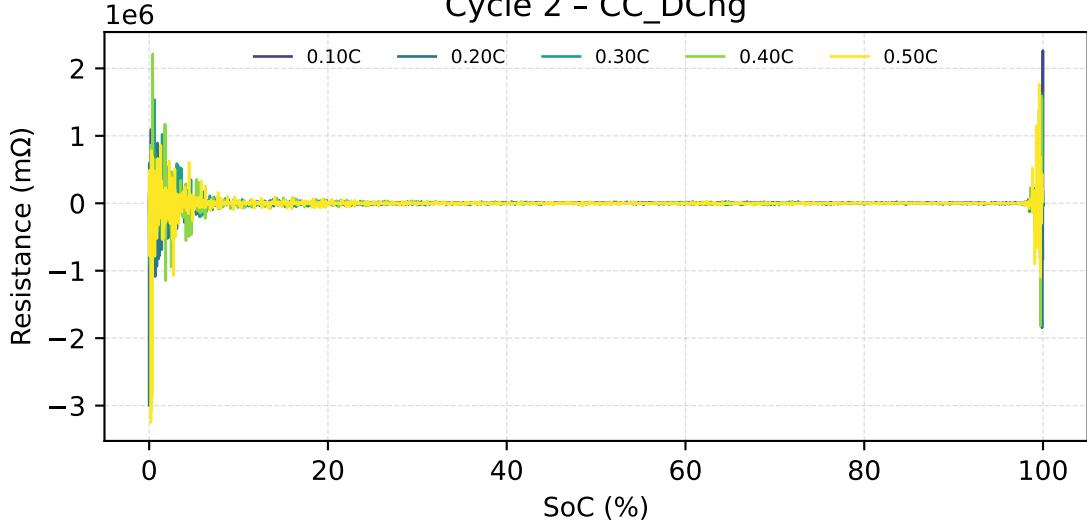


# SoC vs Resistance – RD\_RateCapability\_0074

Cycle 2 – CCCV\_Chg

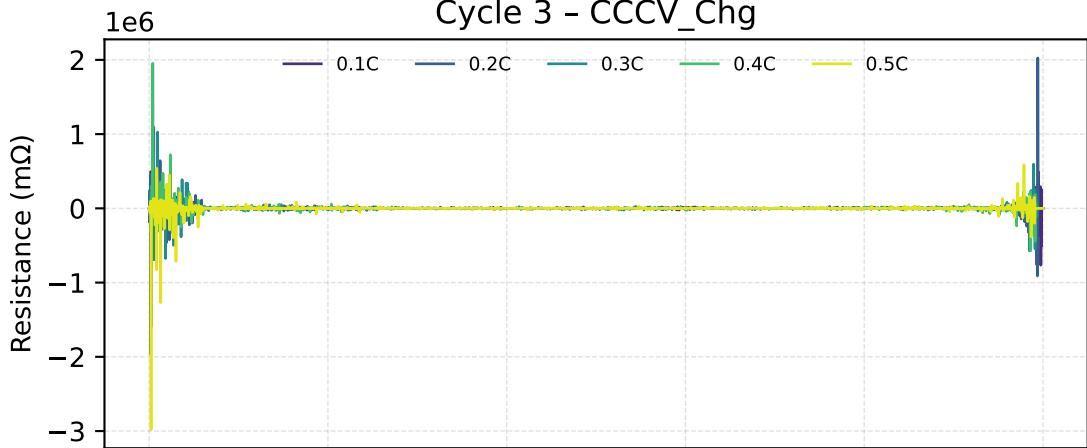


Cycle 2 – CC\_DChg

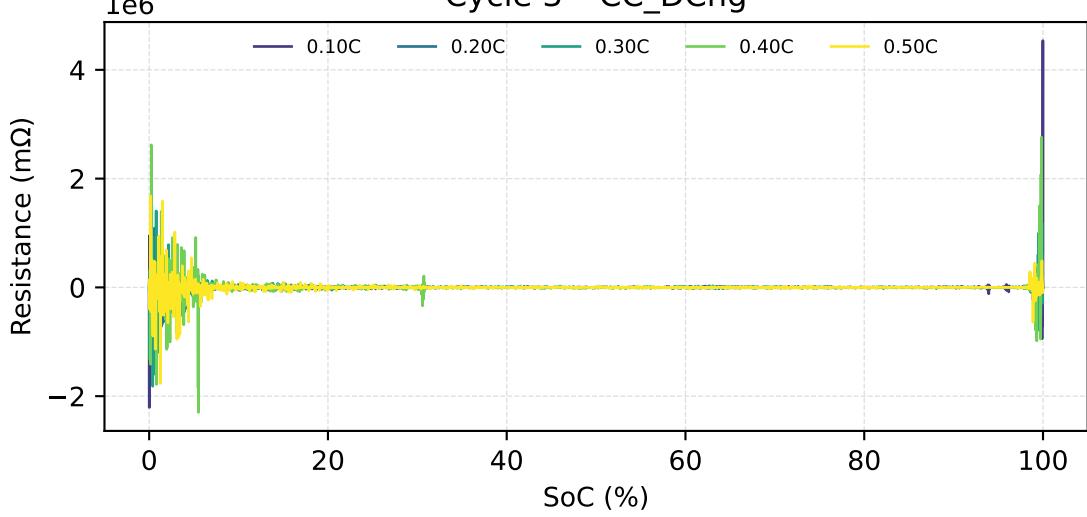


# SoC vs Resistance – RD\_RateCapability\_0074

Cycle 3 – CCCV\_Chg

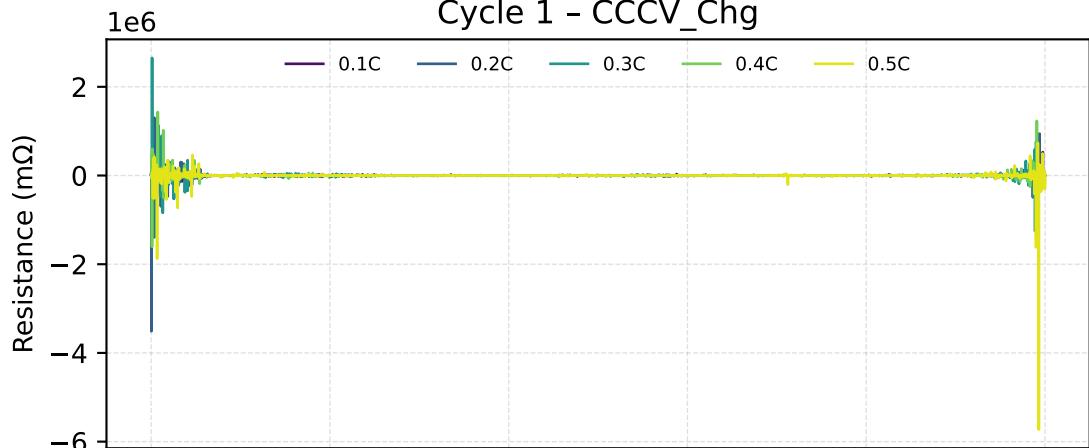


Cycle 3 – CC\_DChg

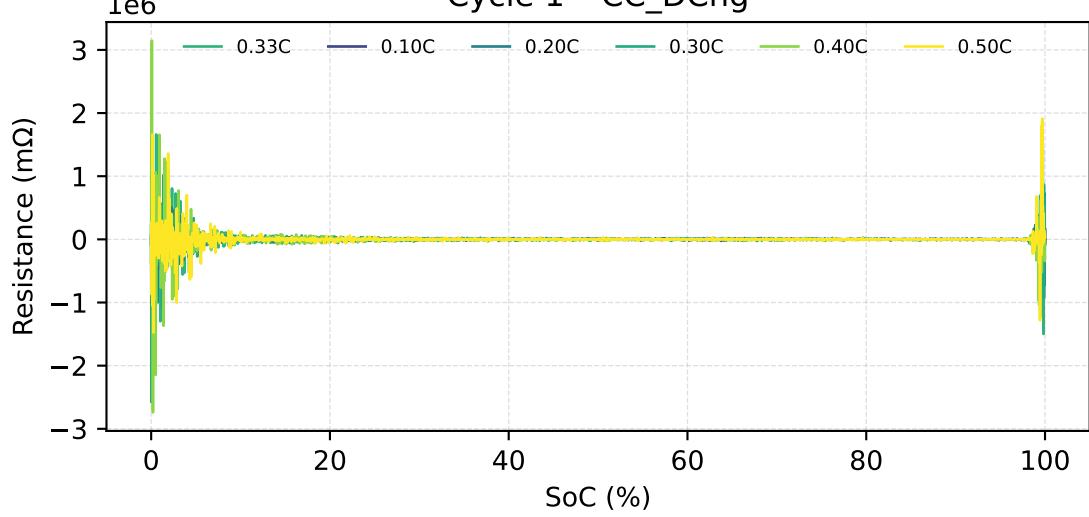


# SoC vs Resistance – RD\_RateCapability\_0078

Cycle 1 - CCCV\_Chg

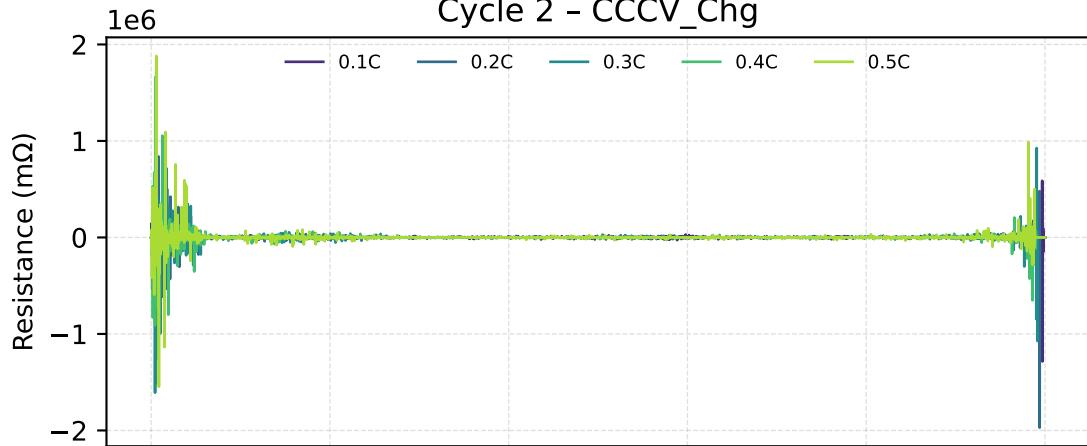


Cycle 1 - CC\_DChg

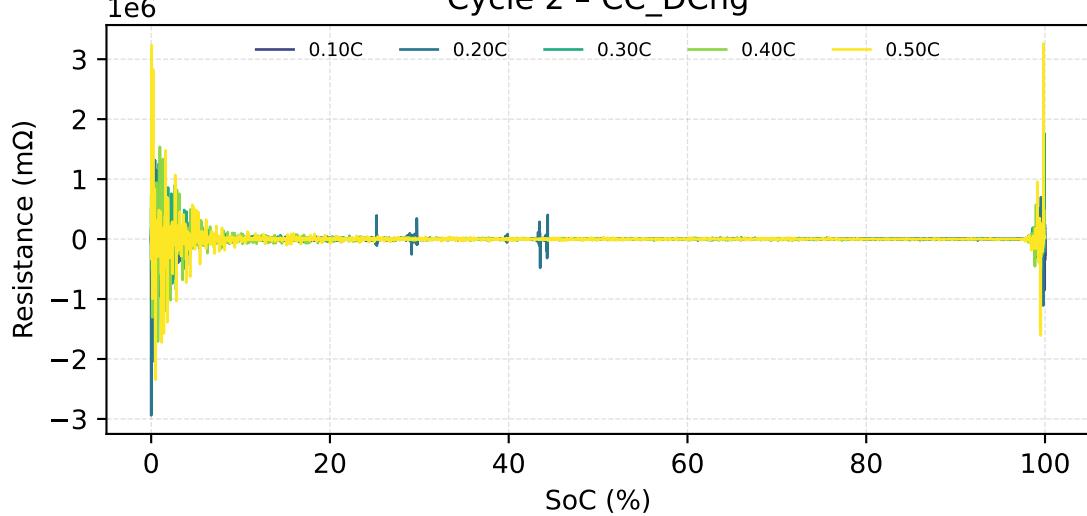


# SoC vs Resistance – RD\_RateCapability\_0078

Cycle 2 – CCCV\_Chg

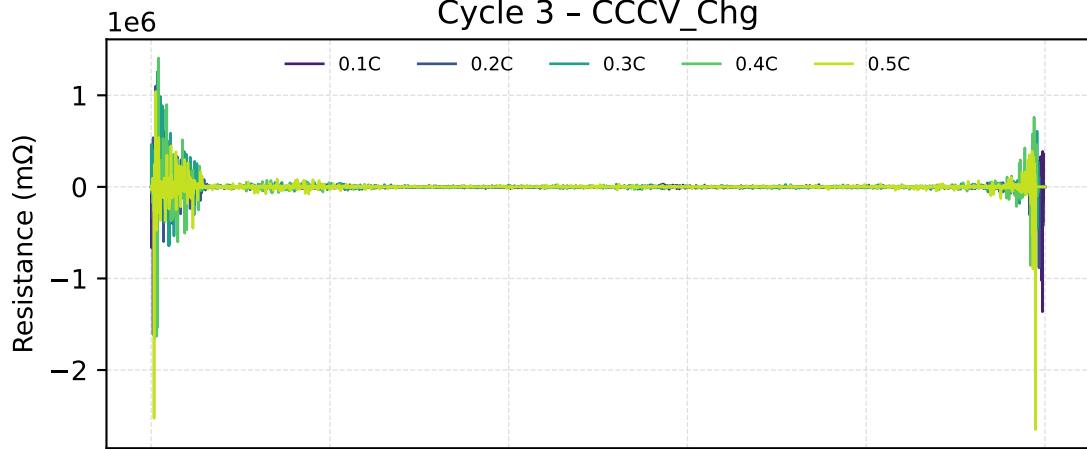


Cycle 2 – CC\_DChg

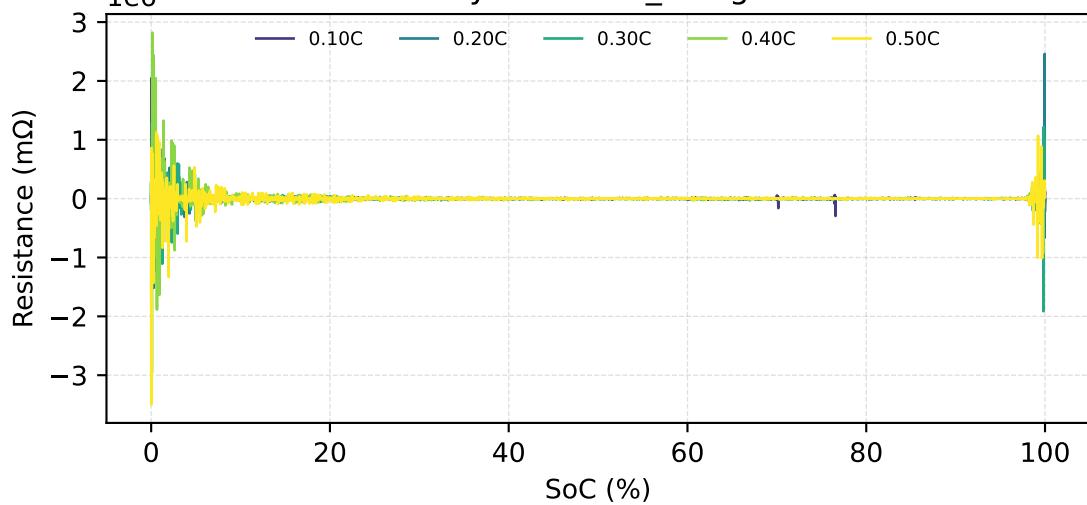


# SoC vs Resistance – RD\_RateCapability\_0078

Cycle 3 – CCCV\_Chg

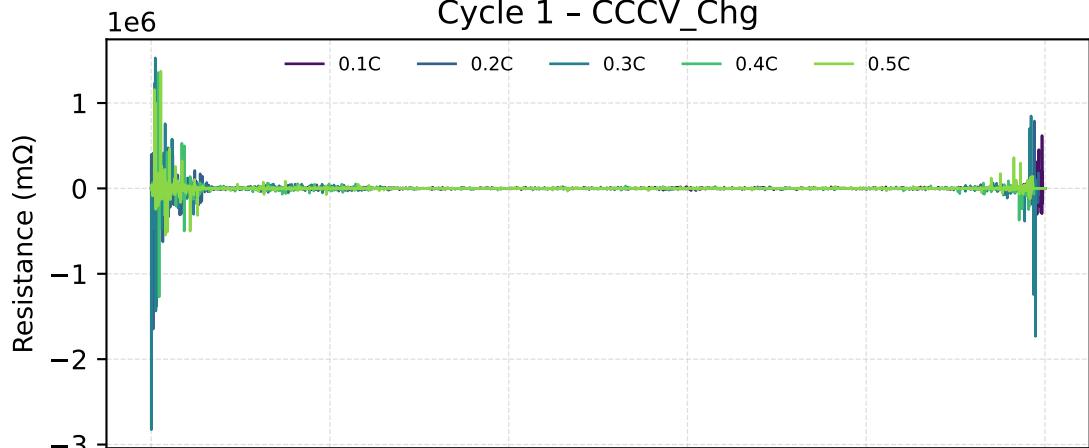


Cycle 3 – CC\_DChg

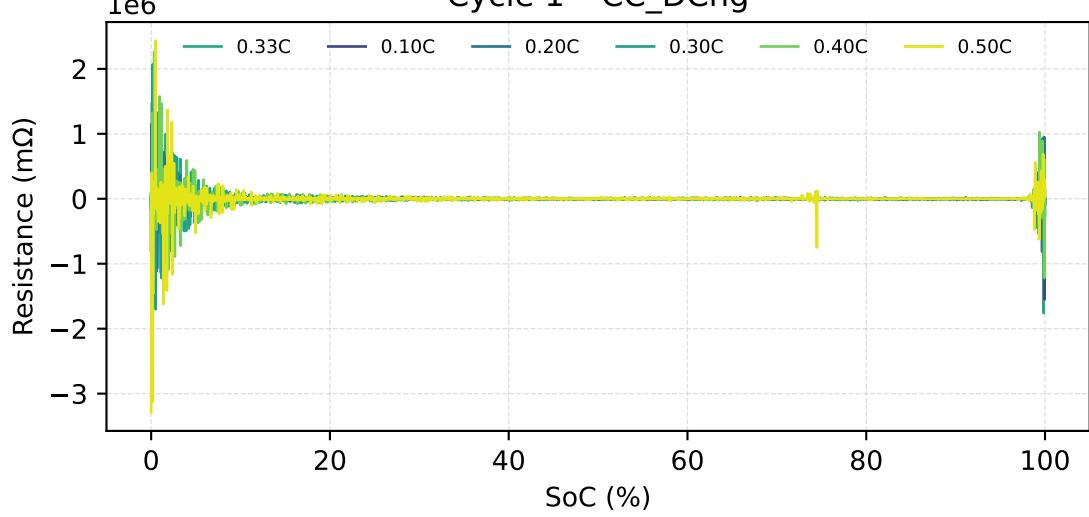


# SoC vs Resistance – RD\_RateCapability\_0080

## Cycle 1 - CCCV\_Chg

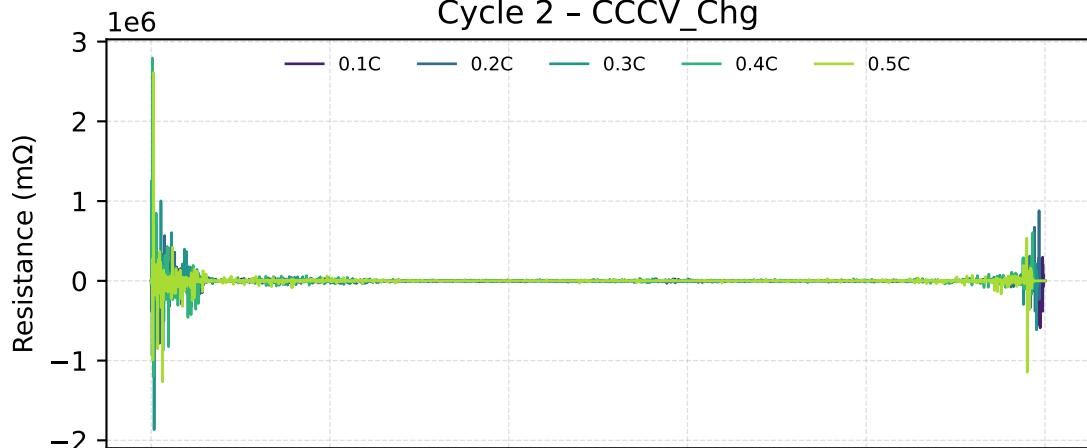


## Cycle 1 - CC\_DChg

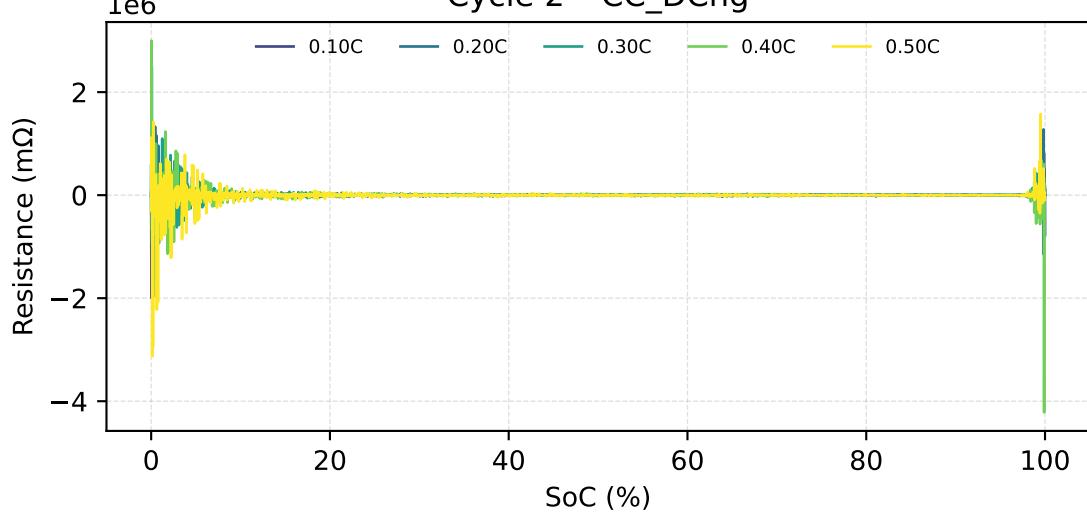


# SoC vs Resistance – RD\_RateCapability\_0080

Cycle 2 – CCCV\_Chg

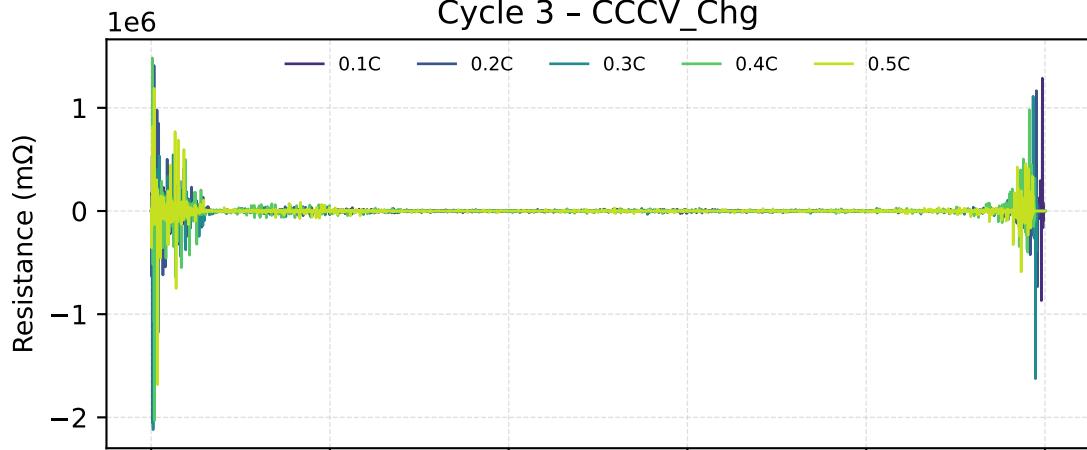


Cycle 2 – CC\_DChg

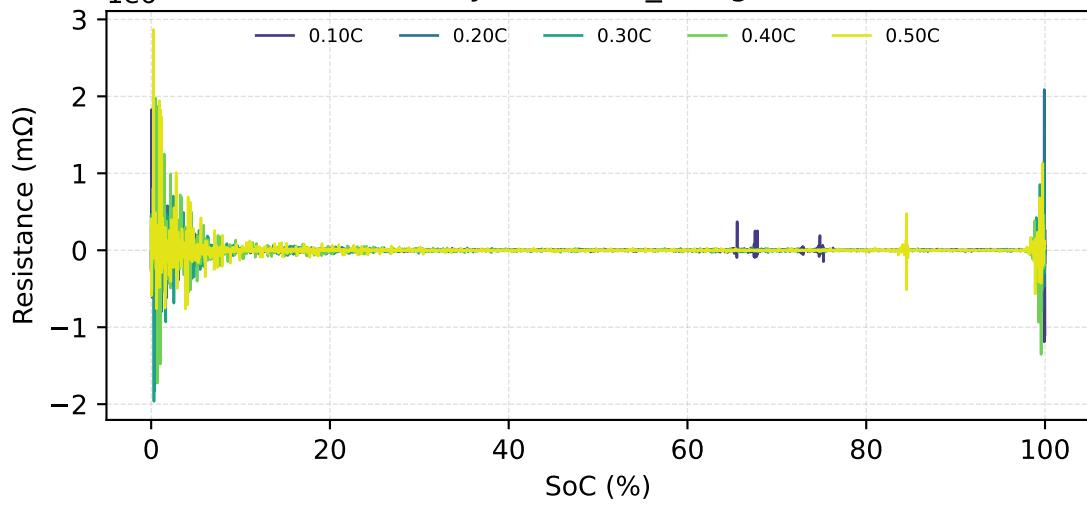


# SoC vs Resistance – RD\_RateCapability\_0080

Cycle 3 – CCCV\_Chg

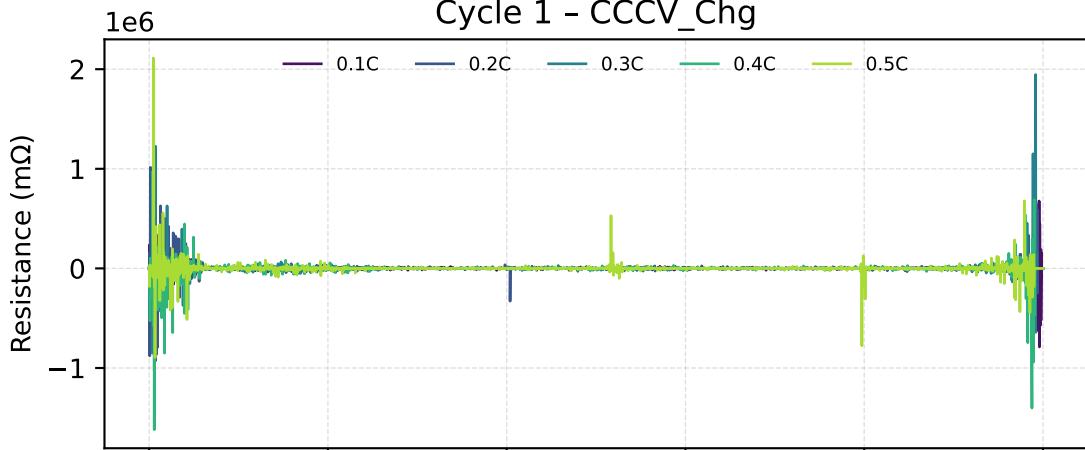


Cycle 3 – CC\_DChg

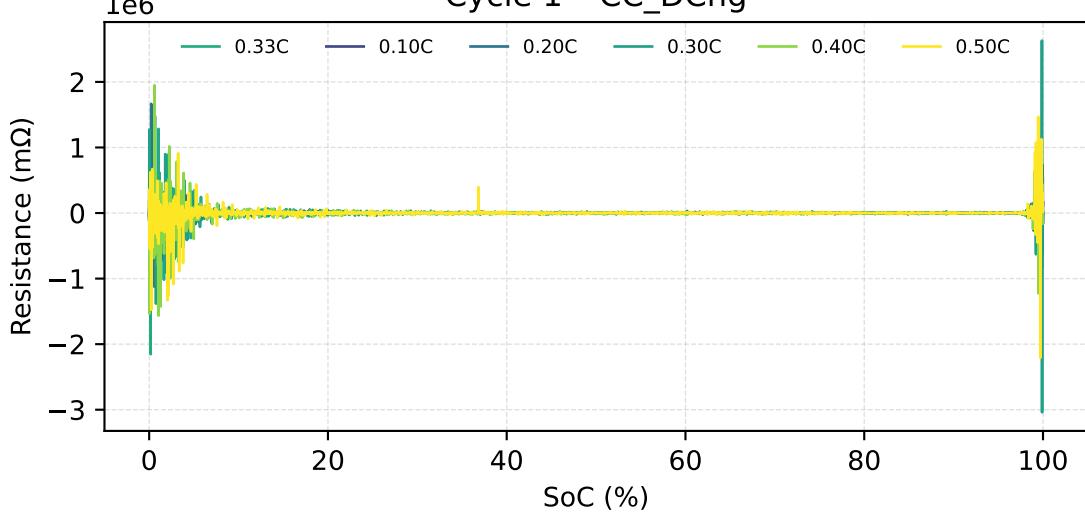


# SoC vs Resistance – RD\_RateCapability\_0087

## Cycle 1 – CCCV\_Chg



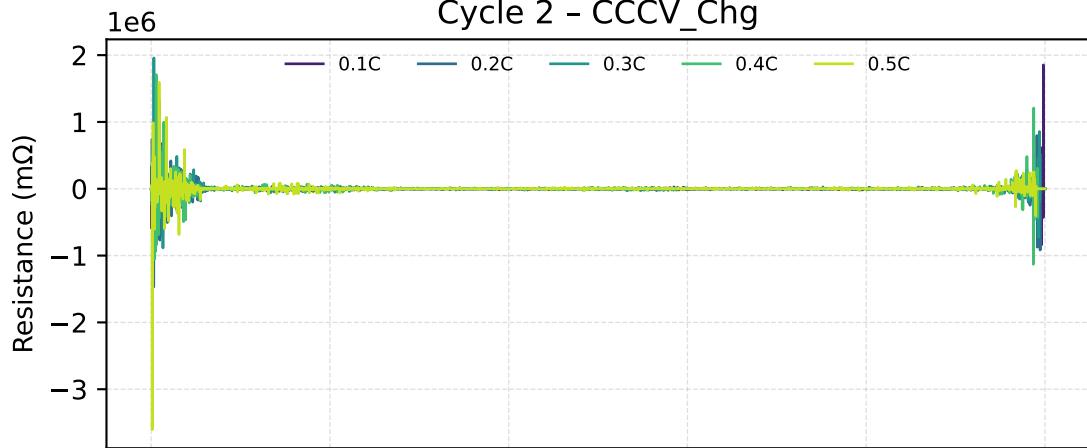
Cycle 1 – CC\_DChg



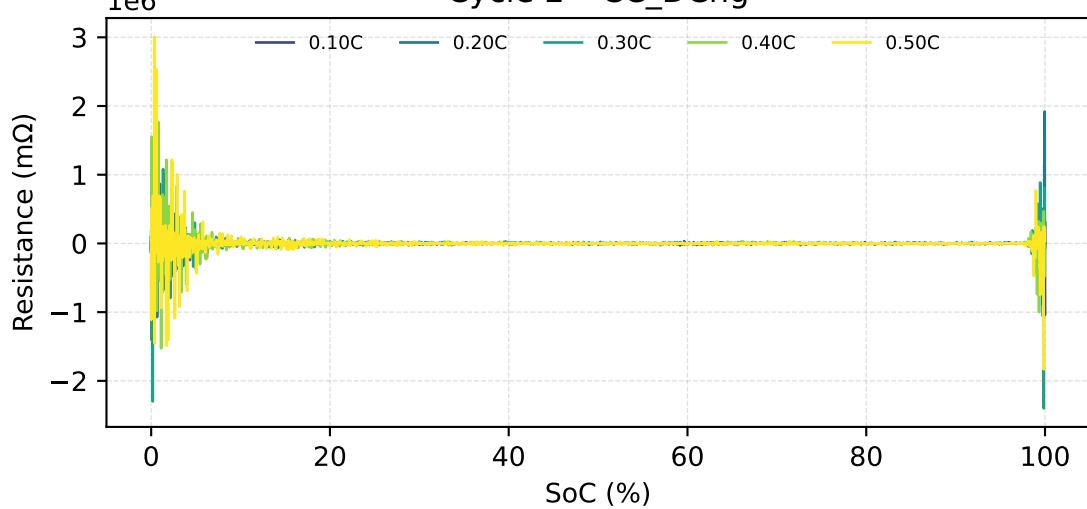
SoC (%)

# SoC vs Resistance – RD\_RateCapability\_0087

Cycle 2 – CCCV\_Chg

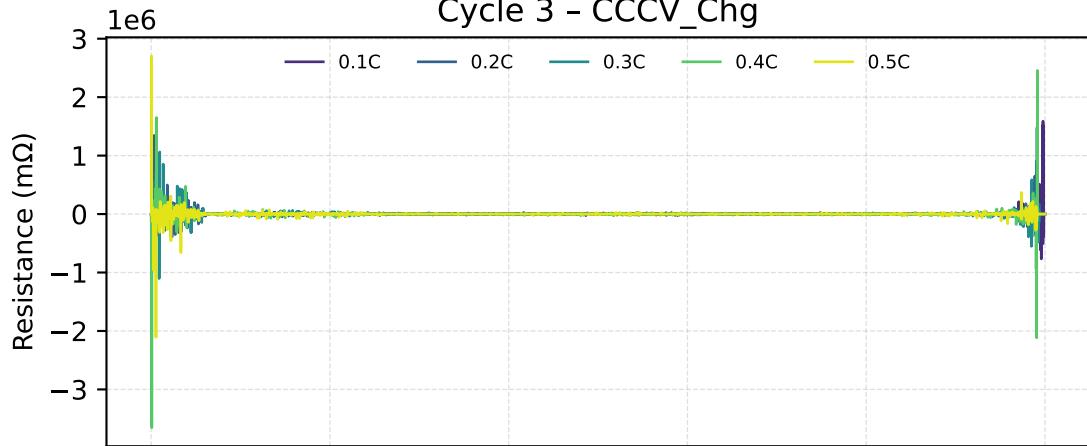


Cycle 2 – CC\_DChg

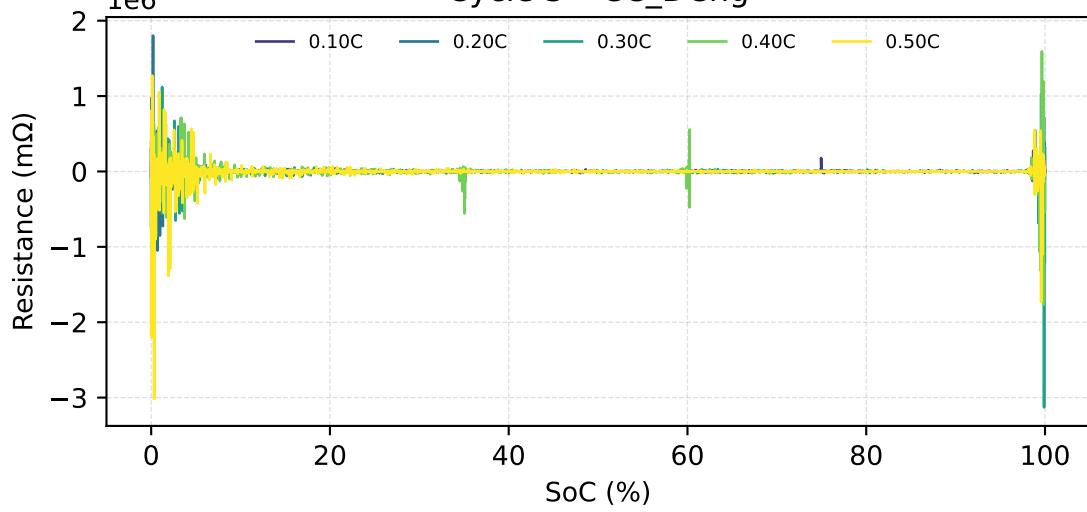


# SoC vs Resistance – RD\_RateCapability\_0087

Cycle 3 – CCCV\_Chg

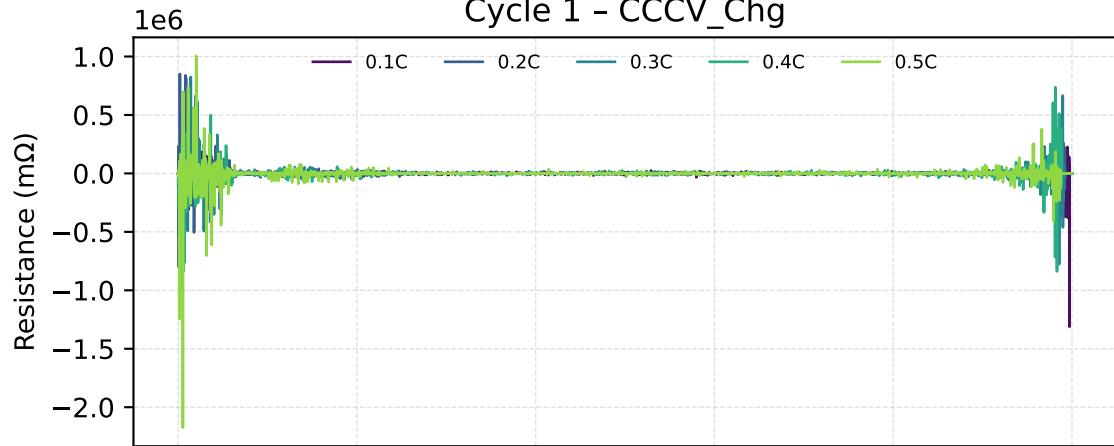


Cycle 3 – CC\_DChg

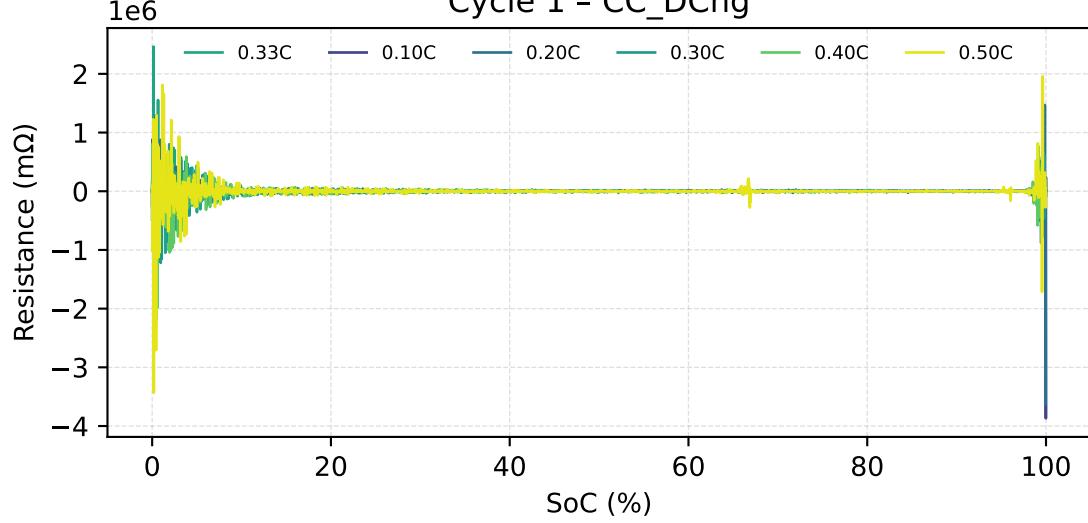


# SoC vs Resistance – RD\_RateCapability\_0091

Cycle 1 - CCCV\_Chg

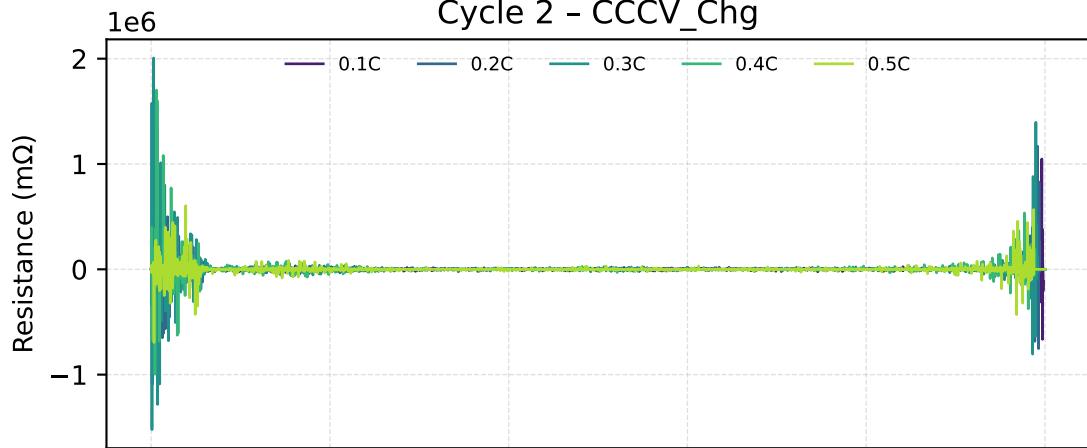


Cycle 1 - CC\_DChg

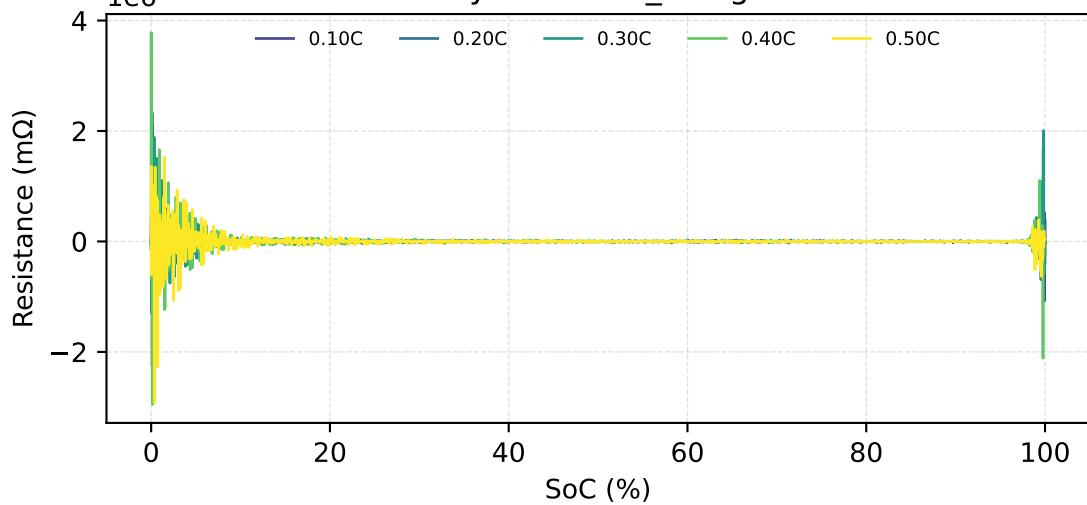


# SoC vs Resistance – RD\_RateCapability\_0091

Cycle 2 – CCCV\_Chg



Cycle 2 – CC\_DChg



# SoC vs Resistance – RD\_RateCapability\_0091

## Cycle 3 – CCCV\_Chg

