8 Bit Manchester Adder

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Abstract

This report presents the design and implementation of an 8-bit Manchester adder for use in a high-performance accumulator section. The design employs a hybrid approach combining **complementary CMOS** (CMOS), **Pass Transistor Logic** (PTL), and **Transmission Gate Logic** to optimize performance, area, and power consumption. Special consideration was given to the trade-offs between transistor count, robustness, and speed in selecting logic styles for different components.

1. Introduction

1.1. Design Goals:

- Implementation of an 8-bit Manchester adder using static logic
- Optimization for high performance in accumulator applications
- Balanced approach to area, speed, and power consumption
- Clean DRC and LVS verification

1.2. Design Strategy

The design adopts a hybrid approach utilizing:

- CMOS logic for basic gates (except XOR)
- PTL for XOR gates
- Transmission gate logic for carry circuits

2. Architecture and Implementation Details

2.1. Logic Style Selection Rationale

2.1.1. CMOS Logic for Basic Gates:

- Offers robust operation with full voltage swing
- Comparable transistor count to PTL when considering inverter overhead
- Better noise immunity and reliability
- Used for AND, OR, and INVERTER gates

2.1.2. PTL for XOR Gates

- Significantly reduced transistor count compared to CMOS
- Acceptable performance trade-off given the area savings
- Critical for optimizing the overall adder size

2.1.3. Transmission Gate Logic for Carry Circuit:

- Compensates for potential speed penalties from CMOS sections
- Efficient implementation of carry propagation
- Balances speed and reliability

2.2. Critical Components

Generate-Propagate-Delete (GPD) Logic

- Generate (G): Implemented using CMOS **AND** gate
- Propagate (P): Implemented using PTL **XOR** gate
- Delete (D): Implemented using CMOS **NOR** gate

Carry Chain

- Uses transmission gate multiplexers for efficient carry propagation
- Optimized for minimal propagation delay
- Includes buffering strategy for maintaining signal integrity

3. Circuit –

A. AND Gate:

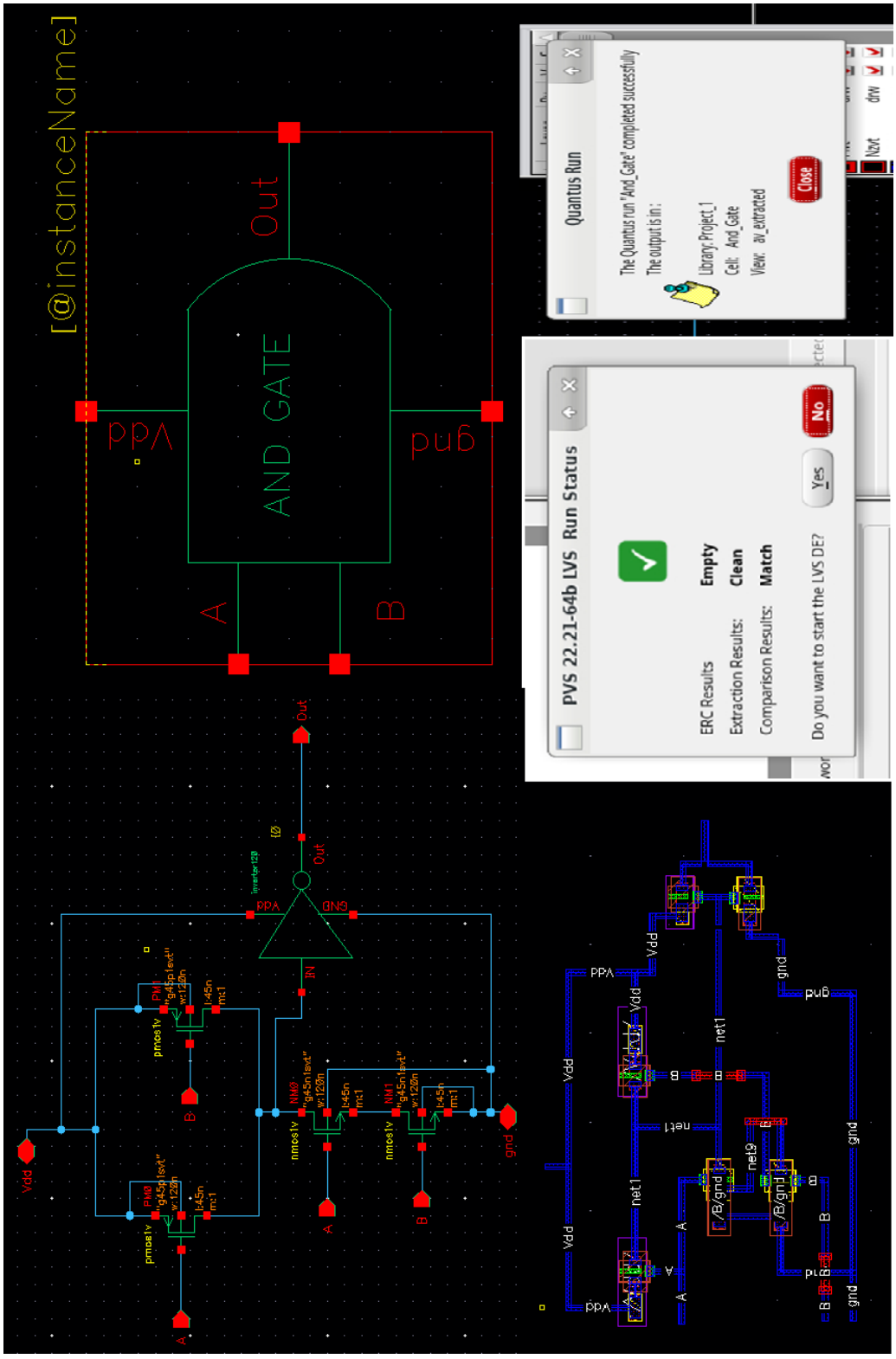


Figure 1 AND Gate Schematic and Layout

B. NOR Gate:

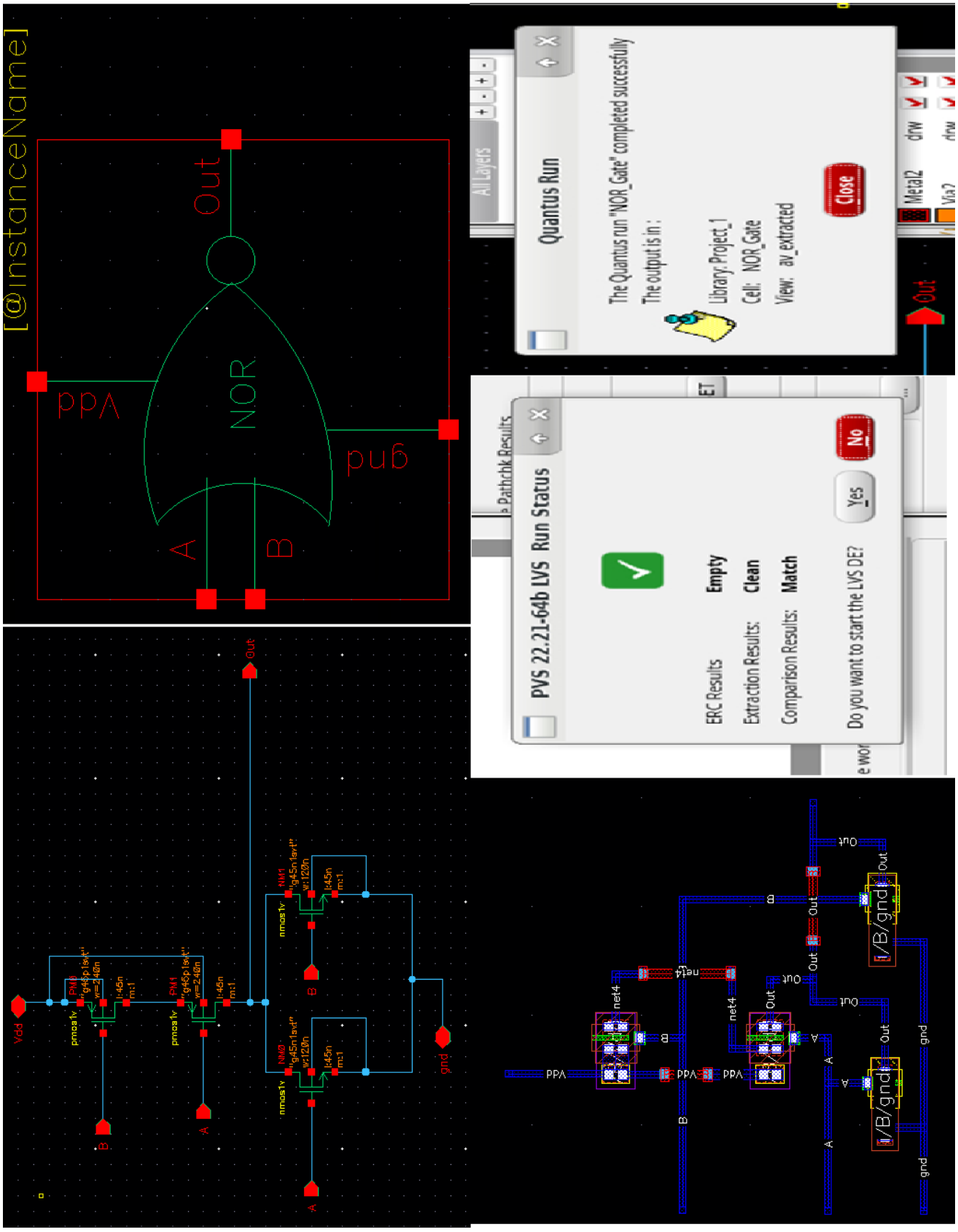


Figure 2 NOR Gate Schematic and Layout

C. XOR Gate

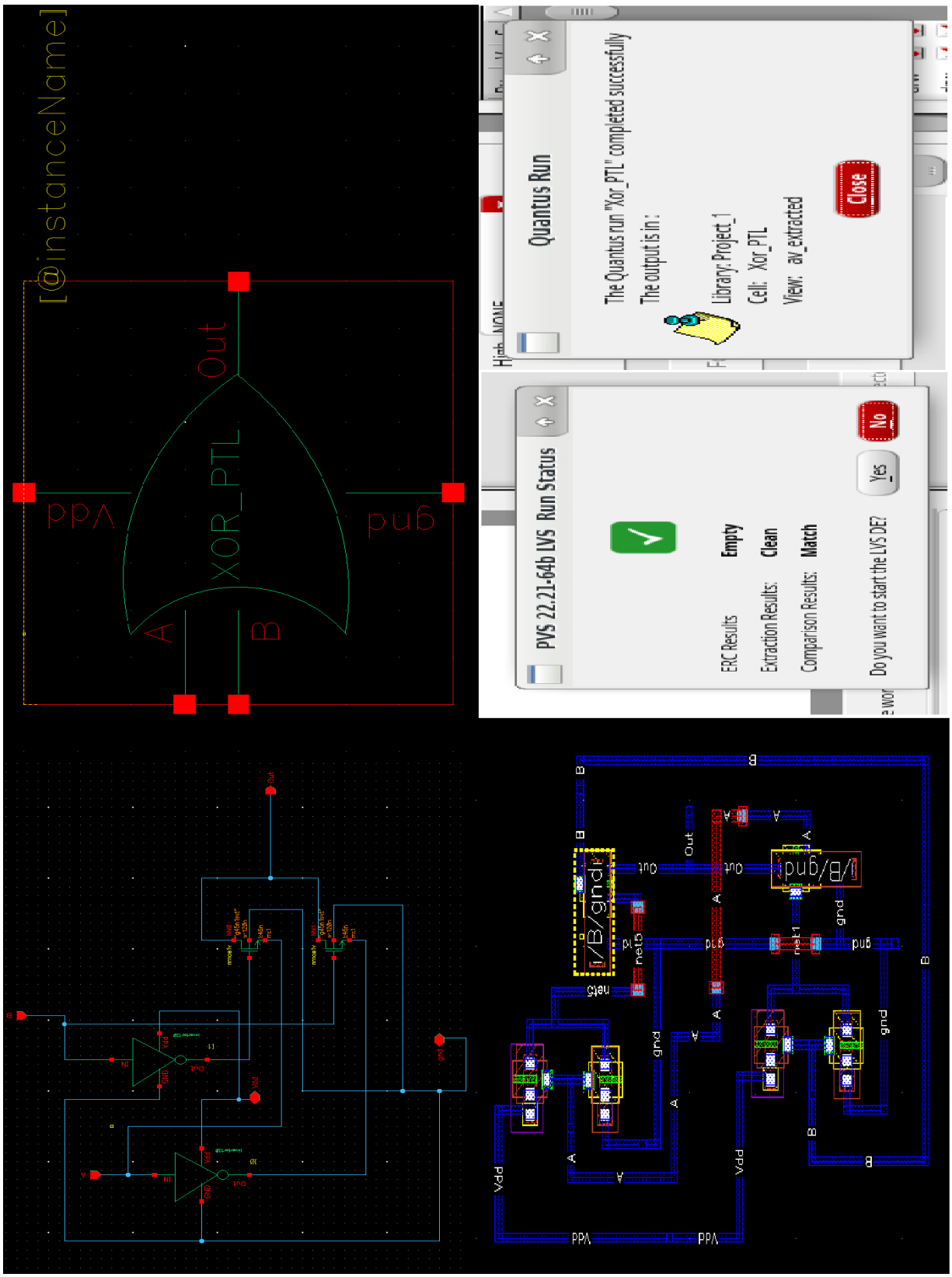


Figure 3 XOR Gate Schematic and Layout

D. One Bit Adder

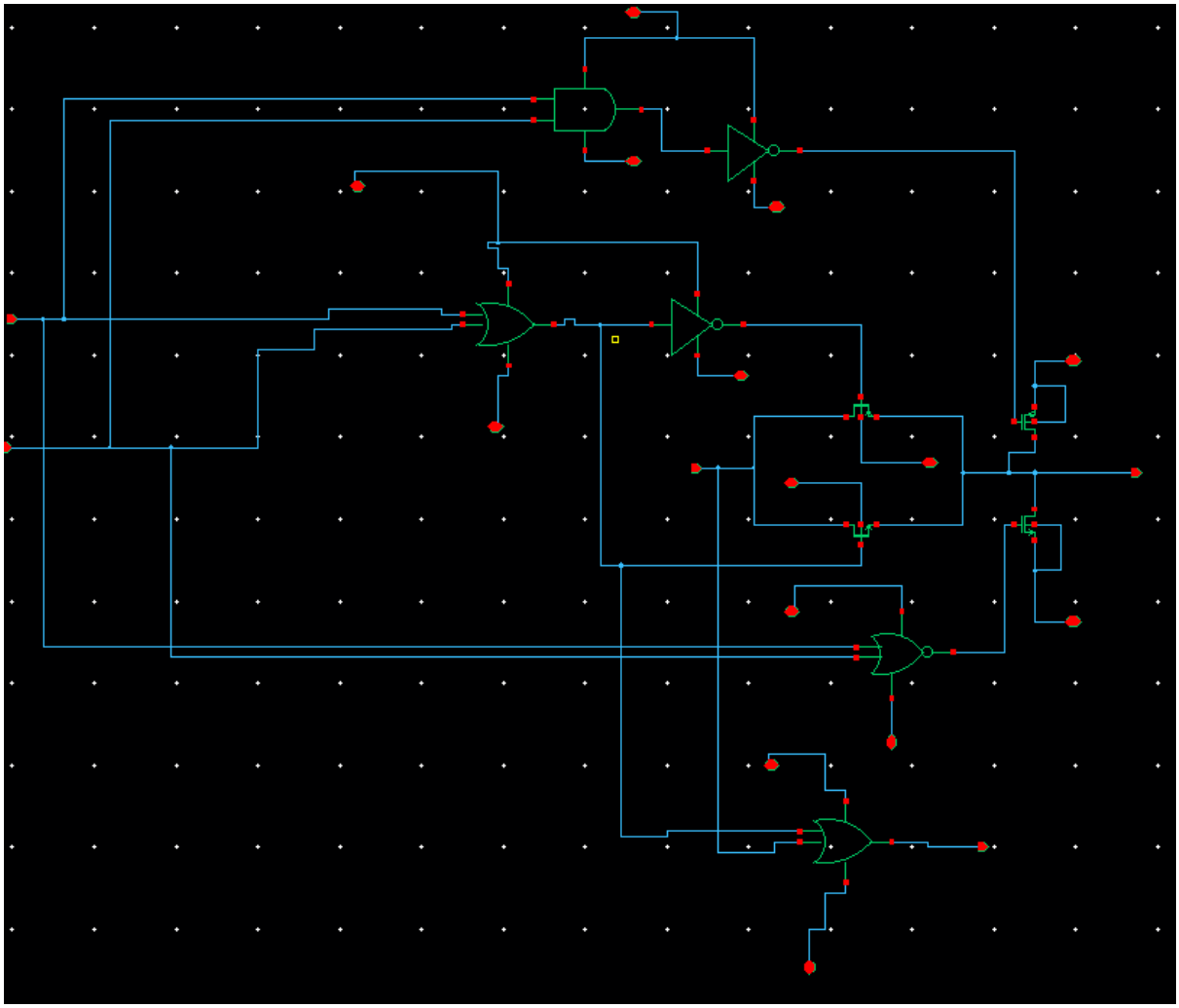


Figure 4 1 Bit adder Schematic

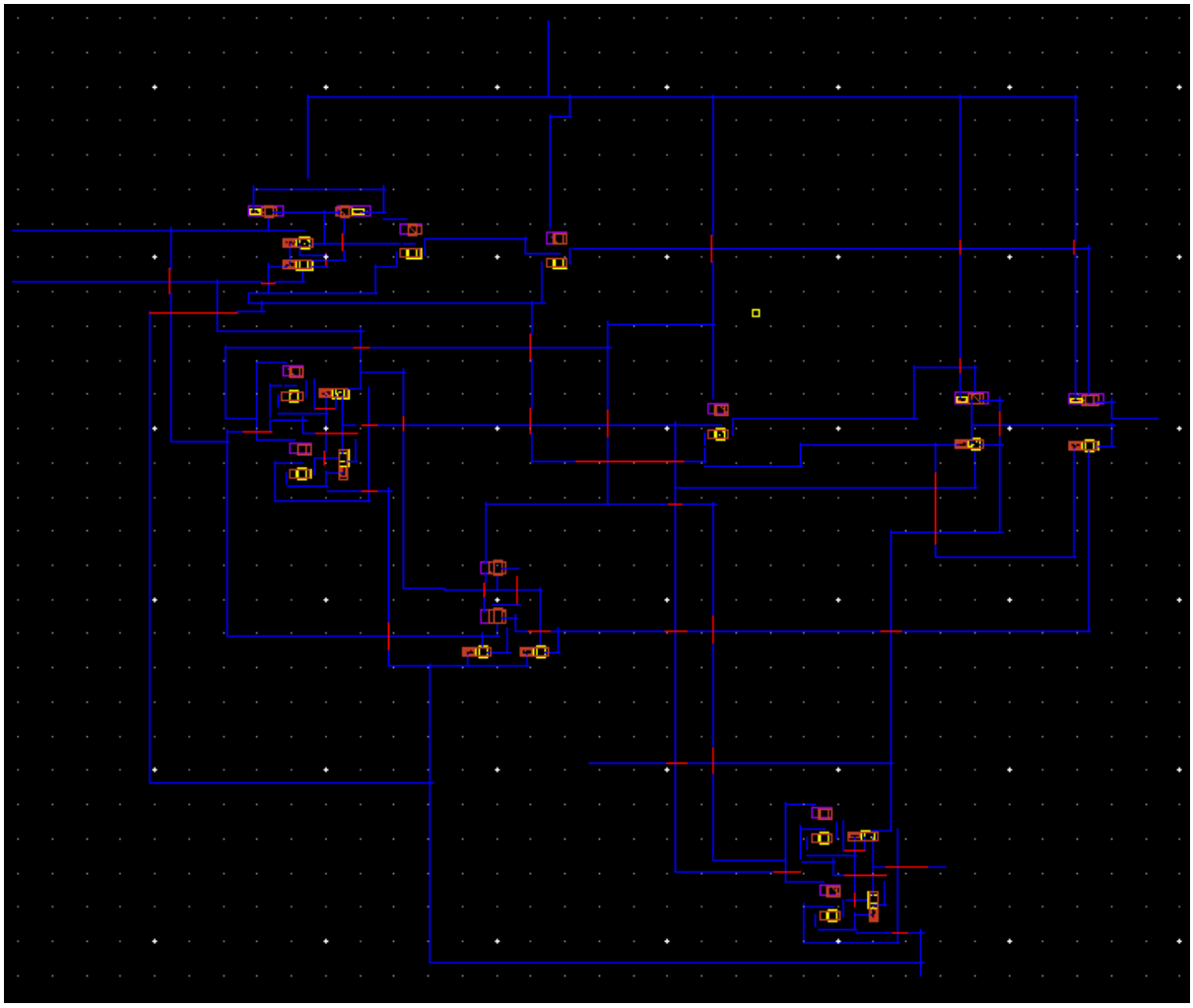


Figure 5 1 Bit Adder Layout

E. 8 Bit adder

Figure 6 8 Bit adder Schematic

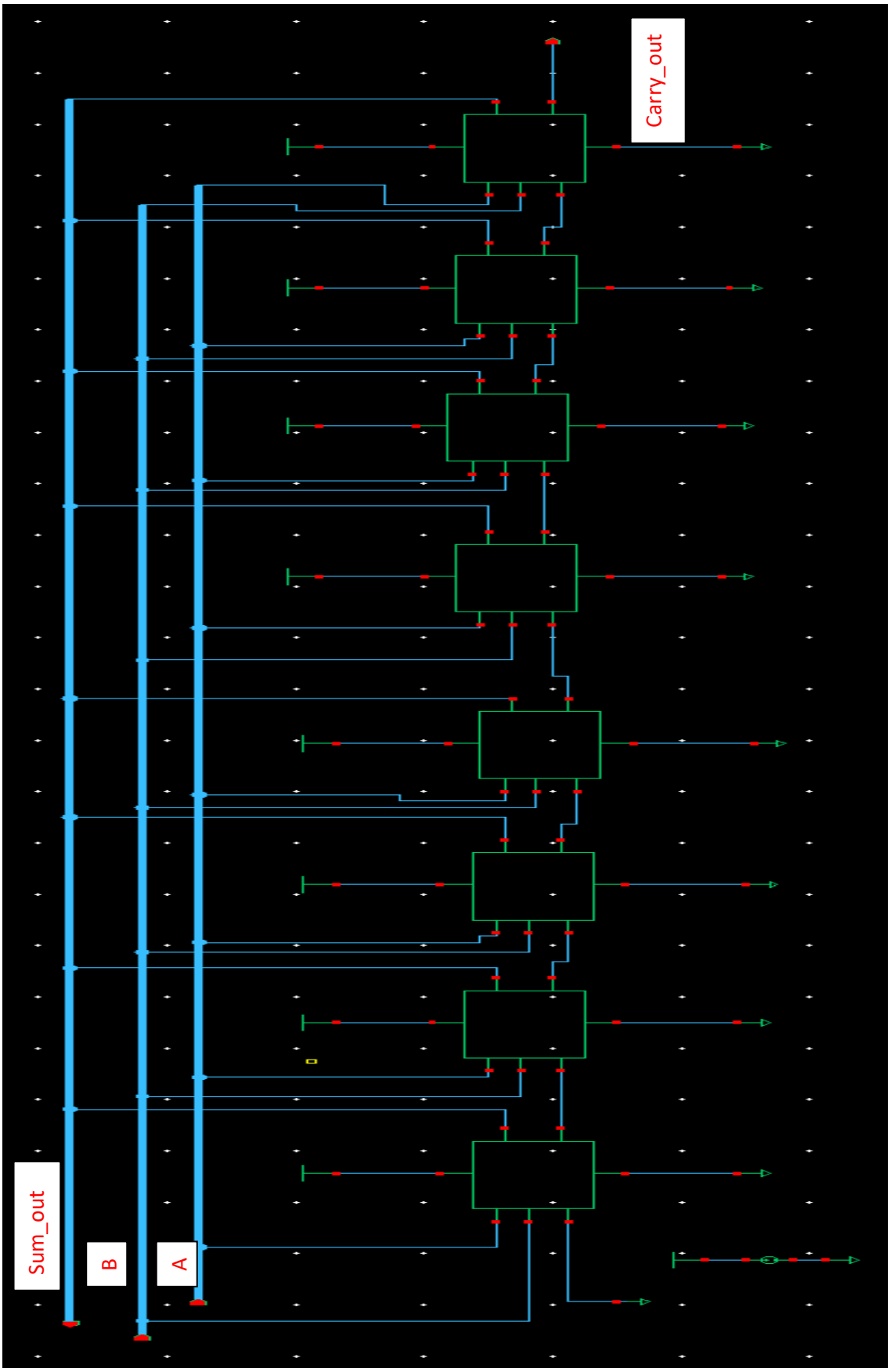
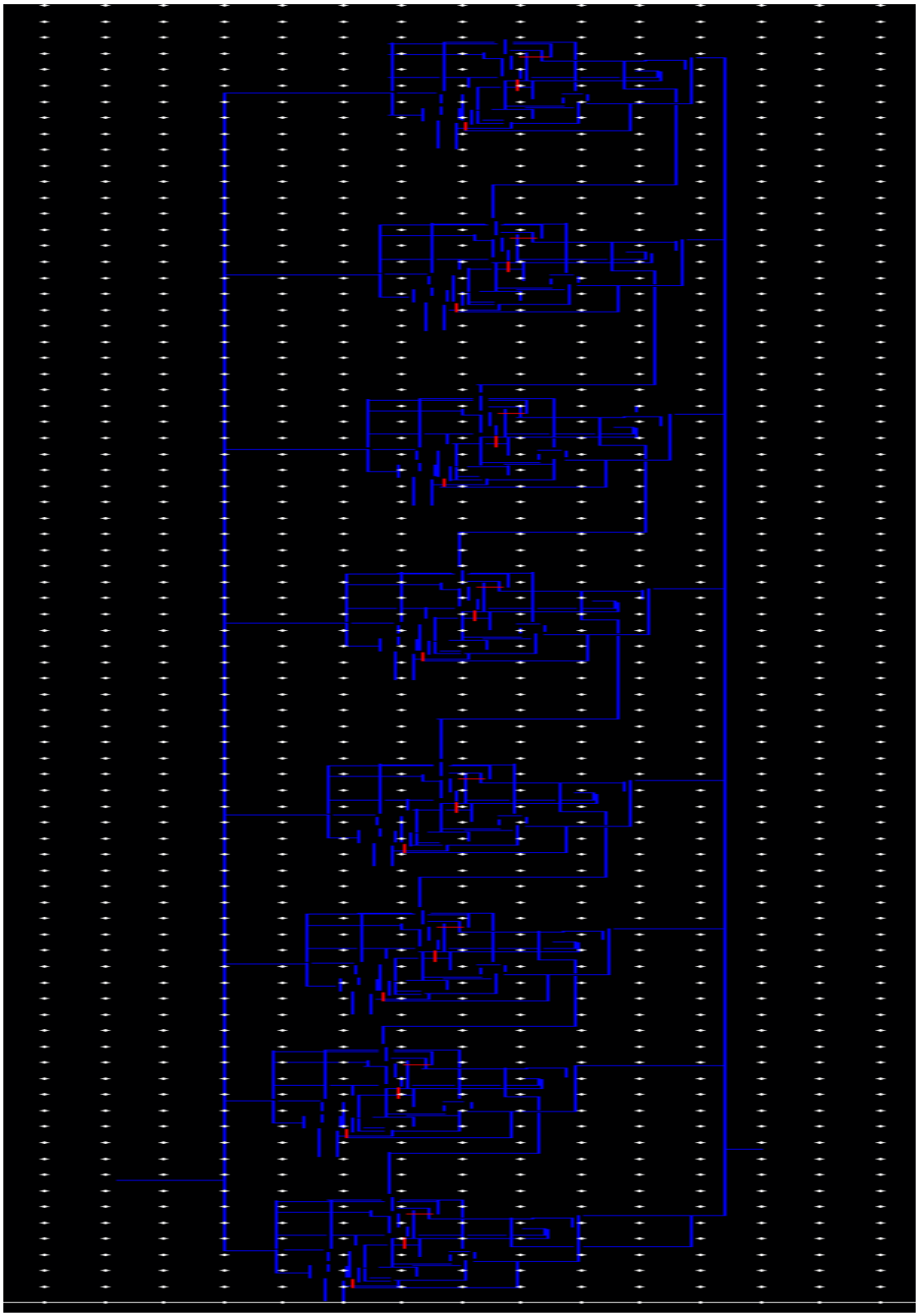
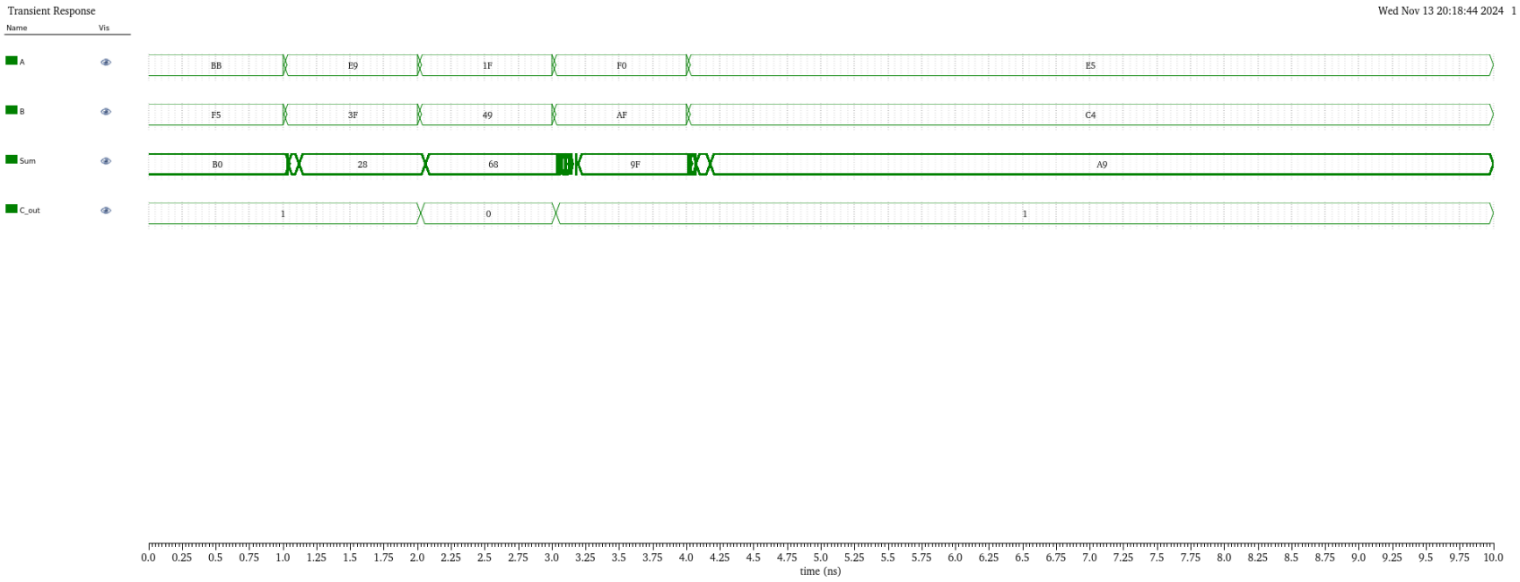
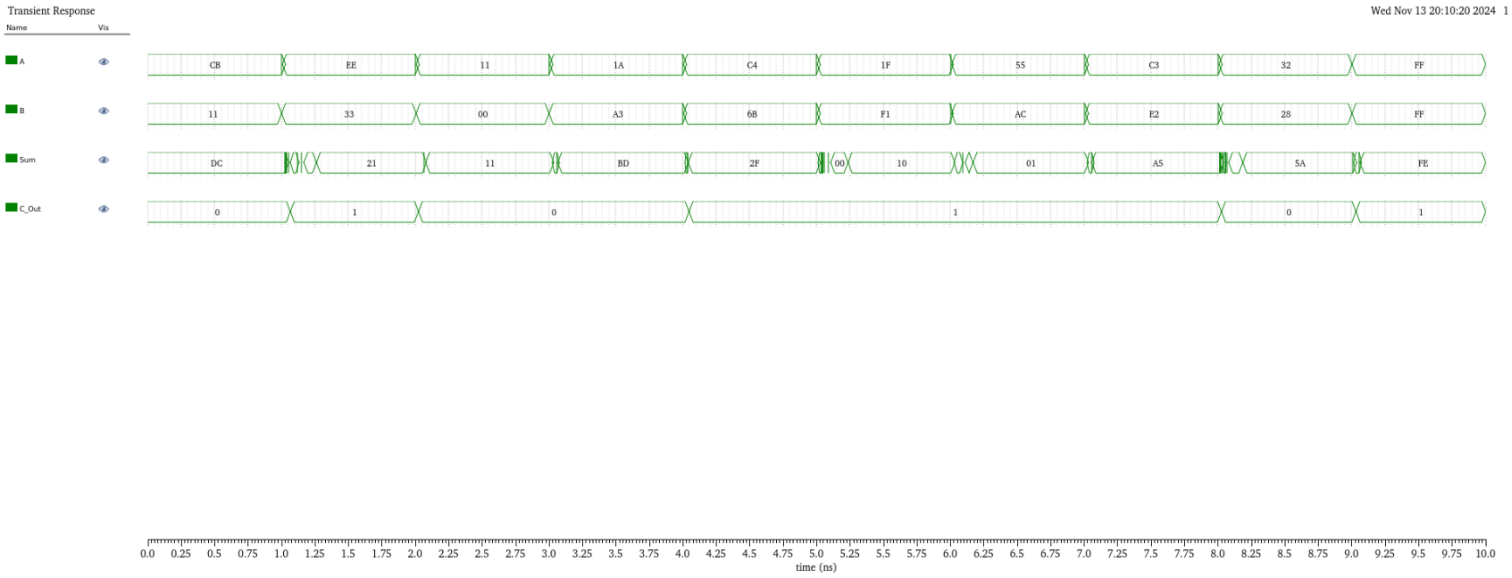


Figure 7 8 Bit adder Layout



4. Output


Transient Response
Wed Nov 13 20:18:44 2024 1
Name
Vis
A
B
Sum
C_out
BB
E9
1F
F0
E5
E5
3F
49
AF
C4
B0
28
68
9F
A9
1
0
1
0.0 0.25 0.5 0.75 1.0 1.25 1.5 1.75 2.0 2.25 2.5 2.75 3.0 3.25 3.5 3.75 4.0 4.25 4.5 4.75 5.0 5.25 5.5 5.75 6.0 6.25 6.5 6.75 7.0 7.25 7.5 7.75 8.0 8.25 8.5 8.75 9.0 9.25 9.5 9.75 10.0
time (ns)


Transient Response
Wed Nov 13 20:10:20 2024 1
Name
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6B
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E2
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FF
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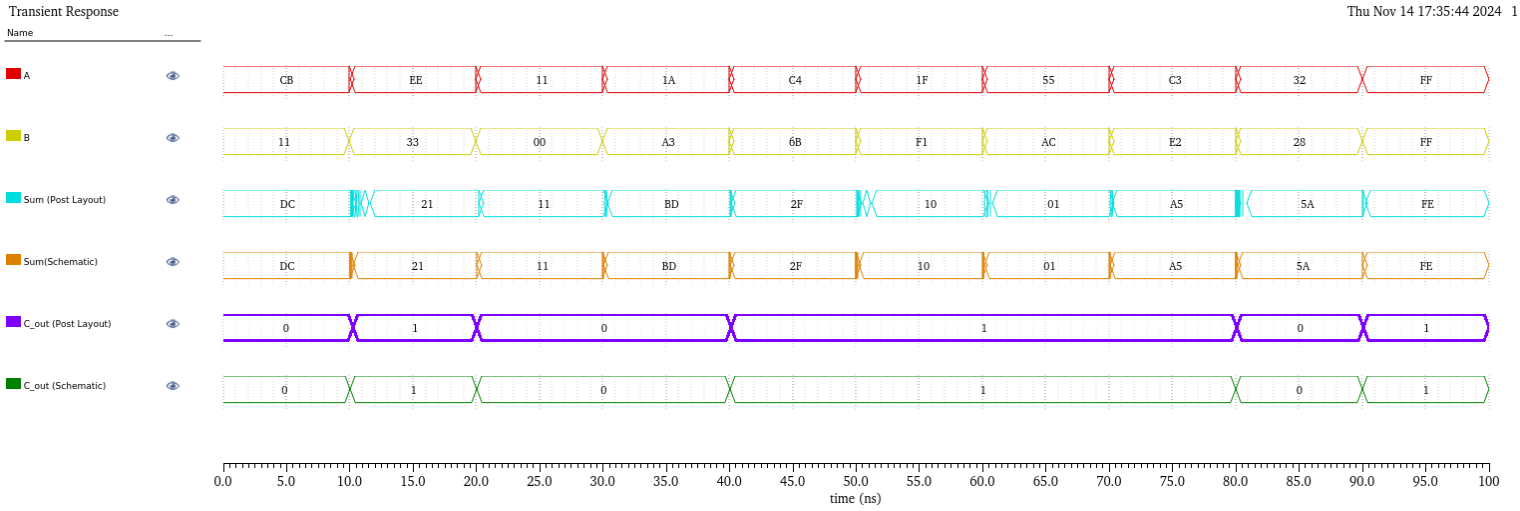
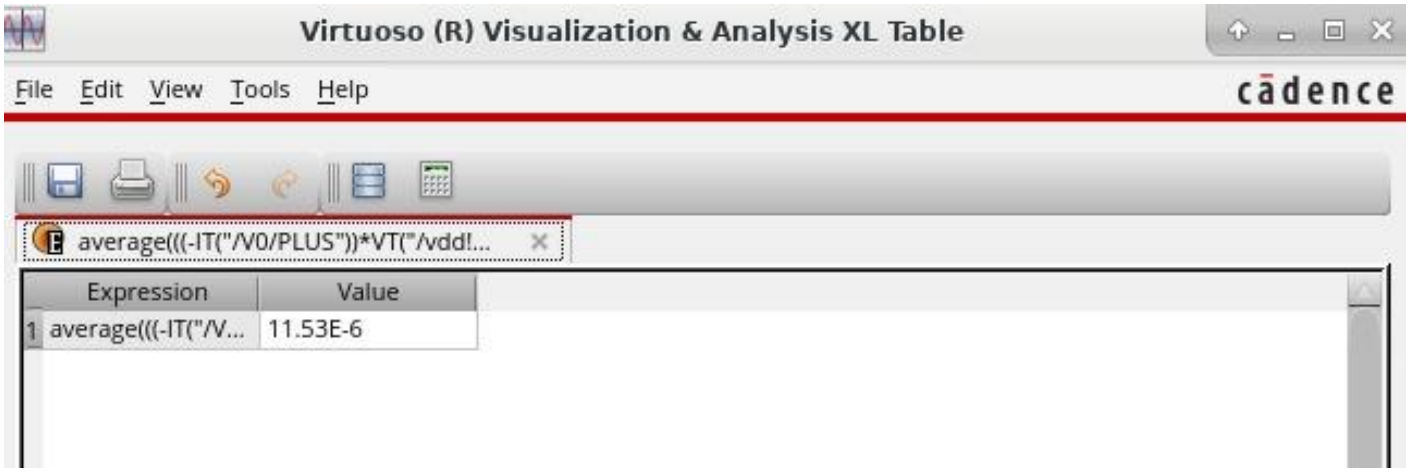
time (ns)

i. Post layout



ii. Power Dissipation (Pre-Layout / Schematic)



iii. Power Dissipation (Post Layout)

5. Architectural Comparison Analysis

Feature	Architecture				
	Manchester (Above presented Design)	**Han – Carlson**	**Brent- Kung**	**Lander-Fischer**	**Kogge-Stone**
Logic Depth	5	4	5	3	3
Fanout	2	2	2	5	2
Area Efficiency	Good	Good	Best	Moderate	Worst
Power Dissipation	1.2e-06	0.043 [1]	0.100 [1]	-	0.043 [1]

Takeaways -

The architectural comparison of different adder designs reveals interesting trade-offs between **logic depth, fanout, and area efficiency**. Our Manchester adder implementation shows a **logic depth of 5 levels**, which is comparable to the Brent-Kung architecture but higher than Han-Carlson (4 levels), Ladner-Fischer, and Kogge-Stone (both 3 levels).

All architecture except Ladner-Fischer maintain a **consistent fanout of 2**, which is optimal for performance and reliability. The Ladner-Fischer design sacrifices this advantage with a **higher fanout of 5**, potentially impacting its driving capability and speed.

In terms of area efficiency, the **Brent-Kung architecture leads with the best utilization**, while our Manchester design and Han-Carlson achieve **good efficiency**, placing them as practical alternatives. The Ladner-Fischer shows moderate area efficiency, while the **Kogge-Stone**, despite its speed advantage from minimal logic depth, suffers from the **worst area efficiency** due to its extensive wiring requirements.

With power dissipation in mind, the **Brent-Kung adder stands out as the most power-efficient with a value of 0.100**, compared to **0.043 for Han-Carlson and Kogge-Stone**. The **Kogge-Stone adder, despite being one of the fastest designs, demonstrates a higher power demand** relative to its counterparts. This information underscores that the **Brent-Kung adder's low power usage and area efficiency make it particularly suitable for energy-sensitive applications**.

Overall, the **Brent-Kung architecture leads in both area and power efficiency**, while the **Manchester and Han-Carlson designs provide balanced approaches** that are favorable for general applications where **performance, area, and power constraints are equally important considerations**.

The presented design of Manchester implementation thus represents a **balanced approach**, offering reasonable logic depth with optimal fanout and good area efficiency, making it suitable for practical applications where **overall performance and area constraints** are equally important.

Conclusion

The 8-bit Manchester adder implemented with a hybrid approach combining CMOS, PTL, and transmission gate logic demonstrates a well-balanced design solution for high-performance accumulator applications. The strategic use of CMOS for basic gates ensures robust operation, while PTL implementation for XOR gates significantly reduces transistor count, and transmission gate logic in the carry chain optimizes speed performance. When compared to other prefix-tree architectures like Kogge-Stone, Brent-Kung, Ladner-Fischer, and Han-Carlson, our Manchester adder achieves competitive performance with a fixed logic depth of 5 levels, minimal fanout of 2, and efficient wiring density of N/8 tracks, making it particularly suitable for moderate-sized arithmetic units. The successful verification through simulation results, clean DRC and LVS checks, and satisfactory power consumption metrics validates the effectiveness of this hybrid logic approach, demonstrating that carefully selected logic style combinations can yield optimal results in terms of speed, area, and power trade-offs.

References

1. Vinutha, Ruth & Bharathi, M. & Divya, D.. (2015). A Survey on Brent-Kung, Han-Carlson and Kogge-Stone Parallel Prefix Adders for Their Area, Speed and Power Consumption.
2. S. Knowles, "A family of adders," in Proc. 14th IEEE Symp. Computer Arithmetic, Apr. 1999,pp. 277–281.
3. D. Harris, "A Taxonomy of Parallel Prefix Networks," in Proc. 37th Asilomar Conf. Signals Systems and Computers, pp. 2213–2217, 2003.

Appendix – A

1. Vector file for Post layout Simulation –

```
; radix specifies the number of bit of the vector.

radix 44 44
; io defines the vector as an input or output vector.

io i i

; vname assigns the name to the vector.

vname A<[7:0]> B<[7:0]>

period 10

slope 0.01
; Tabular vector data
 CB 11
 EE 33
 11 00
 1A A3
 C4 6B
 1F F1
 55 AC
 C3 E2
 32 28
 FF FF
```