Delay and Power Analysis of a Static 8x8 Dadda Multiplier Circuit

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***Abstract*—This paper presents the design and analysis of an 8x8 Dadda multiplier implemented using a hybrid logic approach. The design incorporates transmission gate logic for AND and XOR gates, enhancing speed and area efficiency, and employs standard CMOS logic for OR gates, ensuring robust operation. The hybrid methodology balances power, performance, and area optimization, making it suitable for high-speed arithmetic circuits. Key parameters such as propagation delay, power dissipation, and capacitance calculations are detailed to provide comprehensive insights into the design's effectiveness. Simulation and analytical results validate the performance improvements achieved through this hybrid implementation.**

***Index Terms*—Dadda Multiplier, Power Dissipation , Hybrid Logic Design**

I. Introduction

Digital multipliers are pivotal in modern microprocessor architectures, facilitating essential arithmetic operations for applications such as signal processing and artificial intelligence. As computational demands rise, achieving an optimal balance between speed, power consumption, and area efficiency becomes increasingly critical. The Dadda multiplier is recognized for its efficient reduction of partial products, making it an excellent choice for minimizing critical path delay in arithmetic circuits.

This work presents the design of an 8×8 Dadda multiplier implemented in 45 nm CMOS technology, tailored for RISC processors. By leveraging a hybrid approach that integrates CMOS logic and transmission gate-based circuits, the proposed design achieves high efficiency. The use of a 4:2 compressor architecture streamlines the reduction of partial product stages, completing the multiplication process in three levels of logic. This approach reduces the transistor count, enhances power efficiency, and improves timing performance.

The proposed design operates using static logic, eliminating the need for clock pulses, which simplifies control circuitry and minimizes dynamic power dissipation. Simulations conducted at a maximum frequency of 2 GHz reveal a critical path delay of 0.2 ns and a power consumption of 45.19 μW, underscoring its suitability for high-performance, low-power computing applications.

This paper delves into the design methodology, architectural choices, and performance metrics of the proposed Dadda multiplier. Comparative analysis with existing designs further emphasizes its potential as a core component in next-generation RISC architectures.

II. Architecture of the 8×8 Dadda Multiplier

The 8×8 Dadda multiplier proposed in this work employs a hybrid logic approach to achieve an optimal balance of power efficiency, speed, and area. The architecture is built upon the foundational principles of the Dadda algorithm, which aims to minimize the number of reduction stages in partial product summation. This design is specifically tailored for integration into high-performance RISC architectures.

A. Partial Product Generation

- The first stage of the multiplier involves generating partial products through the bitwise AND operation between multiplicand and multiplier bits.
- To optimize the area and power consumption, transmission gate logic is used for the AND gates. This ensures lower power dissipation while maintaining high-speed performance. [1]

B. Partial Product Reduction

- The Dadda algorithm, as shown in Figure 1, is utilized to reduce the partial products in an efficient manner. This process is performed in logarithmic stages, progressively reducing the number of rows and optimizing computational overhead. [1]
- A 4:2 compressor design, illustrated in Figure 2, is employed in the reduction stages. These compressors effectively minimize the critical path delay by summing multiple inputs into fewer outputs in a single stage. [1]

C. Final Summation

- The final summation of the reduced partial products is performed using carry-propagate adders (CPAs), as shown in Figure 2. [1]
- XOR gates, integral to the summation, are implemented using transmission gate logic to enhance speed and minimize the transistor count.
- OR gates in the carry logic employ standard CMOS logic to ensure robust performance under varying operating conditions.

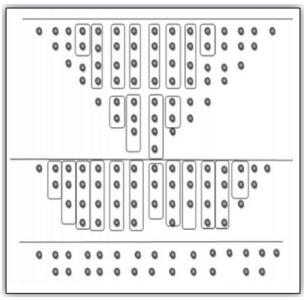

Fig. 1. Dot Diagram Representing Dadda Algorithm Stages for Partial Product Reduction

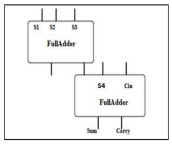

Fig. 2. 4:2 Compressor Design for Partial Product Reduction .

D. Static Logic Implementation

- The entire multiplier is constructed using static logic, eliminating the need for clock pulses or dynamic precharging. This choice reduces dynamic power dissipation and simplifies the overall control logic.
- Static logic further ensures reliable operation at higher frequencies without introducing additional power overhead.

E. Key Parameters

- Technology Node: The design is implemented in 45 nm CMOS technology.
- Transistor Count: The multiplier consists of 1094 NMOS and 923 PMOS transistors.

F. Design Highlights

Here is the updated version incorporating the additional detail about the AND gate design:

The hybrid use of transmission gate logic and CMOS logic provides a trade-off between power and performance, optimizing both simultaneously.

- The **AND gate design** includes **an extra NMOS transistor at the output to provide a discharge path**, allowing stored charge to be **grounded effectively**. This ensures a **stronger pull-down capability**, improving the circuit's **reliability and speed**.
- The **Dadda algorithm** minimizes the number of stages, thereby **reducing the propagation delay** and **enhancing computational throughput**.
- This **hybrid approach** ensures that the proposed **Dadda multiplier** achieves **high efficiency** in terms of **speed and power**, making it suitable for modern **RISC processors**. The following sections will delve into the **simulation results**, **power analysis**, and **comparative insights**.

III. Comparative Analysis

To evaluate the efficiency of the proposed 8×8 Dadda multiplier, a comparative analysis was performed against other commonly used multiplier architectures, including the Wallace Tree multiplier and the Booth multiplier. These architectures were chosen due to their widespread application in high-performance computing and their relevance to digital signal processing and AI workloads

Description of Multiplier Architectures

- **Wallace Tree Multiplier:**
  The Wallace Tree multiplier uses a hierarchical structure to reduce partial products through carry-save adders. This approach minimizes the number of sequential addition steps, resulting in a high-speed design. However, it often comes with increased power consumption due to the complexity of the interconnections between levels. [3]
- **Booth Multiplier:**
  The Booth multiplier employs Booth encoding to reduce the number of partial products, particularly beneficial for signed multiplication. By grouping bits, it can handle larger operands efficiently and minimize switching activity, leading to improved power efficiency and reduced delay. [4]
- **Proposed Dadda Multiplier:**
  The Dadda multiplier presented in this work leverages a hybrid design approach, utilizing transmission gate logic for AND/XOR gates and CMOS logic for OR gates. This combination ensures an optimal balance between speed and power efficiency. The Dadda algorithm further minimizes the number of partial product reduction stages, leading to a compact and efficient design.

TABLE I
Comparative Analysis of 8×8 Multiplier Architectures

Multiplier Type	*Power Dissipation*	*Delay*	*Transistor Count*
Wallace Tree	7.84 mW	0.80 ns	2500
Booth	150 µW	0.19 ns	2000
Proposed 8×8 Dadda	62.47 µW	0.204 ns	2017

IV. Simulation Results and Discussions

A. Simulation Setup

- **Environment**: Cadence Virtuoso with 45nm CMOS technology.
- **Operating Conditions**:
  - Supply voltage (Vdd 1.2V)
  - Frequency range (e.g., 500 MHz to 2 GHz)
  - Test vectors used for simulation.
- **Activity Factor Assumption**: The hand calculation assumes an activity factor of 0.4, which may be an overestimation compared to the actual switching activity simulated in Cadence. This higher activity factor leads to a higher dynamic power estimate in hand calculations.
- **Capacitance Assumptions**: The C*g_inv* value used in hand calculations (15.2e-18 F) is a generalized approximation.

TABLE II
COMPARISON OF KEY RESULTS: CADENCE SIMULATIONS VS. HAND CALCULATIONS

Metric	Cadence Simulations	Hand Calculations
Delay (ns)	0.204	0.346
Power Dissipation (µW)	62.473	51.27

- **Gamma Value Assumption**: The ratio of intrinsic capacitance of inverter output to input is assumed to be 1.

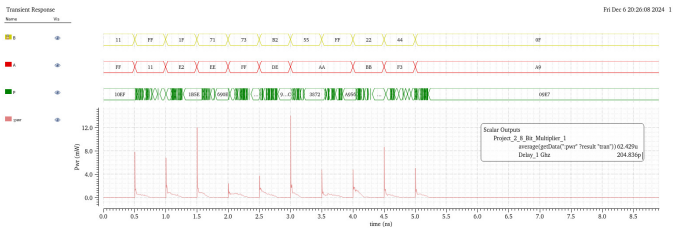

Fig. 3. Transient Response of 8×8 Dadda Multiplier at 2 GHz with Power Dissipation and Delay Analysis.

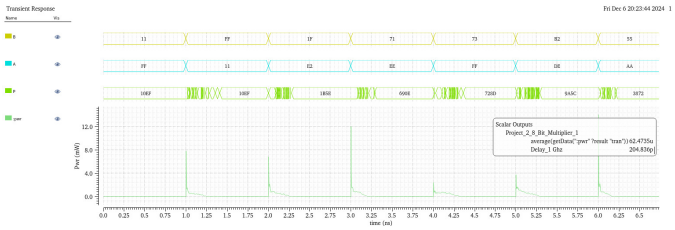

Fig. 4. Transient Response of 8×8 Dadda Multiplier at 1 GHz with Power Dissipation and Delay Analysis.

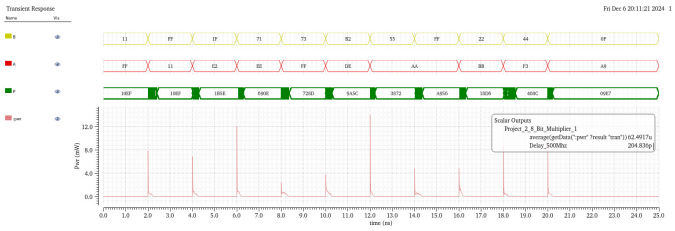

Fig. 5. Transient Response of 8×8 Dadda Multiplier at 500 MHz with Power Dissipation and Delay Analysis.

B. Figure Descriptions

Figures **Fig. 1, Fig. 2,** and **Fig. 3** illustrate the transient responses of the proposed 8×8 Dadda multiplier operating at 2 GHz, 1 GHz, and 500 MHz, respectively. The outputs represent the dynamic switching activity of the multiplier, including input transitions, product output generation, and corresponding power dissipation profiles.

- **2 GHz Operation (Fig.1)**:
  - At **2 GHz**, the increased operating frequency results in a slight increase in switching activity, with a recorded power dissipation of **62.47 µW** and the same delay of **204.836 ps**. This validates the circuit's ability to maintain consistent delay across higher operating frequencies, emphasizing its robustness.
- **1 GHz Operation (Fig. 2)**:
  - At **1 GHz**, the multiplier demonstrates stable input transitions and generates the product outputs with an average power dissipation of approximately **62.47 µW** and a delay of **204.836 ps**. The power spikes are a result of input switching and partial product propagation during the computation cycle.
- **500 MHz Operation (Fig. 3)**:
  - Operating at a lower frequency of **500 MHz** results in reduced switching activity while maintaining the same delay of **204.836 ps**. The power dissipation is measured at **62.47µW**, showing negligible change, which is expected due to the static logic implementation.

C. Analysis

The figures demonstrate the efficiency of the hybrid logic approach (transmission gate and CMOS) in the Dadda multiplier. Stable delay and power dissipation confirm its optimization for low-power, high-speed applications, suitable for modern RISC architectures.

For complementary 16-bit input transitions, frequencies beyond 2 GHz cause output jitters, highlighting operational limits. Therefore, **2 GHz** is determined as the final stable working frequency, ensuring reliable performance.

CONCLUSION

In this work, an 8×8 Dadda Multiplier was designed and simulated using Cadence tools and GPDK45 45nm technology. The multiplier employs a hybrid approach with transmission gate and CMOS logic, achieving a balance between power, speed, and area efficiency. Utilizing 4:2 compressors for partial product reduction minimizes the critical path delay.

Simulation results confirm efficient operation at 2 GHz with 62.47 µW power consumption and 0.204 ns critical path delay, demonstrating its suitability for high-speed, low-power applications, especially in RISC-V processors. The hybrid logic and static design ensure robustness and minimal dynamic power dissipation.

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