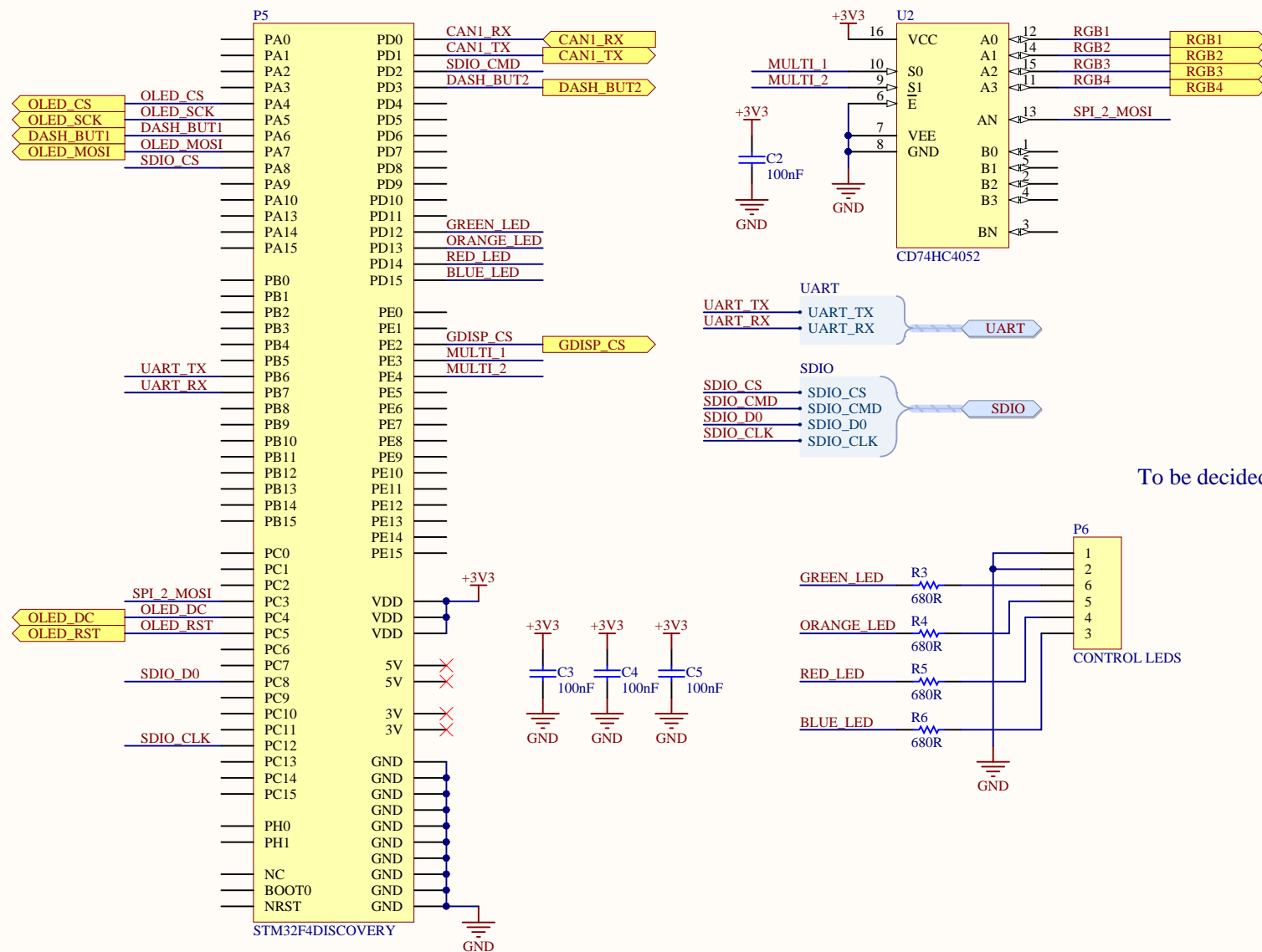


Mode (RS pin):
VCC - low power mode
GND - high speed mode
GND via 10k..100k - clope control mode



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Project name:		DataLogger.PrjPcb	
Document name:		CAN_Module.SchDoc	
Designer Name:	Wojciech Grędel	Date/Time:	2016-07-11 23:03:58
Revision:		1	



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Project name: DataLogger.PrjPcb

Document name: Discovery.SchDoc

Designer Name: Wojciech Grędel

Date/Time: 2016-07-11 23:03:58

Revision: 1

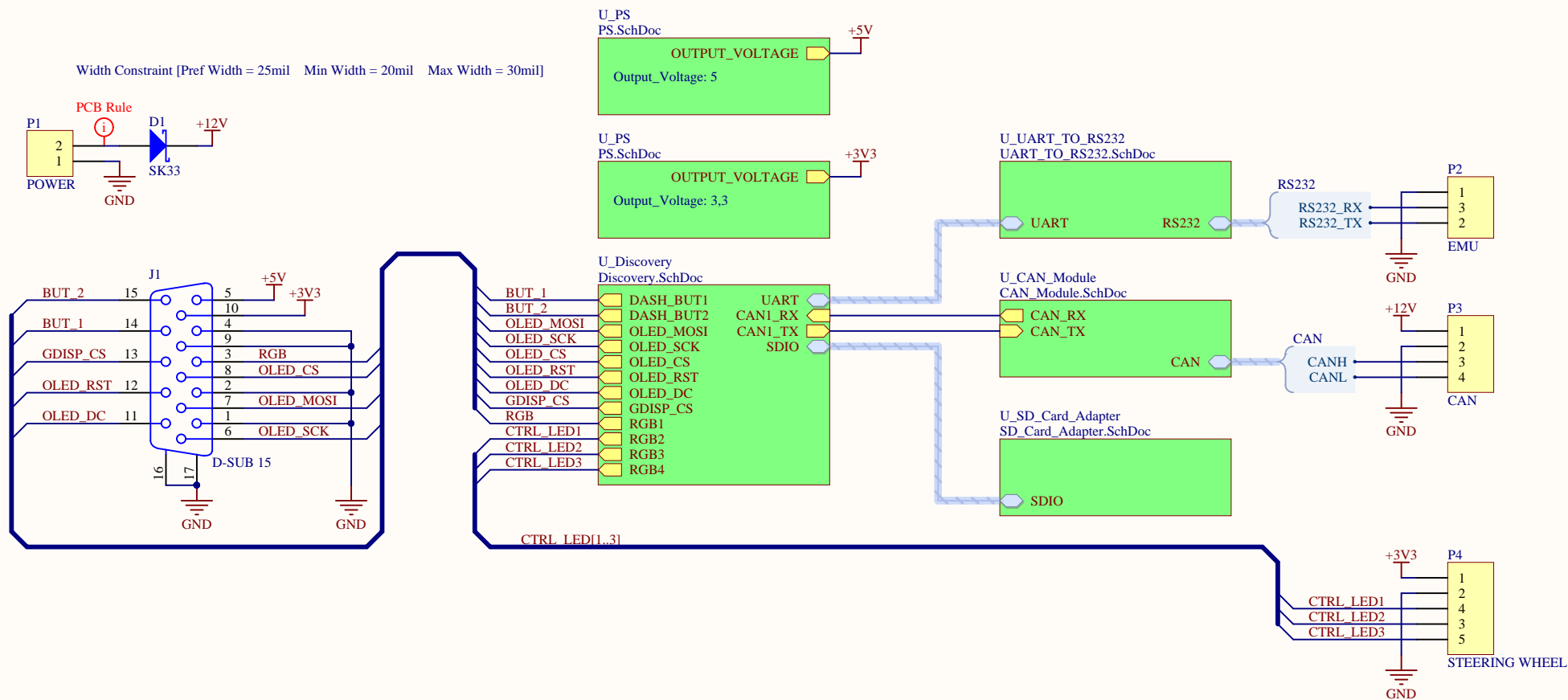
1

2

3

4

Width Constraint [Pref Width = 25mil Min Width = 20mil Max Width = 30mil]



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Project name: DataLogger.PrjPcb

Document name: Main.SchDoc

Designer Name: Wojciech Gredel

Date/Time: 2016-07-11 23:03:58

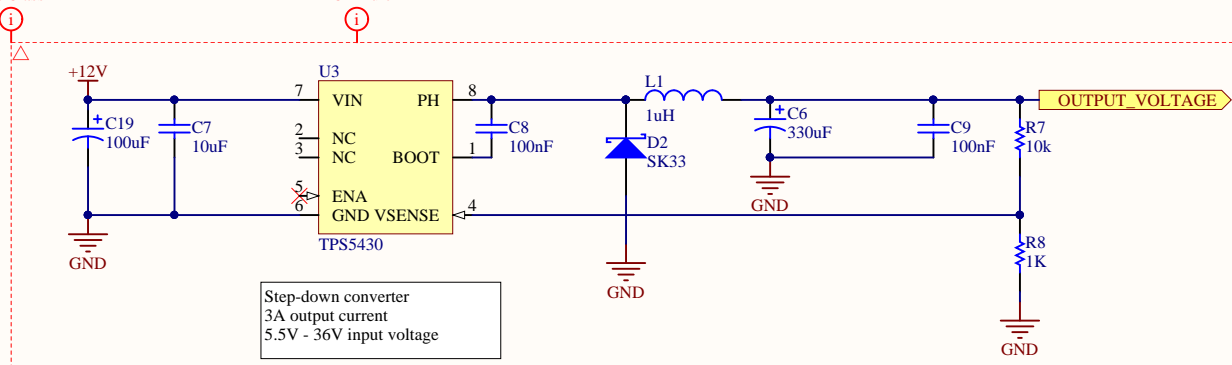
Revision: 1

ClassName: PowerNets

Width Constraint [Pref Width = 25mil Min Width = 20mil Max Width = 30mil]

Net Class

PCB Rule



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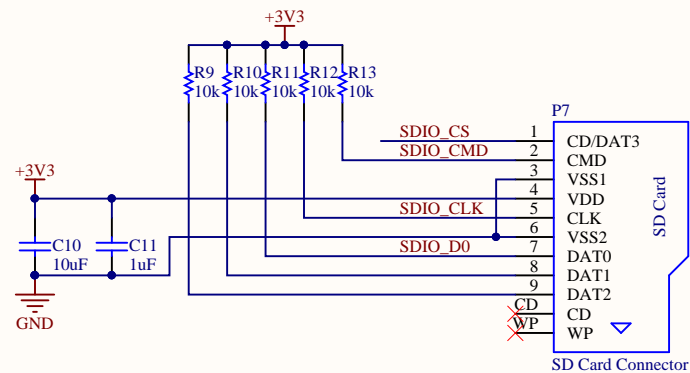
Project name: DataLogger.PrjPcb

Document name: PS.SchDoc

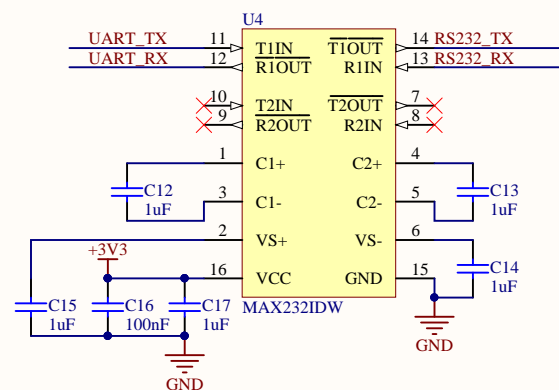
Designer Name: Wojciech Grędel

Date/Time: 2016-07-11 23:03:58

Revision: 1



Title		
Size	Number	Revision
A4		
Date:	2016-07-11	Sheet of
File:	C:\Users\...\SD_Card_Adapter.SchDoc	Drawn By:



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Project name:		DataLogger.PrjPcb	
Document name:		UART_TO_RS232.SchDoc	
Designer Name:		Wojciech Grędel	Date/Time: 2016-07-11 23:03:58
Revision:		1	

