EE 230 Experiment - 2

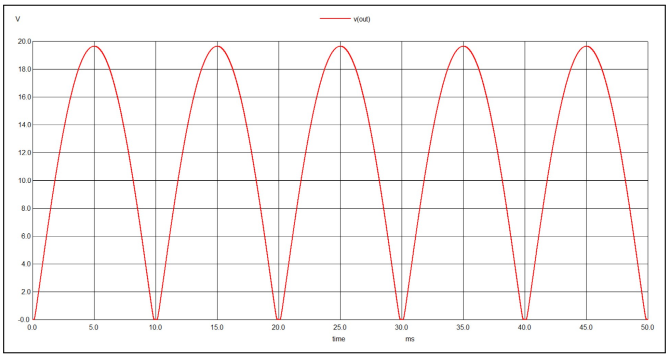
DC Power Supply

6th August, 2021

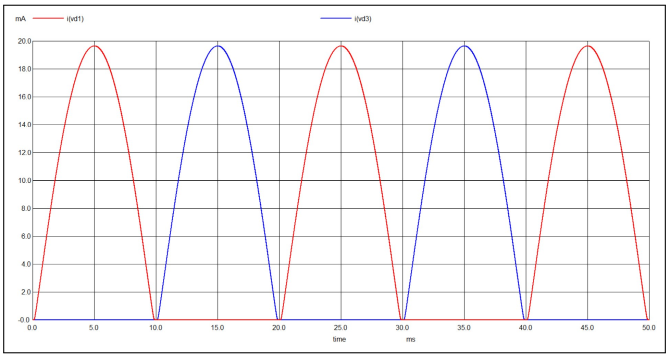
Vinamra Baghel 190010070

1 Unregulated DC Power Supply (using Bridge Rectifier)

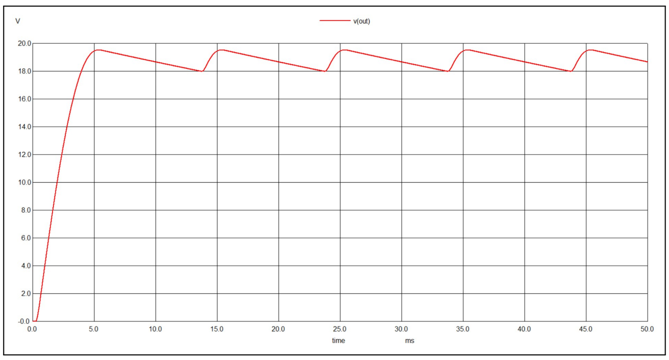
```
Vinamra Baghel 190010070 Unregulated supply with Bridge Rectifier
.MODEL 1N4007 D IS=6.2229E-9 N=1.9224 RS=0.33636 IKF=42.843E-3 CJO=764.38E-15 + M
    =0.1001 VJ=0.99900 BV=1000 IBV=1 TT=2.8854E-9
*Netlist
d1 in1 dum1 1N4007
d2 gnd in1 1N4007
d3 in2 dum3 1N4007
d4 gnd in2 1N4007
r out gnd 1k
c out gnd 100u
vd1 dum1 out dc 0
vd3 dum3 out dc 0
vin in1 in2 sin(0 21.2132 50 0 0)
*Analysis
.tran 1u 50m
.control
run
plot v(out)
plot i(vd1) i(vd3)
.endc
.end
```



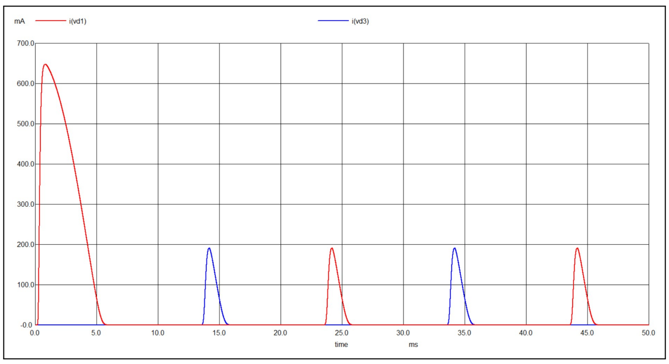
(a) V_{out}



(b) Diode currents



(c) V_{out} with **C**



(d) Diode currents with **C**

Learnings:

A large capacitance decreases ripple but increases response time and so too large a capacitance may cause the initial increase in voltage to not correctly happen.

2 DC Power Supply with Zener Diode Regulator

```
Vinamra Baghel 190010070 DC Power Supply with Zener Diode Regulator
.SUBCKT ZENER_12 1 2
D1 1 2 DF
DZ 3 1 DR
VZ 2 3 10.8
.MODEL DF D (IS=27.5p RS=0.620 N=1.10 CJO=78.3p VJ=1.00 M=0.330 TT=50.1n)
.MODEL DR D (IS=5.49f RS=50 N=1.77)
.ENDS
*Netlist
rs in 1 470
X gnd 2 ZENER_12
rl out 3 1k
vs 1 out dc 0
vz out 2 dc 0
vl 3 gnd dc 0
vin in gnd dc 20
*Analysis
.op
.control
run
print v(out) i(vs) i(vz) i(vl)
.endc
.end
```

a Values of Vout and currents for following

For $V_{in} = 20V$, $R_S = 470\Omega$, $R_L = 1k\Omega$,
$V_{out} = 12.26V$, $I_S = 16.46mA$, $I_Z = 4.20mA$, $I_L = 12.26mA$.

b Values of Vout and currents for following

For $V_{in} = 20V$, $R_S = 470\Omega$, $R_L = 500\Omega$,
$V_{out} = 12.86V$, $I_S = 15.17mA$, $I_Z = 15.14mA$, $I_L = 0.03mA$.

Learnings:

There is a minimum value of the load resistance, R_L because of Zener activation.

3 DC Power Supply with a BJT Series Regulator

```
Vinamra Baghel 190010070 DC Power Supply with BJT Series Regulator
.model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3 BR=9.5 VAF=80 IKR=12m
    ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40 tr=0.3u tf=0.5n cje=12p vje=0.48 mje
    =0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f
.model SL100 NPN IS=100f BF=80 ISE=10.3f IKF=50m NE=1.3 BR=9.5 VAF=80 IKR=12m ISC
    =47p NC=2 VAR=10 RB=100 RE=1 RC=10 tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5
    cjc=6p vjc=0.7 mjc=0.33 kf=2f
.SUBCKT ZENER_12 1 2
D1 1 2 DF
DZ 3 1 DR
VZ 2 3 10.8
.MODEL DF D (IS=27.5p RS=0.620 N=1.10 CJO=78.3p VJ=1.00 M=0.330 TT=50.1n)
.MODEL DR D (IS=5.49f RS=50 N=1.77)
.ENDS
*Netlist
Q1 in 1 out SL100
Q2 1 2 3 bc547a
X gnd 3 ZENER_12
rc in 1 1k
r1 out 2 12.5k
r2 2 gnd 12.5k
rl out gnd 1k
vin in gnd dc 20
*Analysis
.op
.control
run
print all
.endc
.end
```

For $V_{in} = 20V$, $R_1 = R_2 = 12.5k\Omega$, $R_L = 1k\Omega$,
$V_{out} = 18.89V$, $V_{pot} = 9.44V$, $V_{Q1-base} = 19.63V$, $V_{Q2-emitter} = 9.24V$.

Learnings:

This is the best regulator given its flexibility and performance.

Files associated: https://github.com/VNMR-35/EE-230-Lab