

# EE 230 Experiment - 3

## BJT Voltage Amplifiers (CE and CC)

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190010070

## 1 Common-Emitter Amplifier

### 1.1 Biasing Circuit

```
1 Vinamra Baghel 190010070 Common-Emitter Amplifier: Biasing Circuit
2 .model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3 BR=9.5 VAF=80 IKR=12m
   ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40 tr=0.3u tf=0.5n cje=12p vje=0.48 mje
   =0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f
3 *Netlist
4 r1 cc db 10k
5 r2 db gnd 2.2k
6 rc cc dc 1.2k
7 re e gnd 1k
8 Q c b e bc547a
9 vb db b 0
10 vc dc c 0
11 Vcc cc gnd 12
12 *Analysis
13 .op
14 .control
15 run
16 print i(vb) i(vc) v(b) v(c) v(e)
17 .endc
18 .end
```

### Analysis

The first step is to apply **Thevenin's Theorem** to the base node of the transistor and ground. We can find the Thevenin equivalent of the voltage and resistors R1 and R2 as follows:

$$V_{Th} = \frac{V_{cc} \cdot R_2}{R_1 + R_2} = 2.164V, \text{ and } R_{Th} = \frac{R_1 \cdot R_2}{R_1 + R_2} = 1.803k\Omega$$

We then take the base and emitter branches and apply KVL to find  $i_b = 7.22 \mu A$  as follows:

$$V_{Th} - i_b \cdot R_{Th} - V_{be} - (\beta + 1) \cdot i_b \cdot R_E = 0$$

We finally find the other values:  $i_c = \beta \cdot i_b = 1.444 \text{ mA}$ ,  $V_e = (\beta + 1) \cdot i_b \cdot R_E = 1.45 \text{ V}$ ,  $V_b = V_e + 0.7 = 2.15 \text{ V}$ , and  $V_c = V_{cc} - i_c \cdot R_C = 10.26 \text{ V}$ .

### Simulation

$i_b = 11.25 \mu A$   
 $i_c = 1.463 \text{ mA}$   
 $V_b = 2.14 \text{ V}$   
 $V_c = 10.24 \text{ V}$   
 $V_e = 1.47 \text{ V}$

### Learnings:

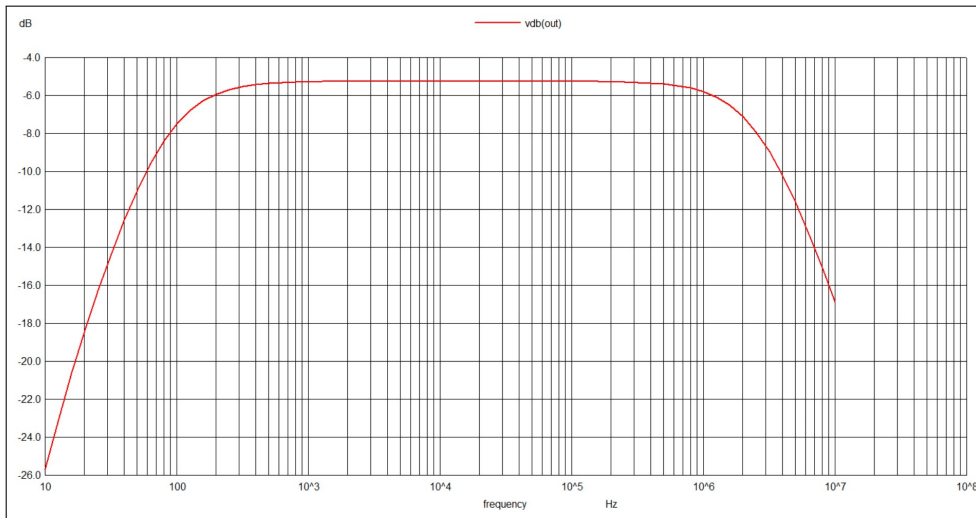
Biasing circuit DC analysis is important to know the operating voltage and transistor conditions.

## 1.2 Common-Emitter Amplifier (with bypass Capacitor CE): Midband Voltage Gain

```

1 Vinamra Baghel 190010070 Common-Emitter Amplifier: Midband Voltage Gain
2 .model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3 BR=9.5 VAF=80 IKR=12m
   ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40 tr=0.3u tf=0.5n cje=12p vje=0.48 mje
   =0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f
3 *Netlist
4 r1 cc b 10k
5 r2 b gnd 2.2k
6 rc cc c 1.2k
7 re e gnd 1k
8 rs in in2 0
9 rl out gnd 100k
10 ce e gnd 100u
11 c1 in2 b 10u
12 c2 c out 10u
13 Q c b e bc547a
14 Vcc cc gnd 12
15 Vin in gnd dc 0 ac 10m
16 *Analysis
17 .ac dec 10 10 10Meg
18 .control
19 run
20 print v(out)*100
21 plot vdb(out)
22 .endc
23 .end

```



(a) Decibel plot of  $V_{out}$  vs frequency

0	1.000000e+01	2.151897e+00	-4.72095e+00
1	1.258925e+01	2.179284e+00	-6.67629e+00
2	1.584893e+01	1.840397e+00	-9.10569e+00
3	1.995262e+01	9.22154e-01	-1.19977e+01
4	2.511886e+01	-5.73120e-01	-1.53036e+01
5	3.162278e+01	-3.03608e+00	-1.89020e+01
6	3.981072e+01	-6.61294e-01	-2.25482e+01
7	5.011872e+01	-1.14225e+01	-2.58411e+01
8	6.309573e+01	-1.73695e+01	-2.82644e+01
9	7.943282e+01	-2.40545e+01	-2.93570e+01
10	1.000000e+02	-3.08288e+01	-2.88371e+01
11	1.258925e+02	-3.70165e+01	-2.69100e+01
12	1.584893e+02	-4.21578e+01	-2.40275e+01
13	1.995262e+02	-4.61037e+01	-2.06976e+01
14	2.511886e+02	-4.89523e+01	-1.73639e+01
15	3.162278e+02	-5.09191e+01	-1.42975e+01
16	3.981072e+02	-5.22355e+01	-1.16236e+01
17	5.011872e+02	-5.30895e+01	-9.36945e+00
18	6.309573e+02	-5.36566e+01	-7.50997e+00
19	7.943282e+02	-5.40142e+01	-5.99614e+00
20	1.000000e+03	-5.42421e+01	-4.77398e+00
21	1.258925e+03	-5.43868e+01	-3.79203e+00
22	1.584893e+03	-5.44785e+01	-3.00494e+00
23	1.995262e+03	-5.45365e+01	-2.37430e+00
24	2.511886e+03	-5.45731e+01	-1.86830e+00
25	3.162278e+03	-5.45967e+01	-1.46070e+00
26	3.981072e+03	-5.46108e+01	-1.13085e+00
27	5.011872e+03	-5.46195e+01	-8.60785e-01
28	6.309573e+03	-5.46256e+01	-6.36451e-01
29	7.943282e+03	-5.46291e+01	-4.45955e-01
30	1.000000e+04	-5.46312e+01	-2.79178e-01
31	1.258925e+04	-5.46322e+01	-1.27256e-01
32	1.584893e+04	-5.46324e+01	1.76091e-01
33	1.995262e+04	-5.46319e+01	1.63995e-01
34	2.511886e+04	-5.46305e+01	3.188227e-01
35	3.162278e+04	-5.46280e+01	4.906100e-01
36	3.981072e+04	-5.46238e+01	6.88480e-01
37	5.011872e+04	-5.46170e+01	9.229500e-01
38	6.309573e+04	-5.46061e+01	1.206412e+00
39	7.943282e+04	-5.45887e+01	1.553814e+00
40	1.000000e+05	-5.45612e+01	1.983355e+00
41	1.258925e+05	-5.45177e+01	2.517307e+00
42	1.584893e+05	-5.44488e+01	3.182904e+00
43	1.995262e+05	-5.43400e+01	4.013214e+00
44	2.511886e+05	-5.41684e+01	5.047748e+00
45	3.162278e+05	-5.38986e+01	6.332339e+00
46	3.981072e+05	-5.34765e+01	7.917314e+00
47	5.011872e+05	-5.28205e+01	9.852224e+00
48	6.309573e+05	-5.18129e+01	1.217421e+01
49	7.943282e+05	-5.05917e+01	1.488612e+01
50	1.000000e+06	-4.80519e+01	1.792107e+01
51	1.258925e+06	-4.48791e+01	2.109675e+01
52	1.584893e+06	-4.06163e+01	2.408010e+01
53	1.995262e+06	-3.52807e+01	2.640712e+01
54	2.511886e+06	-2.91641e+01	2.760375e+01

(b) Gain values

Midband Voltage Gain = **-54.6324**

### Learnings:

Common-Emitter Amplifiers have **high gain** but poor  $R_{in}$  and  $R_{out}$ . Common-Collector Amplifiers have gain only unity but good input and output resistances (high  $R_{in}$  and low  $R_{out}$ ). Using them together gives us optimum resistance and gain values.

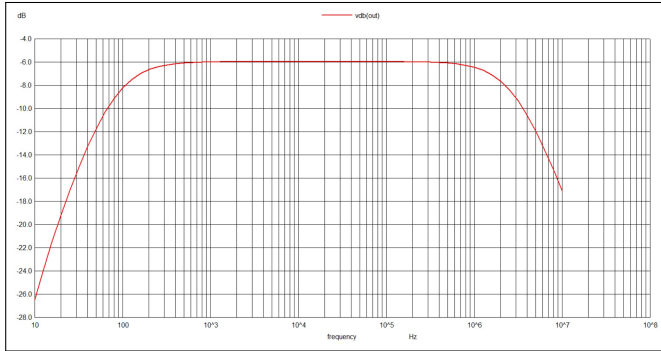
### 1.3 Common-Emitter Amplifier (with bypass Capacitor CE): Effect of $R_L$ on the Mid-band Gain

$$R_L = 12 \text{ k}\Omega$$

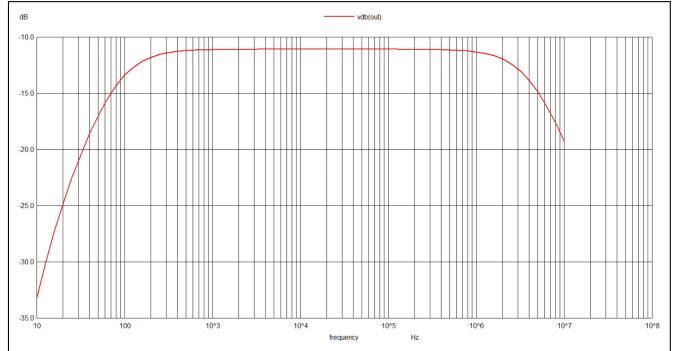
```
1 r1 out gnd 12k
```

$$R_L = 1.2 \text{ k}\Omega$$

```
1 r1 out gnd 1.2k
```



(a) Decibel plot of  $V_{out}$  vs frequency for  $R_L = 12 \text{ k}\Omega$   
**Gain = -50.3408**



(b) Decibel plot of  $V_{out}$  vs frequency for  $R_L = 1.2 \text{ k}\Omega$   
**Gain = -27.9142**

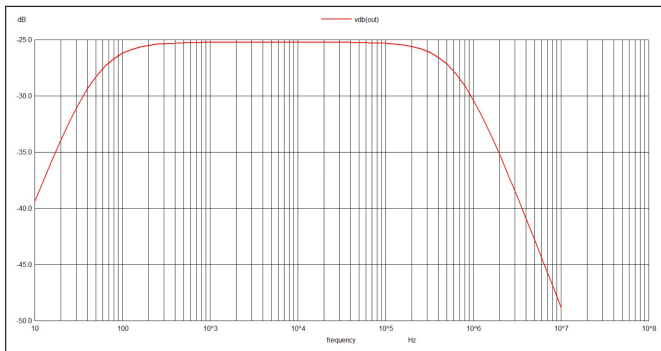
### 1.4 Common-Emitter Amplifier (with bypass Capacitor CE): Effect of $R_S$ on the Mid-band Gain

$$R_S = 10 \text{ k}\Omega$$

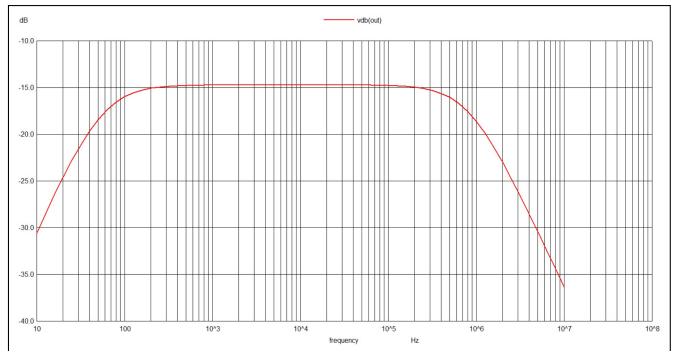
```
1 rs in in2 10k
```

$$R_S = 2.2 \text{ k}\Omega$$

```
1 rs in in2 2.2k
```



(a) Decibel plot of  $V_{out}$  vs frequency for  $R_S = 10 \text{ k}\Omega$   
**Gain = -5.47875**



(b) Decibel plot of  $V_{out}$  vs frequency for  $R_S = 2.2 \text{ k}\Omega$   
**Gain = -18.3715**

## 2 Two-stage Amplifier (CE and CC)

```
1 Vinamra Baghel 190010070 Two Stage Amplifier: Biasing Circuit
2 .model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3 BR=9.5 VAF=80 IKR=12m
   ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40 tr=0.3u tf=0.5n cje=12p vje=0.48 mje
   =0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f
3 *Netlist
4 rs in in2 0
5 r1 cc b1 10k
6 r2 b1 gnd 2.2k
7 rc cc c1 1.2k
8 re1 e1 gnd 1k
9 re2 de2 gnd 10k
10 rl out gnd 10k
11 cap1 in2 b1 10u
12 cape e1 gnd 100u
13 cap2 e2 out 10u
14 Q1 c1 b1 e1 bc547a
15 Q2 cc b2 e2 bc547a
16 vb2 c1 b2 0
17 ve2 e2 de2 0
18 Vcc cc gnd 12
19 Vin in gnd dc 0 ac 10m
20 *Analysis
21 .ac dec 10 10 10Meg
22 .control
23 run
24 print v(out)*100
25 plot vdb(out)
26 .endc
27 .end
```

### 2.1 Biasing Circuit - Simulation

$$i_{b2} = 8.075 \mu\text{A}$$

$$i_{e2} = 957.609 \mu\text{A}$$

### 2.2 Midband Gain

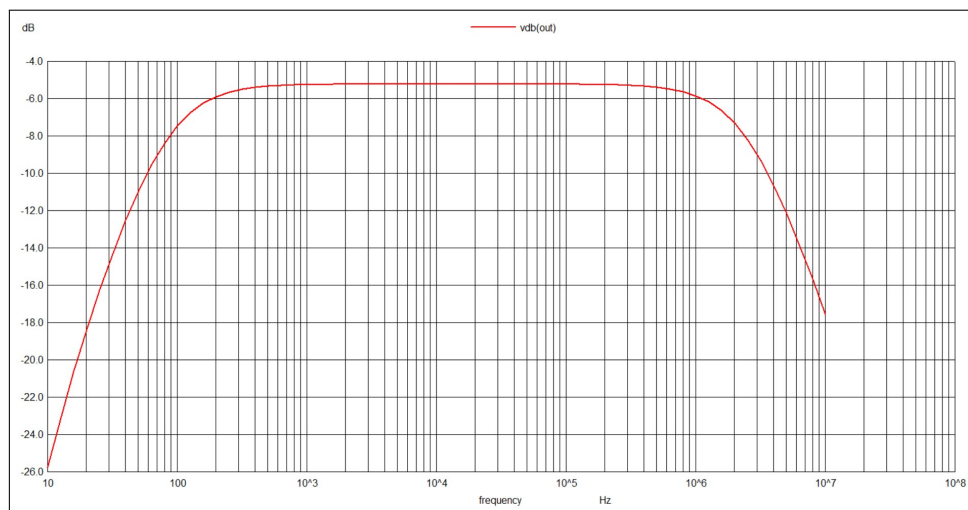


Figure 4: Decibel plot of  $V_{out}$  vs frequency

Gain = -54.8072

Files associated: <https://github.com/VNMR-35/EE-230-Lab>