

CHAPTER 8

Building Blocks of Integrated-Circuit Amplifiers

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IN THIS CHAPTER YOU WILL LEARN

1. The basic integrated-circuit (IC) design philosophy and how it differs from that for discrete-circuit design.
2. How current sources are used to bias IC amplifiers and how the use of current mirrors allows the replication of the reference current generated in one location at various other locations on the IC chip.
3. The basic gain cells of IC amplifiers, namely, the CS and CE amplifiers with current-source loads.
4. How the CG and CB amplifiers act as current buffers.
5. How to increase the gain realized in the basic gain cells by employing the principle of cascoding.
6. Analysis and design of the cascode amplifier and the cascode current source in both their MOS and bipolar forms.
7. Some ingenious analog circuit-design techniques that result in current mirrors with vastly improved characteristics.
8. How to pair transistors to realize amplifiers with characteristics superior to those obtained from a single-transistor stage.

Introduction

Having studied the two major transistor types, the MOSFET and the BJT, and their basic discrete-circuit amplifier configurations, we are now ready to begin the study of integrated-circuit (IC) amplifiers. This chapter is devoted to the design of the basic building blocks of IC amplifiers.

We begin with a brief section on the design philosophy of integrated circuits and how it differs from that of discrete circuits. This is followed by the study of IC biasing in Section 8.2, highlighting the design of current sources and current mirrors. The current mirror is one of the most important building blocks of analog integrated circuits. More advanced mirror circuits are presented in Section 8.6.

The heart of this chapter is the material in Sections 8.3 to 8.5. In Section 8.3 we present the basic gain cell of IC amplifiers, namely, the current-source-loaded common-source (common-emitter) amplifier. Then, in determining how to increase its gain, we discover the

need for current buffers. The two amplifier configurations capable of implementing a current buffer, the common-gate and common-base amplifiers, are studied in Section 8.4. This study differs from that in Chapter 7 in that r_o of the transistor is included, as must always be the case in integrated circuits. The study of the CG and CB leads naturally and seamlessly to the principle of cascoding and its applications in amplifier design: namely, the cascode amplifier and the cascode current source, which are very important building blocks of IC amplifiers.

The chapter concludes with the presentation in Section 8.7 of an interesting and useful collection of amplifier configurations, each utilizing a pair of transistors. Throughout this chapter, MOS and bipolar circuits are presented side by side, which allows a certain economy in presentation and, more important, provides an opportunity to compare and contrast the two circuit types.

8.1 IC Design Philosophy

Integrated-circuit fabrication technology (Appendix A) imposes constraints on and provides opportunities to the circuit designer. To cope with the constraints and take advantage of the opportunities, IC designers have over the years invented (and continue to invent) many ingenious techniques, and a distinct philosophy has emerged for the design of integrated circuits. In the following we provide a brief summary of the important constraints and opportunities and the major features of the IC design philosophy.

- 1. Resistors.** To minimize the chip area, large and even moderate-size resistors are to be avoided. As well, economic considerations discourage the use of resistors of precise values. On the other hand, transistors can be made small and cheaply, and the designer is encouraged to use transistors in preference to resistors wherever possible. As a result, the classical biasing arrangement, popular in discrete-circuit amplifier design, is abandoned in IC amplifiers in favor of biasing with constant-current sources implemented with transistors operating in the active mode. As well, the collector and drain resistors in amplifiers are replaced with constant-current sources that have much higher incremental resistance, thus providing larger gains.
- 2. Capacitors.** Chip-area considerations also make it impossible to fabricate large-valued capacitors such as those employed for signal coupling and bypass in discrete-circuit amplifiers. As a result, IC amplifiers are all direct coupled and utilize clever techniques, which we will study in this chapter and the next.
- 3. Power Supplies.** To pack a large number of devices on the same IC chip, and thus reduce system cost and increase reliability, the trend has been to reduce the device dimensions. (For a discussion of Moore's law and device scaling, see Section 14.5.) By 2014, CMOS process technologies capable of producing devices with a 14-nm channel length were in use. To avoid breaking down the thin oxide layers (less than 1 nm) used in these devices, power supplies are limited to 1 V or so. Low power-supply voltages help with another major design challenge; namely, keeping the power dissipated in the chip within acceptable limits. However, the use of such low dc power-supply voltages presents the circuit designer with a host of challenges. For instance, MOS

transistors must be operated with overdrive voltages of only 0.1 V to 0.2 V. In our study of MOS amplifiers, we will frequently comment on such issues.

4. **Device Variety.** Unlike the designer of discrete circuits, who is limited to available off-the-shelf transistors, the IC designer has the freedom to specify the device dimensions and to utilize device matching and arrays of devices having dimensions with specified ratios. For instance, one can utilize an array of bipolar transistors whose emitter-base-junction areas have binary-weighted ratios. CMOS technology provides even more flexibility, with the W and L values of MOS transistors selected to fit a very wide range of design requirements.
5. **Bipolar Technology.** BJTs are still used in special analog applications, such as high-quality general-purpose op-amp packages that are intended for assembly on printed-circuit (PC) boards (as opposed to being part of a system-on-a-chip). Bipolar circuits can also be combined with CMOS circuits in innovative and exciting ways in what is known as BiCMOS technology.
6. **CMOS Technology.** Currently the vast majority of analog integrated circuits are designed using CMOS technology. This practice was initially motivated by the need to be compatible with digital circuits, which have become predominantly CMOS. Now, however, the richness and the versatility that CMOS provides the analog designer is an even stronger reason for its dominance. We hope that the reader will come to appreciate this point in Chapters 8 and 9.

SOLID CIRCUITS WITH “FLYING WIRES”:

As the importance of transistors grew during the 1950s, packaging became a problem. While it was possible to create smaller and smaller active devices, individual transistor packages had to be large enough to be held in the assembly of an electronic system. As one solution to this problem, Texas Instruments (TI) initiated a program of package modular electronics in the creation, on a ceramic substrate, of larger, more functional system elements. Employed to work in this direction, Jack Kilby believed it was necessary to go one step further and design the multiplicity of active and passive elements on a single piece of semiconductor. Thus, in 1958 he created the first “solid circuit,” incorporating many transistors and resistors formed on a single slab of germanium and coupled by “flying wire” interconnections to form system elements such as oscillators and amplifiers. In 1959 TI began to use this technique to manufacture the 507 Binary Flip-Flop. While the approach was successful in producing small space-efficient modules, it was not suited for mass production. In 2000 Kilby received the Nobel Prize in Physics, in recognition of his part in the invention of the integrated circuit.

8.2 IC Biasing—Current Sources, Current Mirrors, and Current-Steering Circuits

Biasing in integrated-circuit design is based on the use of constant-current sources. On an IC chip with a number of amplifier stages, a constant dc current (called a **reference current**) is generated at one location and is then replicated at various other locations for biasing the various amplifier stages through a process known as **current steering**. This approach has the advantage that the effort expended on generating a predictable and stable reference current,

usually utilizing a precision resistor external to the chip or a special circuit on the chip, need not be repeated for every amplifier stage. Furthermore, the bias currents of the various stages track each other in case of changes in power-supply voltage or in temperature.

In this section we study circuit building blocks and techniques employed in the bias design of IC amplifiers. These current-source circuits are also utilized as amplifier load elements, as will be seen in Sections 8.3 and 8.4.

8.2.1 The Basic MOSFET Current Source

Figure 8.1 shows the circuit of a simple MOS constant-current source. The heart of the circuit is transistor Q_1 , the drain of which is shorted to its gate,¹ thereby forcing it to operate in the saturation mode with

$$I_{D1} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_1 (V_{GS} - V_{in})^2 \quad (8.1)$$

where we have neglected channel-length modulation. The drain current of Q_1 is supplied by V_{DD} through resistor R , which in most cases would be outside the IC chip. Since the gate currents are zero,

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R} \quad (8.2)$$

where the current through R is considered to be the reference current of the current source and is denoted I_{REF} . Equations (8.1) and (8.2) can be used to determine the value required for R .

Now consider transistor Q_2 : It has the same V_{GS} as Q_1 ; thus, if we assume that it is operating in saturation, its drain current, which is the output current I_O of the current source, will be

$$I_O = I_{D2} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_2 (V_{GS} - V_{in})^2 \quad (8.3)$$

where we have neglected channel-length modulation. Equations (8.1) and (8.3) enable us to relate the output current I_O to the reference current I_{REF} as follows:

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \quad (8.4)$$

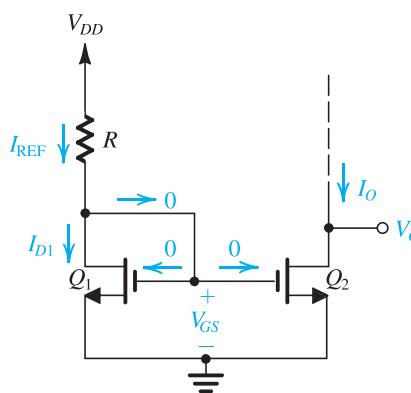


Figure 8.1 Circuit for a basic MOSFET constant-current source. For proper operation, the output terminal, that is, the drain of Q_2 , must be connected to a circuit that ensures that Q_2 operates in saturation.

¹Such a transistor is said to be *diode connected*.

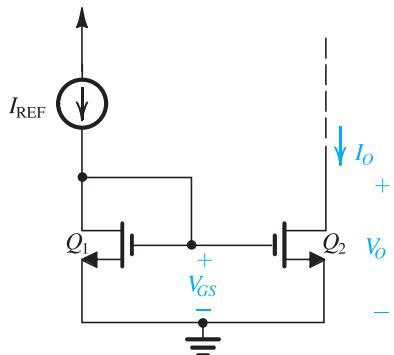


Figure 8.2 Basic MOSFET current mirror.

This is a simple and attractive relationship: The special connection of Q_1 and Q_2 provides an output current I_O that is related to the reference current I_{REF} by the aspect ratios of the transistors. In other words, the relationship between I_O and I_{REF} is solely determined by the geometries of the transistors. In the special case of identical transistors, $I_O = I_{\text{REF}}$, and the circuit simply replicates or mirrors the reference current in the output terminal. This has given the circuit composed of Q_1 and Q_2 the name **current mirror**, a name that is used irrespective of the ratio of device dimensions.

Figure 8.2 depicts the current-mirror circuit with the input reference current shown as being supplied by a current source for both simplicity and generality. The **current gain** or **current transfer ratio** of the current mirror is given by Eq. (8.4).

Effect of V_O on I_O In the description above for the operation of the current source of Fig. 8.1, we assumed Q_2 to be operating in saturation. This is essential if Q_2 is to supply a constant-current output. To ensure that Q_2 is saturated, the circuit to which the drain of Q_2 is to be connected must establish a drain voltage V_O that satisfies the relationship

$$V_O \geq V_{GS} - V_{tn} \quad (8.5)$$

or, equivalently, in terms of the overdrive voltage V_{OV} of Q_1 and Q_2 ,

$$V_O \geq V_{OV} \quad (8.6) \quad \leftarrow$$

In other words, the current source will operate properly with an output voltage V_O as low as V_{OV} , which is a few tenths of a volt.

Although thus far neglected, channel-length modulation can have a significant effect on the operation of the current source. Consider, for simplicity, the case of identical devices Q_1 and Q_2 . The drain current of Q_2 , I_O , will equal the current in Q_1 , I_{REF} , at the value of V_O that causes the two devices to have the same V_{DS} , that is, at $V_O = V_{GS}$. As V_O is increased above this value, I_O will increase according to the incremental output resistance r_{o2} of Q_2 . This is illustrated in Fig. 8.3, which shows I_O versus V_O . Observe that since Q_2 is operating at a constant V_{GS} (determined by passing I_{REF} through the matched device Q_1), the curve in Fig. 8.3 is simply the $i_D - v_{DS}$ characteristic curve of Q_2 for v_{GS} equal to the particular value V_{GS} .

In summary, the current source of Fig. 8.1 and the current mirror of Fig. 8.2 have a finite output resistance R_o ,

$$R_o \equiv \frac{\Delta V_O}{\Delta I_O} = r_{o2} = \frac{V_{A2}}{I_O} \quad (8.7)$$

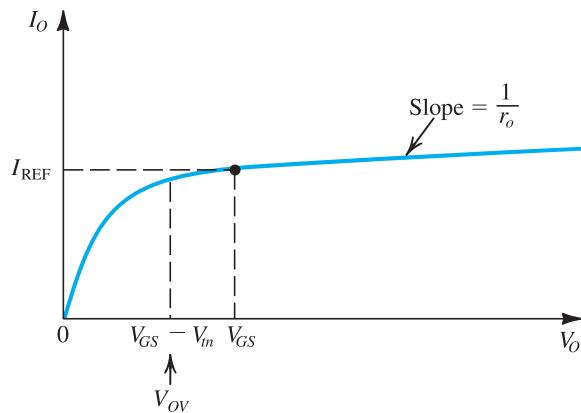


Figure 8.3 Output characteristic of the current source in Fig. 8.1 and the current mirror of Fig. 8.2 for the case of Q_2 matched to Q_1 .

where I_O is given by Eq. (8.3) and V_{A2} is the Early voltage of Q_2 . Also, recall that for a given process technology, V_A is proportional to the transistor channel length; thus, to obtain high output-resistance values, current sources are usually designed using transistors with relatively long channels. Finally, note that we can express the current I_O as

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{\text{REF}} \left(1 + \frac{V_O - V_{GS}}{V_{A2}} \right) \quad (8.8)$$

Example 8.1

Given $V_{DD} = 3$ V and using $I_{\text{REF}} = 100 \mu\text{A}$, design the circuit of Fig. 8.1 to obtain an output current whose nominal value is $100 \mu\text{A}$. Find R if Q_1 and Q_2 are matched and have channel lengths of $1 \mu\text{m}$, channel widths of $10 \mu\text{m}$, $V_t = 0.7$ V, and $k'_n = 200 \mu\text{A/V}^2$. What is the lowest possible value of V_O ? Assuming that for this process technology, the Early voltage $V'_A = 20 \text{ V}/\mu\text{m}$, find the output resistance of the current source. Also, find the change in output current resulting from a $+1\text{-V}$ change in V_O .

Solution

$$I_{D1} = I_{\text{REF}} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_1 V_{ov}^2$$

$$100 = \frac{1}{2} \times 200 \times 10 V_{ov}^2$$

Thus,

$$V_{ov} = 0.316 \text{ V}$$

and

$$\begin{aligned}V_{GS} &= V_t + V_{ov} = 0.7 + .316 \simeq 1 \text{ V} \\R &= \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{3 - 1}{0.1 \text{ mA}} = 20 \text{ k}\Omega \\V_{ov\min} &= V_{ov} \simeq 0.3 \text{ V}\end{aligned}$$

For the transistors used, $L = 1 \mu\text{m}$. Thus,

$$\begin{aligned}V_A &= 20 \times 1 = 20 \text{ V} \\r_{o2} &= \frac{20 \text{ V}}{100 \mu\text{A}} = 0.2 \text{ M}\Omega\end{aligned}$$

The output current will be $100 \mu\text{A}$ at $V_o = V_{GS} = 1 \text{ V}$. If V_o changes by $+1 \text{ V}$, the corresponding change in I_o will be

$$\Delta I_o = \frac{\Delta V_o}{r_{o2}} = \frac{1 \text{ V}}{0.2 \text{ M}\Omega} = 5 \mu\text{A}$$

EXERCISE

- D8.1** In the current source of Example 8.1, it is required to reduce the change in output current, ΔI_o , corresponding to a change in output voltage, ΔV_o , of 1 V to 1% of I_o . What should the dimensions of Q_1 and Q_2 be changed to? Assume that Q_1 and Q_2 are to remain matched.

Ans. $L = 5 \mu\text{m}$; $W = 50 \mu\text{m}$

8.2.2 MOS Current-Steering Circuits

As mentioned earlier, once a constant current has been generated, it can be replicated to provide dc bias or load currents for the various amplifier stages in an IC. Current mirrors can obviously be used to implement this current-steering function. Figure 8.4 shows a simple current-steering circuit. Here Q_1 together with R determine the reference current I_{REF} . Transistors Q_1 , Q_2 , and Q_3 form a two-output current mirror,

$$I_2 = I_{REF} \frac{(W/L)_2}{(W/L)_1} \quad (8.9)$$

$$I_3 = I_{REF} \frac{(W/L)_3}{(W/L)_1} \quad (8.10)$$

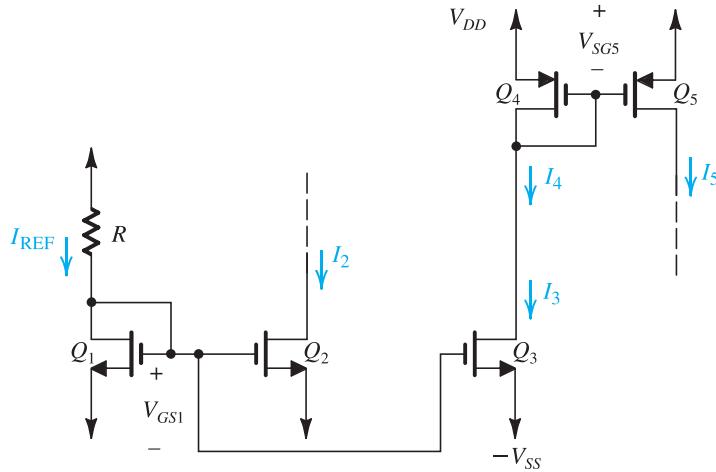


Figure 8.4 A current-steering circuit.

To ensure operation in the saturation region, the voltages at the drains of Q_2 and Q_3 are constrained as follows:

$$V_{D2}, V_{D3} \geq -V_{SS} + V_{GS1} - V_{tn} \quad (8.11)$$

or, equivalently,

$$V_{D2}, V_{D3} \geq -V_{SS} + V_{OV1} \quad (8.12)$$

where V_{OV1} is the overdrive voltage at which Q_1 , Q_2 , and Q_3 are operating. In other words, the drains of Q_2 and Q_3 will have to remain higher than $-V_{SS}$ by at least the overdrive voltage, which is usually a few tenths of a volt.

Continuing our discussion of the circuit in Fig. 8.4, we see that current I_3 is fed to the input side of a current mirror formed by PMOS transistors Q_4 and Q_5 . This mirror provides

$$I_5 = I_4 \frac{(W/L)_5}{(W/L)_4} \quad (8.13)$$

where $I_4 = I_3$. To keep Q_5 in saturation, its drain voltage should be

$$V_{D5} \leq V_{DD} - |V_{OV5}| \quad (8.14)$$

where V_{OV5} is the overdrive voltage at which Q_5 is operating.

The constant current I_2 generated in the circuit of Fig. 8.4 can be used to bias a source-follower amplifier such as that implemented by transistor Q_6 in Fig. 8.5(a). Similarly, the constant current I_5 can be used as the load for a common-source amplifier such as that implemented with transistor Q_7 in Fig. 8.5(b). We will discuss the use of current sources as load elements for CS amplifiers in Section 8.3.

Finally, an important point to note is that in the circuit of Fig. 8.4, while Q_2 *pulls* its current I_2 from a circuit (not shown in Fig. 8.4), Q_5 *pushes* its current I_5 into a circuit (not shown in Fig. 8.4). Thus Q_5 is appropriately called a **current source**, whereas Q_2 should more properly be called a **current sink**. In an IC, both current sources and current sinks are usually needed. The difference between a current source and a current sink is further illustrated in Fig. 8.6, where V_{CSmin} denotes the minimum voltage needed across the current source (or sink) for its proper operation.

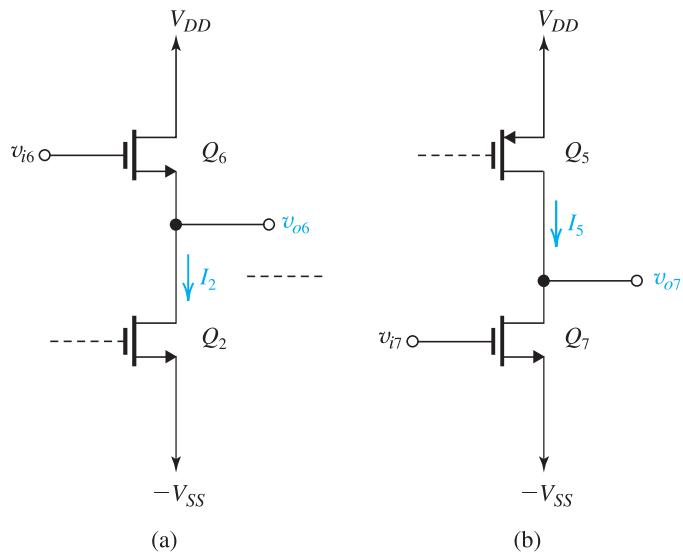


Figure 8.5 Application of the constant currents I_2 and I_5 generated in the current-steering circuit of Fig. 8.4. Constant-current I_2 is the bias current for the source follower Q_6 , and constant-current I_5 is the load current for the common-source amplifier Q_7 .

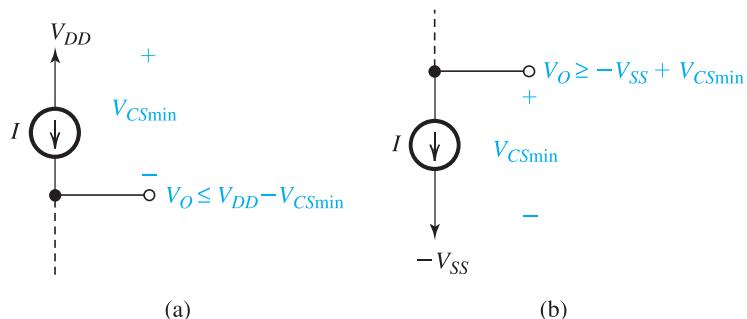


Figure 8.6 (a) A current source; and (b) a current sink.

EXERCISE

D8.2 For the circuit of Fig. 8.4, let $V_{DD} = V_{SS} = 1.5$ V, $V_{tn} = 0.6$ V, $V_{tp} = -0.6$ V, all channel lengths = 1 μm , $k'_n = 200 \mu\text{A/V}^2$, $k'_p = 80 \mu\text{A/V}^2$, and $\lambda = 0$. For $I_{\text{REF}} = 10 \mu\text{A}$, find the widths of all transistors to obtain $I_2 = 60 \mu\text{A}$, $I_3 = 20 \mu\text{A}$, and $I_5 = 80 \mu\text{A}$. It is further required that the voltage at the drain of Q_2 be allowed to go down to within 0.2 V of the negative supply and that the voltage at the drain of Q_5 be allowed to go up to within 0.2 V of the positive supply.

Ans. $W_1 = 2.5 \mu\text{m}$; $W_2 = 15 \mu\text{m}$; $W_3 = 5 \mu\text{m}$; $W_4 = 12.5 \mu\text{m}$; $W_5 = 50 \mu\text{m}$

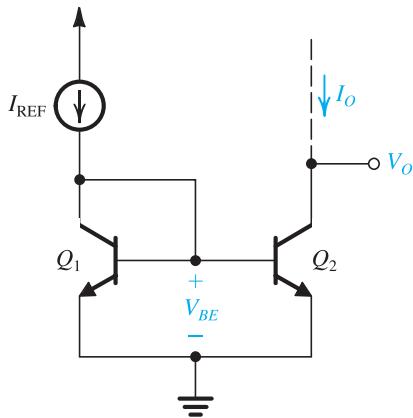


Figure 8.7 The basic BJT current mirror.

8.2.3 BJT Circuits

The basic BJT current mirror is shown in Fig. 8.7. It works in a fashion very similar to that of the MOS mirror. However, there are two important differences: First, the nonzero base current of the BJT (or, equivalently, the finite β) causes an error in the current transfer ratio of the bipolar mirror. Second, the current transfer ratio is determined by the relative areas of the emitter-base junctions of Q_1 and Q_2 .

Let us first consider the case of β sufficiently high that we can neglect the base currents. The reference current I_{REF} is passed through the diode-connected transistor Q_1 and thus establishes a corresponding voltage V_{BE} , which in turn is applied between base and emitter of Q_2 . Now, if Q_2 is matched to Q_1 or, more specifically, if the EBJ area of Q_2 is the same as that of Q_1 , and thus Q_2 has the same scale current I_s as Q_1 , then the collector current of Q_2 will be equal to that of Q_1 ; that is,

$$I_O = I_{\text{REF}} \quad (8.15)$$

For this to happen, however, Q_2 must be operating in the active mode, which in turn is achieved as long as the collector voltage V_O is 0.3 V or so higher than that of the emitter.

To obtain a current transfer ratio other than unity, say m , we simply arrange that the area of the EBJ of Q_2 is m times that of Q_1 . In this case,

$$I_O = mI_{\text{REF}} \quad (8.16)$$

In general, the current transfer ratio is given by

$$\frac{I_O}{I_{\text{REF}}} = \frac{I_{S2}}{I_{S1}} = \frac{\text{Area of EBJ of } Q_2}{\text{Area of EBJ of } Q_1} \quad (8.17)$$

Alternatively, if the area ratio m is an integer, one can think of Q_2 as equivalent to m transistors, each matched to Q_1 and connected in parallel.

Next we consider the effect of finite transistor β on the current transfer ratio. The analysis for the case in which the current transfer ratio is nominally unity—that is, for the case in which Q_2 is matched to Q_1 —is illustrated in Fig. 8.8. The key point here is that since Q_1 and Q_2 are matched and have the same V_{BE} , their collector currents will be equal. The rest of the analysis is straightforward. A node equation at the collector of Q_1 yields

$$I_{\text{REF}} = I_C + 2I_C/\beta = I_C \left(1 + \frac{2}{\beta} \right)$$

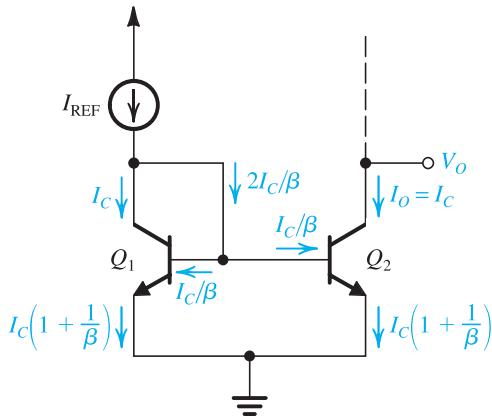


Figure 8.8 Analysis of the current mirror taking into account the finite β of the BJTs.

Finally, since $I_O = I_C$, the current transfer ratio can be found as

$$\frac{I_O}{I_{\text{REF}}} = \frac{I_C}{I_C \left(1 + \frac{2}{\beta}\right)} = \frac{1}{1 + \frac{2}{\beta}} \quad (8.18)$$

Note that as β approaches ∞ , I_O/I_{REF} approaches the nominal value of unity. For typical values of β , however, the error in the current transfer ratio can be significant. For instance, $\beta = 100$ results in a 2% error in the current transfer ratio. Furthermore, the error due to the finite β increases as the nominal current transfer ratio is increased. The reader is encouraged to show that for a mirror with a nominal current transfer ratio m —that is, one in which $I_{S2} = mI_{S1}$ —the actual current transfer ratio is given by

$$\frac{I_O}{I_{\text{REF}}} = \frac{m}{1 + \frac{m+1}{\beta}} \quad (8.19)$$

In common with the MOS current mirror, the BJT mirror has a finite output resistance R_o ,

$$R_o \equiv \frac{\Delta V_o}{\Delta I_o} = r_{o2} = \frac{V_{A2}}{I_o} \quad (8.20)$$

where V_{A2} and r_{o2} are the Early voltage and the output resistance, respectively, of Q_2 . Thus, even if we neglect the error due to finite β , the output current I_o will be at its nominal value only when Q_2 has the same V_{CE} as Q_1 , namely, at $V_o = V_{BE}$. As V_o is increased, I_o will correspondingly increase. Taking both the finite β and the finite R_o into account, we can express the output current of a BJT mirror with a nominal current transfer ratio m as

$$I_o = I_{\text{REF}} \frac{m}{1 + \frac{m+1}{\beta}} \left(1 + \frac{V_o - V_{BE}}{V_{A2}}\right) \quad (8.21)$$

where we note that the error term due to the Early effect is expressed in a form that shows that it reduces to zero for $V_o = V_{BE}$.

EXERCISE

- 8.3** Consider a BJT current mirror with a nominal current transfer ratio of unity. Let the transistors have $I_s = 10^{-15}$ A, $\beta = 100$, and $V_A = 100$ V. For $I_{\text{REF}} = 1$ mA, find I_o when $V_o = 5$ V. Also, find the output resistance.

Ans. 1.02 mA; 100 k Ω

A Simple Current Source In a manner analogous to that in the MOS case, the basic BJT current mirror can be used to implement a simple current source, as shown in Fig. 8.9. Here the reference current is

$$I_{\text{REF}} = \frac{V_{CC} - V_{BE}}{R} \quad (8.22)$$

where V_{BE} is the base-emitter voltage corresponding to the desired value of I_{REF} . The output current I_o is given by

$$I_o = \frac{I_{\text{REF}}}{1 + (2/\beta)} \left(1 + \frac{V_o - V_{BE}}{V_A} \right) \quad (8.23)$$

The output resistance of this current source is r_o of Q_2 ,

$$R_o = r_{o2} \simeq \frac{V_A}{I_o} \simeq \frac{V_A}{I_{\text{REF}}} \quad (8.24)$$

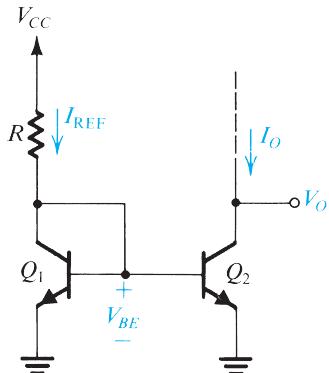


Figure 8.9 A simple BJT current source.

EXERCISE

- D8.4** Assuming the availability of BJTs with scale currents $I_s = 10^{-15}$ A, $\beta = 100$, and $V_A = 50$ V, design the current-source circuit of Fig. 8.9 to provide an output current $I_o = 0.5$ mA at $V_o = 2$ V. The power supply $V_{CC} = 5$ V. Give the values of I_{REF} , R , and $V_{o\text{min}}$. Also, find I_o at $V_o = 5$ V.

Ans. 0.497 mA; 8.71 k Ω ; 0.3 V; 0.53 mA

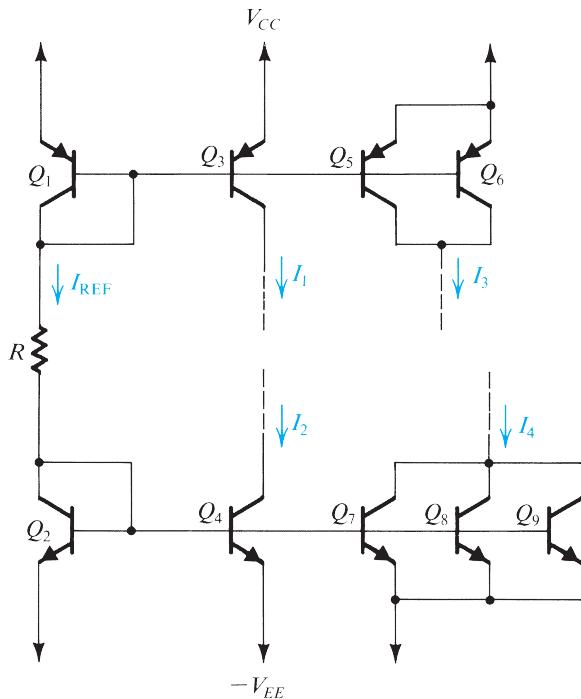


Figure 8.10 Generation of a number of constant currents of various magnitudes.

Current Steering To generate bias currents for different amplifier stages in an IC, the current-steering approach described for MOS circuits can be applied in the bipolar case. As an example, consider the circuit shown in Fig. 8.10. The dc reference current I_{REF} is generated in the branch that consists of the diode-connected transistor Q_1 , resistor R , and the diode-connected transistor Q_2 :

$$I_{\text{REF}} = \frac{V_{CC} + V_{EE} - V_{EB1} - V_{BE2}}{R} \quad (8.25)$$

Now, for simplicity, assume that all the transistors have high β and thus that the base currents are negligibly small. We will also neglect the Early effect. The diode-connected transistor Q_1 forms a current mirror with Q_3 ; thus Q_3 will supply a constant current I_1 equal to I_{REF} . Transistor Q_3 can supply this current to any load as long as the voltage that develops at the collector does not exceed ($V_{CC} - 0.3$ V); otherwise Q_3 would enter the saturation region.

To generate a dc current twice the value of I_{REF} , two transistors, Q_5 and Q_6 , each of which is matched to Q_1 , are connected in parallel, and the combination forms a mirror with Q_1 . Thus $I_3 = 2I_{\text{REF}}$. Note that the parallel combination of Q_5 and Q_6 is equivalent to a transistor with an EBJ area double that of Q_1 , which is precisely what is done when this circuit is fabricated in IC form.

Transistor Q_4 forms a mirror with Q_2 ; thus Q_4 provides a constant current I_2 equal to I_{REF} . Note that while Q_3 sources its current to parts of the circuit whose voltage should not exceed ($V_{CC} - 0.3$ V), Q_4 sinks its current from parts of the circuit whose voltage should not decrease below ($-V_{EE} + 0.3$ V). Finally, to generate a current three times I_{REF} , three transistors, Q_7 , Q_8 , and Q_9 , each of which is matched to Q_2 , are connected in parallel, and the combination is placed in a mirror configuration with Q_2 . Again, in an IC implementation, Q_7 , Q_8 , and Q_9 would be replaced with a transistor having a junction area three times that of Q_2 .

EXERCISE

- 8.5** Figure E8.5 shows an N -output current mirror. Assuming that all transistors are matched and have finite β and ignoring the effect of finite output resistances, show that

$$I_1 = I_2 = \dots = I_N = \frac{I_{\text{REF}}}{1 + (N+1)/\beta}$$

For $\beta = 100$, find the maximum number of outputs for an error not exceeding 10%.

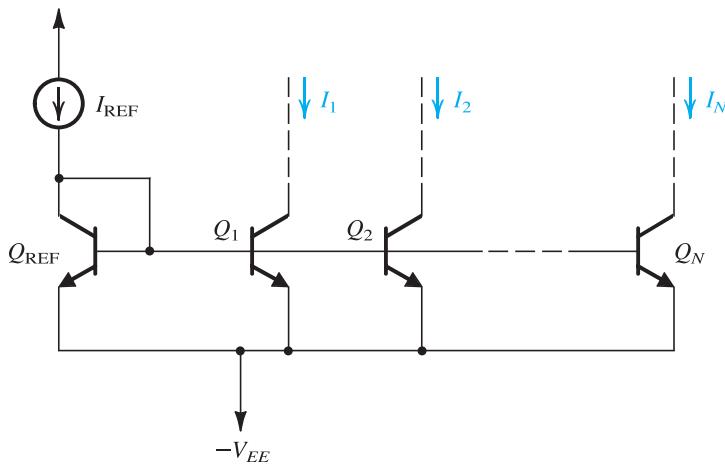


Figure E8.5

Ans. 9

A Bipolar Mirror with Base-Current Compensation Figure 8.11 shows a bipolar current mirror with a current transfer ratio that is much less dependent on β than that of the simple current mirror. The reduced dependence on β is achieved by including transistor Q_3 , the emitter of which supplies the base currents of Q_1 and Q_2 . The sum of the base currents is then divided by $(\beta_3 + 1)$, resulting in a much smaller error current that has to be supplied by I_{REF} . Detailed analysis is shown on the circuit diagram; it is based on the assumption that Q_1 and Q_2 are matched and thus have equal collector currents, I_C . A node equation at the node labeled x gives

$$I_{\text{REF}} = I_C \left[1 + \frac{2}{\beta(\beta + 1)} \right]$$

Since

$$I_o = I_C$$

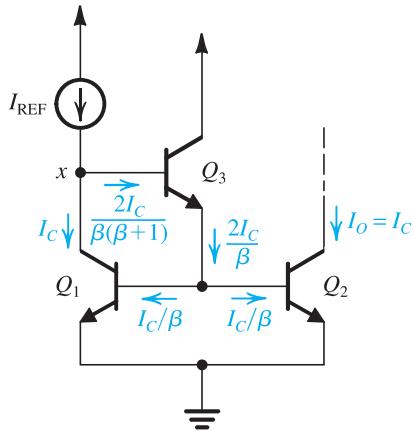


Figure 8.11 A current mirror with base-current compensation.

the current transfer ratio of the mirror will be

$$\begin{aligned}\frac{I_O}{I_{\text{REF}}} &= \frac{1}{1 + 2/(\beta^2 + \beta)} \\ &\simeq \frac{1}{1 + 2/\beta^2}\end{aligned}\quad (8.26)$$

which means that the error due to finite β has been reduced from $2/\beta$ in the simple mirror to $2/\beta^2$, a tremendous improvement. Unfortunately, however, the output resistance remains approximately equal to that of the simple mirror, namely r_o . Finally, note that if a reference current I_{REF} is not available, we simply connect node x to the power supply, V_{CC} , through a resistance R . The result is a reference current given by

$$I_{\text{REF}} = \frac{V_{CC} - V_{BE1} - V_{BE3}}{R} \quad (8.27)$$

8.2.4 Small-Signal Operation of Current Mirrors

In addition to their use in biasing, current mirrors are sometimes employed as current amplifiers. It is therefore useful to derive the small-signal parameters of the current mirror, that is, R_{in} , A_{is} , and R_o .

Figure 8.12(a) shows a MOS current mirror biased with a dc input current I_{D1} and fed with a small-signal input current i_i . Note that V_{GS} and I_{D2} are the resulting dc quantities, while v_{gs} and i_o are signal quantities. Although we are not showing the circuit to which the output terminal is connected, we are assuming that the voltage at the drain of Q_2 exceeds the minimum required to keep Q_2 in saturation.

Replacing Q_1 and Q_2 with their small-signal models results in the circuit in Fig. 8.12(b). Observe that the controlled current source $g_{m1} v_{gs}$ appears across its control voltage v_{gs} and thus can be replaced by a resistance, $1/g_{m1}$, as shown in Fig. 8.12(c). For the latter circuit we can obtain

$$R_{\text{in}} = r_{o1} \left\| \frac{1}{g_{m1}} \right\| \simeq \frac{1}{g_{m1}} \quad (8.28)$$

$$R_o = r_{o2} \quad (8.29)$$

$$A_{\text{is}} \equiv \left. \frac{i_o}{i_i} \right|_{v_{d2}=0} = \frac{g_{m2} v_{gs}}{i_i} \simeq \frac{g_{m2} i_i / g_{m1}}{i_i}$$

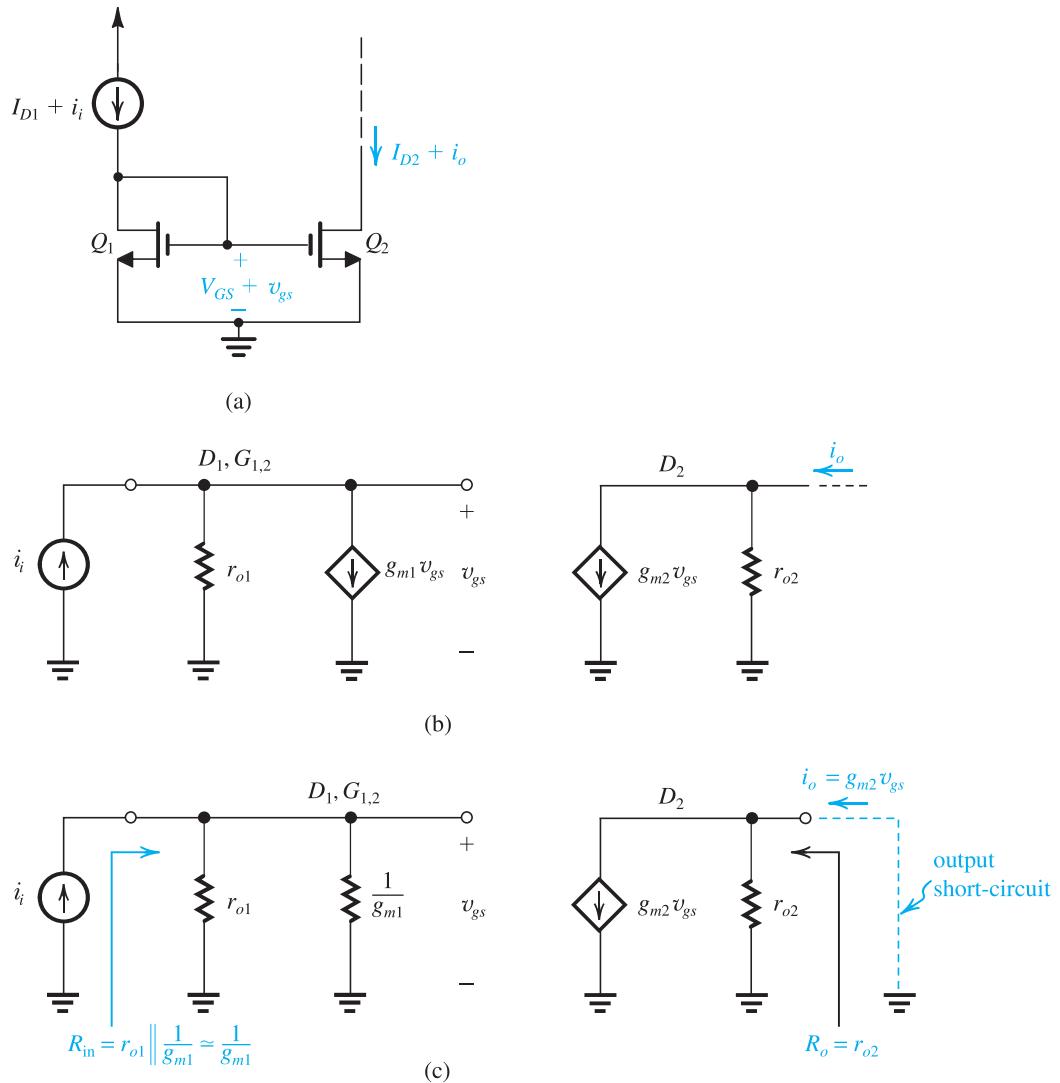


Figure 8.12 Obtaining the small-signal parameters of the MOS current mirror as a current amplifier.

Thus,

$$A_{is} = \frac{g_{m2}}{g_{m1}} \quad (8.30)$$

Substituting for $g_{m1,2} = \mu_n C_{ox} (W/L)_{1,2} V_{OV}$, where V_{OV} is the overdrive voltage at which Q_1 and Q_2 are operating, yields for the short-circuit current gain

$$A_{is} = \frac{(W/L)_2}{(W/L)_1} \quad (8.31)$$

which is equal to the dc or large-signal current transfer function—a clear indication of the excellent linearity of the current mirror.

We conclude that the current mirror is an excellent current amplifier: It has a relatively low input resistance ($1/g_{m1}$), a relatively high output resistance (r_{o2}), and a gain determined

by the aspect ratios of the MOSFETs. Finally, a similar development can be used to obtain the small-signal parameters of the bipolar mirror.

EXERCISE

- D8.6** The MOSFETs in the current mirror of Fig. 8.12(a) have equal channel lengths, $\mu_n C_{ox} = 400 \mu\text{A/V}^2$, and $V_A' = 20 \text{ V}/\mu\text{m}$. If the input bias current is $100 \mu\text{A}$, find W_1 , W_2 , L_1 , and L_2 to obtain a short-circuit current gain of 5, an input resistance of $1 \text{ k}\Omega$, and an output resistance of $40 \text{ k}\Omega$.

Ans. $12.5 \mu\text{m}$; $62.5 \mu\text{m}$; $1 \mu\text{m}$; and $1 \mu\text{m}$

THE INTEGRATED CIRCUIT:

In 1959, at the same time that Kilby and TI applied for a patent on “miniaturized electronic circuits,” Robert Noyce (a cofounder of Fairchild Semiconductor and later of Intel) filed a patent on the “monolithic silicon-based integrated circuit.” He later acknowledged the critical importance of Kurt Lehovac’s idea of using reverse-biased junctions to isolate multiple devices on a single die. Lehovac, of Sprague Electric Company, also filed a patent in 1959. Regrettably, Noyce, who died in 1990, did not live to share in the Nobel Prize with Kilby.

8.3 The Basic Gain Cell

8.3.1 The CS and CE Amplifiers with Current-Source Loads

The basic gain cell in an IC amplifier is a common-source (CS) or common-emitter (CE) transistor loaded with a constant-current source, as shown in Fig. 8.13(a) and (b). These circuits are similar to the CS and CE amplifiers studied in Section 7.3, except that here we have replaced the resistances R_D and R_C with constant-current sources. This is done for two reasons: First, as mentioned in Section 8.1, it is difficult in IC technology to implement resistances with reasonably precise values; rather, it is much easier to use current sources, which are implemented using transistors. Second, by using a constant-current source we are in effect operating the CS and CE amplifiers with a very high (ideally infinite) load resistance; thus we can obtain a much higher gain than if a finite R_D or R_C is used. This is particularly the case because, even if passive resistances were available, they would have very small values because the dc power supplies are now limited to only 1 V to 2 V. These voltages, however, do allow the use of current sources that have large output resistances. The circuits in Fig. 8.13(a) and (b) are said to be **current-source loaded** or **active loaded**.

Before we consider the small-signal analysis of the active-loaded CS and CE amplifiers, a word on their dc bias is in order. Obviously, in each circuit Q_1 is biased at $I_D = I$ and $I_C = I$. But what determines the dc voltages at the drain (collector) and at the gate (base)? Usually, these gain cells will be part of larger circuits in which negative feedback is utilized to fix the values of V_{DS} and V_{GS} (V_{CE} and V_{BE}). In the next chapter we will begin to see complete IC amplifiers including biasing. For the time being, however, we shall assume that the MOS transistor in

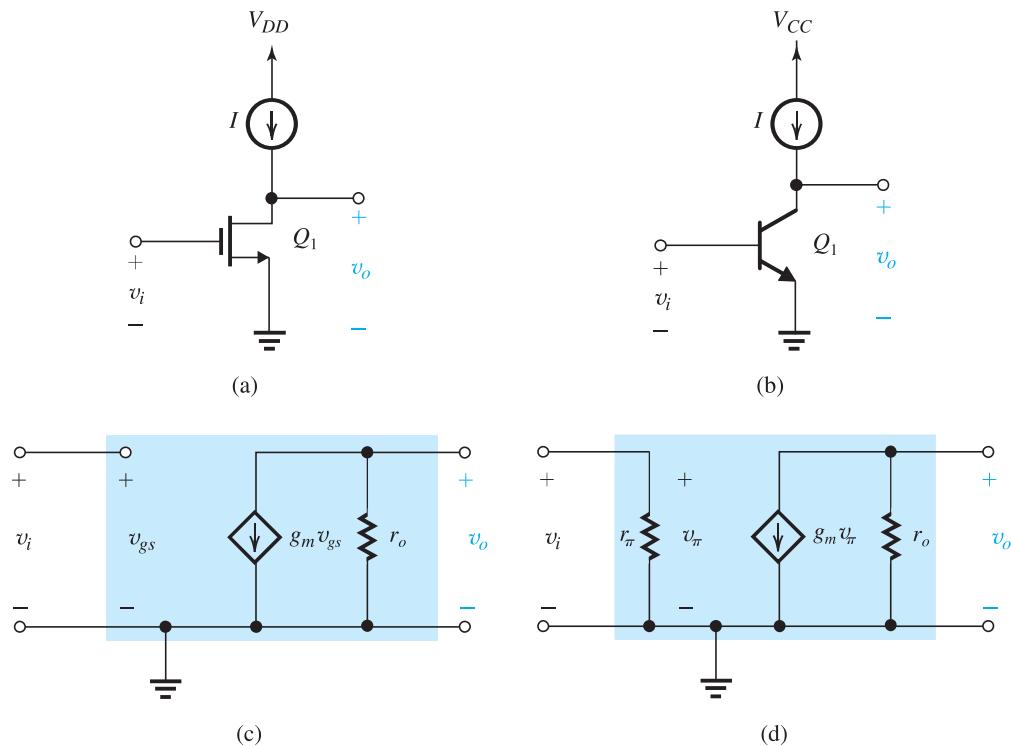


Figure 8.13 The basic gain cells of IC amplifiers: (a) current-source- or active-loaded common-source amplifier; (b) current-source- or active-loaded common-emitter amplifier; (c) small-signal equivalent circuit of (a); and (d) small-signal equivalent circuit of (b).

Fig. 8.13(a) is biased to operate in the saturation region and that the BJT in Fig. 8.13(b) is biased to operate in the active region. We will often refer to both the MOSFET and the BJT as operating in the “active region.”

Small-signal analysis of the current-source-loaded CS and CE amplifiers can be performed by utilizing their equivalent-circuit models, shown respectively in Fig. 8.13(c) and (d). Observe that since the current-source load is assumed to be ideal, it is represented in the models by an infinite resistance. Practical current sources have finite output resistance, as we have seen in the previous section. For the time being, however, note that the CS and CE amplifiers of Fig. 8.13 are in effect operating in an open-circuit fashion. The only resistance between their output node and ground is the output resistance of the transistor itself, r_o . Thus the voltage gain obtained in these circuits is the maximum possible for a CS or a CE amplifier.

From Fig. 8.13(c) we obtain for the active-loaded CS amplifier:

$$R_{in} = \infty \quad (8.32)$$

$$A_{vo} = -g_m r_o \quad (8.33)$$

$$R_o = r_o \quad (8.34)$$

Similarly, from Fig. 8.13(d) we obtain for the active-loaded CE amplifier:

$$R_{in} = r_\pi \quad (8.35)$$

$$A_{vo} = -g_m r_o \quad (8.36)$$

$$R_o = r_o \quad (8.37)$$

Thus both circuits realize a voltage gain of magnitude $g_m r_o$. Since this is the maximum gain obtainable in a CS or CE amplifier, we refer to it as the **intrinsic gain** and give it the symbol A_0 . Furthermore, it is useful to examine the nature of A_0 in a little more detail.

8.3.2 The Intrinsic Gain

For the BJT, we can derive a formula for the intrinsic gain $A_0 = g_m r_o$ by using the following formulas for g_m and r_o :

$$g_m = \frac{I_C}{V_T} \quad (8.38)$$

$$r_o = \frac{V_A}{I_C} \quad (8.39)$$

The result is

$$A_0 = g_m r_o = \frac{V_A}{V_T} \quad (8.40)$$

Thus A_0 is simply the ratio of the Early voltage V_A , which is a technology-determined parameter, and the thermal voltage V_T , which is a physical parameter (approximately 0.025 V at room temperature). The value of V_A ranges from 5 V to 35 V for modern IC fabrication processes to 100 V to 130 V for the older, so-called high-voltage processes (see Appendix G). As a result, the value of A_0 will be in the range of 200 V/V to 5000 V/V, with the lower values characteristic of modern small-feature-size devices. It is important to note that for a given bipolar-transistor fabrication process, A_0 is independent of the transistor junction area and of its bias current. This is not the case for the MOSFET, as we shall now see.

Recall from our study of the MOSFET g_m in Section 7.2 that there are three possible expressions for g_m . Two of these are particularly useful for our purposes here:

$$g_m = \frac{I_D}{V_{OV}/2} \quad (8.41)$$

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)} \sqrt{I_D} \quad (8.42)$$

For the MOSFET r_o we have

$$r_o = \frac{V_A}{I_D} = \frac{V'_A L}{I_D} \quad (8.43)$$

where V_A is the Early voltage and V'_A is the technology-dependent component of the Early voltage. Utilizing each of the g_m expressions together with the expression for r_o , we obtain for A_0 ,

$$A_0 = \frac{V_A}{V_{OV}/2} \quad (8.44)$$

which can be expressed in the alternate forms

$$A_0 = \frac{2V'_A L}{V_{OV}} \quad (8.45)$$

and

$$A_0 = \frac{V'_A \sqrt{2(\mu_n C_{ox})(WL)}}{\sqrt{I_D}} \quad (8.46)$$

The expression in Eq. (8.44) is the one most directly comparable to that of the BJT (Eq. 8.40). Here, however, we note the following:

1. The quantity in the denominator is $V_{ov}/2$, which is a design parameter. Although the value of V_{ov} that designers use for modern submicron technologies has been steadily decreasing, it is still about 0.15 V to 0.3 V. Thus $V_{ov}/2$ is 0.075 V to 0.15 V, which is 3 to 6 times higher than V_T . Furthermore, there are reasons for selecting higher values for V_{ov} (to be discussed in later chapters).
2. The numerator quantity is both process dependent (through V'_A) and device dependent (through L), and its value has been steadily decreasing with the scaling down of the technology (see Appendix K).
3. From Eq. (8.45) we see that for a given technology (i.e., a given value of V'_A) the intrinsic gain A_0 can be increased by using a longer MOSFET and operating it at a lower V_{ov} . As usual, however, there are design trade-offs. For instance, we will see in Chapter 10 that increasing L and lowering V_{ov} result, independently, in decreasing the amplifier bandwidth.

As a result, the intrinsic gain realized in a MOSFET fabricated in a modern short-channel technology is only 10 V/V to 40 V/V, an order of magnitude lower than that for a BJT.

The alternative expression for the MOSFET A_0 given in Eq. (8.46) reveals a very interesting fact: For a given process technology (V'_A and $\mu_n C_{ox}$) and a given device (W and L), the intrinsic gain is inversely proportional to $\sqrt{I_D}$. This is illustrated in Fig. 8.14, which shows a typical plot for A_0 versus the bias current I_D . The plot confirms that the gain increases as the bias current is lowered. The gain, however, levels off at very low currents. This is because the MOSFET enters the **subthreshold region** of operation (Section 5.1.9), where it becomes very much like a BJT with an exponential current–voltage characteristic. The intrinsic gain then becomes constant, just like that of a BJT. Note, however, that although higher gain is

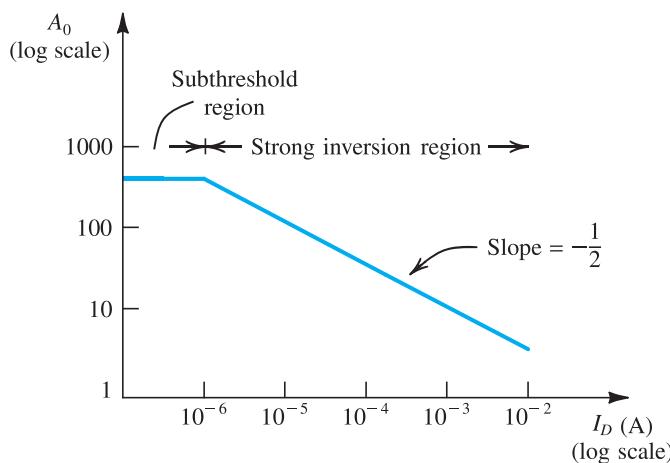


Figure 8.14 The intrinsic gain of the MOSFET versus bias current I_D . Outside the subthreshold region, this is a plot of $A_0 = V'_A \sqrt{2\mu_n C_{ox} WL/I_D}$ for the case: $\mu_n C_{ox} = 20 \mu\text{A/V}^2$, $V'_A = 20 \text{ V}/\mu\text{m}$, $L = 2 \mu\text{m}$, and $W = 20 \mu\text{m}$.

obtained at lower values of I_D , the price paid is a lower g_m (Eq. 8.42) and less ability to drive capacitive loads, and thus a decrease in bandwidth. This point will be studied in Chapter 10.

Example 8.2

We wish to compare the values of g_m , R_{in} , R_o , and A_0 for a CS amplifier that is designed using an NMOS transistor with $L = 0.4 \mu\text{m}$ and $W = 4 \mu\text{m}$ and fabricated in a $0.25\text{-}\mu\text{m}$ technology specified to have $\mu_n C_{ox} = 267 \mu\text{A/V}^2$ and $V'_A = 10 \text{ V}/\mu\text{m}$, with those for a CE amplifier designed using a BJT fabricated in a process with $\beta = 100$ and $V_A = 10 \text{ V}$. Assume that both devices are operating at a drain (collector) current of $100 \mu\text{A}$.

Solution

For simplicity, we shall neglect the Early effect in the MOSFET in determining V_{ov} ; thus,

$$\begin{aligned} I_D &= \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{ov}^2 \\ 100 &= \frac{1}{2} \times 267 \times \left(\frac{4}{0.4} \right) V_{ov}^2 \end{aligned}$$

resulting in

$$\begin{aligned} V_{ov} &= 0.27 \text{ V} \\ g_m &= \frac{2I_D}{V_{ov}} = \frac{2 \times 0.1}{0.27} = 0.74 \text{ mA/V} \\ R_{in} &= \infty \\ r_o &= \frac{V'_A L}{I_D} = \frac{10 \times 0.4}{0.1} = 40 \text{ k}\Omega \\ R_o &= r_o = 40 \text{ k}\Omega \\ A_0 &= g_m r_o = 0.74 \times 40 = 29.6 \text{ V/V} \end{aligned}$$

For the CE amplifier we have

$$\begin{aligned} g_m &= \frac{I_C}{V_T} = \frac{0.1 \text{ mA}}{0.025 \text{ V}} = 4 \text{ mA/V} \\ R_{in} &= r_\pi = \frac{\beta}{g_m} = \frac{100}{4} = 25 \text{ k}\Omega \\ r_o &= \frac{V_A}{I_C} = \frac{10}{0.1} = 100 \text{ k}\Omega \\ R_o &= r_o = 100 \text{ k}\Omega \\ A_0 &= g_m r_o = 4 \times 100 = 400 \text{ V/V} \end{aligned}$$

EXERCISE

- 8.7 A CS amplifier utilizes an NMOS transistor with $L = 0.36 \mu\text{m}$ and $W/L = 10$; it was fabricated in a $0.18\text{-}\mu\text{m}$ CMOS process for which $\mu_n C_{ox} = 387 \mu\text{A/V}^2$ and $V_A' = 5 \text{ V}/\mu\text{m}$. Find the values of g_m and A_0 obtained at $I_D = 10 \mu\text{A}$, $100 \mu\text{A}$, and 1 mA .

Ans. 0.28 mA/V , 50 V/V ; 0.88 mA/V , 15.8 V/V ; 2.78 mA/V , 5 V/V

8.3.3 Effect of the Output Resistance of the Current-Source Load

The current-source load of the CS amplifier in Fig. 8.13(a) can be implemented using a PMOS transistor biased in the saturation region to provide the required current I , as shown in Fig. 8.15(a). We can use the large-signal MOSFET model (Section 5.2, Fig. 5.18) to model

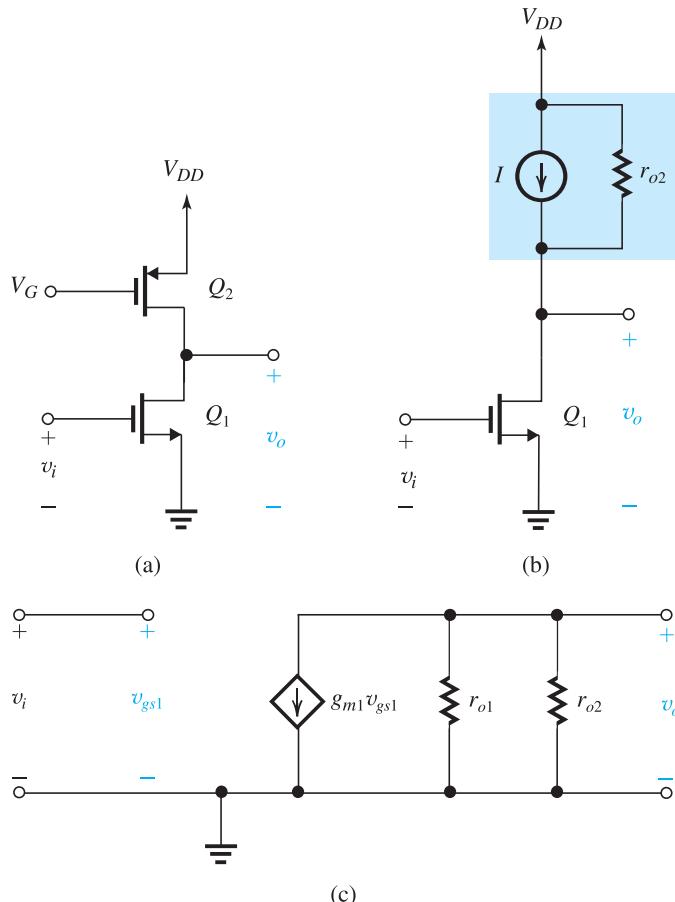


Figure 8.15 (a) The CS amplifier with the current-source load implemented with a *p*-channel MOSFET Q_2 ; (b) the circuit with Q_2 replaced with its large-signal model; and (c) small-signal equivalent circuit of the amplifier.

Q_2 as shown in Fig. 8.15(b), where

$$I = \frac{1}{2}(\mu_p C_{ox}) \left(\frac{W}{L} \right)_2 [V_{DD} - V_G - |V_{tp}|]^2 \quad (8.47)$$

and

$$r_{o2} = \frac{|V_{A2}|}{I} \quad (8.48)$$

Thus the current-source load no longer has an infinite resistance; rather, it has a finite output resistance r_{o2} . This resistance will in effect appear in parallel with r_{o1} , as shown in the amplifier equivalent-circuit model in Fig. 8.15(c), from which we obtain

$$A_v \equiv \frac{v_o}{v_i} = -g_{m1}(r_{o1} \parallel r_{o2}) \quad (8.49)$$

Thus, not surprisingly, the finite output resistance of the current-source load reduces the magnitude of the voltage gain from $(g_{m1} r_{o1})$ to $g_{m1}(r_{o1} \parallel r_{o2})$. This reduction can be substantial. For instance, if Q_2 has an Early voltage equal to that of Q_1 , $r_{o2} = r_{o1}$ and the gain is reduced by half,

$$A_v = -\frac{1}{2} g_m r_o \quad (8.50)$$

Finally, we note that a similar development can be used for the bipolar case.

Example 8.3

A practical circuit implementation of the common-source amplifier is shown in Fig. 8.16(a). Here the current-source transistor Q_2 is the output transistor of a current mirror formed by Q_2 and Q_3 and fed with a reference current I_{REF} . The NMOS version of this current source was studied in Section 8.1. Assume that Q_2 and Q_3 are matched. To be able to clearly see the region of v_L over which the circuit operates as an almost-linear amplifier, determine the voltage-transfer characteristic (VTC), that is, v_o versus v_L .

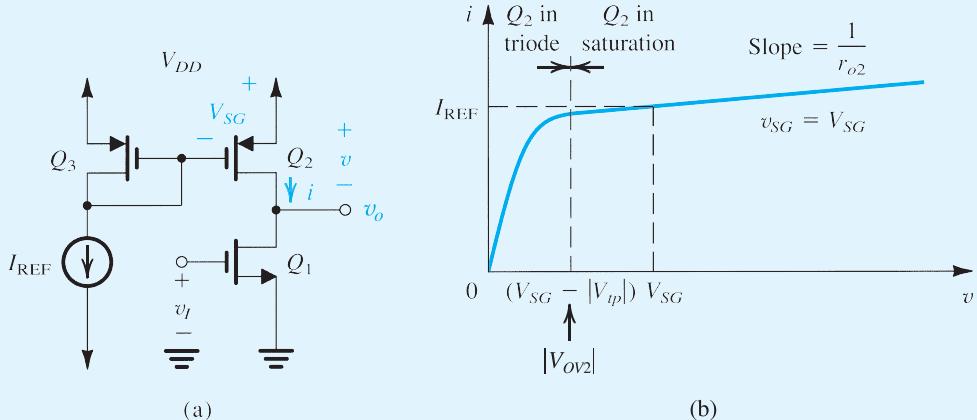
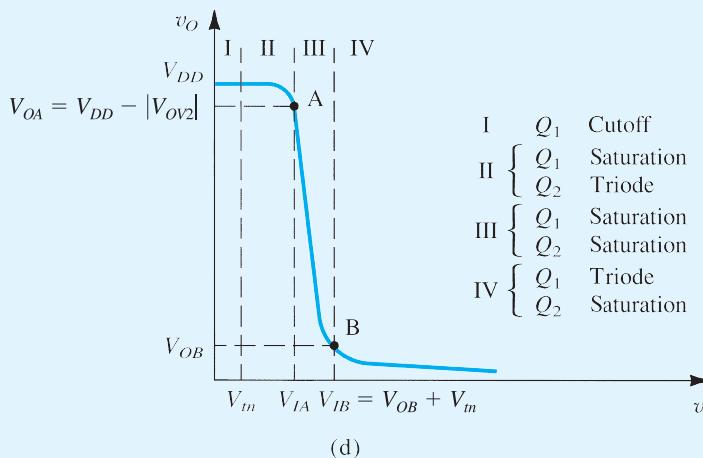
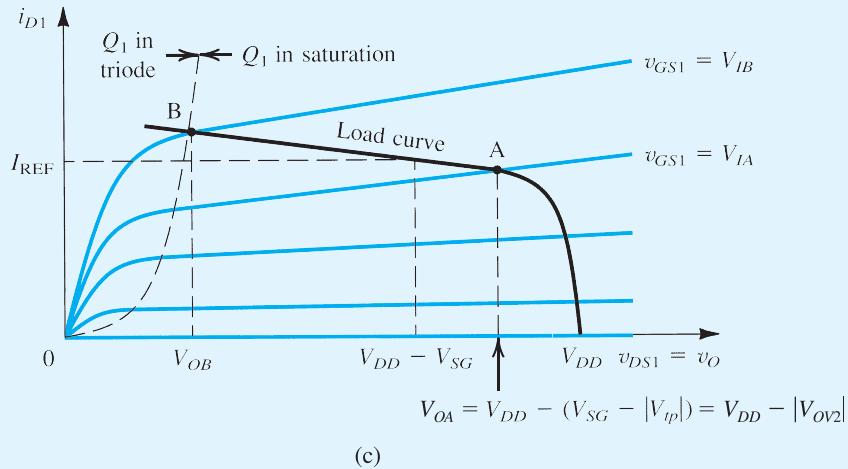


Figure 8.16 Practical implementation of the common-source amplifier: (a) circuit; (b) i - v characteristic of the active-load Q_2 ; (c) graphical construction to determine the transfer characteristic; (d) transfer characteristic.

Example 8.3 *continued***Figure 8.16** *continued***Solution**

First we concern ourselves with the current mirror, with the objective of determining the $i-v$ characteristic of the current source Q_2 . Toward that end, we note that the current I_{REF} flows through the diode-connected transistor Q_3 and thus determines V_{SG} of Q_3 , which is in turn applied between the source and the gate of Q_2 . Thus, the $i-v$ characteristic of the current source Q_2 will be the i_v - v_{SD} characteristic curve of Q_2 obtained for $v_{SG} = V_{SG}$. This is shown in Fig. 8.16(b), where we note that i will be equal to I_{REF} at one point only, namely, at $v_{SD2} = V_{SG}$, this being the only point at which the two matched transistors Q_2 and Q_3 have identical operating conditions. We also observe the effect of channel-length modulation in Q_2 (the Early effect), which is modeled by the finite output resistance r_{o2} . Finally, note that Q_2 operates as

a current source when v is equal to or greater than $|V_{ov2}| = V_{sg} - |V_{tp}|$. This in turn is obtained when $v_o \leq V_{dd} - |V_{ov2}|$. This is the maximum permitted value of the output voltage v_o .

Now, with the $i-v$ characteristic of the current-source load Q_2 in hand, we can proceed to determine v_o versus v_i . Figure 8.16(c) shows a graphical construction for doing this. It is based on the graphical analysis method employed in Section 7.1.6 except that here the load line is not a straight line but is the $i-v$ characteristic curve of Q_2 shifted along the v_o axis by V_{dd} volts and “flipped around.” The reason for this is that

$$v_o = V_{dd} - v$$

The term V_{dd} necessitates the shift, and the minus sign of v gives rise to the “flipping around” of the load curve.

The graphical construction of Fig. 8.16(c) can be used to determine v_o for every value of v_i , point by point: The value of v_i determines the particular characteristic curve of Q_1 on which the operating point lies. The operating point will be at the intersection of this particular graph and the load curve. The horizontal coordinate of the operating point then gives the value of v_o .

Proceeding in the manner just explained, we obtain the VTC shown in Fig. 8.16(d). As indicated, it has four distinct segments, labeled I, II, III, and IV. Each segment is obtained for one of the four combinations of the modes of operation of Q_1 and Q_2 , which are also indicated in the diagram. Note that we have labeled two important break points on the transfer characteristic (A and B) in correspondence with the intersection points (A and B) in Fig. 8.16(c). We urge the reader to carefully study the transfer characteristic and its various details.

Not surprisingly, segment III is the one of interest for amplifier operation. Observe that in region III the transfer curve is almost linear and is very steep, indicating large voltage gain. In region III both the amplifying transistor Q_1 and the load transistor Q_2 are operating in saturation. The end points of region III are A and B: At A, defined by $v_o = V_{dd} - |V_{ov2}|$, Q_2 enters the triode region, and at B, defined by $v_o = v_i - V_{tn}$, Q_1 enters the triode region. When the amplifier is biased at a point in region III, the small-signal voltage gain can be determined as we have done in Fig. 8.15(c). The question remains as to how we are going to guarantee that the dc component of v_i will have such a value that will result in operation in region III. That is why overall negative feedback is needed, as will be demonstrated later.

Before leaving this example it is useful to reiterate that the upper limit of the amplifier region (i.e., point A) is defined by $V_{OA} = V_{dd} - |V_{ov2}|$ and the lower limit (i.e., point B) is defined by $V_{OB} = V_{ov1}$, where V_{ov1} can be approximately determined by assuming that $I_{D1} \approx I_{REF}$. A more precise value for V_{OB} can be obtained by taking into account the Early effect in both Q_1 and Q_2 , as will be demonstrated in the next example.

Example 8.4

Consider the CMOS common-source amplifier in Fig. 8.16(a) for the case $V_{dd} = 3$ V, $V_{tn} = |V_{tp}| = 0.6$ V, $\mu_n C_{ox} = 200 \mu\text{A/V}^2$, and $\mu_p C_{ox} = 65 \mu\text{A/V}^2$. For all transistors, $L = 0.4 \mu\text{m}$ and $W = 4 \mu\text{m}$. Also, $V_{An} = 20$ V, $|V_{Ap}| = 10$ V, and $I_{REF} = 100 \mu\text{A}$. Find the small-signal voltage gain. Also, find the coordinates of the extremities of the amplifier region of the transfer characteristic—that is, points A and B.

Example 8.4 *continued***Solution**

$$\begin{aligned} g_{m1} &= \sqrt{2k'_n \left(\frac{W}{L}\right)_1 I_{\text{REF}}} \\ &= \sqrt{2 \times 200 \times \frac{4}{0.4} \times 100} = 0.63 \text{ mA/V} \\ r_{o1} &= \frac{V_{A1}}{I_{D1}} = \frac{20 \text{ V}}{0.1 \text{ mA}} = 200 \text{ k}\Omega \\ r_{o2} &= \frac{|V_{Ap}|}{I_{D2}} = \frac{10 \text{ V}}{0.1 \text{ mA}} = 100 \text{ k}\Omega \end{aligned}$$

Thus,

$$\begin{aligned} A_v &= -g_{m1}(r_{o1} \parallel r_{o2}) \\ &= -0.63(\text{mA/V}) \times (200 \parallel 100)(\text{k}\Omega) = -42 \text{ V/V} \end{aligned}$$

Approximate values for the extremities of the amplifier region of the transfer characteristic [region III in Fig. 8.16(d)] can be determined as follows: Neglecting the Early effect, all three transistors are carrying equal currents I_{REF} , and thus we can determine the overdrive voltages at which they are operating. Transistors Q_2 and Q_3 will have equal overdrive voltages, $|V_{ov3}|$, determined from

$$I_{D3} = I_{\text{REF}} \simeq \frac{1}{2} (\mu_p C_{ox}) \left(\frac{W}{L}\right)_3 |V_{ov3}|^2$$

Substituting $I_{\text{REF}} = 100 \mu\text{A}$, $\mu_p C_{ox} = 65 \mu\text{A/V}^2$, $(W/L)_3 = 4/0.4 = 10$ results in

$$|V_{ov3}| = 0.55 \text{ V}$$

Thus,

$$V_{OA} = V_{DD} - |V_{ov3}| = 2.45 \text{ V}$$

Next we determine $|V_{ov1}|$ from

$$I_{D1} \simeq I_{\text{REF}} \simeq \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L}\right)_1 V_{ov1}^2$$

Substituting $I_{\text{REF}} = 100 \mu\text{A}$, $\mu_n C_{ox} = 200 \mu\text{A/V}^2$, $(W/L)_1 = 4/0.4 = 10$ results in

$$V_{ov1} = 0.32 \text{ V}$$

Thus,

$$V_{OB} = V_{ov1} = 0.32 \text{ V.}$$

More precise values for V_{OA} and V_{OB} can be determined by taking the Early effect in all transistors into account as follows.

First, we determine V_{SG} of Q_2 and Q_3 corresponding to $I_{D3} = I_{REF} = 100 \mu\text{A}$ using

$$I_{D3} = \frac{1}{2} k'_p \left(\frac{W}{L} \right)_3 (V_{SG} - |V_{tp}|)^2 \left(1 + \frac{V_{SD}}{|V_{Ap}|} \right)$$

Thus,

$$100 = \frac{1}{2} \times 65 \left(\frac{4}{0.4} \right) |V_{ov3}|^2 \left(1 + \frac{0.6 + |V_{ov3}|}{10} \right) \quad (8.51)$$

where $|V_{ov3}|$ is the magnitude of the overdrive voltage at which Q_3 and Q_2 are operating, and we have used the fact that, for Q_3 , $V_{SD} = V_{SG}$. Equation (8.51) can be manipulated to the form

$$0.29 = |V_{ov3}|^2 (1 + 0.09 |V_{ov3}|)$$

which by a trial-and-error process yields

$$|V_{ov3}| = 0.526 \text{ V}$$

Thus,

$$V_{SG} = 0.6 + 0.526 = 1.126 \text{ V}$$

and

$$V_{OA} = V_{DD} - V_{ov3} = 2.47 \text{ V}$$

To find the corresponding value of v_I , V_{IA} , we derive an expression for v_o versus v_I in region III. Noting that in region III, Q_1 and Q_2 are in saturation and obviously conduct equal currents, we can write

$$\begin{aligned} i_{D1} &= i_{D2} \\ \frac{1}{2} k'_n \left(\frac{W}{L} \right)_1 (v_I - V_{tn})^2 \left(1 + \frac{v_o}{|V_{An}|} \right) &= \frac{1}{2} k'_p \left(\frac{W}{L} \right)_2 (V_{SG} - |V_{tp}|)^2 \left(1 + \frac{V_{DD} - v_o}{|V_{Ap}|} \right) \end{aligned}$$

Substituting numerical values, we obtain

$$8.55(v_I - 0.6)^2 = \frac{1 - 0.08v_o}{1 + 0.05v_o} \quad (8.52)$$

This is the equation of segment III of the transfer characteristic. Although it includes v_I^2 , the reader should not be alarmed: Because region III is very narrow, v_I changes very little, and the characteristic is nearly linear. Substituting $v_o = 2.47 \text{ V}$ gives the corresponding value of v_I ; that is, $V_{IA} = 0.89 \text{ V}$. To determine the coordinates of B, we note that they are related by $V_{OB} = V_{IB} - V_{tn}$. Substituting in Eq. (8.52) and solving by trial and error gives $V_{IB} = 0.935 \text{ V}$ and $V_{OB} = 0.335 \text{ V}$. The width of the amplifier region is therefore

$$\Delta v_I = V_{IB} - V_{IA} = 0.045 \text{ V}$$

and the corresponding output range is

$$\Delta v_o = V_{OB} - V_{OA} = -2.135 \text{ V}$$

Example 8.4 *continued*

Thus, the “large-signal” voltage gain is

$$\frac{\Delta v_o}{\Delta v_i} = -\frac{2.135}{0.045} = -47.4 \text{ V/V}$$

which is reasonably close to the small-signal value of -42 , indicating that segment III of the transfer characteristic is quite linear.

EXERCISES

- 8.8** A CMOS common-source amplifier such as that in Fig. 8.16(a), fabricated in a $0.18\text{-}\mu\text{m}$ technology, has $W/L = 7.2\text{ }\mu\text{m}/0.36\text{ }\mu\text{m}$ for all transistors, $k'_n = 387\text{ }\mu\text{A/V}^2$, $k'_p = 86\text{ }\mu\text{A/V}^2$, $I_{\text{REF}} = 100\text{ }\mu\text{A}$, $V'_{An} = 5\text{ V}/\mu\text{m}$, and $|V'_{Ap}| = 6\text{ V}/\mu\text{m}$. Find g_{m1} , r_{o1} , r_{o2} , and the voltage gain.

Ans. 1.24 mA/V ; $18\text{ k}\Omega$; $21.6\text{ k}\Omega$; -12.2 V/V

- 8.9** Consider the active-loaded CE amplifier when the constant-current source I is implemented with a *pnp* transistor. Let $I = 0.1\text{ mA}$, $|V_A| = 50\text{ V}$ (for both the *npn* and the *pnp* transistors), and $\beta = 100$. Find R_{in} , r_o (for each transistor), g_m , A_0 , and the amplifier voltage gain.

Ans. $25\text{ k}\Omega$; $0.5\text{ M}\Omega$; 4 mA/V ; 2000 V/V ; -1000 V/V

8.3.4 Increasing the Gain of the Basic Cell

We conclude this section by considering a question: How can we increase the voltage gain obtained from the basic gain cell? The answer lies in finding a way to raise the level of the output resistance of both the amplifying transistor and the load transistor. That is, we seek a circuit that passes the current $g_m v_i$ provided by the amplifying transistor right through, but increases the resistance from r_o to a much larger value. This requirement is illustrated in Fig. 8.17. Figure 8.17(a) shows the CS amplifying transistor Q_1 together with its output equivalent circuit. Note that for the time being we are not showing the load device. In Fig. 8.17(b) we have inserted a shaded box between the drain of Q_1 and a new output terminal labeled d_2 . Here again we are not showing the load to which d_2 will be connected. Our “black box” takes in the output current of Q_1 and passes it to the output; thus at its output we have the equivalent circuit shown, consisting of the same controlled source $g_{m1} v_i$ but with the output resistance increased by a factor K .

Now, what does the black box really do? Since it passes the *current* but *raises* the resistance level, it is a **current buffer**. It is the dual of the voltage buffer (the source and emitter followers), which passes the *voltage* but *lowers* the resistance level.

Now searching our repertoire of transistor amplifier configurations studied in Section 7.3, the only candidate for implementing this current-buffering action is the common-gate (or common-base in bipolar) amplifier. Indeed, recall that the CG and CB circuits have a unity current gain. What we have not yet investigated, however, is their resistance transformation property. We shall do this in the next section.

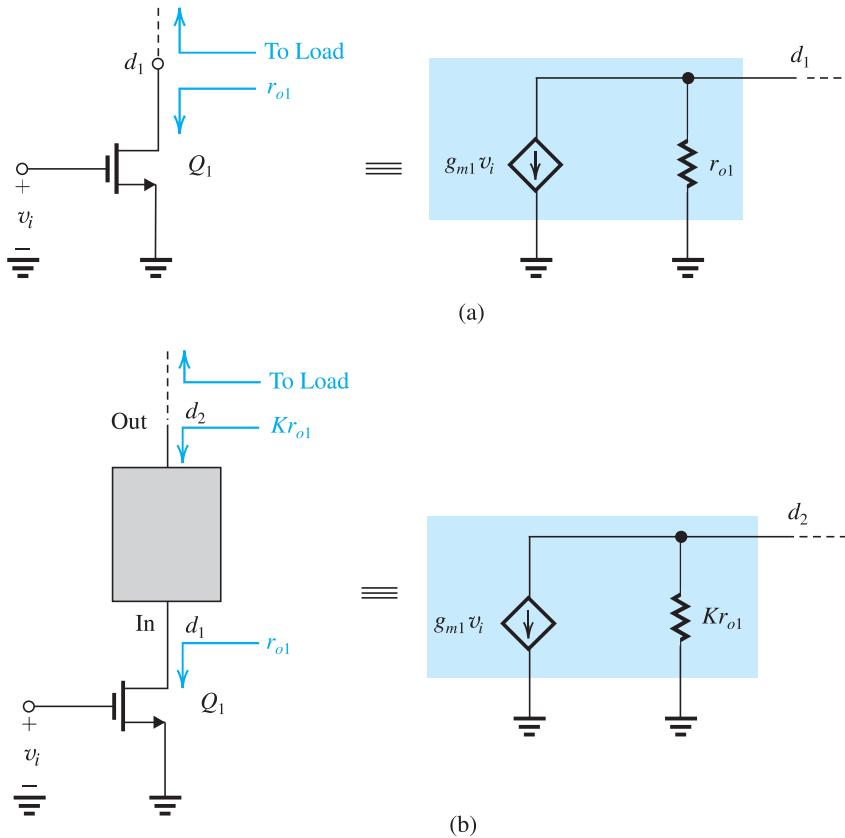


Figure 8.17 To increase the voltage gain realized in the basic gain cell shown in (a), a functional block, shown as a black box in (b), is connected between d_1 and the load. This new block is required to pass the current $g_{m1}v_i$ right through but raise the resistance level by a factor K . The functional block is a current buffer and can be realized with a common-gate transistor, as demonstrated in the next section.

8.4 The Common-Gate and Common-Base Amplifiers

In this section we study the IC versions of the CG and CB amplifier configurations. This study differs in a significant way from that of the discrete-circuit versions (Section 7.3.5) because here we have to take into account the output resistance of the transistor, r_o . In the following, we show that both the CG and CB configurations provide excellent implementations of the current buffer discussed in the previous section.

8.4.1 The CG Circuit

Figure 8.18(a) shows a CG amplifier with the biasing arrangement shown only partially. The amplifier is fed with a signal source v_{sig} having a resistance R_s , and it has a load resistance R_L . The latter is usually implemented using a PMOS current source, as discussed earlier.

To characterize the signal performance of the CG amplifier, we show in Fig. 8.18(b) the circuit with the dc voltages eliminated. Observe that because the gate current is zero, the input

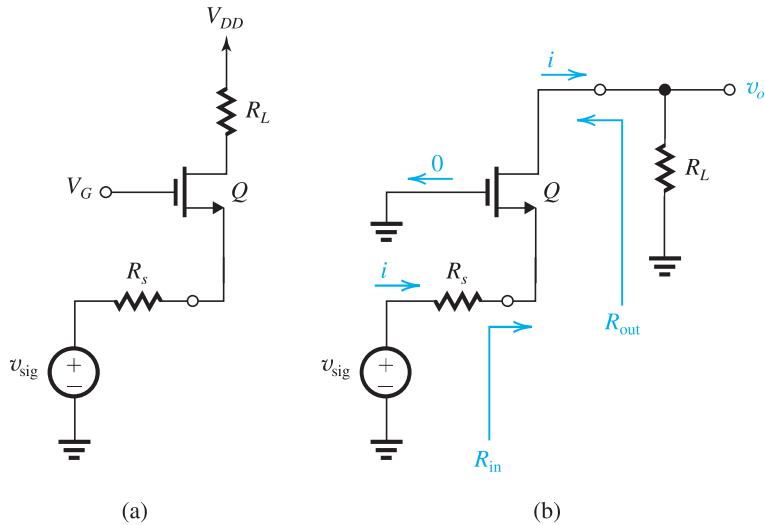


Figure 8.18 (a) A CG amplifier with the bias arrangement only partially shown. (b) The circuit with the dc sources eliminated.

current i passes through to the drain and on to the load—the first requirement of a current buffer.

Input Resistance The input resistance R_{in} can be found using the circuit of Fig. 8.19. Here we have employed the T model of the MOSFET and applied a test voltage v_x to the input. The input resistance is given by

$$R_{in} \equiv \frac{v_x}{i_x}$$

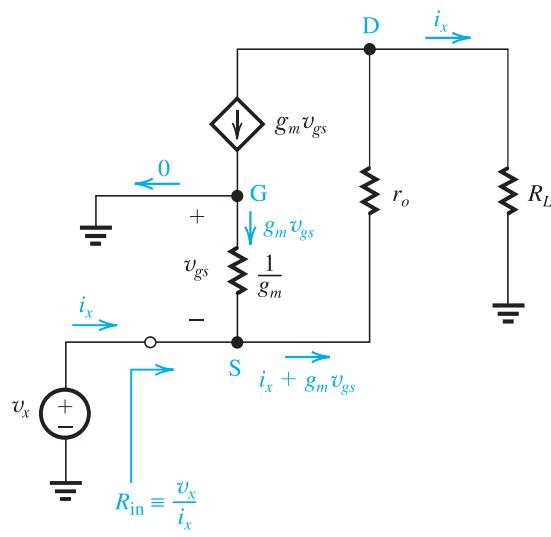


Figure 8.19 Determining the input resistance R_{in} of the CG amplifier.

The analysis proceeds as follows.

A node equation at the input yields the current in r_o as $(i_x + g_m v_{gs})$. A node equation at the output shows that the current through R_L is i_x . Next, a loop equation for the loop comprising v_x , r_o , and R_L gives

$$v_x = (i_x + g_m v_{gs}) r_o + i_x R_L$$

Since the voltage at the source node v_x is equal to $-v_{gs}$, we can replace v_{gs} by $-v_x$ and rearrange terms to obtain $R_{in} \equiv v_x/i_x$,

$$R_{in} = \frac{r_o + R_L}{1 + g_m r_o} \quad (8.53)$$

For $g_m r_o \gg 1$,

$$R_{in} \simeq \frac{1}{g_m} + \frac{R_L}{g_m r_o} \quad (8.54)$$

This is a very interesting result. First, it shows that if r_o is infinite, as was the case in our analysis of the discrete CG amplifier in Section 7.3.5, then R_{in} reduces to $1/g_m$, verifying the result we found there. If r_o cannot be neglected, as is always the case in IC amplifiers, we see that the input resistance depends on R_L in an interesting fashion: The load resistance R_L is transformed to the input by dividing it by the intrinsic gain $A_0 = g_m r_o$. Thus, even as R_L is increased, this impedance transformation property ensures that R_{in} remains relatively low, an important characteristic of a current buffer.

Output Resistance To obtain the output resistance R_{out} we utilize the circuit shown in Fig. 8.20. Here we have short circuited v_{sig} but left the source resistance R_s , and applied a test voltage v_x to the output. The output resistance is given by

$$R_{out} = \frac{v_x}{i_x}$$

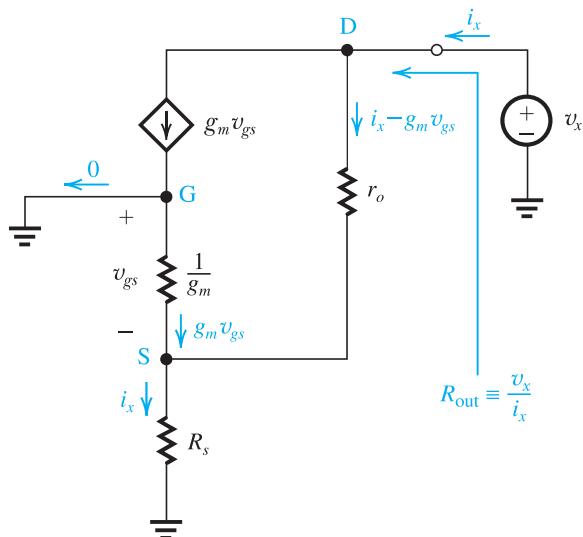


Figure 8.20 Determining the output resistance R_{out} of the CG amplifier.

The analysis proceeds as follows.

A node equation at the drain gives the current through r_o as $(i_x - g_m v_{gs})$. A node equation at the source gives the current in R_s as i_x . Next, a loop equation for the loop comprising v_x , r_o , and R_s gives

$$v_x = (i_x - g_m v_{gs})r_o + i_x R_s \quad (8.55)$$

Finally, we observe that the voltage at the source terminal is $-v_{gs}$ and can also be expressed as $i_x R_s$, thus

$$v_{gs} = -i_x R_s$$

Substituting this value for v_{gs} into Eq. (8.55) and rearranging terms to obtain $R_{\text{out}} \equiv v_x/i_x$ yields



$$R_{\text{out}} = r_o + R_s + g_m r_o R_s \quad (8.56)$$

which can be written in the alternate form

$$R_{\text{out}} = r_o + (1 + g_m r_o) R_s \quad (8.57)$$

For $g_m r_o \gg 1$,



$$R_{\text{out}} \simeq r_o + (g_m r_o) R_s \quad (8.58)$$

and if we also have $g_m R_s \gg 1$ then



$$R_{\text{out}} \simeq (g_m r_o) R_s \quad (8.59)$$

Equation (8.58) indicates that the output resistance of the CG amplifier includes, in addition to the transistor's r_o , a component related to the resistance in the source load R_s . The significant point is that the CG amplifier transforms the source resistance R_s to the output by multiplying it by the intrinsic gain $A_0 = g_m r_o$. This impedance transformation is the inverse to that observed from output to input. Now, if R_s is large then the output resistance of the CG circuit can be very large; this also is an important characteristic of a current buffer.

To summarize: the CG circuit has a unity current gain; a low input resistance, obtained by dividing R_L by $g_m r_o$; and a high output resistance, obtained by multiplying R_s by $g_m r_o$. Thus it makes for an excellent current buffer and can be used to implement the shaded functional box in Fig. 8.17. As a useful summary, Fig. 8.21 illustrates the impedance transformation properties of the common-gate amplifier.

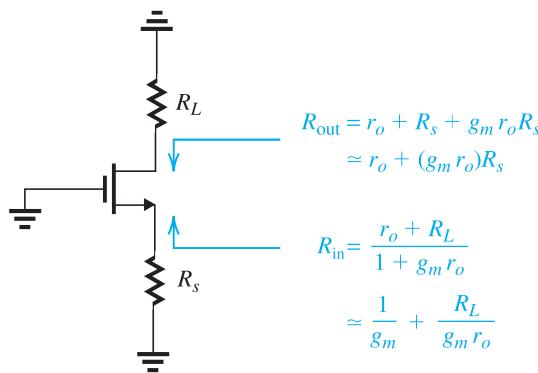


Figure 8.21 The impedance transformation properties of the common-gate amplifier. Depending on the values of R_s and R_L , we can sometimes write $R_{\text{in}} \simeq R_L/(g_m r_o)$ and $R_o \simeq (g_m r_o) R_s$. However, such approximations are not always justified.

EXERCISES

- 8.10** For the CG amplifier in Fig. 8.18, show that the voltage gain is given by

$$\frac{v_o}{v_{\text{sig}}} = \frac{R_L}{R_s + R_{\text{in}}}$$

- 8.11** For a CG amplifier for which $g_m r_o \gg 1$, find R_{in} for the following cases: $R_L = 0$; r_o ; $(g_m r_o) r_o$; ∞ .

Ans. $\frac{1}{g_m}$; $\frac{2}{g_m}$; r_o ; ∞

- 8.12** For a CG amplifier for which $g_m r_o \gg 1$, find R_{out} for the following cases: $R_s = 0$; r_o ; $(g_m r_o) r_o$; ∞ .

Ans. r_o ; $(g_m r_o) r_o$; $(g_m r_o)^2 r_o$; ∞

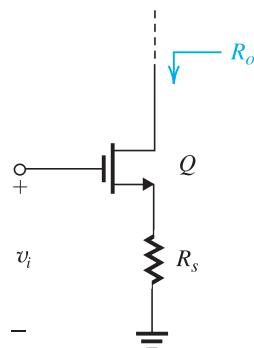
8.4.2 Output Resistance of a CS Amplifier with a Source Resistance

In Section 7.3.4 we discussed some of the benefits that are obtained when a resistance R_s is included in the source lead of a CS amplifier, as in Fig. 8.22. Such a resistance is referred to as a source-degeneration resistance because of its action in reducing the effective transconductance of the CS stage to $g_m/(1 + g_m R_s)$, that is, by a factor $(1 + g_m R_s)$. This also is the factor by which a number of performance parameters are increased, such as linearity and bandwidth (as will be seen in Chapter 10). At this juncture we simply wish to point out that the expression we derived above for the output resistance of the CG amplifier applies directly to the case of a source-degenerated CS amplifier. This is because when we determine R_o , we ground the input terminal, making transistor Q appear as a CG transistor. Thus R_o is given by Eq. (8.56), namely,

$$R_o = r_o + R_s + g_m r_o R_s \quad (8.60)$$

Since $g_m r_o \gg 1$, the second term on the right-hand side will be much lower than the third and can be neglected, resulting in

$$R_o \simeq (1 + g_m R_s) r_o \quad (8.61)$$



$$R_o = R_s + r_o + g_m r_o R_s$$

$$R_o \simeq (1 + g_m R_s) r_o$$

Figure 8.22 The output resistance expression of the CG amplifier can be used to find the output resistance of a source-degenerated common-source amplifier. Here, a useful interpretation of the result is that R_s increases the output resistance by the factor $(1 + g_m R_s)$.

Thus source degeneration increases the output resistance of the CS amplifier from r_o to $(1 + g_m R_s) r_o$, again by the same factor $(1 + g_m R_s)$. In Chapter 11, we will find that R_s introduces negative (degenerative) feedback of an amount $(1 + g_m R_s)$.

EXERCISE

- 8.13** Given that source degeneration reduces the transconductance of a CS amplifier from g_m to approximately $g_m/(1 + g_m R_s)$ and increases its output resistance by approximately the same factor, what happens to the open-circuit voltage gain A_{vo} ? Now, find an expression for A_v when a load resistance R_L is connected to the output.

Ans. A_{vo} remains constant at $g_m r_o$:

$$A_v = (g_m r_o) \frac{R_L}{R_L + (1 + g_m R_s) r_o} \quad (\text{E.8.13})$$

8.4.3 The Body Effect

Since in the CG amplifier the source cannot be connected to the substrate, the body effect (see Section 5.4) plays a role in the operation of the CG amplifier. It turns out, however, that taking the body effect into account in the analysis of the CG circuit is a very simple matter. To see how this can be done, refer to Fig. 8.23(a) and recall that the body terminal acts as another gate for the MOSFET. Thus, just as a signal voltage v_{gs} between the gate and the source gives

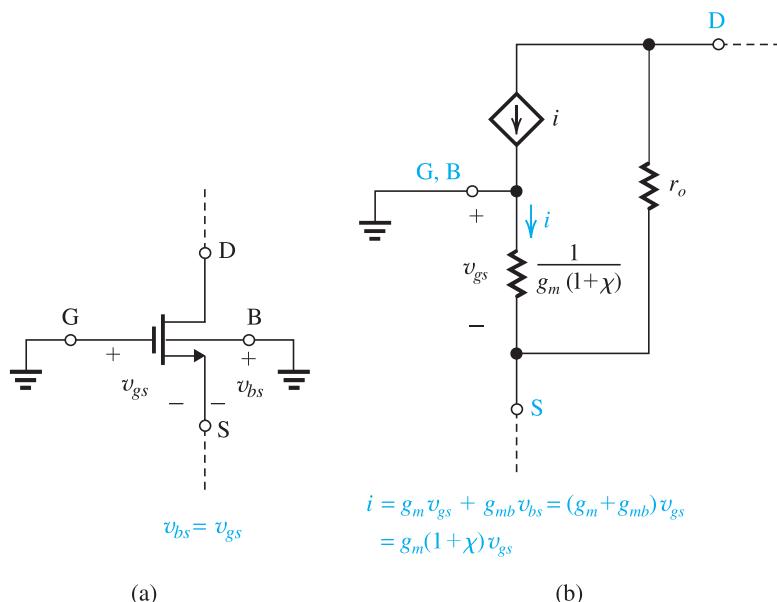


Figure 8.23 The body effect can be easily taken into account in the analysis of the CG circuit by replacing g_m by $(1 + \chi) g_m$, where $\chi = g_{mb}/g_m = 0.1$ to 0.2.

rise to a drain current signal $g_m v_{gs}$, a signal voltage v_{bs} between the body and the source gives rise to a drain current signal $g_{mb} v_{bs}$. Thus the drain signal current becomes $(g_m v_{gs} + g_{mb} v_{bs})$, where the body transconductance g_{mb} is a small fraction χ of g_m ; $g_{mb} = \chi g_m$ and $\chi = 0.1$ to 0.2 . For the CG circuit, $v_{bs} = v_{gs}$, thus the two current signals can be combined as $(g_m + g_{mb})v_{gs}$ or $g_m(1 + \chi)v_{gs}$. Thus, the body effect can be taken into account by simply replacing g_m by $g_m(1 + \chi)$ as illustrated in the T equivalent model shown in Fig. 8.23(b). Normally, however, we will not bother with the factor $(1 + \chi)$ in our calculations.

8.4.4 The CB Circuit

Analysis of the CB amplifier parallels that of the CG amplifier except it is a little more involved because of the finite base current. Figure 8.24(a) shows a CB amplifier with the bias details only partially shown and with a load resistance R_L that is normally implemented with a *pnp* current source. The circuit, prepared for small-signal analysis, is shown in Fig. 8.24(b). Note that since $\alpha \simeq 1$ the current gain is nearly unity, an important characteristic of a current buffer.

Input Resistance The circuit for determining the input resistance R_{in} is shown in Fig. 8.25, which also shows the currents in all branches, obtained by writing node equations for the three nodes. Of special note is the use of the identity $g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$ to obtain the current in the base as v_π/r_π . Writing a loop equation for the loop comprising v_x , r_o , and R_L , and replacing v_π by $-v_x$, results in the following expression for $R_{in} \equiv v_x/i_x$,

$$R_{in} = \frac{r_o + R_L}{1 + \frac{r_o}{r_e} + \frac{R_L}{(\beta + 1)r_e}} \quad (8.62)$$

where we have utilized the relationship $r_\pi = (\beta + 1)r_e$. Since $r_o \gg r_e$,

$$R_{in} \simeq r_e \frac{r_o + R_L}{r_o + \frac{R_L}{\beta + 1}} \quad (8.63)$$

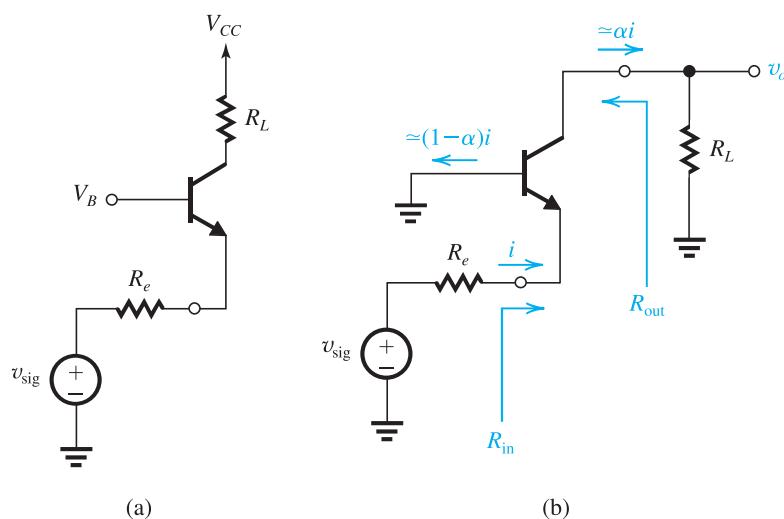


Figure 8.24 (a) A CB amplifier with the bias arrangement only partially shown. (b) The circuit with the dc sources eliminated.

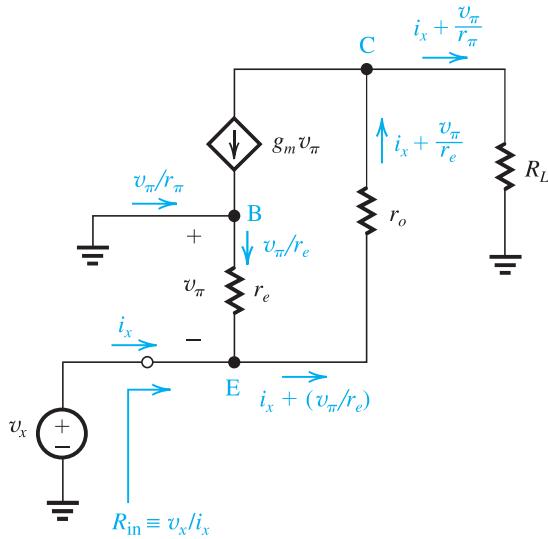


Figure 8.25 Determining the input resistance R_{in} of the CB amplifier.

Note that setting $r_o = \infty$ yields $R_{in} = r_e$, which is consistent with the case of the discrete-circuit CB amplifier studied in Section 7.3.5. Also, for $R_L = 0$, $R_{in} = r_e$. The value of R_{in} increases as R_L is raised, reaching a maximum of

$$R_{in}|_{\max} = (\beta + 1)r_e = r_\pi, \text{ for } R_L = \infty \quad (8.64)$$

that is, for the amplifier operating open circuited. Finally, for $\frac{R_L}{\beta + 1} \ll r_o$, Eq. (8.63) can be approximated by

$$R_{in} \simeq r_e + \frac{R_L}{g_m r_o} \quad (8.65)$$

which is very similar to the case of the MOSFET (Eq. 8.54). We conclude by noting that the impedance transformation property of the CB circuit ensures that its input resistance is kept small, an important characteristic of a current buffer.

Output Resistance The determination of the output resistance R_{out} of the CB amplifier is illustrated in Fig. 8.26. The result is

$$R_{out} = r_o + (R_e \parallel r_\pi) + (R_e \parallel r_\pi)g_m r_o \quad (8.66)$$

which is very similar to the corresponding expression for the MOSFET case (Eq. 8.56) except that R_s is replaced by $(R_e \parallel r_\pi)$. The expression in Eq. (8.66) can be written in the alternate form

$$R_{out} = r_o + (1 + g_m r_o)(R_e \parallel r_\pi) \quad (8.67)$$

For $g_m r_o \gg 1$,

$$R_{out} \simeq r_o + (g_m r_o)(R_e \parallel r_\pi) \quad (8.68)$$

Thus, similar to the CG amplifier, the CB amplifier exhibits an impedance transformation property that raises the output resistance. Unlike the CG case, however, the output resistance of the CB circuit has an absolute maximum value obtained by setting $R_e = \infty$ as

$$R_{out}|_{\max} = r_o + g_m r_o r_\pi = (\beta + 1)r_o \quad (8.69)$$

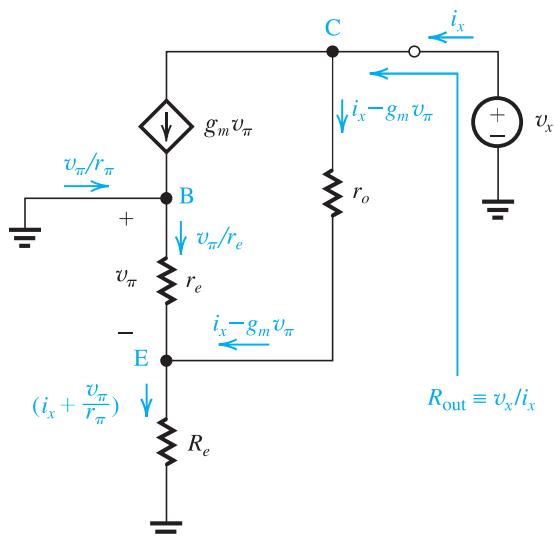


Figure 8.26 Determining the output resistance R_{out} of the CB amplifier.

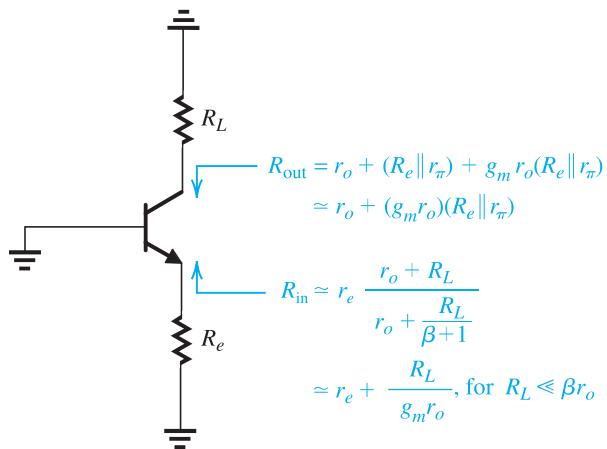


Figure 8.27 The impedance transformation properties of the CB amplifier. Note that for $\beta = \infty$, these formulas reduce to those for the MOSFET case (Fig. 8.21).

We conclude that the CB circuit has a current gain of nearly unity, a low input resistance, and a high output resistance; thus it makes for an excellent current buffer. The impedance transformation properties of the CB circuit are summarized in Fig. 8.27.

EXERCISES

- 8.14** For a CB amplifier, find approximate values for R_{in} for the following cases: $R_L = 0; r_o; (\beta + 1)r_o; \infty$.

Ans. $r_e; 2r_e; \frac{1}{2}r_\pi; r_\pi$

- 8.15** For a CB amplifier, find approximate values for R_{out} for the following cases: $R_e = 0; r_e; r_\pi; r_o; \infty$.

Ans. $r_o; 2r_o; (\frac{1}{2}\beta + 1)r_o; (\beta + 1)r_o; (\beta + 1)r_o$

8.4.5 Output Resistance of an Emitter-Degenerated CE Amplifier

As we have done in the MOS case, we shall adapt the expression for R_o derived for the CB amplifier (Eq. 8.68) for the case of a CE amplifier with a resistance R_e connected in its emitter, as shown in Fig. 8.28(a),

$$R_o \simeq r_o + g_m r_o (R_e \parallel r_\pi)$$

which can be written in the alternate form

➤ $R_o = [1 + g_m (R_e \parallel r_\pi)] r_o$ (8.70)

Thus, emitter degeneration multiplies the transistor output resistance r_o by the factor $[1 + g_m (R_e \parallel r_\pi)]$. Note that this factor has a maximum value of $(1 + g_m r_\pi)$ or $(\beta + 1)$, obtained when $R_e \gg r_\pi$. Thus the theoretical maximum output resistance realized is $(\beta + 1)r_o$ and is achieved when the emitter is open circuited.

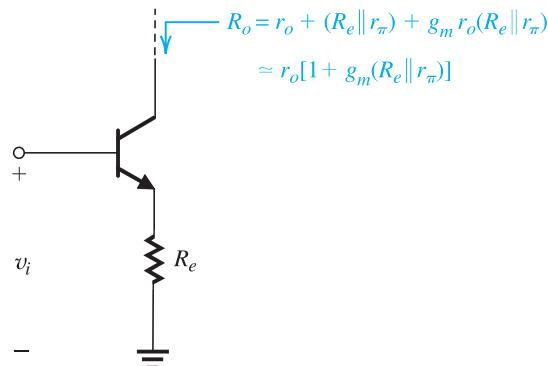


Figure 8.28 Output resistance of a CE amplifier with an emitter resistance R_e .

EXERCISE

- 8.16 Find the output resistance of a CE amplifier biased at $I_C = 1$ mA and having a resistance of 500Ω connected in its emitter. Let $\beta = 100$ and $V_A = 10$ V. What is the value of the output resistance without degeneration?

Ans. $177 \text{ k}\Omega$; $10 \text{ k}\Omega$

8.5 The Cascode Amplifier

8.5.1 Cascoding

Cascoding refers to the use of a transistor connected in the common-gate (or the common-base) configuration to provide **current buffering** for the output of a common-source (or a common-emitter) amplifying transistor. Figure 8.29 illustrates the technique for the MOS case. Here the CS transistor Q_1 is the amplifying transistor and Q_2 , connected in the CG

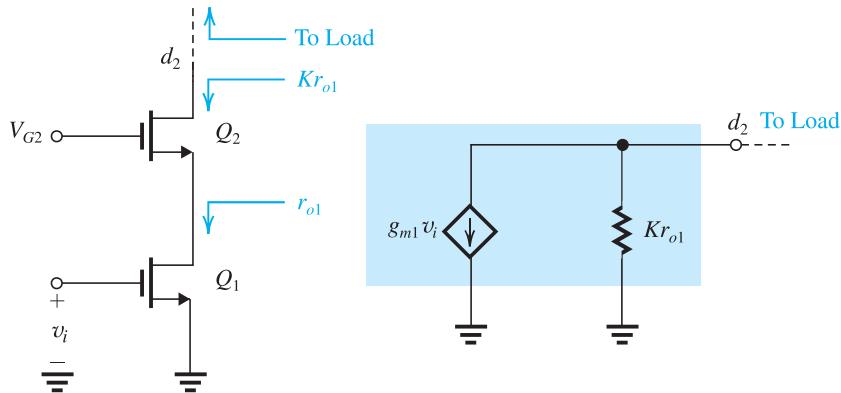


Figure 8.29 The current-buffering action of Fig. 8.17(b) is implemented using a transistor Q_2 connected in the CG configuration. Here V_{G2} is a dc bias voltage. The output equivalent circuit indicates that the CG transistor passes the current $g_{m1} v_i$ through but raises the resistance level by a factor K . Transistor Q_2 is called a cascode transistor.

configuration with a dc bias voltage V_{G2} (signal ground) at its gate, is the cascode transistor.² A similar arrangement applies for the bipolar case and will be considered later.

From our study of the CG amplifier characteristics, we can see that the cascode transistor passes the current $g_{m1} v_i$ to the output node while multiplying the resistance in its source (r_{o1} of Q_1) by a factor K . The result is the equivalent circuit of Fig. 8.29, which can be utilized to determine the voltage gain of the cascode amplifier for various load resistances. We shall consider the MOS cascode amplifier in detail next.

EXERCISE

8.17 Give an approximate value of the factor K of the circuit in Fig. 8.29.

Ans. $K \approx g_{m2} r_{o2}$

8.5.2 The MOS Cascode Amplifier

The Ideal Case Figure 8.30(a) shows a MOS cascode amplifier loaded with an ideal constant-current source. The voltage gain realized can be found from the equivalent circuit in Fig. 8.30(b). Since the load is an ideal constant-current source, the load resistance is infinite. That is, the amplifier is operating with an open-circuit load, and the gain is

$$A_{vo} \equiv \frac{v_o}{v_i} = -g_{m1} R_o \quad (8.71)$$

²The name *cascode* is a carryover from the days of vacuum tubes and is a shortened version of “cascaded cathode”; in the tube version, the anode of the amplifying tube (corresponding to the drain of Q_1) feeds the cathode of the cascode tube (corresponding to the source of Q_2).

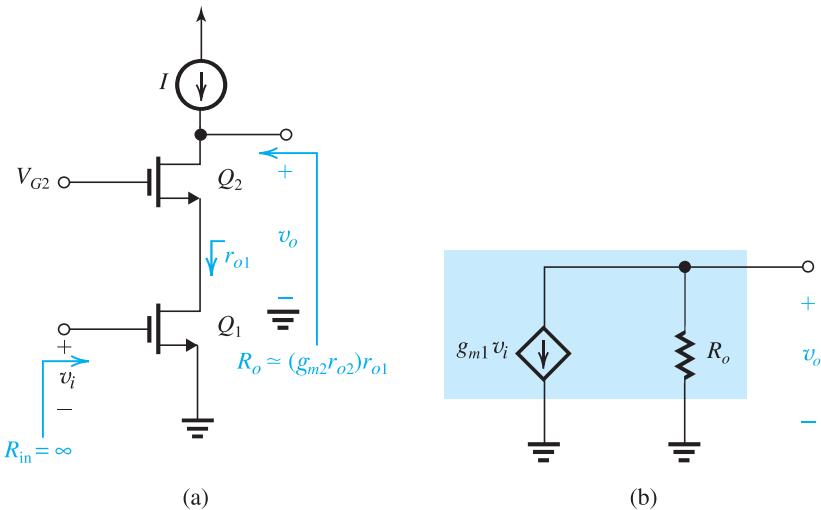


Figure 8.30 (a) A MOS cascode amplifier with an ideal current-source load; (b) equivalent circuit representation of the cascode output.

Now, since R_s of Q_2 is r_{o1} , the output resistance R_o is given by the approximate expression

$$R_o \simeq (g_{m2} r_{o2}) r_{o1} \quad (8.72)$$

Substituting in Eq. (8.71) results in

$$A_{vo} = -(g_{m1} r_{o1})(g_{m2} r_{o2}) \quad (8.73)$$

For the case $g_{m1} = g_{m2} = g_m$ and $r_{o1} = r_{o2} = r_o$,

$$\begin{aligned} A_{vo} &= -(g_m r_o)^2 \\ &= -A_0^2 \end{aligned} \quad (8.74)$$

Thus cascoding increases the gain magnitude from A_0 to A_0^2 .

Implementation of the Constant-Current Source Load If the current source load is implemented with a PMOS transistor (which can be part of a PMOS current mirror) as shown in Fig. 8.31(a), the load resistance R_L will be equal to the output resistance of Q_3 , r_{o3} ,

$$R_L = r_{o3}$$

and the voltage gain of the cascode amplifier will be

$$\begin{aligned} A_v &= -g_{m1}(R_o \parallel R_L) \\ &= -g_{m1}(g_{m2}r_{o2}r_{o1} \parallel r_{o3}) \end{aligned} \quad (8.75)$$

from which we can readily see that since $R_L \ll R_o$, the total resistance will be approximately equal to r_{o3} and the gain will be

$$A_v \simeq -g_{m1}r_{o3} \quad (8.76)$$

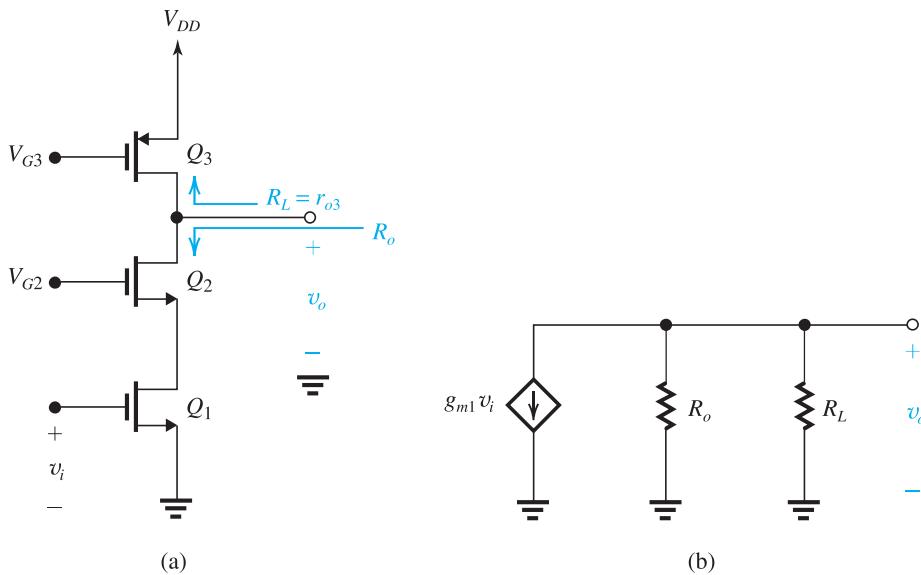


Figure 8.31 (a) A MOS cascode amplifier loaded in a simple PMOS current source Q_3 . (b) Equivalent circuit at the amplifier output.

Thus the gain magnitude will be back to A_0 , of the same order as that realized by a CS amplifier. In other words, the use of a simple current-source load with a relatively low output resistance has in effect destroyed the cascoding advantage of increased output resistance. Nevertheless, it turns out that this cascode amplifier, whose gain is of the same order as that of a CS amplifier, does in fact have a major advantage over the CS circuit: It exhibits a much wider bandwidth. We will demonstrate this point in Chapter 10.

The Use of a Cascode Current Source To realize a gain of the order of A_0^2 , the load resistance R_L must be of the same order as R_o of the cascode amplifier. This can be achieved by using a cascode current source such as that shown in Fig. 8.32. Here Q_4 is the current-source transistor, and Q_3 is the CG cascode transistor. Voltages V_{G4} and V_{G3} are dc bias voltages. The cascode transistor Q_3 multiplies the output resistance of Q_4 , r_{o4} by $(g_{m3}r_{o3})$ to provide an

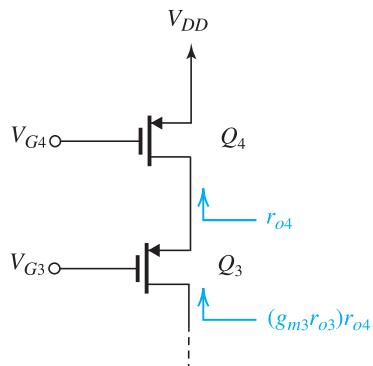


Figure 8.32 Employing a cascode transistor Q_3 to raise the output resistance of the current source Q_4 .

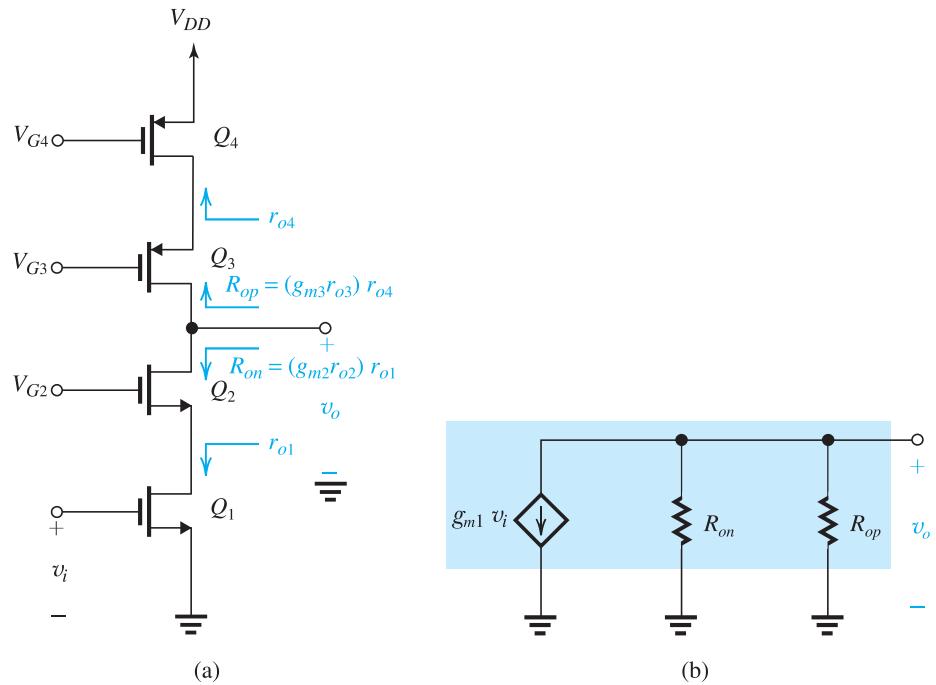


Figure 8.33 A cascode amplifier with a cascode current-source load.

output resistance for the cascode current source of

$$R_o = (g_{m3}r_{o3})r_{o4} \quad (8.77)$$

Combining a cascode amplifier with a cascode current source results in the circuit of Fig. 8.33(a). The equivalent circuit at the output side is shown in Fig. 8.33(b), from which the voltage gain can be easily found as

$$A_v = \frac{v_o}{v_i} = -g_{m1} [R_{on} \parallel R_{op}]$$

Thus,

$$\Rightarrow A_v = -g_{m1} \{ [(g_{m2}r_{o2})r_{o1}] \parallel [(g_{m3}r_{o3})r_{o4}] \} \quad (8.78)$$

For the case in which all transistors are identical,

$$\Rightarrow A_v = -\frac{1}{2}(g_m r_o)^2 = -\frac{1}{2}A_0^2 \quad (8.79)$$

By comparison to the gain expression in Eq. (8.50), we see that using the cascode configuration for both the amplifying transistor and the current-source load transistor results in an increase in the magnitude of gain by a factor equal to A_0 .

Example 8.5

It is required to design the cascode current source of Fig. 8.32 to provide a current of $100 \mu\text{A}$ and an output resistance of $500 \text{k}\Omega$. Assume the availability of a $0.18\text{-}\mu\text{m}$ CMOS technology for which $V_{DD} = 1.8 \text{ V}$, $V_{tp} = -0.5 \text{ V}$, $\mu_p C_{ox} = 90 \mu\text{A/V}^2$, and $V'_A = -5 \text{ V}/\mu\text{m}$. Use $|V_{ov}| = 0.3 \text{ V}$ and determine L and W/L for each transistor, and the values of the bias voltages V_{G3} and V_{G4} .

Solution

The output resistance R_o is given by

$$R_o = (g_m r_o) r_o$$

Assuming Q_3 and Q_4 are identical,

$$\begin{aligned} R_o &= (g_m r_o) r_o \\ &= \frac{|V_A|}{|V_{ov}|/2} \times \frac{|V_A|}{I_D} \end{aligned}$$

Using $|V_{ov}| = 0.3 \text{ V}$, we write

$$500 \text{k}\Omega = \frac{|V_A|}{0.15} \times \frac{|V_A|}{0.1 \text{ mA}}$$

Thus we require

$$|V_A| = 2.74 \text{ V}$$

Now, since $|V_A| = |V'_A| L$ we need to use a channel length of

$$L = \frac{2.74}{5} = 0.55 \mu\text{m}$$

which is about three times the minimum channel length. With $|V_t| = 0.5 \text{ V}$ and $|V_{ov}| = 0.3 \text{ V}$,

$$V_{SG4} = 0.5 + 0.3 = 0.8 \text{ V}$$

and thus,

$$V_{G4} = 1.8 - 0.8 = 1.0 \text{ V}$$

To allow for the largest possible signal swing at the output terminal, we shall use the minimum required voltage across Q_4 , namely, $|V_{ov}|$ or 0.3 V . Thus,

$$V_{D4} = 1.8 - 0.3 = 1.5 \text{ V}$$

Since the two transistors are identical and are carrying equal currents,

$$V_{SG3} = V_{SG4} = 0.8 \text{ V}$$

Thus,

$$V_{G3} = 1.5 - 0.8 = +0.7 \text{ V}$$

Example 8.5 *continued*

We note that the maximum voltage allowed at the output terminal of the current source will be constrained by the need to allow a minimum voltage of $|V_{ov}|$ across Q_3 ; thus;

$$v_{D3\max} = 1.5 - 0.3 = +1.2 \text{ V}$$

To determine the required W/L ratios of Q_3 and Q_4 , we use

$$\begin{aligned} I_D &= \frac{1}{2}(\mu_p C_{ox}) \left(\frac{W}{L} \right) |V_{ov}|^2 \left(1 + \frac{V_{SD}}{|V_A|} \right) \\ 100 &= \frac{1}{2} \times 90 \times \left(\frac{W}{L} \right) \times 0.3^2 \left(1 + \frac{0.3}{2.74} \right) \end{aligned}$$

which yields

$$\frac{W}{L} = 22.3$$

EXERCISES

- D8.18** If in Example 8.5, L of each of Q_3 and Q_4 is halved while W/L is changed to allow I_D and V_{ov} to remain unchanged, find the new values of R_o and W/L . [Hint: In computing the required (W/L), note that $|V_A|$ has changed.]

Ans. 125 kΩ; 20.3

- 8.19** Consider the cascode amplifier of Fig. 8.33 with the dc component at the input, $V_i = 0.7 \text{ V}$, $V_{G2} = 1.0 \text{ V}$, $V_{G3} = 0.8 \text{ V}$, $V_{G4} = 1.1 \text{ V}$, and $V_{DD} = 1.8 \text{ V}$. If all devices are matched (i.e., if $k_{n1} = k_{n2} = k_{p3} = k_{p4}$), and have equal $|V_t|$ of 0.5 V, what is the overdrive voltage at which the four transistors are operating? What is the allowable voltage range at the output?

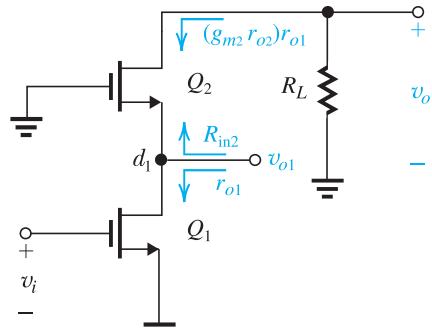
Ans. 0.2 V; 0.5 V to 1.3 V

- 8.20** The cascode amplifier in Fig. 8.33 is operated at a current of 0.2 mA with all devices operating at $|V_{ov}| = 0.2 \text{ V}$. All devices have $|V_A| = 2 \text{ V}$. Find g_{m1} , the output resistance of the amplifier, R_{on} , and the output resistance of the current source, R_{op} . Also find the overall output resistance and the voltage gain realized.

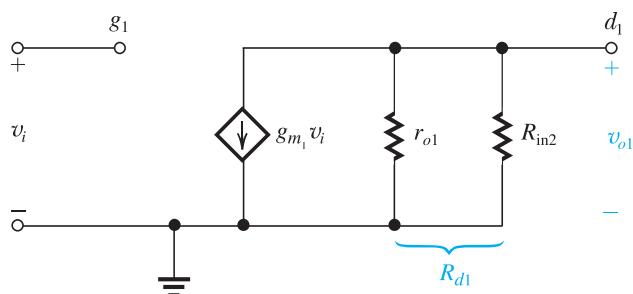
Ans. 2 mA/V; 200 kΩ, 200 kΩ; 100 kΩ; -200 V/V

8.5.3 Distribution of Voltage Gain in a Cascode Amplifier

It is often useful to know how much of the overall voltage gain of a cascode amplifier is realized in each of its two stages: the CS stage Q_1 , and the CG stage Q_2 . For this purpose, consider the cascode amplifier shown in Fig. 8.34(a). Here, for generality we have included



(a)



(b)

Figure 8.34 (a) The cascode amplifier with a load resistance R_L . Only signal quantities are shown. (b) Determining v_{o1} .

a load resistance R_L , which represents the output resistance of the current-source load plus any additional resistance that may be connected to the output node. The voltage gain A_v of the amplifier can be found as

$$A_v = -g_{m1}(R_o \parallel R_L)$$

Thus,

$$A_v = -g_{m1}(g_{m2}r_{o2}r_{o1} \parallel R_L) \quad (8.80)$$

The overall gain A_v can be expressed as the product of the voltage gains of Q_1 and Q_2 as

$$A_v = A_{v1}A_{v2} = \left(\frac{v_{o1}}{v_i}\right)\left(\frac{v_o}{v_{o1}}\right) \quad (8.81)$$

To obtain $A_{v1} \equiv v_{o1}/v_i$ we need to find the total resistance between the drain of Q_1 and ground. Referring to Fig. 8.34(b) and denoting this resistance R_{d1} , we can express A_{v1} as

$$A_{v1} = \frac{v_{o1}}{v_i} = -g_{m1}R_{d1} \quad (8.82)$$

Observe that R_{d1} is the parallel equivalent of r_{o1} and R_{in2} , where R_{in2} is the input resistance of the CG transistor Q_2 . From Eq. (8.54), we can write

$$R_{in2} \simeq \frac{R_L}{g_{m2}r_{o2}} + \frac{1}{g_{m2}} \quad (8.83)$$

Table 8.1 Gain Distribution in the MOS Cascode Amplifier for Various Values of R_L

Case	R_L	R_{in2}	R_{d1}	A_{v1}	A_{v2}	A_v
1	∞	∞	r_o	$-g_m r_o$	$g_m r_o$	$-(g_m r_o)^2$
2	$(g_m r_o) r_o$	r_o	$r_o/2$	$-\frac{1}{2}(g_m r_o)$	$g_m r_o$	$-\frac{1}{2}(g_m r_o)^2$
3	r_o	$\frac{2}{g_m}$	$\frac{2}{g_m}$	-2	$\frac{1}{2}(g_m r_o)$	$-(g_m r_o)$
4	0	$\frac{1}{g_m}$	$\frac{1}{g_m}$	-1	0	0

Now we can obtain R_{d1} as

$$R_{d1} = r_{o1} \parallel R_{in2} \quad (8.84)$$

and A_{v1} as

$$A_{v1} = -g_{m1} R_{d1} = -g_{m1} (r_{o1} \parallel R_{in2}) \quad (8.85)$$

Finally, we can obtain A_{v2} by dividing the total gain A_v given by Eq. (8.80) by A_{v1} . To provide insight into the effect of the value of R_L on the overall gain of the cascode as well as on how this gain is distributed among the two stages of the cascode amplifier, we provide in Table 8.1 approximate values for the case $r_{o1} = r_{o2} = r_o$ and for four different values of R_L : (1) $R_L = \infty$, obtained with an ideal current-source load; (2) $R_L = (g_m r_o) r_o$, obtained with a cascode current-source load; (3) $R_L = r_o$, obtained with a simple current-source load; and (4) for completeness, $R_L = 0$, that is, a signal short circuit at the output.

Observe that while case 1 represents an idealized situation, it is useful in that it provides the theoretical maximum voltage gain achievable in a MOS cascode amplifier. Case 2, which assumes a cascode current-source load with an output resistance equal to that of the cascode amplifier, provides a realistic estimate of the gain achieved if one aims to maximize the realized gain. In certain situations, however, that is not our objective. This point is important, for as we shall see in Chapter 10, there is an entirely different application of the cascode amplifier: namely, to obtain wideband amplification by extending the upper-3-dB frequency f_H . As will be seen, for such an application one opts for the situation represented by case 3, where the gain achieved in the CS amplifier is only -2 V/V, and of course the overall gain is now only $-(g_m r_o)$. However, as will be seen in Chapter 10, this trade-off of the overall gain to obtain extended bandwidth is in some cases a good bargain!

EXERCISE

- 8.21** Consider a cascode amplifier for which the CS and CG transistors are identical and are biased to operate at $I_D = 0.1$ mA with $V_{ov} = 0.2$ V. Also let $V_A = 2$ V. Find A_{v1} , A_{v2} , and A_v for two cases: (a) $R_L = 20$ k Ω and (b) $R_L = 400$ k Ω .

Ans. (a) -1.82 V/V, 10.5 V/V, -19.0 V/V; (b) -10.2 V/V, 19.6 V/V, -200 V/V

8.5.4 Double Cascoding

If a still higher output resistance and correspondingly higher gain are required, it is possible to add another level of cascoding, as illustrated in Fig. 8.35. Observe that Q_3 is the second cascode transistor, and it raises the output resistance by $(g_{m3}r_{o3})$. For the case of identical transistors, the output resistance will be $(g_m r_o)^2 r_o$ and the voltage gain, assuming an ideal current-source load, will be $(g_m r_o)^3$ or A_0^3 . Of course, we have to generate another dc bias voltage for the second cascode transistor, Q_3 .

A drawback of double cascoding is that an additional transistor is now stacked between the power-supply rails. Furthermore, to realize the advantage of double cascoding, the current-source load will also need to use double cascoding with an additional transistor. Since for proper operation each transistor needs a certain minimum v_{DS} (at least equal to V_{OV}), and recalling that modern MOS technology utilizes power supplies in the range of 1 V to 2 V, we see that there is a limit on the number of transistors in a cascode stack.

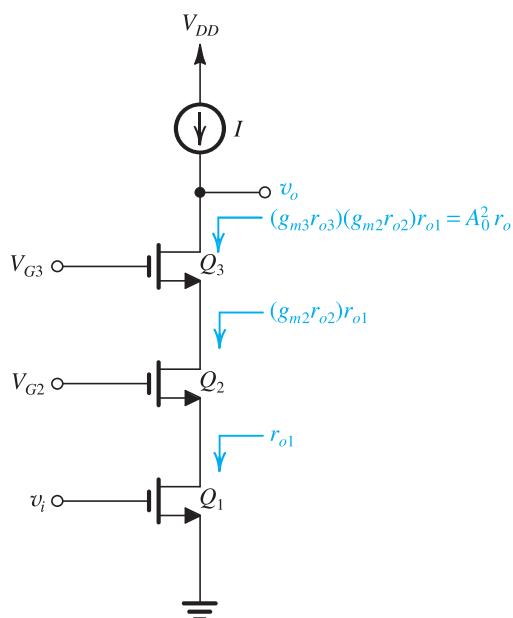


Figure 8.35 Double cascoding.

8.5.5 The Folded Cascode

To avoid the problem of stacking a large number of transistors across a low-voltage power supply, one can use a PMOS transistor for the cascode device, as shown in Fig. 8.36. Here, as before, the NMOS transistor Q_1 is operating in the CS configuration, but the CG stage is implemented using the PMOS transistor Q_2 . An additional current source I_2 is needed to bias Q_2 and provide it with its active load. Note that Q_1 is now operating at a bias current of $(I_1 - I_2)$. Finally, a dc voltage V_{G2} is needed to provide an appropriate dc level for the gate of the cascode transistor Q_2 . Its value has to be selected so that Q_2 and Q_1 operate in the saturation region.

The small-signal operation of the circuit in Fig. 8.36 is similar to that of the NMOS cascode. The difference here is that the signal current $g_m v_i$ is *folded down* and made to flow

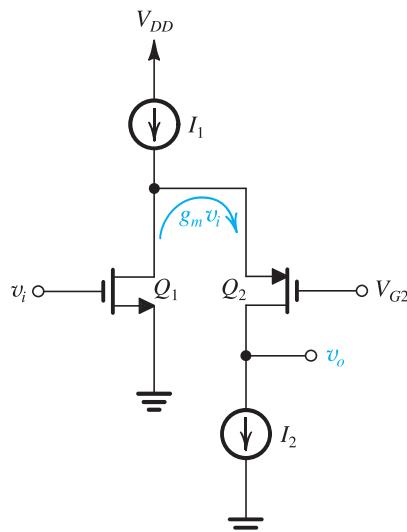


Figure 8.36 The folded cascode.

into the source terminal of Q_2 , which gives the circuit the name **folded cascode**.³ The folded cascode is a very popular building block in CMOS amplifiers.

EXERCISE

D8.22 Consider the folded-cascode amplifier of Fig. 8.36 for the following case: $V_{DD} = 1.8$ V, $k'_n = 4k'_p$, and $V_{tn} = -V_{tp} = 0.5$ V. To operate Q_1 and Q_2 at equal bias currents I , $I_1 = 2I$ and $I_2 = I$. While current source I_1 is implemented using the simple circuit studied in Section 8.2, current source I_2 is realized using a cascaded circuit (i.e., the NMOS version of the circuit in Fig. 8.32). The transistor W/L ratios are selected so that each operates at an overdrive voltage of 0.2 V.

- What must the relationship of $(W/L)_2$ to $(W/L)_1$ be?
- What is the minimum dc voltage required across current source I_1 for proper operation? Now, if a 0.1-V peak-to-peak signal swing is to be allowed at the drain of Q_1 , what is the highest dc bias voltage that can be used at that node?
- What is the value of V_{SG} of Q_2 , and hence what is the largest value to which V_{G2} can be set?
- What is the minimum dc voltage required across current-source I_2 for proper operation?
- Given the results of (c) and (d), what is the allowable range of signal swing at the output?

Ans. (a) $(W/L)_2 = 4(W/L)_1$; (b) 0.2 V, 1.55 V; (c) 0.7 V, 0.85 V; (d) 0.4 V; (e) 0.4 V to 1.35 V

³The circuit itself can be thought of as having been folded. In this same vein, the regular cascode is sometimes referred to as a **telescopic cascode** because the stacking of transistors resembles the extension of a telescope.

8.5.6 The BJT Cascode

Figure 8.37(a) shows the BJT cascode amplifier with an ideal current-source load. Voltage V_{B2} is a dc bias voltage for the CB cascode transistor Q_2 . The circuit is very similar to the MOS cascode, and the small-signal analysis will follow in a parallel fashion. First, note that the input resistance of the bipolar cascode amplifier is finite,

$$R_{in} = r_{\pi 1} \quad (8.86)$$

Second, recall that the current signal in the collector of Q_2 will be approximately equal to $g_{m1} v_i$. Thus, the equivalent circuit of the output of the cascode amplifier will be that shown in Fig. 8.37(b). To obtain R_o we use the formula in Eq. (8.68) and note that the resistance R_e in the emitter of Q_2 is r_{o1} , thus

$$R_o \simeq r_{o2} + (g_{m2} r_{o2})(r_{o1} \parallel r_{\pi 2}) \quad (8.87)$$

Since $g_{m2}(r_{o1} \parallel r_{\pi 2}) \gg 1$, we can neglect the first term on the right-hand side of Eq. (8.87),

$$R_o \simeq (g_{m2} r_{o2})(r_{o1} \parallel r_{\pi 2}) \quad (8.88)$$

This result is similar but certainly *not identical* to that for the MOS cascode. Here, because of the finite β of the BJT, we have $r_{\pi 2}$ appearing in parallel with r_{o1} . This poses a very significant constraint on R_o of the BJT cascode. Specifically, because $(r_{o1} \parallel r_{\pi 2})$ will always be lower than $r_{\pi 2}$, it follows that the maximum possible value of R_o is

$$\begin{aligned} R_o|_{max} &= g_{m2} r_{o2} r_{\pi 2} \\ &= (g_{m2} r_{\pi 2}) r_{o2} = \beta_2 r_{o2} \end{aligned} \quad (8.89)$$

Thus the maximum output resistance realizable by cascoding is $\beta_2 r_{o2}$. This means that unlike the MOS case, double cascading with a BJT would not be useful.

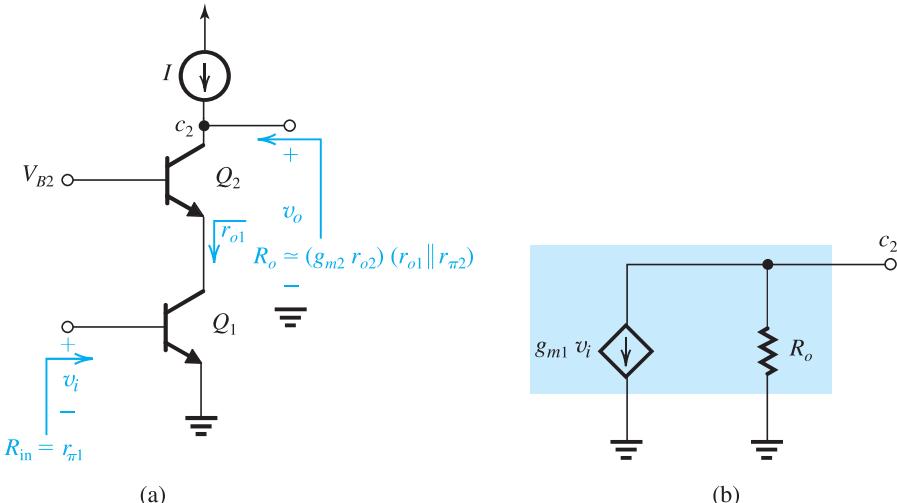


Figure 8.37 (a) A BJT cascode amplifier with an ideal current-source load; (b) small-signal, equivalent-circuit representation of the output of the cascode amplifier.

The open-circuit voltage gain of the bipolar cascode can be found using the equivalent circuit of Fig. 8.37(b) as

$$A_{vo} = \frac{v_o}{v_i} = -g_{m1}R_o$$

Thus,

$$A_{vo} = -g_{m1}(g_{m2}r_{o2})(r_{o1} \parallel r_{\pi2}) \quad (8.90)$$

For the case $g_{m1} = g_{m2}$, $r_{o1} = r_{o2}$,

➤

$$A_{vo} = -(g_m r_o)[g_m(r_o \parallel r_\pi)] \quad (8.91)$$

which will be less than $(g_m r_o)^2$ in magnitude. In fact, the maximum possible gain magnitude is obtained when $r_o \gg r_\pi$ and is given by

➤

$$|A_{vo}|_{\max} = \beta g_m r_o = \beta A_0 \quad (8.92)$$

Finally, we note that to be able to realize gains approaching this level, the current-source load must also be cascaded. Figure 8.38 shows a cascode BJT amplifier with a cascode current-source load.

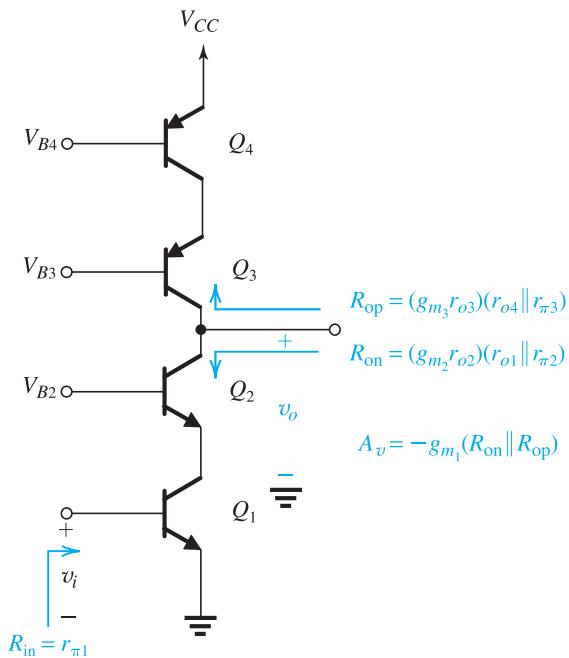


Figure 8.38 A BJT cascode amplifier with a cascode current source.

EXERCISES

- 8.23** Find an expression for the maximum voltage gain achieved in the amplifier of Fig. 8.38.

Ans. $|A_{vmax}| = g_{m1}(\beta_2 r_{o2} \parallel \beta_3 r_{o3})$

- 8.24** Consider the BJT cascode amplifier of Fig. 8.38 when biased at a current of 0.2 mA. Assuming that *npn* transistors have $\beta = 100$ and $V_A = 5$ V and that *pnp* transistors have $\beta = 50$ and $|V_A| = 4$ V, find R_{on} , R_{op} , and A_v . Also use the result of Exercise 8.23 to determine the maximum achievable gain.

Ans. 1.67 M Ω ; 0.762 M Ω ; -4186 V/V; -5714 V/V

8.6 Current-Mirror Circuits with Improved Performance

A

As we have seen throughout this chapter, current sources play a major role in the design of IC amplifiers: The constant-current source is used both in biasing and as active load. Simple forms of both MOS and bipolar current sources and, more generally, current mirrors were studied in Section 8.2. The need to improve the characteristics of the simple sources and mirrors has already been demonstrated.

Specifically, three performance parameters need to be addressed:

1. The accuracy of the current transfer ratio of the mirror. For bipolar mirrors, this parameter is primarily affected by the transistor β . For both bipolar and MOS mirrors, the Early effect affects the current transfer ratio.
2. The output resistance, R_o . The need to increase the output resistance of current sources is motivated by the need to increase the voltage gain achievable in an amplifier stage. While simple bipolar and MOS mirrors have output resistances equal to r_o , cascoding can be used to increase the output resistance.
3. The minimum dc voltage required across the current source. The need to keep this voltage as small as possible stems from the low dc voltage supplies employed in modern IC technologies. Simple BJT and MOS sources can operate with dc voltages in the range of 0.2 V to 0.3 V. More elaborate mirror circuits usually require higher voltages.

In this section we study MOS and bipolar current mirrors that feature improvements in one or more of these characteristics.

8.6.1 Cascode MOS Mirrors

The use of cascoding in the design of current sources was presented in Section 8.5. Figure 8.39 shows the basic cascode current mirror. Observe that in addition to the diode-connected transistor Q_1 , which forms the basic mirror Q_1-Q_2 , another diode-connected transistor, Q_4 , is used to provide a suitable bias voltage for the gate of the cascode transistor Q_3 . To determine the output resistance of the cascode mirror at the drain of Q_3 , we assume that the voltages

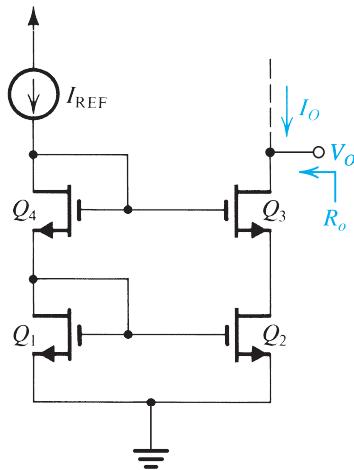


Figure 8.39 A cascode MOS current mirror.

across Q_1 and Q_4 are constant, and thus the signal voltages at the gates of Q_2 and Q_3 will be zero. Thus R_o will be that of the cascode current source formed by Q_2 and Q_3 ,

$$R_o \simeq g_{m3}r_{o3}r_{o2} \quad (8.93)$$

Thus, as expected, cascoding raises the output resistance of the current source by the factor ($g_{m3}r_{o3}$), which is the intrinsic gain of the cascode transistor.

A drawback of the cascode current mirror is that it consumes a relatively large portion of the steadily shrinking supply voltage V_{DD} . While the simple MOS mirror operates properly with a voltage as low as V_{OV} across its output transistor, the cascode circuit of Fig. 8.39 requires a minimum voltage of $V_t + 2V_{OV}$. This is because the gate of Q_3 is at $2V_{GS} = 2V_t + 2V_{OV}$. Thus the minimum voltage required across the output of the cascode mirror is 1 V or so. This obviously limits the signal swing at the output of the mirror (i.e., at the output of the amplifier that utilizes this current source as a load). In Chapter 13 we shall study a wide-swing cascode mirror.

EXERCISE

- 8.25 For a cascode MOS mirror utilizing devices with $V_t = 0.5$ V, $\mu_nC_{ox} = 387 \mu\text{A/V}^2$, $V_A' = 5 \text{ V}/\mu\text{m}$, $W/L = 3.6 \mu\text{m}/0.36 \mu\text{m}$, and $I_{REF} = 100 \mu\text{A}$, find the minimum voltage required at the output and the output resistance.

Ans. 0.95 V; 285 kΩ

8.6.2 The Wilson Current Mirror

A simple but ingenious modification of the basic bipolar mirror results in both reducing the β dependence and increasing the output resistance. The resulting circuit, known as the **Wilson mirror** after its inventor George Wilson, an IC design engineer working for Tektronix, is shown in Fig. 8.40(a). The analysis to determine the effect of finite β on the current transfer

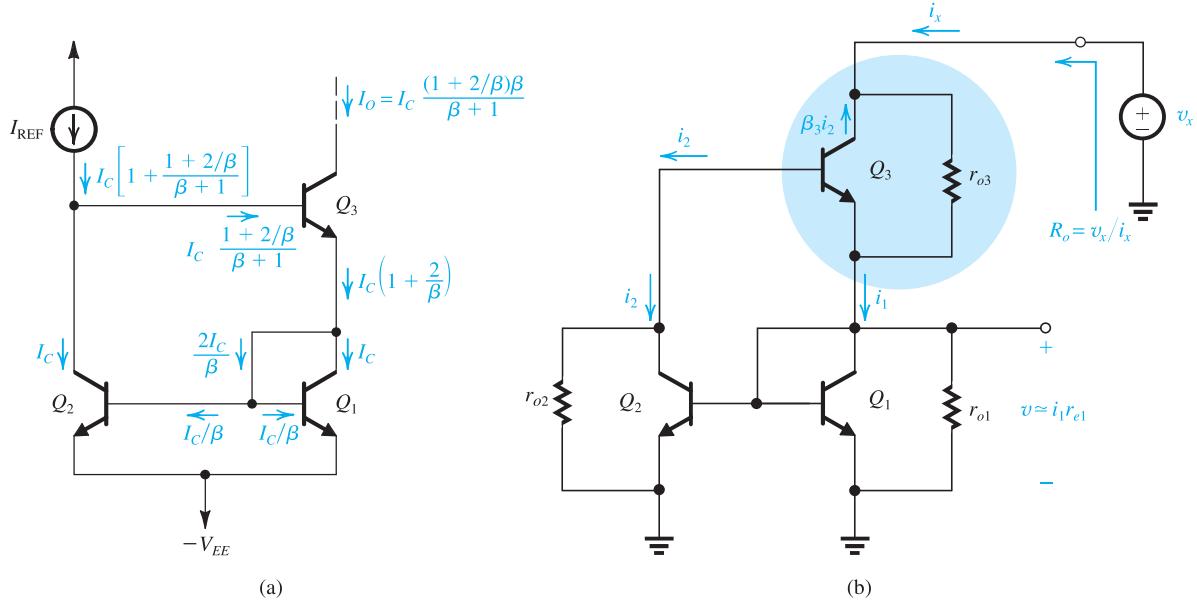


Figure 8.40 The Wilson bipolar current mirror: (a) circuit showing analysis to determine the current transfer ratio; (b) determining the output resistance.

ratio is shown in Fig. 8.40(a), from which we can write

$$\begin{aligned}
 \frac{I_o}{I_{\text{REF}}} &= \frac{I_c \left(1 + \frac{2}{\beta}\right) \beta / (\beta + 1)}{I_c \left[1 + \left(1 + \frac{2}{\beta}\right) / (\beta + 1)\right]} \\
 &= \frac{\beta + 2}{\beta + 1 + \frac{\beta + 2}{\beta}} = \frac{\beta + 2}{\beta + 2 + \frac{2}{\beta}} \\
 &= \frac{1}{1 + \frac{2}{\beta(\beta + 2)}} \\
 &\simeq \frac{1}{1 + 2/\beta^2} \tag{8.94}
 \end{aligned}$$

which is much less dependent on β than in the case of the simple current mirror.

This analysis assumes that Q_1 and Q_2 conduct equal collector currents. There is, however, a slight problem with this assumption: The collector-to-emitter voltages of Q_1 and Q_2 are not equal, which introduces a current offset or a systematic error. The problem can be solved by adding a diode-connected transistor in series with the collector of Q_2 , as we shall shortly show for the MOS version.

To determine the output resistance of the Wilson mirror, we set $I_{\text{REF}} = 0$ and apply a test voltage v_x to the output node, as shown in Fig. 8.40(b). Our purpose is to determine the current i_x and hence R_o as

$$R_o = v_x / i_x$$

Rather than replacing each transistor with its hybrid- π model, we shall do the analysis directly on the circuit diagram. For this purpose, we have “pulled r_o out” of each transistor and shown it separately.

Observe that transistor Q_3 , viewed as a supernode (highlighted in color), has a current i_x entering it and two currents i_1 and i_2 exiting it; thus,

$$i_1 + i_2 = i_x$$

Next note that the action of current mirror Q_1-Q_2 forces i_2 to be approximately equal to i_1 ; thus,

$$i_2 \simeq i_1 = i_x/2$$

Current i_2 flows into the base of Q_3 and thus gives rise to a collector current $\beta_3 i_2$ in the direction indicated. We are now in a position to write a node equation at the collector of Q_3 and thus determine the current through r_{o3} as $i_x + \beta_3 i_2 = i_x + \beta_3(i_x/2) = i_x(\beta_3/2 + 1)$. Finally, we can express the voltage between the collector of Q_3 and ground as the sum of the voltage drop across r_{o3} and the voltage v across Q_1 ,

$$\begin{aligned} v_x &= i_x \left(\frac{\beta_3}{2} + 1 \right) r_{o3} + i_1 r_{e1} \\ &= i_x \left(\frac{\beta_3}{2} + 1 \right) r_{o3} + \left(\frac{i_x}{2} \right) r_{e1} \end{aligned}$$

Since $r_o \gg r_e$ and $\beta_3 \gg 2$

$$v_x \simeq i_x \left(\frac{\beta_3}{2} \right) r_{o3}$$

and

➤ $R_o = \beta_3 r_{o3}/2$ (8.95)

Thus the Wilson current mirror has an output resistance ($\frac{1}{2}\beta_3$) times higher than that of Q_3 alone. This is a result of the negative feedback obtained by feeding the collector current of Q_2 (i_2) back to the base of Q_3 . As can be seen from the above analysis, this feedback results in increasing the current through r_{o3} to approximately $\frac{1}{2}\beta_3 i_x$, and thus the voltage across r_{o3} and the output resistance increase by the same factor, $\frac{1}{2}\beta_3$. Finally, note that the factor $\frac{1}{2}$ is because only half of i_x is mirrored back to the base of Q_3 .

The Wilson mirror is preferred over the cascode circuit because the latter has the same dependence on β as the simple mirror. However, like the cascode mirror, the Wilson mirror requires an additional V_{BE} drop for its operation; that is, for proper operation we must allow for 1 V or so across the Wilson mirror output.

EXERCISE

- 8.26** For $\beta = 100$ and $r_o = 100 \text{ k}\Omega$, contrast the Wilson mirror and the simple mirror by evaluating the transfer-ratio error due to finite β , and the output resistance.

Ans. Transfer-ratio error: 0.02% for Wilson as opposed to 2% for the simple circuit; $R_o = 5 \text{ M}\Omega$ for Wilson compared to $100 \text{ k}\Omega$ for the simple circuit

8.6.3 The Wilson MOS Mirror

Figure 8.41(a) shows the MOS version of the Wilson mirror. Obviously there is no β error to reduce here, and the advantage of the MOS Wilson lies in its enhanced output resistance.

To determine the output resistance of the Wilson MOS mirror, we set $I_{\text{REF}} = 0$, and apply a test voltage v_x to the output node, as shown in Fig. 8.41(b). Our purpose is to determine the current i_x and hence R_o as

$$R_o = v_x/i_x$$

Rather than replacing each transistor with its hybrid- π equivalent-circuit model, we shall perform the analysis directly on the circuit. For this purpose, we have “pulled r_o out” of each transistor and shown it separately.

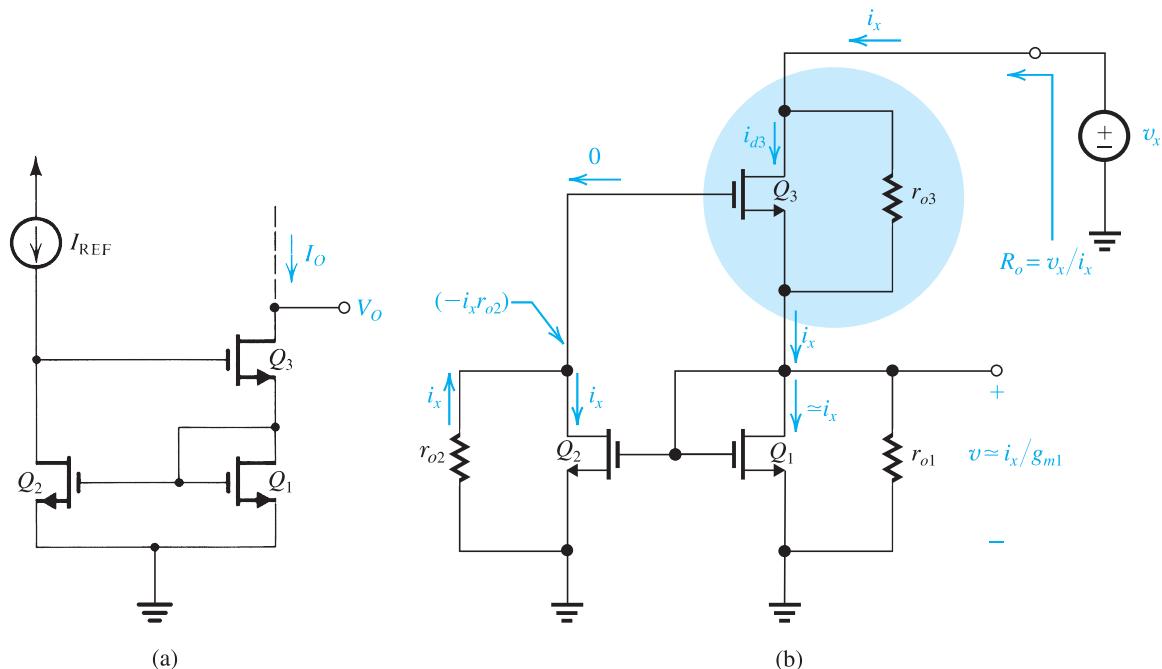
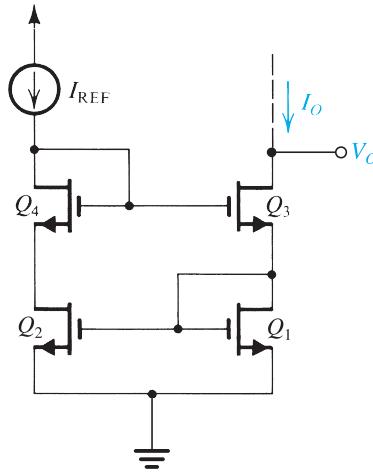


Figure 8.41 The Wilson MOS mirror: (a) circuit; (b) analysis to determine output resistance; (c) modified circuit.



(c)

Figure 8.41 continued

Observe that the current i_x that enters the drain of Q_3 must exit at its source. Thus the current that feeds the input side of the Q_1-Q_2 mirror is equal to i_x . Most of this current will flow in the drain proper of Q_1 (i.e., only a very small fraction flows through r_{o1}) and will give rise to a voltage $v \simeq i_x/g_{m1}$, where $1/g_{m1}$ is the approximate resistance of the diode-connected transistor Q_1 . The current-mirror action of (Q_1, Q_2) forces a current equal to i_x to flow through the drain proper of Q_2 . Now, since the current in the drain of Q_2 is forced (by the connection to the gate of Q_3) to be zero, all of i_x must flow through r_{o2} , resulting in a voltage $-i_x r_{o2}$. This is the voltage fed back to the gate of Q_3 . The drain current of Q_3 can now be found as

$$\begin{aligned} i_{d3} &= g_{m3} v_{gs3} \\ &= g_{m3} (v_{g3} - v_{s3}) \\ &= g_{m3} (-i_x r_{o2} - i_x/g_{m1}) \\ &\simeq -g_{m3} r_{o2} i_x \end{aligned}$$

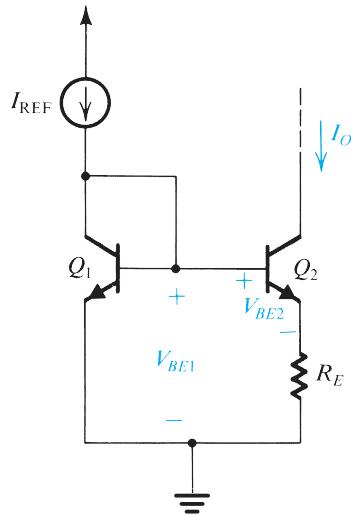
A node equation at the drain of Q_3 gives the current through r_{o3} as $(i_x - i_{d3}) = i_x + g_{m3} r_{o2} i_x \simeq g_{m3} r_{o2} i_x$. Finally, we can express v_x as the sum of the voltage drop across r_{o3} and the voltage v across Q_1 ,

$$\begin{aligned} v_x &= g_{m3} r_{o2} i_x r_{o3} + v \\ &= (g_{m3} r_{o3} r_{o2}) i_x + (i_x/g_{m1}) \\ &\simeq g_{m3} r_{o3} r_{o2} i_x \end{aligned}$$

and obtain

$$R_o = \frac{v_x}{i_x} = (g_{m3} r_{o3}) r_{o2} \quad (8.96)$$

Thus, the Wilson MOS mirror exhibits an increase of output resistance by a factor $(g_{m3} r_{o3})$, an identical result to that achieved in the cascode mirror. Here the increase in R_o , as demonstrated in the analysis above, is a result of the negative feedback obtained by connecting the drain of Q_2 to the gate of Q_3 . Finally, to balance the two branches of the mirror and thus avoid the systematic current error resulting from the difference in V_{DS} between Q_1 and Q_2 , the circuit can be modified as shown in Fig. 8.41(c).

**Figure 8.42** The Widlar current source.

8.6.4 The Widlar Current Source⁴

Our final current-source circuit, known as the **Widlar current source**, is shown in Fig. 8.42. It differs from the basic current-mirror circuit in an important way: A resistor R_E is included in the emitter lead of Q_2 . Neglecting base currents we can write

$$V_{BE1} = V_T \ln\left(\frac{I_{REF}}{I_S}\right) \quad (8.97)$$

and

$$V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right) \quad (8.98)$$

where we have assumed that Q_1 and Q_2 are matched devices. Combining Eqs. (8.97) and (8.98) gives

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{REF}}{I_O}\right) \quad (8.99)$$

But from the circuit we see that

$$V_{BE1} = V_{BE2} + I_O R_E \quad (8.100)$$

Thus,

$$I_O R_E = V_T \ln\left(\frac{I_{REF}}{I_O}\right) \quad (8.101) \quad \blacktriangleleft$$

The design and advantages of the Widlar current source are illustrated in the following example.

⁴Named after Robert Widlar, a pioneer in analog IC design.

Example 8.6

The two circuits for generating a constant current $I_o = 10 \mu\text{A}$ shown in Fig. 8.43 operate from a 10-V supply. Determine the values of the required resistors, assuming that V_{BE} is 0.7 V at a current of 1 mA and neglecting the effect of finite β .

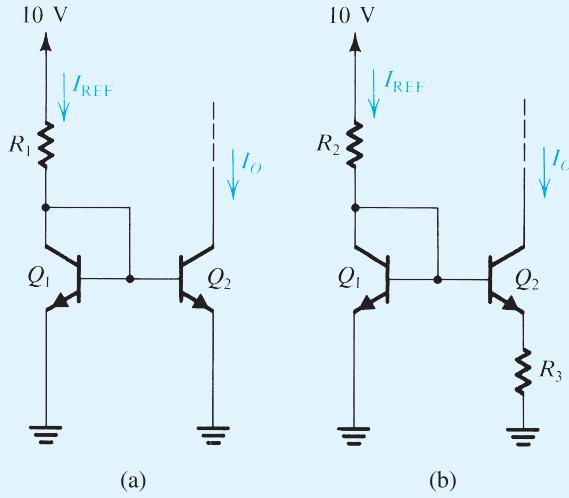


Figure 8.43 Circuits for Example 8.6.

Solution

For the basic current-source circuit in Fig. 8.43(a) we choose a value for R_1 to result in $I_{\text{REF}} = 10 \mu\text{A}$. At this current, the voltage drop across Q_1 will be

$$V_{BE1} = 0.7 + V_T \ln\left(\frac{10 \mu\text{A}}{1 \text{mA}}\right) = 0.58 \text{ V}$$

Thus,

$$R_1 = \frac{10 - 0.58}{0.01} = 942 \text{ k}\Omega$$

For the Widlar circuit in Fig. 8.43(b) we must first decide on a suitable value for I_{REF} . If we select $I_{\text{REF}} = 1 \text{ mA}$, then $V_{BE1} = 0.7 \text{ V}$ and R_2 is given by

$$R_2 = \frac{10 - 0.7}{1} = 9.3 \text{ k}\Omega$$

The value of R_3 can be determined using Eq. (8.101) as follows:

$$10 \times 10^{-6} R_3 = 0.025 \ln\left(\frac{1 \text{ mA}}{10 \mu\text{A}}\right)$$

$$R_3 = 11.5 \text{ k}\Omega$$

From the above example we observe that using the Widlar circuit allows the generation of a small constant current using relatively small resistors. This is an important advantage that results in considerable savings in chip area. In fact the circuit of Fig. 8.43(a), requiring a 942-k Ω resistance, is totally impractical for implementation in IC form because of the very high value of resistor R_1 .

Another important characteristic of the Widlar current source is that its output resistance is high. The increase in the output resistance, above that achieved in the basic current source, is due to the emitter-degeneration resistance R_E . To determine the output resistance of Q_2 , we assume that since the base of Q_2 is connected to ground via the small resistance r_e of Q_1 , the incremental voltage at the base will be small. Thus we can use the formula in Eq. (8.70) and adapt it for our purposes here as follows:

$$R_{\text{out}} \simeq [1 + g_m(R_E \parallel r_\pi)]r_o \quad (8.102)$$



Thus the output resistance is increased above r_o by a factor that can be significant.

EXERCISE

- 8.27** Find the output resistance of each of the two current sources designed in Example 8.6. Let $V_A = 100$ V and $\beta = 100$.

Ans. 10 M Ω ; 54 M Ω



8.7 Some Useful Transistor Pairings

The cascode configuration studied in Section 8.5 combines CS and CG MOS transistors (CE and CB bipolar transistors) to great advantage. The key to the superior performance of the resulting combination is that the transistor pairing is done in a way that maximizes the advantages and minimizes the shortcomings of each of the two individual configurations. In this section we present a number of other such transistor pairings. In each case the transistor pair can be thought of as a compound device; thus the resulting amplifier may be considered as a single stage.

8.7.1 The CC–CE, CD–CS, and CD–CE Configurations

Figure 8.44(a) shows an amplifier formed by cascading a common-collector (emitter-follower) transistor Q_1 with a common-emitter transistor Q_2 . This circuit has two main advantages over the CE amplifier. First, the emitter follower increases the input resistance by a factor equal to $(\beta_1 + 1)$. As a result, the overall voltage gain is increased, especially if the resistance of the signal source is large. Second, it will be shown in Chapter 10 that the CC–CE amplifier can exhibit much wider bandwidth than that obtained with the CE amplifier.

The MOS counterpart of the CC–CE amplifier, namely, the CD–CS configuration, is shown in Fig. 8.44(b). Here, since the CS amplifier alone has an infinite input resistance, the

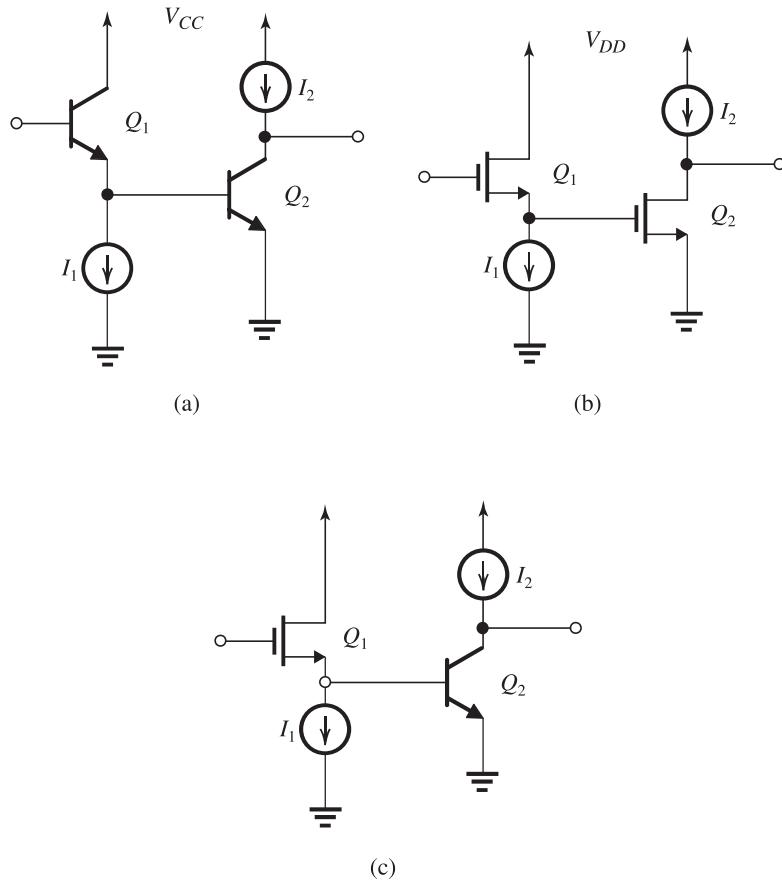


Figure 8.44 (a) CC-CE amplifier; (b) CD-CS amplifier; (c) CD-CE amplifier.

sole purpose for adding the source-follower stage is to increase the amplifier bandwidth, as will be seen in Chapter 10. Finally, Fig. 8.44(c) shows the BiCMOS version of this circuit type. Compared to the bipolar circuit in Fig. 8.44(a), the BiCMOS circuit has an infinite input resistance. Compared to the MOS circuit in Fig. 8.44(b), the BiCMOS circuit typically has a higher g_{m2} .

The IC Source Follower Since a number of the circuit configurations discussed in this section utilize an input source follower, we digress briefly to consider the IC source follower (the discrete-circuit source follower was studied in Section 7.3.6). Figure 8.45(a) shows a source follower formed by transistor Q_1 and biased by a constant-current supplied by the current mirror Q_2-Q_3 . Observe that since the source of Q_1 cannot be connected to the body (which is at signal ground potential) a voltage signal v_{bs} develops between body and source and gives rise to a current signal $g_{mb}v_{bs}$, as indicated in the equivalent circuit in Fig. 8.45(b). The equivalent circuit shows also the output resistance r_{o3} of the bias current source Q_3 , which acts as a load resistance for the follower Q_1 .

An important observation to make from the equivalent circuit is that the controlled source ($g_{mb}v_{bs}$) appears across its control voltage v_{bs} . Thus we can use the source-absorption theorem (Appendix G) to replace the controlled source with a resistance $1/g_{mb}$. Next, note that the three

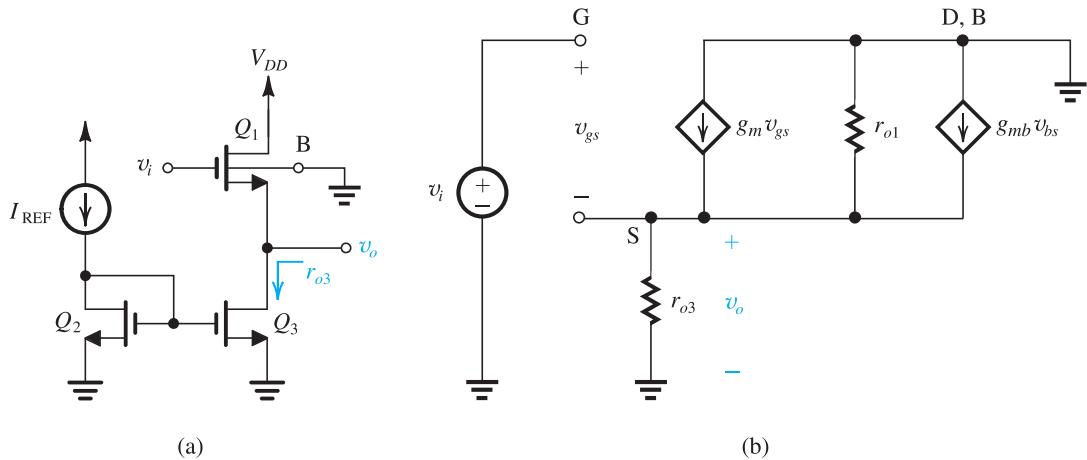


Figure 8.45 (a) A source follower biased with a current mirror \$Q_2-Q_3\$ and with the body terminal indicated. Note that the source cannot be connected to the body and thus the body effect should be taken into account. (b) Equivalent circuit.

resistances \$1/g_{mb}\$, \$r_{o1}\$, and \$r_{o3}\$ appear in parallel between the source and ground. If we denote their parallel equivalent \$R_L\$, we can easily show that the voltage gain of the source follower is given by

$$\frac{v_o}{v_i} = \frac{R_L}{R_L + \frac{1}{g_m}} \quad (8.103)$$

where

$$R_L = r_{o1} \parallel r_{o3} \parallel \frac{1}{g_{mb}} \quad (8.104)$$

In cases where \$\frac{1}{g_{mb}} \ll r_{o1}, r_{o3}\$,

$$R_L \simeq \frac{1}{g_{mb}}$$

and

$$\frac{v_o}{v_i} \simeq \frac{g_{mb}}{g_m + g_{mb}} \quad (8.105)$$

Substituting for \$g_{mb} = \chi g_m\$ where \$\chi = 0.1\$ to \$0.2\$,

$$\frac{v_o}{v_i} \simeq \frac{1}{1 + \chi} \quad (8.106)$$

This is the maximum possible gain obtained from an IC source follower. The actual gain realized will usually be lower because of the effect of \$r_{o1}\$ and \$r_{o3}\$.

EXERCISE

- 8.28** For the source follower in Fig. 8.45(a), let the bias current of \$Q_1\$ be \$200 \mu\text{A}\$ and assume \$Q_1\$ is operating at \$V_{ov} = 0.2 \text{ V}\$. If \$V_A = 5 \text{ V}\$ and \$\chi = 0.2\$, find the voltage gain of the source follower.

Ans. \$0.81 \text{ V/V}\$

Example 8.7

For the CC–CE amplifier in Fig. 8.44(a) let $I_1 = I_2 = 1 \text{ mA}$ and assume identical transistors with $\beta = 100$. Find the input resistance R_{in} and the overall voltage gain obtained when the amplifier is fed with a signal source having $R_{\text{sig}} = 4 \text{ k}\Omega$ and loaded with a resistance $R_L = 4 \text{ k}\Omega$. Compare the results with those obtained with a common-emitter amplifier operating under the same conditions. Ignore r_o .

Solution

At an emitter current of 1 mA, Q_1 and Q_2 have

$$\begin{aligned} g_m &= 40 \text{ mA/V} \\ r_e &= 25 \Omega \\ r_\pi &= \frac{\beta}{g_m} = \frac{100}{40} = 2.5 \text{ k}\Omega \end{aligned}$$

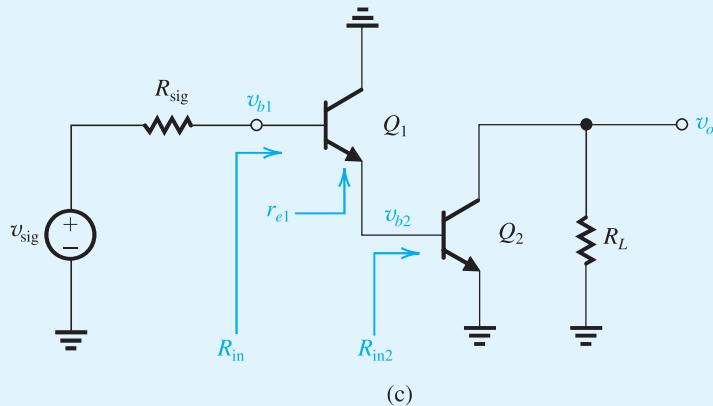


Figure 8.46 Circuit for Example 8.7.

Referring to Fig. 8.46 we can find

$$\begin{aligned} R_{\text{in}2} &= r_\pi = 2.5 \text{ k}\Omega \\ R_{\text{in}} &= (\beta_1 + 1)(r_{e1} + R_{\text{in}2}) \\ &= 101(0.025 + 2.5) = 255 \text{ k}\Omega \\ \frac{v_{b1}}{v_{\text{sig}}} &= \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} = \frac{255}{255 + 4} = 0.98 \text{ V/V} \\ \frac{v_{b2}}{v_{b1}} &= \frac{R_{\text{in}2}}{R_{\text{in}2} + r_{e1}} = \frac{2.5}{2.5 + 0.025} = 0.99 \text{ V/V} \\ \frac{v_o}{v_{b2}} &= -g_{m2}R_L = -40 \times 4 = -160 \text{ V/V} \end{aligned}$$

Thus,

$$G_v = \frac{v_o}{v_{\text{sig}}} = -160 \times 0.99 \times 0.98 = -155 \text{ V/V}$$

For comparison, a CE amplifier operating under the same conditions will have

$$\begin{aligned} R_{\text{in}} &= r_\pi = 2.5 \text{ k}\Omega \\ G_v &= \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} (-g_m R_L) \\ &= \frac{2.5}{2.5 + 4} (-40 \times 4) \\ &= -61.5 \text{ V/V} \end{aligned}$$

EXERCISE

- 8.29** Repeat Example 8.7 for the CD–CE configuration of Fig. 8.44(c). Let $I_1 = I_2 = 1 \text{ mA}$, $\beta_2 = 100$, $R_L = 4 \text{ k}\Omega$, and $k_{n1} = 8 \text{ mA/V}^2$; neglect the body effect in Q_1 and r_o of both transistors. Find R_{in} and G_v when $R_{\text{sig}} = 4 \text{ k}\Omega$ (as in Example 8.7) and $R_{\text{sig}} = 400 \text{ k}\Omega$. What would G_v of the CC–CE amplifier in Example 8.7 become for $R_{\text{sig}} = 400 \text{ k}\Omega$?

Ans. $R_{\text{in}} = \infty$; $G_v = -145.5 \text{ V/V}$, independent of R_{sig} ; -61.7 V/V

8.7.2 The Darlington Configuration⁵

Figure 8.47(a) shows a popular BJT circuit known as the **Darlington configuration**. It can be thought of as a variation of the CC–CE circuit with the collector of Q_1 connected to that of Q_2 . Alternatively, the **Darlington pair** can be thought of as a composite transistor with $\beta = \beta_1 \beta_2$. It can therefore be used to implement a high-performance voltage follower, as illustrated in Fig. 8.47(b). Note that in this application the circuit can be considered as the cascade connection of two common-collector transistors (i.e., a CC–CC configuration).

Since the transistor β depends on the dc bias current, it is possible that Q_1 will be operating at a very low β , rendering the β -multiplication effect of the Darlington pair rather ineffective. A simple solution to this problem is to provide a bias current for Q_1 , as shown in Fig. 8.47(c).

⁵Named after Sidney Darlington, a pioneer in filter design and transistor circuit design.

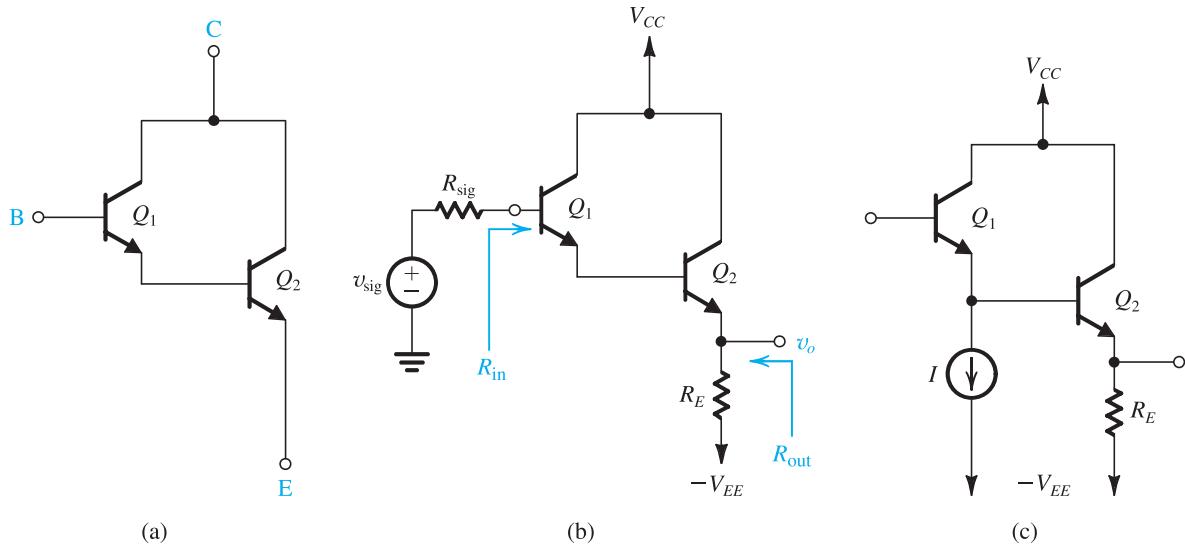


Figure 8.47 (a) The Darlington configuration; (b) voltage follower using the Darlington configuration; (c) the Darlington follower with a bias current I supplied to Q_1 to ensure that its β remains high.

EXERCISE

8.30 For the Darlington voltage follower in Fig. 8.47(b), show that:

$$\begin{aligned} R_{in} &= (\beta_1 + 1)[r_{e1} + (\beta_2 + 1)(r_{e2} + R_E)] \\ R_{out} &= R_E \parallel \left[r_{e2} + \frac{r_{e1} + [R_{sig}/(\beta_1 + 1)]}{\beta_2 + 1} \right] \\ \frac{v_o}{v_{sig}} &= \frac{R_E}{R_E + r_{e2} + [r_{e1} + R_{sig}/(\beta_1 + 1)]/(\beta_2 + 1)} \end{aligned}$$

Evaluate R_{in} , R_{out} , and v_o/v_{sig} for the case $I_{E2} = 5$ mA, $\beta_1 = \beta_2 = 100$, $R_E = 1$ k Ω , and $R_{sig} = 100$ k Ω .

Ans. 10.3 M Ω ; 20 Ω ; 0.98 V/V

8.7.3 The CC–CB and CD–CG Configurations

Cascading an emitter follower with a common-base amplifier, as shown in Fig. 8.48(a), results in a circuit with a low-frequency gain approximately equal to that of the CB but with the problem of the low input resistance of the CB solved by the buffering action of the CC stage. It will be shown in Chapter 10 that this circuit exhibits wider bandwidth than that obtained with a CE amplifier of the same gain. Note that the biasing current sources shown in Fig. 8.48(a) ensure that each of Q_1 and Q_2 is operating at a bias current I . We are not showing, however, how the dc voltage at the base of Q_1 is set, nor do we show the circuit that determines the

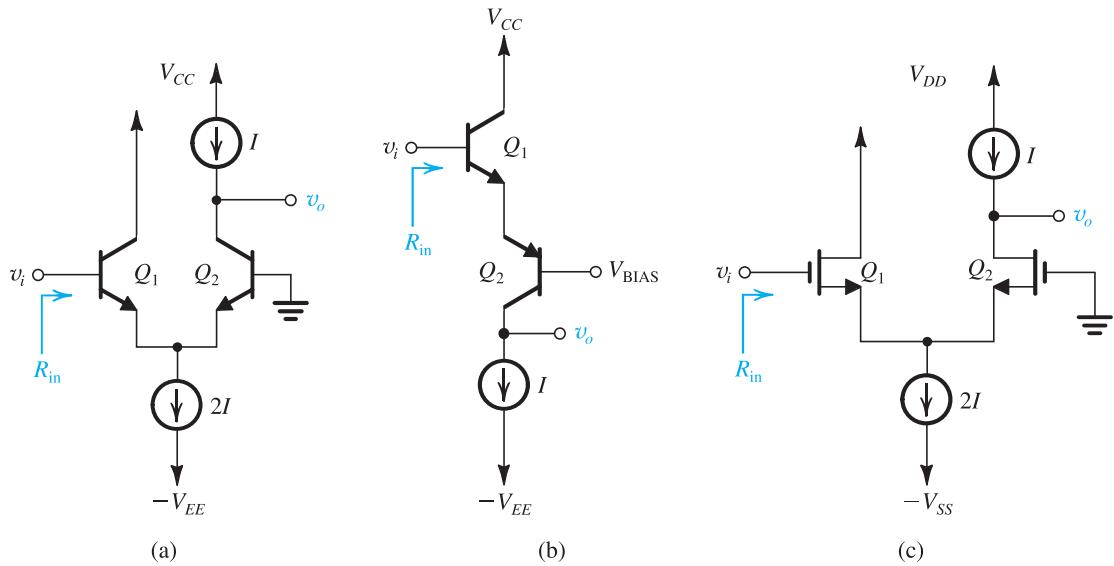


Figure 8.48 (a) A CC–CB amplifier. (b) Another version of the CC–CB circuit with Q_2 implemented using a *pnp* transistor. (c) The MOSFET version of the circuit in (a).

dc voltage at the collector of Q_2 . Both issues are usually looked after in the larger circuit of which the CC–CB amplifier is a part.

An interesting version of the CC–CB configuration is shown in Fig. 8.48(b). Here the CB stage is implemented with a *pnp* transistor. Although only one current source is now needed, observe that we also need to establish an appropriate bias voltage at the base of Q_2 . This circuit is part of the internal circuit of the popular 741 op amp, which will be studied in Chapter 13.

The MOSFET version of the circuit in Fig. 8.48(a) is the CD–CG amplifier shown in Fig. 8.48(c).

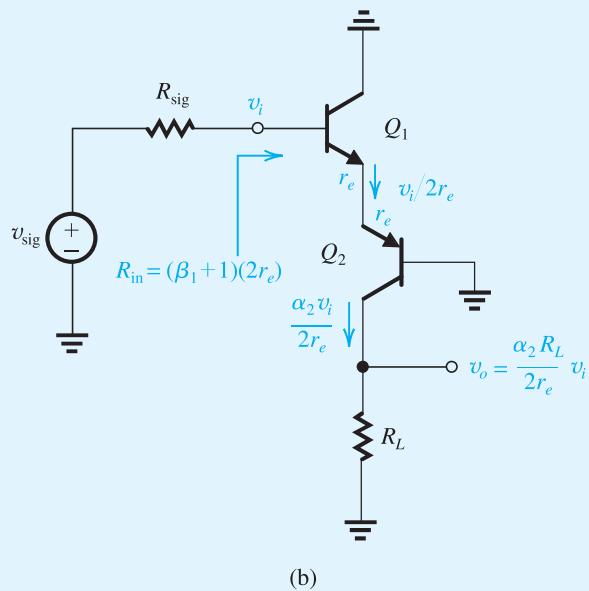
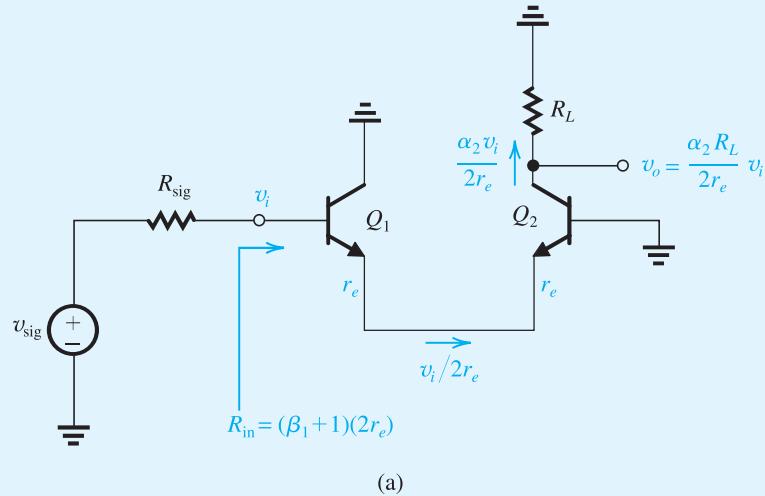
Example 8.8

For the CC–CB amplifiers in Fig. 8.48(a) and (b), find R_{in} , v_o/v_i , and v_o/v_{sig} when each amplifier is fed with a signal source having a resistance R_{sig} , and a load resistance R_L is connected at the output. For simplicity, neglect r_o .

Solution

The analysis of both circuits is illustrated in Fig. 8.49. Observe that both amplifiers have the same R_{in} and v_o/v_i . The overall voltage gain v_o/v_{sig} can be found as

$$\frac{v_o}{v_{\text{sig}}} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} \frac{\alpha_2 R_L}{2r_e}$$

Example 8.8 *continued***Figure 8.49** Circuits for Example 8.8.**EXERCISES**

- 8.31** For the amplifiers in Example 8.8 find R_{in} , v_o/v_i , and v_o/v_{sig} for the case $I = 1\text{ mA}$, $\beta = 100$.
 $R_L = R_{sig} = 5\text{ k}\Omega$.

Ans. 5.05 $\text{k}\Omega$; 100 V/V; 50 V/V

- D8.32** (a) Neglecting r_{o1} and the body effect, show that the voltage gain v_o/v_i of the CD-CG amplifier shown earlier in Fig. 8.48(c) is given by

$$\frac{v_o}{v_i} = \frac{IR_L}{V_{ov}}$$

where R_L is a load resistance connected at the output and V_{ov} is the overdrive voltage at which each of Q_1 and Q_2 is operating.

(b) For $I = 0.1$ mA and $R_L = 20$ k Ω , find W/L for each of Q_1 and Q_2 to obtain a gain of 10 V/V. Assume $k'_n = 200$ μ A/V 2 .

Ans. (b) $W/L = 25$

Summary

- Integrated-circuit fabrication technology offers the circuit designer many exciting opportunities, the most important of which is the large number of inexpensive small-area MOS transistors. An overriding concern for IC designers, however, is the minimization of chip area or “silicon real estate.” As a result, large-valued resistors and capacitors are virtually absent.
- Biasing in integrated circuits utilizes current sources. As well, current sources are used as load devices. Typically an accurate and stable reference current is generated and then replicated to provide bias currents for the various amplifier stages on the chip. The heart of the current-steering circuitry utilized to perform this function is the current mirror.
- The MOS current mirror has a current transfer ratio of $(W/L)_2/(W/L)_1$. For a bipolar mirror, the ratio is I_{S2}/I_{S1} .
- Bipolar mirrors suffer from the finite β , which reduces the accuracy of the current transfer ratio.
- Both bipolar and MOS mirrors of the basic type have a finite output resistance equal to r_o of the output device. Also, for proper operation, a voltage of at least 0.3 V is required across the output transistor of a simple bipolar mirror ($|V_{ov}|$ for the MOS case).
- The basic gain cell of IC amplifiers is the CS (CE) amplifier with a current-source load. For an ideal current-source load (i.e., one with infinite output resistance), the transistor operates in an open-circuit fashion and thus provides the maximum gain possible, $A_{vo} = -g_m r_o = -A_0$.
- The intrinsic gain A_0 is given by $A_0 = V_A/V_T$ for a BJT and $A_0 = V_A/(V_{ov}/2)$ for a MOSFET. For a BJT, A_0 is constant independent of bias current and device dimensions. For a MOSFET, A_0 is inversely proportional to $\sqrt{I_D}$ (see Eq. 8.46).
- Simple current-source loads reduce the gain realized in the basic gain cell because of their finite output resistance (usually comparable to the value of r_o of the amplifying transistor).
- To raise the output resistance of the CS or CE transistor, we stack a CG or CB transistor on top. This is cascoding.
- The CG and CB amplifiers act as current buffers. They have a short-circuit current gain of unity or, equivalently, a short-circuit transconductance equal to g_m of the transistor. For the CG: $R_{in} = \frac{r_o + R_L}{g_m r_o}$ and $R_{out} = R_s + r_o + g_m r_o R_s$. For the CB: $R_{in} = r_e \frac{r_o + R_L}{r_o + \frac{R_L}{\beta + 1}}$ and $R_{out} = (R_e \parallel r_\pi) + r_o + g_m r_o (R_e \parallel r_\pi)$.
- The CG or CB transistor in the cascode passes the current $g_{m1} v_i$ provided by the CS or CE transistor to the output but increases the resistance at the output from r_{o1} to $(g_{m2} r_{o2}) r_{o1}$ in the MOS case [$g_{m2} r_{o2} (r_{o1} \parallel r_{\pi2})$ in the bipolar case]. The maximum output resistance achieved in the bipolar case is $\beta_2 r_{o2}$.
- A MOS cascode amplifier operating with an ideal current-source load achieves a gain of $(g_m r_o)^2 = A_0^2$.
- To realize the full advantage of cascoding, the load current-source must also be cascaded, in which case a gain as high as $\frac{1}{2} A_0^2$ can be obtained.
- Double cascoding is possible in the MOS case only. However, the large number of transistors in the

- stack between the power-supply rails results in the disadvantage of a severely limited output-signal swing. The folded-cascode configuration helps resolve this issue.
- A CS amplifier with a resistance R_s in its source lead has an output resistance $R_o \simeq (1 + g_m R_s) r_o$. The corresponding formula for the BJT case is $R_o = [1 + g_m (R_e \parallel r_\pi)] r_o$.
 - Cascoding can be applied to current mirrors to increase their output resistances. An alternative that also solves the β problem in the bipolar case is the Wilson circuit. The MOS Wilson mirror has an output resistance of $(g_m r_o) r_o$, and the BJT version has an output resistance of $\frac{1}{2} \beta r_o$. Both the cascode and Wilson mirrors require at least 1 V or so for proper operation.
 - The Widlar current source provides an area-efficient way to implement a low-valued constant-current source that also has a high output resistance.
 - Preceding the CE (CS) transistor with an emitter follower (a source follower) results in increased input resistance in the BJT case and wider bandwidth in both the BJT and MOS cases.
 - Preceding the CB (CG) transistor with an emitter follower (a source follower) solves the low-input-resistance problem of the CB and CG configurations.
 - The Darlington configuration results in an equivalent BJT with a current gain approaching β^2 .

PROBLEMS

Computer Simulation Problems

SIM Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 8.2: IC Biasing—Current Sources, Current Mirrors, and Current-Steering Circuits

D 8.1 For $V_{DD} = 1.3$ V and using $I_{REF} = 100 \mu\text{A}$, it is required to design the circuit of Fig. 8.1 to obtain an output current whose nominal value is $100 \mu\text{A}$. Find R if Q_1 and Q_2 are matched with channel lengths of $0.5 \mu\text{m}$, channel widths of $5 \mu\text{m}$, $V_t = 0.4$ V, and $k'_n = 500 \mu\text{A/V}^2$. What is the lowest possible value of V_o ? Assuming that for this process technology the Early voltage $V_A' = 5$ V/ μm , find the output resistance of the current source. Also, find the change in output current resulting from a $+0.5$ -V change in V_o .

D 8.2 Using $V_{DD} = 1.8$ V and a pair of matched MOSFETs, design the current-source circuit of Fig. 8.1 to provide an output current of $150\text{-}\mu\text{A}$ nominal value. To simplify matters,

assume that the nominal value of the output current is obtained at $V_o \simeq V_{GS}$. It is further required that the circuit operate for V_o in the range of 0.3 V to V_{DD} and that the change in I_o over this range be limited to 10% of the nominal value of I_o . Find the required value of R and the device dimensions. For the fabrication-process technology utilized, $\mu_n C_{ox} = 400 \mu\text{A/V}^2$, $V_A' = 10$ V/ μm , and $V_t = 0.5$ V.

D 8.3 Sketch the *p*-channel counterpart of the current-source circuit of Fig. 8.1. Note that while the circuit of Fig. 8.1 should more appropriately be called a current sink, the corresponding PMOS circuit is a current source. Let $V_{DD} = 1.3$ V, $|V_t| = 0.4$ V, Q_1 and Q_2 be matched, and $\mu_p C_{ox} = 80 \mu\text{A/V}^2$. Find the device *W/L* ratios and the value of the resistor that sets the value of I_{REF} so that a nominally $80\text{-}\mu\text{A}$ output current is obtained. The current source is required to operate for V_o as high as 1.1 V. Neglect channel-length modulation.

SIM 8.4 Consider the current-mirror circuit of Fig. 8.2 with two transistors having equal channel lengths but with Q_2 having a width five times that of Q_1 . If I_{REF} is $20 \mu\text{A}$ and the transistors are operating at an overdrive voltage of 0.2 V, what I_o results? What is the minimum allowable value of V_o for proper operation of the current source? If $V_t = 0.5$ V, at what value of V_o will the nominal value of I_o be obtained? If V_o increases by 1 V, what is the corresponding increase in I_o ? Let $V_A = 20$ V.

- 8.5** For the current-steering circuit of Fig. P8.5, find I_o in terms of I_{REF} and device W/L ratios.

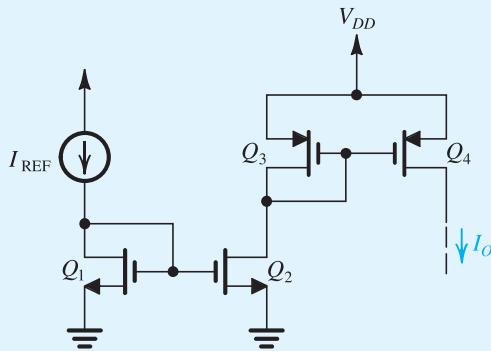


Figure P8.5

- D 8.6** The current-steering circuit of Fig. P8.6 is fabricated in a CMOS technology for which $\mu_n C_{ox} = 400 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{tn} = 0.5 \text{ V}$, $V_{tp} = -0.5 \text{ V}$, $V'_{An} = 5 \text{ V}/\mu\text{m}$, and $|V'_{Ap}| = 5 \text{ V}/\mu\text{m}$. If all devices have $L = 0.5 \mu\text{m}$, design the circuit so that $I_{\text{REF}} = 20 \mu\text{A}$, $I_2 = 100 \mu\text{A}$, $I_3 = I_4 = 40 \mu\text{A}$, and $I_5 = 80 \mu\text{A}$. Use the minimum possible device widths needed to achieve proper operation of the current source Q_2 for voltages at its drain as high as $+0.8 \text{ V}$ and proper operation of the current sink Q_5 with voltages at its drain as low as -0.8 V . Specify the widths of all devices and the value of R . Find the output resistance of the current source Q_2 and the output resistance of the current sink Q_5 .

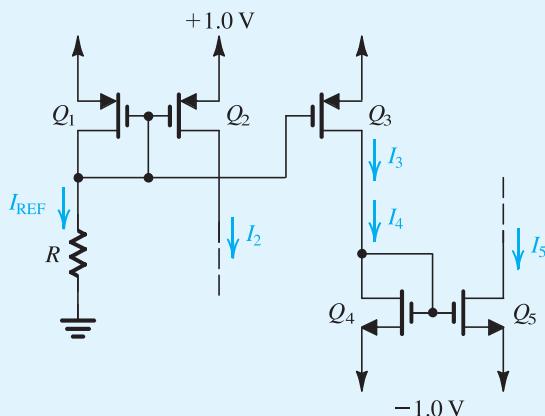


Figure P8.6

- *8.7** A PMOS current mirror consists of three PMOS transistors, one diode connected and two used as current

outputs. All transistors have $|V_t| = 0.6 \text{ V}$, $k'_p = 100 \mu\text{A}/\text{V}^2$, and $L = 1.0 \mu\text{m}$ but three different widths, namely, $10 \mu\text{m}$, $20 \mu\text{m}$, and $40 \mu\text{m}$. When the diode-connected transistor is supplied from a $100-\mu\text{A}$ source, how many different output currents are available? Repeat with two of the transistors diode connected and the third used to provide current output. For each possible input-diode combination, give the values of the output currents and of the V_{SG} that results.

- 8.8** Consider the basic bipolar current mirror of Fig. 8.7 for the case in which Q_1 and Q_2 are identical devices having $I_s = 10^{-17} \text{ A}$.

- (a) Assuming the transistor β is very high, find the range of V_{BE} and I_o corresponding to I_{REF} increasing from $10 \mu\text{A}$ to 10 mA . Assume that Q_2 remains in the active mode, and neglect the Early effect.
(b) Find the range of I_o corresponding to I_{REF} in the range of $10 \mu\text{A}$ to 10 mA , taking into account the finite β . Assume that β remains constant at 100 over the current range 0.1 mA to 5 mA but that at $I_C \simeq 10 \text{ mA}$ and at $I_C \simeq 10 \mu\text{A}$, $\beta = 50$. Specify I_o corresponding to $I_{\text{REF}} = 10 \mu\text{A}$, 0.1 mA , 1 mA , and 10 mA . Note that β variation with current causes the current transfer ratio to vary with current.

- 8.9** Consider the basic BJT current mirror of Fig. 8.7 for the case in which Q_2 has m times the area of Q_1 . Show that the current transfer ratio is given by Eq. (8.19). If β is specified to be a minimum of 80, what is the largest current transfer ratio possible if the error introduced by the finite β is limited to 10%?

- 8.10** Give the circuit for the *pnp* version of the basic current mirror of Fig. 8.7. If β of the *pnp* transistor is 50, what is the current gain (or transfer ratio) I_o/I_{REF} for the case of identical transistors, neglecting the Early effect?

- 8.11** Consider the basic BJT current mirror of Fig. 8.7 when Q_1 and Q_2 are matched and $I_{\text{REF}} = 1 \text{ mA}$. Neglecting the effect of finite β , find the change in I_o , both as an absolute value and as a percentage, corresponding to V_o changing from 1 V to 10 V . The Early voltage is 90 V .

- D 8.12** The current-source circuit of Fig. P8.12 utilizes a pair of matched *pnp* transistors having $I_s = 10^{-15} \text{ A}$, $\beta = 50$, and $|V_A| = 50 \text{ V}$. It is required to design the circuit to provide an output current $I_o = 1 \text{ mA}$ at $V_o = 1 \text{ V}$. What values of I_{REF} and R are needed? What is the maximum allowed value of V_o while the current source continues to operate properly? What change occurs in I_o corresponding to V_o changing from the

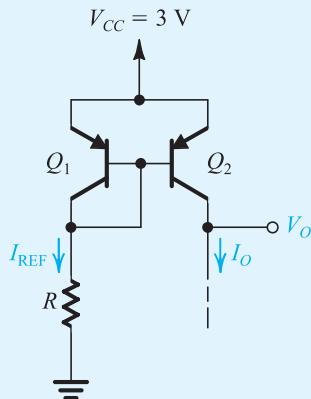


Figure P8.12

maximum positive value to -5 V ? Hint: Adapt Eq. (8.21) for this case as:

$$I_O = I_{\text{REF}} \left[\frac{1 + \frac{3 - V_O - V_{EB}}{|V_A|}}{1 + \frac{2}{\beta}} \right]$$

8.13 Find the voltages at all nodes and the currents through all branches in the circuit of Fig. P8.13. Assume $|V_{BE}| = 0.7\text{ V}$ and $\beta = \infty$.

8.14 For the circuit in Fig. P8.14, let $|V_{BE}| = 0.7\text{ V}$ and $\beta = \infty$. Find I , V_1 , V_2 , V_3 , V_4 , and V_5 for (a) $R = 10\text{ k}\Omega$ and (b) $R = 100\text{ k}\Omega$.

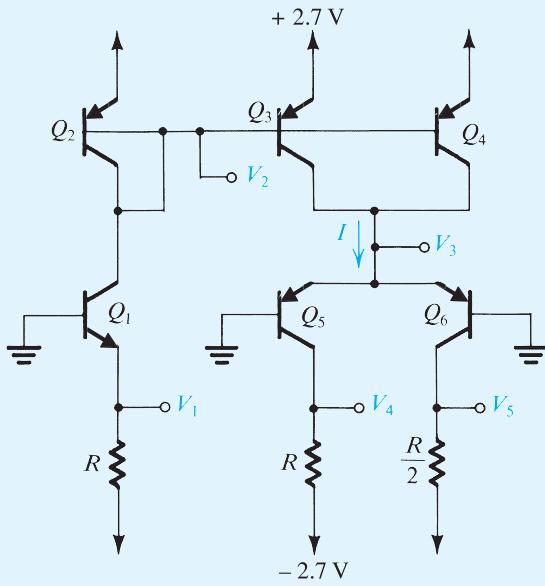


Figure P8.14

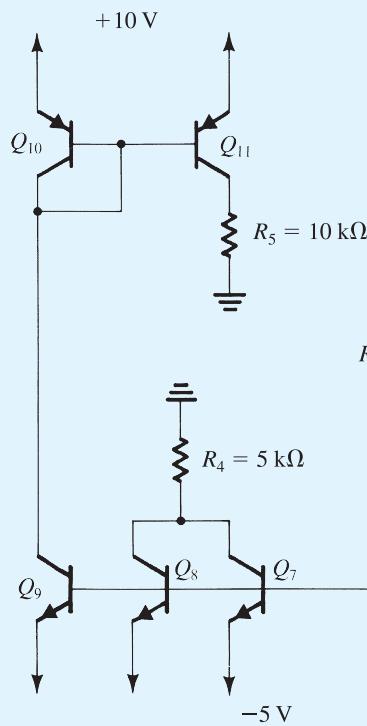


Figure P8.13

D 8.15 Using the ideas embodied in Fig. 8.10, design a multiple-mirror circuit using power supplies of ± 5 V to create source currents of 0.2 mA, 0.4 mA, and 0.8 mA and sink currents of 0.5 mA, 1 mA, and 2 mA. Assume that the BJTs have $|V_{BE}| \approx 0.7$ V and large β . What is the total power dissipated in your circuit?

***8.16** The circuit shown in Fig. P8.16 is known as a **current conveyor**.

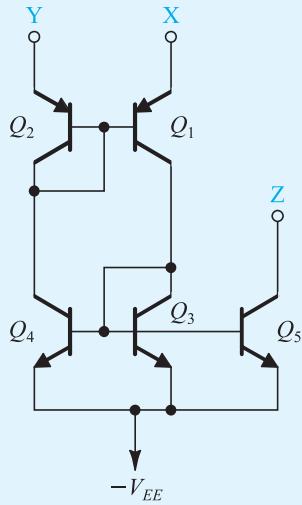


Figure P8.16

- Assuming that Y is connected to a voltage V , a current I is forced into X, and terminal Z is connected to a voltage that keeps Q_5 in the active region, show that a current equal to I flows through terminal Y, that a voltage equal to V appears at terminal X, and that a current equal to I flows through terminal Z. Assume β to be large; corresponding transistors are matched, and all transistors are operating in the active region.
- With Y connected to ground, show that a virtual ground appears at X. Now, if X is connected to a +5-V supply through a 10-k Ω resistor, what current flows through Z?

8.17 The MOSFETs in the current mirror of Fig. 8.12(a) have equal channel lengths of 0.5 μm , $W_1 = 10 \mu\text{m}$, $W_2 = 50 \mu\text{m}$, $\mu_n C_{ox} = 500 \mu\text{A/V}^2$, and $V_A' = 10 \text{ V}/\mu\text{m}$. If the input bias current is 100 μA , find R_{in} , A_{is} , and R_o .

D 8.18 The MOSFETs in the current mirror of Fig. 8.12(a) have equal channel lengths, $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ and $V_A' = 20 \text{ V}/\mu\text{m}$. If the input bias current is 200 μA , find W_1 , W_2 , and L

to obtain a short-circuit current gain of 4, an input resistance of 500 Ω , and an output resistance of 20 k Ω .

8.19 Figure P8.19 shows an amplifier utilizing a current mirror Q_2-Q_3 . Here Q_1 is a common-source amplifier fed with $v_i = V_{GS} + v_i$, where V_{GS} is the gate-to-source dc bias voltage of Q_1 and v_i is a small signal to be amplified. Find the signal component of the output voltage v_o and hence the small-signal voltage gain v_o/v_i . Also, find the small-signal resistance of the diode-connected transistor Q_2 in terms of g_m , and hence the total resistance between the drain of Q_1 and ground. What is the voltage gain of the CS amplifier Q_1 ? Neglect all r_o 's.

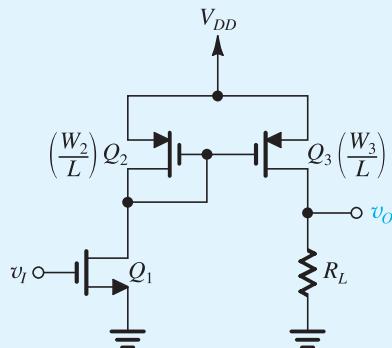


Figure P8.19

***8.20** Figure P8.20 shows a current-mirror circuit prepared for small-signal analysis. Replace the BJTs with their hybrid- π models and find expressions for R_{in} , i_o/i_i , and R_o , where i_o is the output short-circuit current. Assume $r_o \gg r_\pi$.

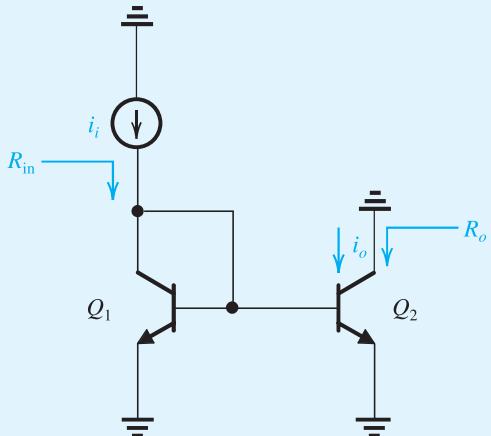


Figure P8.20

8.21 It is required to find the incremental (i.e., small-signal) resistance of each of the diode-connected transistors shown in

Fig. P8.21. Assume that the dc bias current $I = 0.1$ mA. For the MOSFET, let $\mu_n C_{ox} = 200 \mu\text{A/V}^2$ and $W/L = 10$. Neglect r_o for both devices.

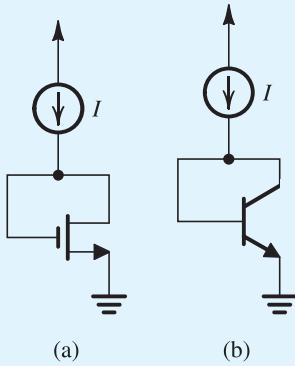


Figure P8.21

8.22 For the base-current-compensated mirror of Fig. 8.11, let the three transistors be matched and specified to have a collector current of 1 mA at $V_{BE} = 0.7$ V. For I_{REF} of 100 μA and assuming $\beta = 100$, what will the voltage at node x be? If I_{REF} is increased to 1 mA, what is the change in V_x ? What is the value of I_O obtained with $V_O = V_x$ in both cases? Give the percentage difference between the actual and ideal value of I_O . What is the lowest voltage at the output for which proper current-source operation is maintained?

D 8.23 Extend the current-mirror circuit of Fig. 8.11 to n outputs. What is the resulting current transfer ratio from the input to each output, I_O/I_{REF} ? If the deviation from unity is to be kept at 0.2% or less, what is the maximum possible number of outputs for BJTs with $\beta = 150$?

***8.24** For the base-current-compensated mirror of Fig. 8.11, show that the incremental input resistance (seen by the reference current source) is approximately $2V_T/I_{REF}$. Evaluate R_{in} for $I_{REF} = 100 \mu\text{A}$. (*Hint:* Q_3 is operating at a current $I_{E3} = 2I_C/\beta$, where I_C is the operating current of each of Q_1 and Q_2 . Replace each transistor with its T model and neglect r_o .)

Section 8.3: The Basic Gain Cell

8.25 Find g_m , r_π , r_o , and A_0 for the CE amplifier of Fig. 8.13(b) when operated at $I = 10 \mu\text{A}$, $100 \mu\text{A}$, and 1 mA . Assume $\beta = 100$ and remains constant as I is varied, and that $V_A = 10$ V. Present your results in a table.

8.26 Consider the CE amplifiers of Fig. 8.13(b) for the case of $I = 0.5$ mA, $\beta = 100$, and $V_A = 100$ V. Find R_{in} , A_{vo} , and R_o . If it is required to raise R_{in} by a factor of 5 by changing I , what value of I is required, assuming that β remains unchanged? What are the new values of A_{vo} and R_o ? If the amplifier is fed with a signal source having $R_{sig} = 5 \text{ k}\Omega$ and is connected to a load of $100-\text{k}\Omega$ resistance, find the overall voltage gain, v_o/v_{sig} .

8.27 Find the intrinsic gain of an NMOS transistor fabricated in a process for which $k'_n = 400 \mu\text{A/V}^2$ and $V'_A = 10 \text{ V}/\mu\text{m}$. The transistor has a $0.5\text{-}\mu\text{m}$ channel length and is operated at $V_{ov} = 0.2$ V. If a 2-mA/V transconductance is required, what must I_D and W be?

8.28 An NMOS transistor fabricated in a certain process is found to have an intrinsic gain of 50 V/V when operated at an I_D of 100 μA . Find the intrinsic gain for $I_D = 25 \mu\text{A}$ and $I_D = 400 \mu\text{A}$. For each of these currents, find the factor by which g_m changes from its value at $I_D = 100 \mu\text{A}$.

D 8.29 Consider an NMOS transistor fabricated in a $0.18\text{-}\mu\text{m}$ technology for which $k'_n = 400 \mu\text{A/V}^2$ and $V'_A = 5 \text{ V}/\mu\text{m}$. It is required to obtain an intrinsic gain of 20 V/V and a g_m of 2 mA/V. Using $V_{ov} = 0.2$ V, find the required values of L , W/L , and the bias current I .

D 8.30 Sketch the circuit for a current-source-loaded CS amplifier that uses a PMOS transistor for the amplifying device. Assume the availability of a single +1.8-V dc supply. If the transistor is operated with $|V_{ov}| = 0.2$ V, what is the highest instantaneous voltage allowed at the drain?

8.31 An NMOS transistor operated with an overdrive voltage of 0.25 V is required to have a g_m equal to that of an *n-p-n* transistor operated at $I_C = 0.1$ mA. What must I_D be? What value of g_m is realized?

8.32 For an NMOS transistor with $L = 1 \mu\text{m}$ fabricated in the $0.5\text{-}\mu\text{m}$ process specified in Table J.1 in Appendix J, find g_m , r_o , and A_0 if the device is operated with $V_{ov} = 0.5$ V and $I_D = 100 \mu\text{A}$. Also, find the required device width W .

8.33 For an NMOS transistor with $L = 0.3 \mu\text{m}$ fabricated in the $0.18\text{-}\mu\text{m}$ process specified in Table J.1 in Appendix J, find g_m , r_o , and A_0 obtained when the device is operated at $I_D = 100 \mu\text{A}$ with $V_{ov} = 0.2$ V. Also, find W .

8.34 Fill in the table below. For the BJT, let $\beta = 100$ and $V_A = 100$ V. For the MOSFET, let $\mu_n C_{ox} = 200 \mu\text{A/V}^2$, $W/L = 40$, and $V_A = 10$ V.

	BJT Cell		MOSFET Cell	
Bias Current	$I_C = 0.1 \text{ mA}$	$I_C = 1 \text{ mA}$	$I_D = 0.1 \text{ mA}$	$I_D = 1 \text{ mA}$
g_m (mA/V)				
r_o ($\text{k}\Omega$)				
A_0 (V/V)				
R_{in} ($\text{k}\Omega$)				

8.35 A CS amplifier utilizes an NMOS transistor with $L = 0.54 \mu\text{m}$ and $W/L = 8$. It was fabricated in a $0.18\text{-}\mu\text{m}$ CMOS process for which $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ and $V'_A = 5 \text{ V}/\mu\text{m}$. What is the bias current of the transistor for which $A_0 = 18 \text{ V/V}$?

8.36 A CS amplifier utilizes an NMOS transistor with $L = 0.36 \mu\text{m}$ and $W/L = 8$. It was fabricated in a $0.18\text{-}\mu\text{m}$ CMOS process for which $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ and $V'_A = 5 \text{ V}/\mu\text{m}$. Find the values of g_m and A_0 obtained at $I_D = 25 \mu\text{A}$, $250 \mu\text{A}$, and 2.5 mA .

D 8.37 An NMOS transistor is fabricated in the $0.18\text{-}\mu\text{m}$ process whose parameters are given in Table J.1 in Appendix J. The device has a channel length twice the minimum and is operated at $V_{ov} = 0.25 \text{ V}$ and $I_D = 10 \mu\text{A}$.

- What values of g_m , r_o , and A_0 are obtained?
- If I_D is increased to $100 \mu\text{A}$, what do V_{ov} , g_m , r_o , and A_0 become?
- If the device is redesigned with a new value of W so that it operates at $V_{ov} = 0.25 \text{ V}$ for $I_D = 100 \mu\text{A}$, what do g_m , r_o , and A_0 become?
- If the redesigned device in (c) is operated at $10 \mu\text{A}$, find V_{ov} , g_m , r_o , and A_0 .
- Which designs and operating conditions produce the lowest and highest values of A_0 ? What are these values? In each of these two cases, if W/L is held at the same value but L is made 10 times larger, what gains result?

D 8.38 Find A_0 for an NMOS transistor fabricated in a CMOS process for which $k'_n = 400 \mu\text{A/V}^2$ and $V'_A = 6 \text{ V}/\mu\text{m}$. The transistor has a $0.5\text{-}\mu\text{m}$ channel length and is operated with an overdrive voltage of 0.15 V . What must W be for the NMOS transistor to operate at $I_D = 100 \mu\text{A}$? Also, find the values of g_m and r_o .

D 8.39 Using a CMOS technology for which $k'_n = 200 \mu\text{A/V}^2$ and $V'_A = 20 \text{ V}/\mu\text{m}$, design a

current-source-loaded CS amplifier for operation at $I = 50 \mu\text{A}$ with $V_{ov} = 0.2 \text{ V}$. The amplifier is to have an open-circuit voltage gain of -100 V/V . Assume that the current-source load is ideal. Specify L and W/L .

D 8.40 The circuit in Fig. 8.15(a) is fabricated in a process for which $\mu_n C_{ox} = 2\mu_p C_{ox} = 200 \mu\text{A/V}^2$, $V'_{An} = |V'_{Ap}| = 20 \text{ V}/\mu\text{m}$, $V_{tn} = -V_{tp} = 0.5 \text{ V}$, and $V_{DD} = 2.5 \text{ V}$. The two transistors have $L = 0.5 \mu\text{m}$ and are to be operated at $I_D = 100 \mu\text{A}$ and $|V_{ov}| = 0.3 \text{ V}$. Find the required values of V_G , $(W/L)_1$, $(W/L)_2$, and A_v .

D 8.41 The circuit in Fig. 8.15(a) is fabricated in a $0.18\text{-}\mu\text{m}$ CMOS technology for which $\mu_n C_{ox} = 400 \mu\text{A/V}^2$, $\mu_p C_{ox} = 100 \mu\text{A/V}^2$, $V_{tn} = -V_{tp} = 0.5 \text{ V}$, $V'_{An} = 5 \text{ V}/\mu\text{m}$, $|V'_{Ap}| = 5 \text{ V}/\mu\text{m}$, and $V_{DD} = 1.8 \text{ V}$. It is required to design the circuit to obtain a voltage gain $A_v = -40 \text{ V/V}$. Use devices of equal length L operating at $I = 100 \mu\text{A}$ and $|V_{ov}| = 0.25 \text{ V}$. Determine the required values of V_G , L , $(W/L)_1$, and $(W/L)_2$.

8.42 Figure P8.42 shows an IC MOS amplifier formed by cascading two common-source stages. Assuming that $V_{An} = |V_{Ap}|$ and that the biasing current sources have output resistances equal to those of Q_1 and Q_2 , find an expression for the overall voltage gain in terms of g_m and r_o of Q_1 and Q_2 . If Q_1 and Q_2 are to be operated at equal overdrive voltages, $|V_{ov}|$, find the required value of $|V_{ov}|$ if $|V_A| = 5 \text{ V}$ and the gain required is 400 V/V .

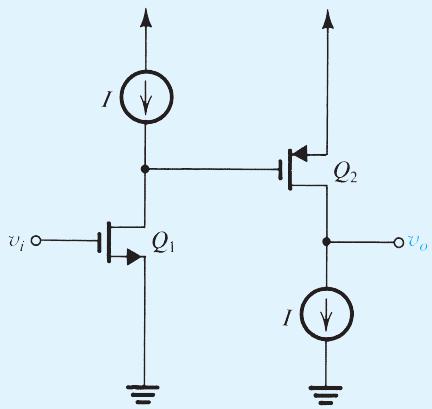


Figure P8.42

***8.43** The NMOS transistor in the circuit of Fig. P8.43 has $V_t = 0.5 \text{ V}$, $k'_n W/L = 2 \text{ mA/V}^2$, and $V_A = 20 \text{ V}$.

- Neglecting the dc current in the feedback network and the effect of r_o , find V_{GS} . Then find the dc current in the feedback network and V_{DS} . Verify that you were justified in neglecting the current in the feedback network when you found V_{GS} .

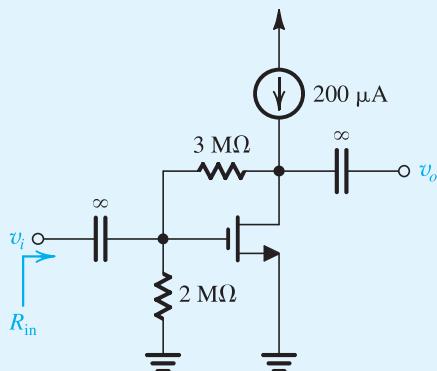


Figure P8.43

- (b) Find the small-signal voltage gain, v_o/v_i . What is the peak of the largest output sine-wave signal that is possible while the NMOS transistor remains in saturation? What is the corresponding input signal?
 (c) Find the small-signal input resistance R_{in} .

D 8.44 Consider the CMOS amplifier of Fig. 8.16(a) when fabricated with a process for which $k'_n = 4k'_p = 400 \mu\text{A/V}^2$, $|V_t| = 0.5 \text{ V}$, and $|V_A| = 5 \text{ V}$. Find I_{REF} and $(W/L)_1$ to obtain a voltage gain of -40 V/V and an output resistance of $100 \text{ k}\Omega$. Recall that Q_2 and Q_3 are matched. If Q_2 and Q_3 are to be operated at the same overdrive voltage as Q_1 , what must their W/L ratios be?

8.45 Consider the CMOS amplifier analyzed in Example 8.4. If v_i consists of a dc bias component on which is superimposed a sinusoidal signal, find the value of the dc component that will result in the maximum possible signal swing at the output with almost-linear operation. What is the amplitude of the output sinusoid resulting? (Note: In practice, the amplifier would have a feedback circuit that caused it to operate at a point near the middle of its linear region.)

8.46 The power supply of the CMOS amplifier analyzed in Example 8.4 is increased to 5 V. What will the extent of the linear region at the output become?

****8.47** Consider the circuit shown in Fig. 8.16(a), using a 3.3-V supply and transistors for which $|V_t| = 0.8 \text{ V}$ and $L = 1 \mu\text{m}$. For Q_1 , $k'_n = 100 \mu\text{A/V}^2$, $V_A = 100 \text{ V}$, and $W = 20 \mu\text{m}$. For Q_2 and Q_3 , $k'_p = 50 \mu\text{A/V}^2$ and $|V_A| = 50 \text{ V}$. For Q_2 , $W = 40 \mu\text{m}$. For Q_3 , $W = 10 \mu\text{m}$.

- (a) If Q_1 is to be biased at $100 \mu\text{A}$, find I_{REF} . For simplicity, ignore the effect of V_A .

- (b) What are the extreme values of v_o for which Q_1 and Q_2 just remain in saturation?
 (c) What is the large-signal voltage gain?
 (d) Find the slope of the transfer characteristic at $v_o = V_{DD}/2$.
 (e) For operation as a small-signal amplifier around a bias point at $v_o = V_{DD}/2$, find the small-signal voltage gain and output resistance.

****8.48** The MOSFETs in the circuit of Fig. P8.48 are matched, having $k'_n(W/L)_1 = k'_p(W/L)_2 = 1 \text{ mA/V}^2$ and $|V_t| = 0.5 \text{ V}$. The resistance $R = 1 \text{ M}\Omega$.

- (a) For G and D open, what are the drain currents I_{D1} and I_{D2} ?
 (b) For $r_o = \infty$, what is the voltage gain of the amplifier from G to D? (Hint: Replace the transistors with their small-signal models.)
 (c) For finite r_o ($|V_A| = 20 \text{ V}$), what is the voltage gain from G to D and the input resistance at G?
 (d) If G is driven (through a large coupling capacitor) from a source v_{sig} having a resistance of $20 \text{ k}\Omega$, find the voltage gain v_d/v_{sig} .
 (e) For what range of output signals do Q_1 and Q_2 remain in the saturation region?

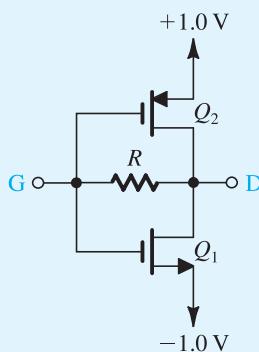


Figure P8.48

8.49 Transistor Q_1 in the circuit of Fig. P8.49 is operating as a CE amplifier with an active load provided by transistor Q_2 , which is the output transistor in a current mirror formed by Q_2 and Q_3 . (Note that the biasing arrangement for Q_1 is not shown.)

- (a) Neglecting the finite base currents of Q_2 and Q_3 and assuming that their $V_{BE} \approx 0.7 \text{ V}$ and that Q_2 has five times the area of Q_3 , find the value of I .
 (b) If Q_1 and Q_2 are specified to have $|V_A| = 30 \text{ V}$, find r_{o1} and r_{o2} and hence the total resistance at the collector of Q_1 .

- (c) Find $r_{\pi 1}$ and g_{m1} assuming that $\beta_1 = 50$.
 (d) Find R_{in} , A_v , and R_o .

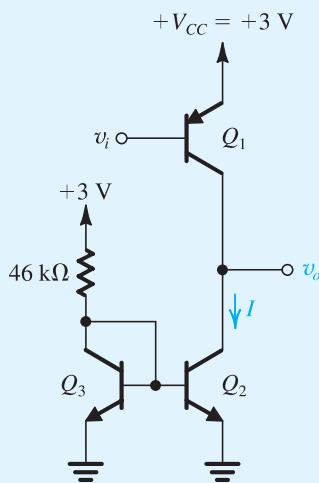


Figure P8.49

D 8.50 It is required to design the CMOS amplifier of Fig. 8.16(a) utilizing a 0.18-μm process for which $k'_n = 387 \mu\text{A/V}^2$, $k'_p = 86 \mu\text{A/V}^2$, $V_{tn} = -V_{tp} = 0.5 \text{ V}$, $V_{DD} = 1.8 \text{ V}$, $V'_{An} = 5 \text{ V}/\mu\text{m}$, and $V'_{Ap} = -6 \text{ V}/\mu\text{m}$. The output voltage must be able to swing to within approximately 0.2 V of the power-supply rails (i.e., from 0.2 V to 1.6 V), and the voltage gain must be at least 10 V/V. Design for a dc bias current of 50 μA, and use devices with the same channel length. If the channel length is an integer multiple of the minimum 0.18 μm, what channel length is needed and what W/L ratios are required? If it is required to raise the gain by a factor of 2, what channel length would be required, and by what factor does the total gate area of the circuit increase?

Section 8.4: The CG and CB Amplifiers

8.51 A CG amplifier operating with $g_m = 2 \text{ mA/V}$ and $r_o = 20 \text{ k}\Omega$ is fed with a signal source having $R_s = 1 \text{ k}\Omega$ and is loaded in a resistance $R_L = 20 \text{ k}\Omega$. Find R_{in} , R_{out} , and v_o/v_{sig} .

8.52 A CG amplifier operating with $g_m = 2 \text{ mA/V}$ and $r_o = 20 \text{ k}\Omega$ is fed with a signal source having a Norton equivalent composed of a current signal i_{sig} and a source resistance $R_s = 20 \text{ k}\Omega$. The amplifier is loaded in a resistance $R_L = 20 \text{ k}\Omega$. Find R_{in} and i_o/i_{sig} , where i_o is the current through the load R_L . If R_L increases by a factor of 10, by

what percentage does the current gain change? Can you see the effectiveness of the CG as a current buffer?

D 8.53 It is required to design the current source in Fig. P8.53 to deliver a current of 0.2 mA with an output resistance of 500 kΩ. The transistor has $V_A = 20 \text{ V}$ and $V_t = 0.5 \text{ V}$. Design for $V_{ov} = 0.2 \text{ V}$ and specify R_s and V_{BIAS} .

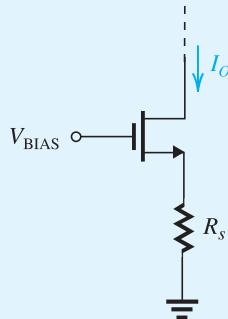


Figure P8.53

D 8.54 Figure P8.54 shows a current source realized using a current mirror with two matched transistors Q_1 and Q_2 . Two equal resistances R_s are inserted in the source leads to increase the output resistance of the current source. If Q_2 is operating at $g_m = 1 \text{ mA/V}$ and has $V_A = 10 \text{ V}$, and if the maximum allowed dc voltage drop across R_s is 0.3 V, what is the maximum available output resistance of the current source? Assume that the voltage at the common-gate node is approximately constant.

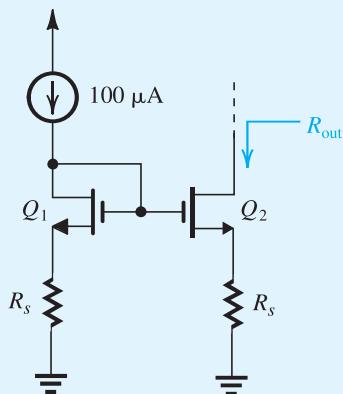


Figure P8.54

8.55 In the common-gate amplifier circuit of Fig. P8.55, Q_2 and Q_3 are matched. $k'_n(W/L)_n = k'_p(W/L)_p = 4 \text{ mA/V}^2$, and all transistors have $|V_t| = 0.8 \text{ V}$ and $|V_A| = 20 \text{ V}$.

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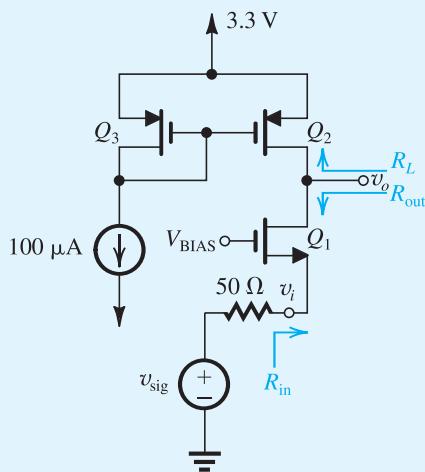


Figure P8.55

The signal v_{sig} is a small sinusoidal signal with no dc component.

- Neglecting the effect of V_A , find the dc drain current of Q_1 and the required value of V_{BIAS} .
- Find the values of g_m and r_o for all transistors.
- Find the value of R_{in} .
- Find the value of R_{out} .
- Calculate the voltage gains v_o/v_i and v_o/v_{sig} .
- How large can v_{sig} be (peak-to-peak) while maintaining saturation-mode operation for Q_1 and Q_2 ?

8.56 For the CB amplifier, use Eq. (8.63) to explore the variation of the input resistance R_{in} with the load resistance R_L . Specifically, find R_{in} as a multiple of r_e for $R_L/r_o = 0, 1, 10, 100, 1000$, and ∞ . Let $\beta = 100$. Present your results in tabular form.

8.57 What value of load resistance R_L causes the input resistance of the CB amplifier to be approximately double the value of r_e ?

8.58 Show that for the CB amplifier,

$$\frac{R_{\text{out}}}{r_o} \approx 1 + \frac{\beta(r_e/r_e)}{\beta + 1 + (R_e/r_e)}$$

Generate a table for R_{out} as a multiple of r_o versus R_e as a multiple of r_e with entries for $R_e = 0, r_e, 2r_e, 10r_e, (\beta/2)r_e, \beta r_e$, and $1000r_e$. Let $\beta = 100$.

8.59 As mentioned in the text, the CB amplifier functions as a current buffer. That is, when fed with a current signal, it passes

it to the collector and supplies the output collector current at a high output resistance. Figure P8.59 shows a CB amplifier fed with a signal current i_{sig} having a source resistance $R_{\text{sig}} = 10 \text{ k}\Omega$. The BJT is specified to have $\beta = 100$ and $V_A = 50 \text{ V}$. (Note that the bias arrangement is not shown.) The output at the collector is represented by its Norton equivalent circuit. Find the value of the current gain k and the output resistance R_{out} . Note that k is the short-circuit current gain and should be evaluated using the T model of the transistor with the collector short-circuited to ground.

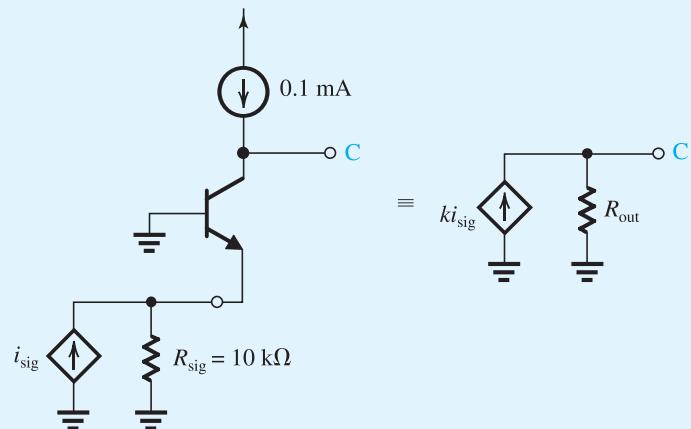


Figure P8.59

8.60 For the constant-current source circuit shown in Fig. P8.60, find the collector current I and the output resistance. The BJT is specified to have $\beta = 100$, $V_{BE} = 0.7 \text{ V}$, and $V_A = 100 \text{ V}$. If the collector voltage undergoes a change of 10 V while the BJT remains in the active mode, what is the corresponding change in collector current?

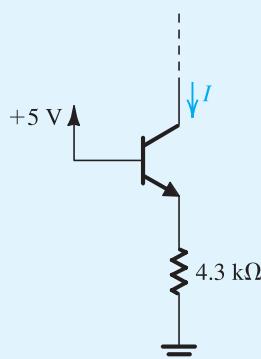


Figure P8.60

8.61 Find the value of the resistance R_o , which, when connected in the emitter lead of a CE BJT amplifier, raises the output resistance by a factor of (a) 5, (b) 10, and (c) 50. What is the maximum possible factor by which the output resistance can be raised, and at what value of R_o is it achieved? Assume the BJT has $\beta = 100$ and is biased at $I_C = 0.5$ mA.

Section 8.5: The Cascode Amplifier

D 8.62 In a MOS cascode amplifier, the cascode transistor is required to raise the output resistance by a factor of 50. If the transistor is operated at $V_{ov} = 0.2$ V, what must its V_A' be? If the process technology specifies V_A' as 5 V/ μm , what channel length must the transistor have?

D 8.63 For a cascode current source such as that in Fig. 8.32, show that if the two transistors are identical, the current I supplied by the current source and the output resistance R_o are related by $IR_o = 2|V_A|^2/|V_{ov}|$. Now consider the case of transistors that have $|V_A| = 4$ V and are operated at $|V_{ov}|$ of 0.2 V. Also, let $\mu_p C_{ox} = 100 \mu\text{A/V}^2$. Find the W/L ratios required and the output resistance realized for the two cases: (a) $I = 0.1$ mA and (b) $I = 0.5$ mA. Assume that V_{SD} for the two devices is the minimum required (i.e., $|V_{ov}|$).

D *8.64 For a cascode current source, such as that in Fig. 8.32, show that if the two transistors are identical, the current I supplied by the current source and the output resistance R_o are related by

$$IR_o = \frac{2|V_A|^2}{|V_{ov}|} L^2$$

Now consider the case of a 0.18- μm technology for which $|V_A'| = 5$ V/ μm and let the transistors be operated at $|V_{ov}| = 0.2$ V. Find the figure-of-merit IR_o for the three cases of L equal to the minimum channel length, twice the minimum, and three times the minimum. Complete the entries of the table at the bottom of the page. Give W/L and the area $2WL$ in terms of n , where n is the value of W/L for the case $I = 0.01$ mA. In the table, A_v denotes the gain obtained in a cascode amplifier such as that in Fig. 8.33 that utilizes our current source as load and which has the same values of g_m and R_o as the current-source transistors.

- (a) For each current value, what is price paid for the increase in R_o and A_v obtained as L is increased?
- (b) For each value of L , what advantage is obtained as I is increased, and what is the price paid? (Hint: We will see in Chapter 10 that the amplifier bandwidth increases with g_m .)
- (c) Contrast the performance obtained from the circuit with the largest area with that obtained from the circuit with the smallest area.

D 8.65 Design the cascode amplifier of Fig. 8.30(a) to obtain $g_{m1} = 2$ mA/V and $R_o = 200$ k Ω . Use a 0.18- μm technology for which $V_{tn} = 0.5$ V, $V_A' = 5$ V/ μm , and $k_n' = 400 \mu\text{A/V}^2$. Determine L , W/L , V_{G2} , and I . Use identical transistors operated at $V_{ov} = 0.25$ V, and design for the maximum possible negative signal swing at the output. What is the value of the minimum permitted output voltage?

8.66 The cascode amplifier of Fig. 8.33 is operated at a current of 0.2 mA with all devices operating at $|V_{ov}| = 0.20$ V.

$L = L_{\min} = 0.18 \mu\text{m}$				$L = 2L_{\min} = 0.36 \mu\text{m}$				$L = 3L_{\min} = 0.54 \mu\text{m}$			
$IR_o = \quad \text{V}$				$IR_o = \quad \text{V}$				$IR_o = \quad \text{V}$			
g_m (mA/V)	R_o (k Ω)	A_v (V/V)	$2WL$ (μm^2)	g_m (mA/V)	R_o (k Ω)	A_v (V/V)	$2WL$ (μm^2)	g_m (mA/V)	R_o (k Ω)	A_v (V/V)	$2WL$ (μm^2)
$I = 0.01 \text{ mA}$ $W/L = n$											
$I = 0.1 \text{ mA}$ $W/L =$											
$I = 1.0 \text{ mA}$ $W/L =$											

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All devices have $|V_A| = 4$ V. Find g_{m1} , the output resistance of the amplifier, R_{on} , the output resistance of the current source, R_{op} , the overall output resistance, R_o , and the voltage gain, A_v .

D 8.67 Design the CMOS cascode amplifier in Fig. 8.33 for the following specifications: $g_{m1} = 1$ mA/V and $A_v = -280$ V/V. Assume that for the available fabrication process, $|V_A| = 5$ V/ μm for both NMOS and PMOS devices and that $\mu_n C_{ox} = 4 \mu_p C_{ox} = 400 \mu\text{A}/\text{V}^2$. Use the same channel length L for all devices and operate all four devices at $|V_{ov}| = 0.25$ V. Determine the required channel length L , the bias current I , and the W/L ratio for each of four transistors. Assume that suitable bias voltages have been chosen, and neglect the Early effect in determining the W/L ratios.

D 8.68 Design the circuit of Fig. 8.32 to provide an output current of $100 \mu\text{A}$. Use $V_{DD} = 3.3$ V, and assume the PMOS transistors to have $\mu_p C_{ox} = 60 \mu\text{A}/\text{V}^2$, $V_{tp} = -0.8$ V, and $|V_A| = 5$ V. The current source is to have the widest possible signal swing at its output. Design for $V_{ov} = 0.2$ V, and specify the values of the transistor W/L ratios and of V_{G3} and V_{G4} . What is the highest allowable voltage at the output? What is the value of R_o ?

8.69 The cascode transistor can be thought of as providing a “shield” for the input transistor from the voltage variations at the output. To quantify this “shielding” property of the cascode, consider the situation in Fig. P8.69. Here we have grounded the input terminal (i.e., reduced v_i to zero), applied a small change v_x to the output node, and denoted the voltage change that results at the drain of Q_1 by v_y . By what factor is v_y smaller than v_x ?

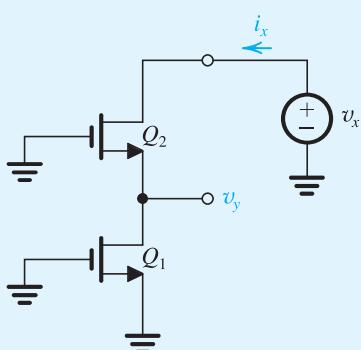


Figure P8.69

***8.70** In this problem we investigate whether, as an alternative to cascoding, we can simply increase the channel length L of the CS MOSFET. Specifically, we wish to compare the

two circuits shown in Fig. P8.70(b) and (c). The circuit in Fig. P8.70(b) is a CS amplifier in which the channel length has been quadrupled relative to that of the original CS amplifier in Fig. P8.70(a) while the drain bias current has been kept constant.

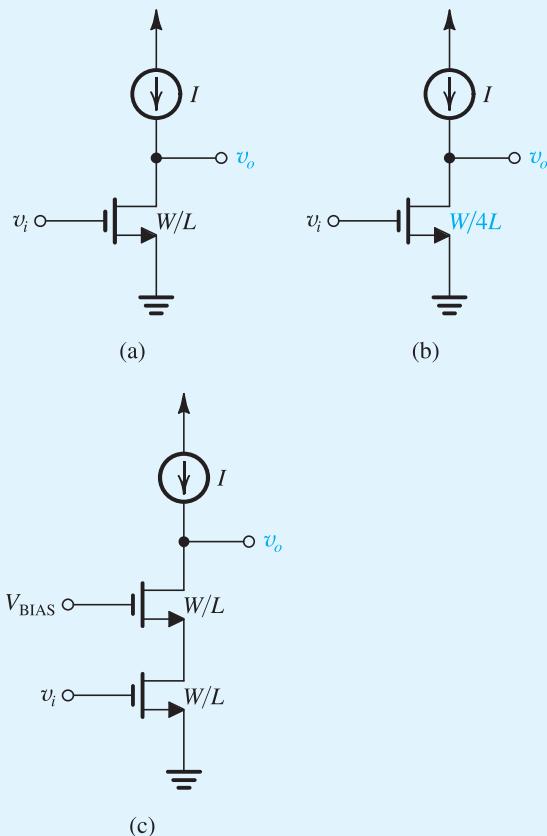


Figure P8.70

- Show that for this circuit V_{ov} is double that of the original circuit, g_m is half that of the original circuit, and $\frac{v_o}{v_i}$ is double that of the original circuit.
- Compare these values to those of the cascode circuit in Fig. P8.70(c), which is operating at the same bias current and has the same minimum voltage requirement at the drain as in the circuit of Fig. P8.70(b).

8.71 Consider the cascode amplifier of Fig. 8.33 with the dc component at the input $V_i = 0.6$ V, $V_{G2} = 0.9$ V, $V_{G3} = 0.4$ V, $V_{G4} = 0.7$ V, and $V_{DD} = 1.3$ V. If all devices are matched, that is, $k_{n1} = k_{n2} = k_{p3} = k_{p4}$, and have equal $|V_t|$ of 0.4 V, what is the overdrive voltage at which the four transistors are operating? What is the allowable voltage range at the output?

SIM 8.72 A CMOS cascode amplifier such as that in Fig. 8.34(a) has identical CS and CG transistors that have $W/L = 5.4 \mu\text{m}/0.36 \mu\text{m}$ and biased at $I = 0.2 \text{ mA}$. The fabrication process has $\mu_n C_{ox} = 400 \mu\text{A/V}^2$, and $V'_A = 5 \text{ V}/\mu\text{m}$. At what value of R_L does the gain become -100 V/V ? What is the voltage gain of the common-source stage?

8.73 The purpose of this problem is to investigate the signal currents and voltages at various points throughout a cascode

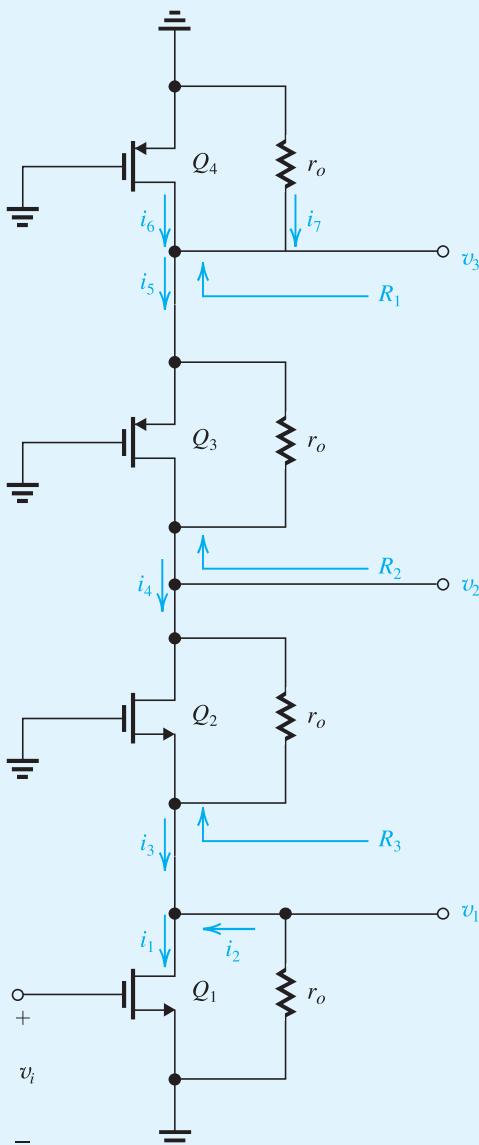


Figure P8.73

amplifier circuit. Knowledge of this signal distribution is very useful in designing the circuit so as to allow for the required signal swings. Figure P8.73 shows a CMOS cascode amplifier with all dc voltages replaced with signal grounds. As well, we have explicitly shown the resistance r_o of each of the four transistors. For simplicity, we are assuming that the four transistors have the same g_m and r_o . The amplifier is fed with a signal v_i .

- Determine R_1 , R_2 , and R_3 . Assume $g_m r_o \gg 1$.
- Determine i_1 , i_2 , i_3 , i_4 , i_5 , i_6 , and i_7 , all in terms of v_i . (Hint: Use the current-divider rule at the drain of Q_1 .)
- Determine v_1 , v_2 , and v_3 , all in terms of v_i .
- If v_i is a 5-mV peak sine wave and $g_m r_o = 20$, sketch and clearly label the waveforms of v_1 , v_2 , and v_3 .

D 8.74 Design the double-cascode current source shown in Fig. P8.74 to provide $I = 0.2 \text{ mA}$ and the largest possible signal swing at the output; that is, design for the minimum allowable voltage across each transistor. The $0.13-\mu\text{m}$ CMOS fabrication process available has $V_{tp} = -0.4 \text{ V}$, $V'_A = -6 \text{ V}/\mu\text{m}$, and $\mu_p C_{ox} = 100 \mu\text{A/V}^2$. Use devices with $L = 0.4 \mu\text{m}$, and operate at $|V_{ov}| = 0.2 \text{ V}$. Specify V_{G1} , V_{G2} , V_{G3} , and the W/L ratios of the transistors. What is the value of R_o achieved?

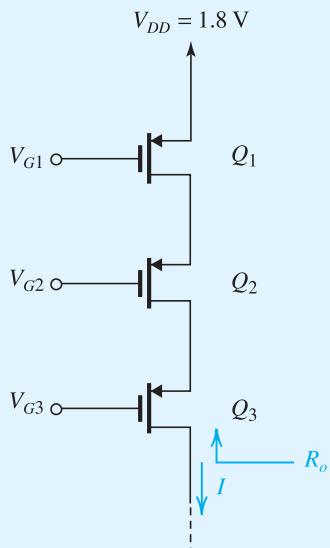


Figure P8.74

***8.75** Figure P8.75 shows a folded-cascode CMOS amplifier utilizing a simple current source Q_2 , supplying a current $2I$, and a cascaded current source (Q_4 , Q_5) supplying a current I . Assume, for simplicity, that all transistors have equal parameters g_m and r_o .

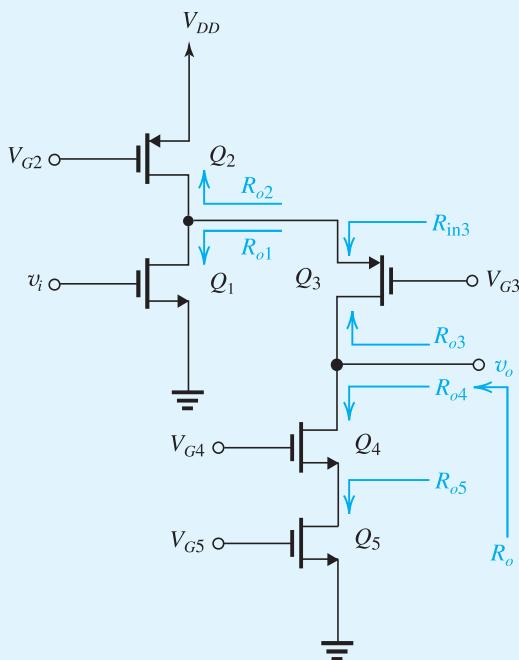


Figure P8.75

- (a) Give approximate expressions for all the resistances indicated.
 (b) Find the amplifier output resistance R_o .
 (c) Show that the short-circuit transconductance G_m is approximately equal to g_{m1} . Note that the short-circuit transconductance is determined by short-circuiting v_o to ground and finding the current that flows through the short circuit, $G_m v_i$.

- (d) Find the overall voltage gain v_o/v_i and evaluate its value for the case $g_{m1} = 2 \text{ mA/V}$ and $A_0 = 30$.

8.76 A cascode current source formed of two *pnp* transistors for which $\beta = 50$ and $V_A = 5 \text{ V}$ supplies a current of 0.2 mA . What is the output resistance?

8.77 Use Eq. (8.88) to show that for a BJT cascode current source utilizing identical *pnp* transistors and supplying a current I ,

$$IR_o = \frac{|V_A|}{(V_T/|V_A|) + (1/\beta)}$$

Evaluate the figure-of-merit IR_o for the case $|V_A| = 5 \text{ V}$ and $\beta = 50$. Now find R_o for the cases of $I = 0.1, 0.5$, and 1.0 mA .

8.78 Consider the BJT cascode amplifier of Fig. 8.38 for the case all transistors have equal β and r_o . Show that the voltage gain A_v can be expressed in the form

$$A_v = -\frac{1}{2} \frac{|V_A|/V_T}{(V_T/|V_A|) + (1/\beta)}$$

Evaluate A_v for the case $|V_A| = 5 \text{ V}$ and $\beta = 50$. Note that except for the fact that β depends on I as a second-order effect, the gain is independent of the bias current I !

8.79 A bipolar cascode amplifier has a current-source load with an output resistance βr_o . Let $\beta = 50$, $|V_A| = 100 \text{ V}$, and $I = 0.2 \text{ mA}$. Find the voltage gain A_v .

D *8.80 Figure P8.80 shows four possible realizations of the folded cascode amplifier. Assume that the BJTs have $\beta = 100$ and that both the BJTs and the MOSFETs have $|V_A| = 5 \text{ V}$.

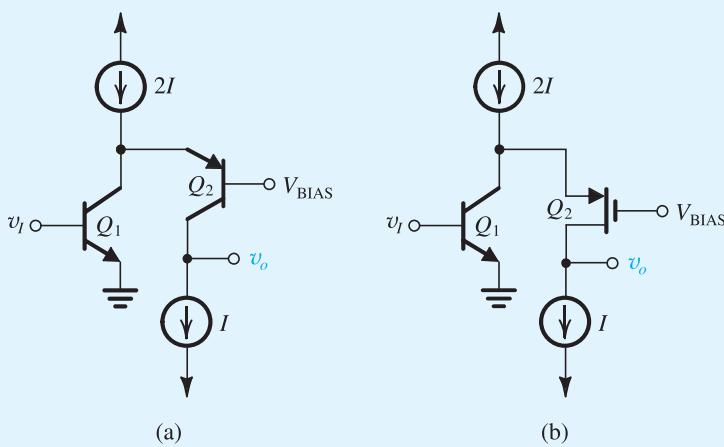
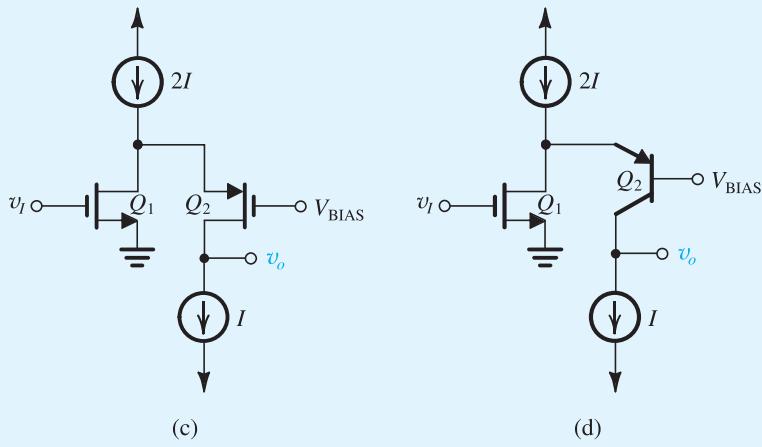


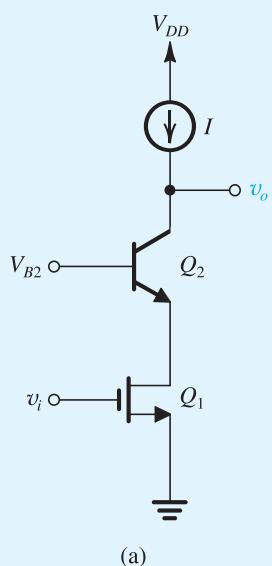
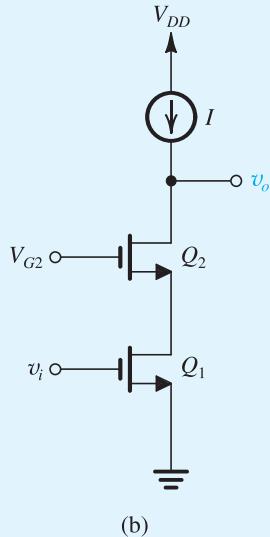
Figure P8.80

Figure P8.80 *continued*

Let $I = 100 \mu\text{A}$, and assume that the MOSFETs are operating at $|V_{ov}| = 0.2 \text{ V}$. Assume the current sources are ideal. For each circuit determine R_{in} , R_{out} , and A_{vo} . Comment on your results.

8.81 In this problem, we will explore the difference between using a BJT as cascode device and a MOSFET as cascode device. Refer to Fig. P8.81. Given the following data, calculate G_m , R_{out} , and A_{vo} for the circuits (a) and (b):

$$I = 100 \mu\text{A}, \beta = 125, \mu_n C_{ox} = 400 \mu\text{A/V}^2, W/L = 25, V_A = 1.8 \text{ V}$$

Figure P8.81 *continued*Figure P8.81 *continued*

Section 8.6: Current-Mirror Circuits with Improved Performance

SIM 8.82 In a particular cascaded current mirror, such as that shown in Fig. 8.39, all transistors have $V_t = 0.6 \text{ V}$, $\mu_n C_{ox} = 160 \mu\text{A/V}^2$, $L = 1 \mu\text{m}$, and $V_A = 10 \text{ V}$. Width $W_1 = W_4 = 4 \mu\text{m}$, and $W_2 = W_3 = 40 \mu\text{m}$. The reference current I_{REF} is $20 \mu\text{A}$. What output current results? What are the voltages at the gates of Q_2 and Q_3 ? What is the lowest voltage at the output for which current-source operation is possible? What are the values of g_m and

r_o of Q_2 and Q_3 ? What is the output resistance of the mirror?

8.83 Find the output resistance of the double-cascode current mirror of Fig. P8.83.

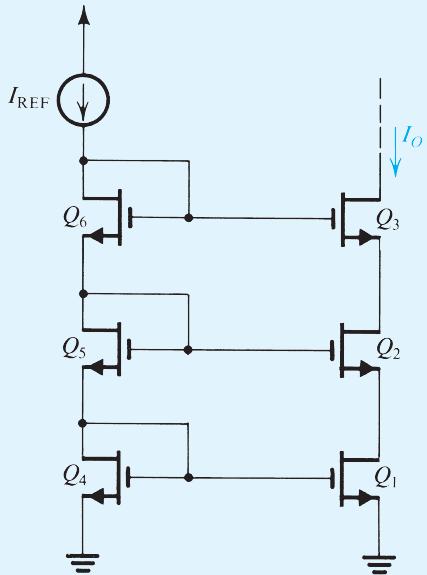


Figure P8.83

8.84 Consider the Wilson current-mirror circuit of Fig. 8.40 when supplied with a reference current I_{REF} of 1 mA. What is the change in I_o corresponding to a change of +10 V in the voltage at the collector of Q_3 ? Give both the absolute value and the percentage change. Let $\beta = 100$ and $V_A = 100$ V.

D 8.85 (a) The circuit in Fig. P8.85 is a modified version of the Wilson current mirror. Here the output transistor is “split” into two matched transistors, Q_3 and Q_4 . Find I_{o1} and I_{o2} in terms of I_{REF} . Assume all transistors to be matched with current gain β .

(b) Use this idea to design a circuit that generates currents of 0.1 mA, 0.2 mA, and 0.4 mA, using a reference current source of 0.7 mA. What are the actual values of the currents generated for $\beta = 50$?

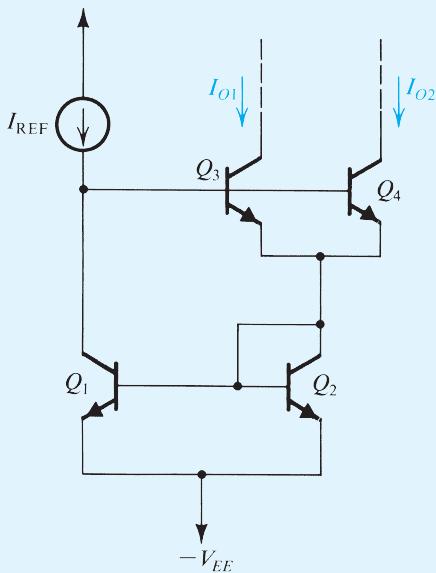


Figure P8.85

D 8.86 Use the *pnp* version of the Wilson current mirror to design a 0.1-mA current source. The current source is required to operate with the voltage at its output terminal as low as -2.5 V. If the power supplies available are ± 2.5 V, what is the highest voltage possible at the output terminal?

***8.87** For the Wilson current mirror of Fig. 8.40, show that the incremental input resistance seen by I_{REF} is approximately $2V_T/I_{\text{REF}}$. (Neglect the Early effect in this derivation and assume a signal ground at the output.) Evaluate R_{in} for $I_{\text{REF}} = 0.2$ mA.

***8.88** Consider the Wilson MOS mirror of Fig. 8.41(a) for the case of all transistors identical, with $W/L = 10$, $\mu_n C_{ox} = 400 \mu\text{A/V}^2$, $V_m = 0.5$ V, and $V_A = 18$ V. The mirror is fed with $I_{\text{REF}} = 180 \mu\text{A}$.

- Obtain an estimate of V_{ov} and V_{gs} at which the three transistors are operating, by neglecting the Early effect.
- Noting that Q_1 and Q_2 are operating at different V_{ds} , obtain an approximate value for the difference in their currents and hence determine I_o .
- To eliminate the systematic error between I_o and I_{REF} caused by the difference in V_{ds} between Q_1 and Q_2 , a diode-connected transistor Q_4 can be added to the circuit

as shown in Fig. 8.41(c). What do you estimate I_o now to be?

- (d) What is the minimum allowable voltage at the output node of the mirror?
- (e) Convince yourself that Q_4 will have no effect on the output resistance of the mirror. Find R_o .
- (f) What is the change in I_o (both absolute value and percentage) that results from $\Delta V_o = 1 \text{ V}$?

8.89 Show that the incremental input resistance (seen by I_{REF}) for the Wilson MOS mirror of Fig. 8.41(a) is $2/g_m$. Assume that all three transistors are identical and neglect the Early effect. Also, assume a signal ground at the output. (*Hint:* Replace all transistors by their T model and remember that Q_1 is equivalent to a resistance $1/g_m$.)

- D 8.90** (a) Utilizing a reference current of $200 \mu\text{A}$, design a Widlar current source to provide an output current of $20 \mu\text{A}$. Assume β to be high.
 (b) If $\beta = 200$ and $V_A = 50 \text{ V}$, find the value of the output resistance, and find the change in output current corresponding to a 5-V change in output voltage.

D 8.91 Design three Widlar current sources, each having a $100\text{-}\mu\text{A}$ reference current: one with a current transfer ratio of 0.8, one with a ratio of 0.10, and one with a ratio of 0.01, all assuming high β . For each, find the output resistance, and contrast it with r_o of the basic unity-ratio source that is providing the desired current and for which $R_E = 0$. Use $\beta = \infty$ and $V_A = 50 \text{ V}$.

- D 8.92** (a) For the circuit in Fig. P8.92, assume BJTs with high β and $v_{BE} = 0.7 \text{ V}$ at 1 mA . Find the value of R that will result in $I_o = 10 \mu\text{A}$.
 (b) For the design in (a), find R_o assuming $\beta = 100$ and $V_A = 40 \text{ V}$.

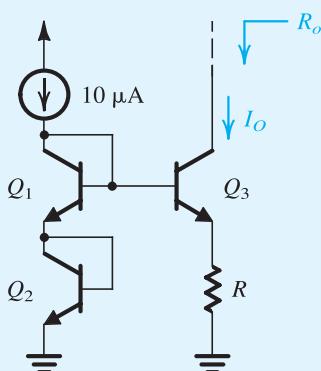


Figure P8.92

D 8.93 If the *pnp* transistor in the circuit of Fig. P8.93 is characterized by its exponential relationship with a scale current I_s , show that the dc current I is determined by $IR = V_T \ln(I/I_s)$. Assume Q_1 and Q_2 to be matched and Q_3 , Q_4 , and Q_5 to be matched. Find the value of R that yields a current $I = 200 \mu\text{A}$. For the BJT, $V_{EB} = 0.7 \text{ V}$ at $I_E = 1 \text{ mA}$.

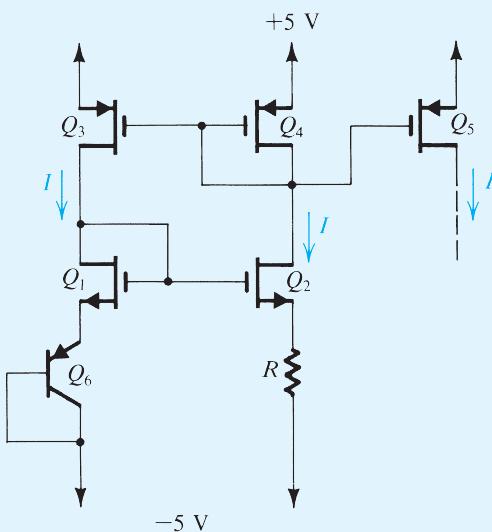


Figure P8.93

Section 8.7: Some Useful Transistor Pairings

8.94 Use the source-follower equivalent circuit in Fig. 8.45(b) to show that its output resistance is given by

$$R_o = r_{o3} \parallel r_{o1} \parallel \frac{1}{g_m + g_{mb}} \approx \frac{1}{g_m + g_{mb}}$$

8.95 A source follower for which $k'_n = 200 \mu\text{A/V}^2$, $V'_A = 20 \text{ V}/\mu\text{m}$, $\chi = 0.2$, $L = 0.5 \mu\text{m}$, $W = 20 \mu\text{m}$, and $V_t = 0.6 \text{ V}$ is required to provide a dc level shift (between input and output of 0.9 V .) What must the bias current be? Find g_m , g_{mb} , r_o , A_{vo} , and R_o . Assume that the bias current source has an output resistance equal to r_o . Also find the voltage gain when a load resistance of $2 \text{ k}\Omega$ is connected to the output.

8.96 The transistors in the circuit of Fig. P8.96 have $\beta = 100$ and $V_A = 50 \text{ V}$.

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- (a) Find R_{in} and the overall voltage gain.
 (b) What is the effect of increasing the bias currents by a factor of 10 on R_{in} , G_v , and the power dissipation?

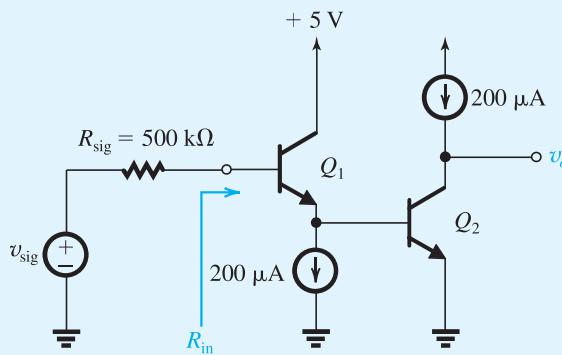


Figure P8.96

D *8.97 Consider the BiCMOS amplifier shown in Fig. P8.97. The BJT has $V_{BE} = 0.7$ V and $\beta = 200$. The MOSFET has $V_t = 1$ V and $k_n = 2 \text{ mA/V}^2$. Neglect the Early effect in both devices.

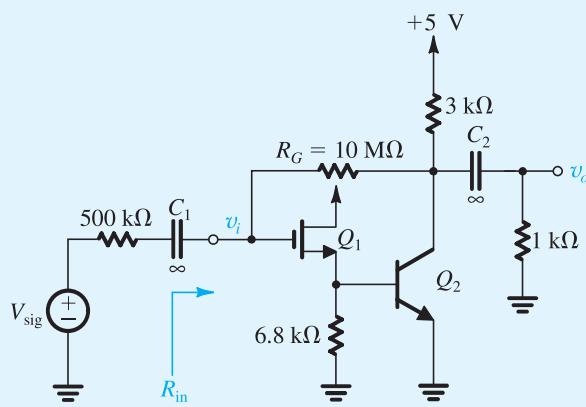


Figure P8.97

- (a) Consider the dc bias circuit. Neglect the base current in Q_2 in determining the current in Q_1 . Find the dc bias currents in Q_1 and Q_2 and show that they are approximately $100 \mu\text{A}$ and 1 mA , respectively.
 (b) Evaluate the small-signal parameters of Q_1 and Q_2 at their bias points.
 (c) Determine the voltage gain $A_v = v_o/v_i$. For this purpose you can neglect R_G .

- (d) Noting that R_G is connected between the input node where the voltage is v_i and the output node where the voltage is $A_v v_i$, find R_{in} and hence the overall voltage gain v_o/v_{sig} .
 (e) To considerably reduce the effect of R_G on R_{in} and hence on G_v , consider the effect of adding another $10\text{-M}\Omega$ resistor in series with the existing one and placing a large bypass capacitor between their joint node and ground. What will R_{in} and G_v become?

8.98 The BJTs in the Darlington follower of Fig. P8.98 have $\beta = 100$. If the follower is fed with a source having a $100\text{-k}\Omega$ resistance and is loaded with $1 \text{ k}\Omega$, find the input resistance and the output resistance (excluding the load). Also find the overall voltage gain, both open-circuited and with load. Neglect the Early effect.

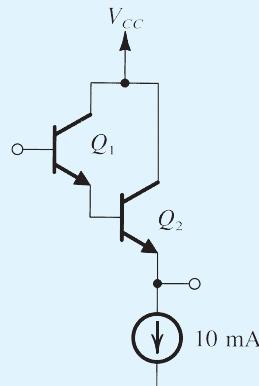


Figure P8.98

8.99 For the amplifier in Fig. 8.48(a), let $I = 0.5 \text{ mA}$ and $\beta = 100$, and neglect r_o . Assume that a load resistance of $10 \text{ k}\Omega$ is connected to the output terminal. If the amplifier is fed with a signal v_{sig} having a source resistance $R_{sig} = 10 \text{ k}\Omega$, find G_v .

8.100 Consider the CD-CG amplifier of Fig. 8.48(c) for the case $g_m = 5 \text{ mA/V}$, $R_{sig} = 500 \text{ k}\Omega$, and $R_L = 10 \text{ k}\Omega$. Neglecting r_o , find G_v .

***8.101** In each of the six circuits in Fig. P8.101, let $\beta = 100$, and neglect r_o . Calculate the overall voltage gain.

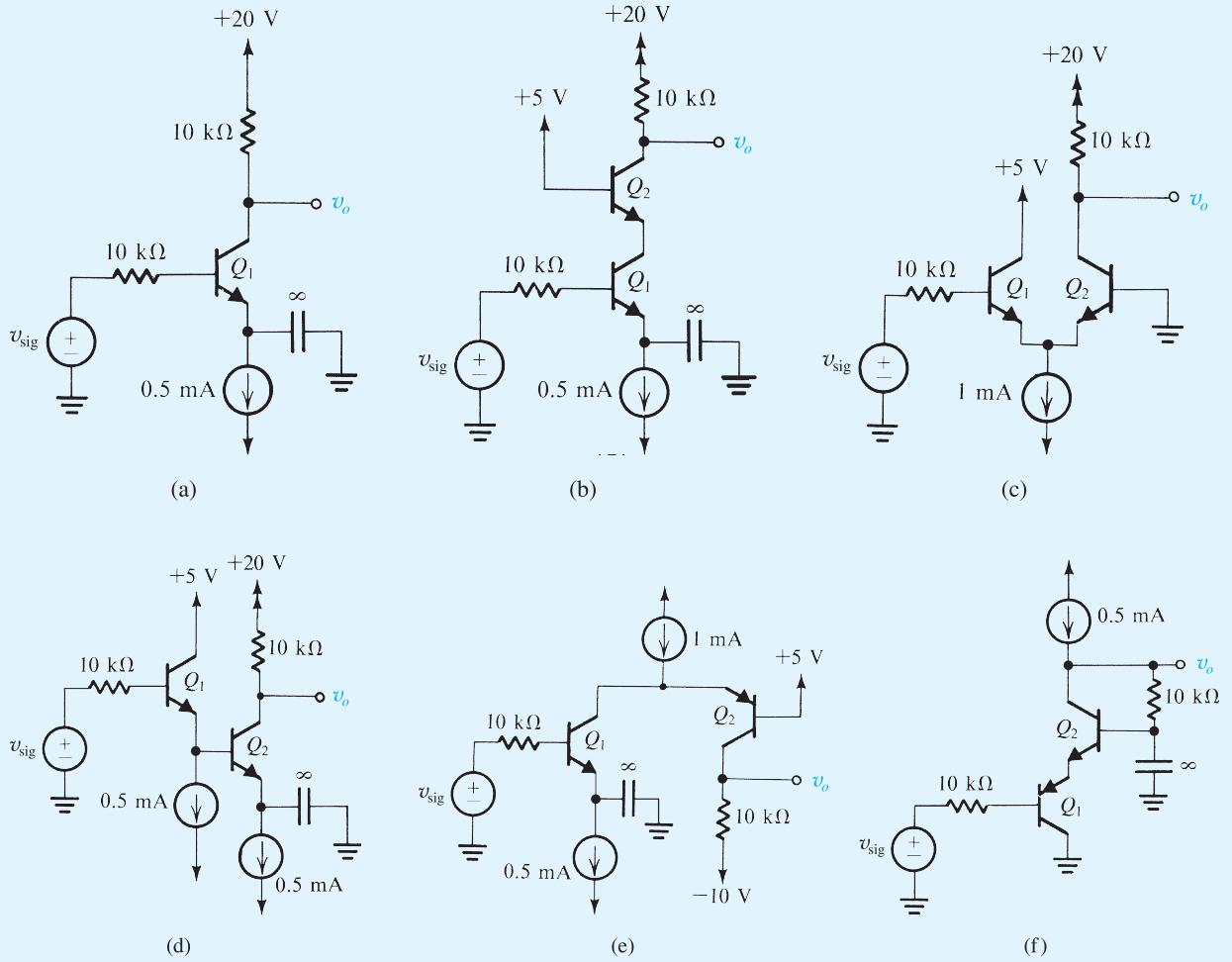


Figure P8.101