EE 236: Experiment No. 6
Study of NMOS and CMOS Characteristics

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1 Overview of the experiment

1.1 Aim of the experiment

The following were the aims of the experiment:

- To measure transfer characteristics of NMOS transistor.
- To analyse the effect of body bias on the characteristics of a NMOS transistor.
- To obtain voltage transfer characteristics of CMOS inverter.
- To obtain transfer characteristics of CMOS inverter.

1.2 Methods

The method overview includes constructing circuit netlists according to the standard circuit, simulating them using *dc* or *tran* analysis and calculating required parameters for all parts. The first plot required us to plot $I_D - V_{DS}$ characteristics, and calculate r_{DS}, Early Voltage (V_0), and r_0. The second and third plots required us to plot $I_D - V_{GS}$ characteristics, and find V_T, g_m and k. The further parts required us to simulate DC and Transient characteristics of a CMOS Inverter and calculate associated values such as Switching Threshold Voltage, rise time, fall time, and propagation delay.

2 Design

2.1 Part 1

The netlist according to the following circuit diagram was made which included an NMOS transistor and voltage sources.

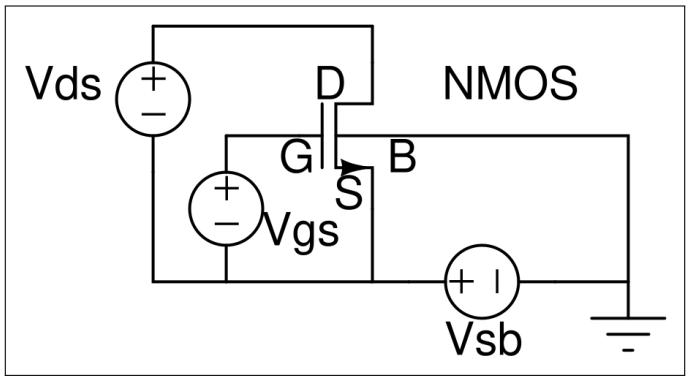


Figure 1: The I-V Characterization Circuit

DC analysis was performed by varying V_{DS} from 0V to 5V in steps of 0.001V and V_{GS} from 2.5V to 4V in steps of 0.5V to obtain the I-V characteristic plots. R_{DS} in the linear region was found using:

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_{DS}}$$

V_0 was found as the x-intercept of the equation in the saturation region:

$$y = mx + c$$

R_0 in the saturation region was found using:

$$R_0 = \frac{\Delta V_{DS}}{\Delta I_{DS}}$$

2.2 Part 2

I_D was plotted against V_{GS}, first keeping $V_{DS} = 200mV$ (linear) and then $V_{DS} = 5V$ (saturation). V_T and g_m were found from the plot.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Then, k was found from the slope of the $\sqrt{I_D}$ vs V_{GS}.

$$k = 2.\left(\frac{\Delta\sqrt{I_D}}{\Delta V_{GS}}\right)^2$$

2.3 Part 3

V_{DS} was set to 200mV. DC analysis was performed by varying V_{GS} from 0V to 5V in steps of 0.001V and V_{SB} from 0V to 4V in steps of 1V to obtain the I-V characteristic plots. V_T values were obtained from the plot and plotted against V_{SB}. γ was calculated from:

$$V_T = V_{T0} + \gamma.(\sqrt{\phi_s - V_{SB}} - \sqrt{\phi_s})$$

2.4 CMOS Inverter DC Characteristics

The netlist according to the following circuit diagram was made which included an NMOS transistor, a PMOS transistor and voltage sources.

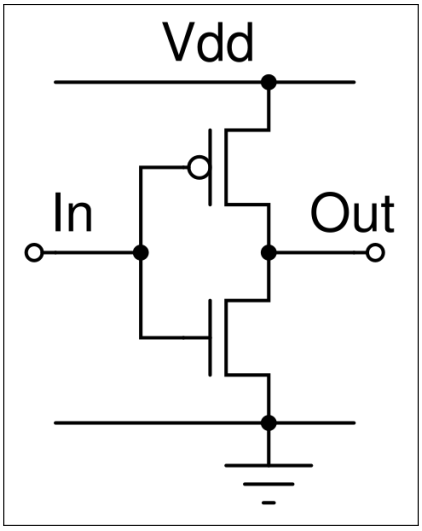


Figure 2: The DC Characterization Circuit

DC analysis was performed by varying V_{in} from 0V to 3.3V in steps of 0.01V. This was done for all three: $W_p/W_n = 60\mu m/30\mu m$, $W_p/W_n = 60\mu m/60\mu m$, and $W_p/W_n = 30\mu m/60\mu m$. The corresponding Switching Threshold Voltages were measured as the voltage at which $V_{out} = V_{in}$.
Next, supply voltage, V_{DD}, was varied as 1.5 and 3V for $W_p/W_n = 60\mu m/30\mu m$ and plots were obtained.

2.5 CMOS Inverter Transient Charcteristics

Transient analysis was performed with a square wave input of $125MHz$ frequency, rise and fall times of $20ps$ on a CMOS Inverter having a load capacitance of $0.05pF$ and $V_{DD} = 3.3V$.
Rise and Fall times, and Propagation Delay were calculated for $W_p/W_n = 60\mu m/30\mu m$, $W_p/W_n = 60\mu m/60\mu m$, and $W_p/W_n = 30\mu m/60\mu m$.
Then, The supply voltage was varied as {2, 2.2, 2.4, 2.6, 2.8, 3, 3.3}V for $W_p/W_n = 60\mu m/30\mu m$ and propagation delays were plotted.

3 Simulation results

3.1 Code snippets

3.1.1 NMOS Part 1

```
Vinamra Baghel 190010070 Part 1 Id-Vds Characteristics
.include ALD1105N.txt

*Netlist
M1 d g s b ALD1105N
Vgs g s dc 2.5
Vds d s dc 0
Vsb s b dc 0
Vb b 0 dc 0

*Analysis
.dc Vds 0 5 0.001 Vgs 2.5 4 0.5

.control
run
let Id1 = -I(Vds)[0, 5000]
let Id2 = -I(Vds)[5001, 10001]
let Id3 = -I(Vds)[10002, 15002]
let Id4 = -I(Vds)[15003, 20003]
let Vds1 = V(d)[0, 5000]
let Vds2 = V(d)[5001, 10001]
let Vds3 = V(d)[10002, 15002]
let Vds4 = V(d)[15003, 20003]
plot Id1 vs Vds1 Id2 vs Vds2 Id3 vs Vds3 Id4 vs Vds4

meas dc i11 find Id1 when Vds1 = 2m
meas dc i12 find Id1 when Vds1 = 5m
let rds1 = 3m/(i12-i11)
meas dc i21 find Id2 when Vds2 = 2m
meas dc i22 find Id2 when Vds2 = 5m
let rds2 = 3m/(i22-i21)
meas dc i31 find Id3 when Vds3 = 2m
meas dc i32 find Id3 when Vds3 = 5m
let rds3 = 3m/(i32-i31)
meas dc i41 find Id4 when Vds4 = 2m
meas dc i42 find Id4 when Vds4 = 5m
let rds4 = 3m/(i42-i41)
print rds1 rds2 rds3 rds4

meas dc i511 find Id1 when Vds1 = 4900m
meas dc i512 find Id1 when Vds1 = 5
let Vo1 = (4900m*i512-5*i511)/(i512-i511)
let ro1 = 100m/(i512-i511)
meas dc i521 find Id2 when Vds2 = 4900m
meas dc i522 find Id2 when Vds2 = 5
```

```
let Vo2 = (4900m*i522-5*i521)/(i522-i521)
let ro2 = 100m/(i522-i521)
meas dc i531 find Id3 when Vds3 = 4900m
meas dc i532 find Id3 when Vds3 = 5
let Vo3 = (4900m*i532-5*i531)/(i532-i531)
let ro3 = 100m/(i532-i531)
meas dc i541 find Id4 when Vds4 = 4900m
meas dc i542 find Id4 when Vds4 = 5
let Vo4 = (4900m*i542-5*i541)/(i542-i541)
let ro4 = 100m/(i542-i541)
print Vo1 Vo2 Vo3 Vo4
print ro1 ro2 ro3 ro4
.endc
.end
```

3.1.2 NMOS Part 2

```
Vinamra Baghel 190010070 Part 2 Id-Vgs Characteristics
.include ALD1105N.txt

*Netlist
M1 d g s b ALD1105N
Vgs g s dc 0
Vds d s dc 5
Vsb s b dc 0
Vb b 0 dc 0

*Analysis
.dc Vgs 0 5 0.001

.control
run
let Id = -I(Vds)
let Vdiff = V(g)-V(s)
plot Id vs Vdiff

meas dc Vt find Vdiff when Id = 1u

meas dc i1 find Id when Vdiff = 4
meas dc i2 find Id when Vdiff = 4010m
let gm = (i2-i1)/10m
print gm

let SId = sqrt(Id)
plot SId vs Vdiff
meas dc si1 find SId when Vdiff = 4
meas dc si2 find SId when Vdiff = 4010m
let k = 2*((si2-si1)/10m)^2
print k
.endc
```

```
.end
```

3.1.3 NMOS Part 3

```
Vinamra Baghel 190010070 Part 3 Id-Vgs Characteristics
.include ALD1105N.txt

*Netlist
M1 d g s b ALD1105N
Vgs g s dc 0
Vds d s dc 200m
Vsb s b dc 0
Vb b 0 dc 0

*Analysis
.dc Vgs 0 5 0.001 Vsb 0 4 1

.control
run
let Id1 = -I(Vds)[0, 5000]
let Id2 = -I(Vds)[5001, 10001]
let Id3 = -I(Vds)[10002, 15002]
let Id4 = -I(Vds)[15003, 20003]
let Id5 = -I(Vds)[20004, 25004]
let Vdiff = V(g)[0, 5000]-V(s)[0, 5000]

plot Id1 vs Vdiff Id2 vs Vdiff Id3 vs Vdiff Id4 vs Vdiff Id5 vs
   Vdiff

meas dc Vt1 find Vdiff when Id1 = 1u
meas dc Vt2 find Vdiff when Id2 = 1u
meas dc Vt3 find Vdiff when Id3 = 1u
meas dc Vt4 find Vdiff when Id4 = 1u
meas dc Vt5 find Vdiff when Id5 = 1u
print Vt1 Vt2 Vt3 Vt4 Vt5
.endc
.end
```

3.1.4 CMOS1

```
Vinamra Baghel 190010070 CMOS Inverter
.include CMOS.txt

*Netlist
M11 out1 in dd dd cmosp L=0.4u W=60u AS={2*60u*0.4u} PS={2*60u
   +4*0.4u} AD={2*60u*0.4u} PD={2*60u+4*0.4u}
M12 out1 in 0 0 cmosn L=0.4u W=30u AS={2*30u*0.4u} PS={2*30u+4*0.4u
   } AD={2*30u*0.4u} PD={2*30u+4*0.4u}
Cl1 out1 0 0.05p

```

```
M21 out2 in dd dd cmosp L=0.4u W=60u AS={2*60u*0.4u} PS={2*60u
   +4*0.4u} AD={2*60u*0.4u} PD={2*60u+4*0.4u}
M22 out2 in 0 0 cmosn L=0.4u W=60u AS={2*60u*0.4u} PS={2*60u+4*0.4u
   } AD={2*60u*0.4u} PD={2*60u+4*0.4u}
Cl2 out2 0 0.05p

M31 out3 in dd dd cmosp L=0.4u W=30u AS={2*30u*0.4u} PS={2*30u
   +4*0.4u} AD={2*30u*0.4u} PD={2*30u+4*0.4u}
M32 out3 in 0 0 cmosn L=0.4u W=60u AS={2*60u*0.4u} PS={2*60u+4*0.4u
   } AD={2*60u*0.4u} PD={2*60u+4*0.4u}
Cl3 out3 0 0.05p

Vdd dd 0 3.3
Vin in 0 0

*Analysis
.dc Vin 0 3.3 0.01

.control
run
plot V(out1) vs V(in) V(out2) vs V(in) V(out3) vs V(in)
meas dc Vth1 find V(out1) when V(out1)=V(in)
meas dc Vth2 find V(out2) when V(out2)=V(in)
meas dc Vth3 find V(out3) when V(out3)=V(in)
print Vth1 Vth2 Vth3
.endc
.end
```

3.1.5 CMOS2

```
Vinamra Baghel 190010070 CMOS Inverter
.include CMOS.txt

*Netlist
M11 out1 in dd dd cmosp L=0.4u W=60u AS={2*60u*0.4u} PS={2*60u
   +4*0.4u} AD={2*60u*0.4u} PD={2*60u+4*0.4u}
M12 out1 in 0 0 cmosn L=0.4u W=30u AS={2*30u*0.4u} PS={2*30u+4*0.4u
   } AD={2*30u*0.4u} PD={2*30u+4*0.4u}
Cl1 out1 0 0.05p

Vdd dd 0 3.3
Vin in 0 0

*Analysis
.dc Vin 0 3.3 0.01 Vdd 1.5 3 1.5

.control
run
let Vout1 = V(out1)[0, 330]
let Vout2 = V(out1)[331, 661]
```

```
plot Vout1 vs V(in)[0, 330] Vout2 vs V(in)[331, 661]
.endc
.end
```

3.1.6 CMOS3

```
Vinamra Baghel 190010070 CMOS Inverter Transient Characteristics
.include CMOS.txt

*Netlist
M11 out1 in dd dd cmosp L=0.4u W=60u AS=48p PS=121.6u AD=48p PD
   =121.6u
M12 out1 in 0 0 cmosn L=0.4u W=30u AS=24p PS=61.6u AD=24p PD=61.6u
Cl1 out1 0 0.05p

M21 out2 in dd dd cmosp L=0.4u W=60u AS=48p PS=121.6u AD=48p PD
   =121.6u
M22 out2 in 0 0 cmosn L=0.4u W=60u AS=48p PS=121.6u AD=48p PD=121.6
   u
Cl2 out2 0 0.05p

M31 out3 in dd dd cmosp L=0.4u W=30u AS=24p PS=61.6u AD=24p PD=61.6
   u
M32 out3 in 0 0 cmosn L=0.4u W=60u AS=48p PS=121.6u AD=48p PD=121.6
   u
Cl3 out3 0 0.05p

Vdd dd 0 3.3
Vin in 0 pulse(0 3.3 0 20p 20p 4n 8n 0)

*Analysis
.tran 0.01n 10n

.control
run
plot V(in) V(out1) V(out2) V(out3)

meas tran tr1 trig V(out1) val=0.1*3.3 td=0 rise=1 targ V(out1) val
   =0.9*3.3 td=0 rise=1
meas tran tf1 trig V(out1) val=0.9*3.3 td=0 fall=2 targ V(out1) val
   =0.1*3.3 td=0 fall=2
meas tran tr2 trig V(out2) val=0.1*3.3 td=0 rise=1 targ V(out2) val
   =0.9*3.3 td=0 rise=1
meas tran tf2 trig V(out2) val=0.9*3.3 td=0 fall=2 targ V(out2) val
   =0.1*3.3 td=0 fall=2
meas tran tr3 trig V(out3) val=0.1*3.3 td=0 rise=1 targ V(out3) val
   =0.9*3.3 td=0 rise=1
meas tran tf3 trig V(out3) val=0.9*3.3 td=0 fall=2 targ V(out3) val
   =0.1*3.3 td=0 fall=2
print tr1 tf1 tr2 tf2 tr3 tf3
```

```

meas tran tin when V(in)=1.65
meas tran tout1 when V(out1)=1.65
print tout1-tin
meas tran tout2 when V(out2)=1.65
print tout2-tin
meas tran tout3 when V(out3)=1.65
print tout3-tin
.endc
.end
```

3.1.7 CMOS4

```
Vinamra Baghel 190010070 CMOS Inverter Transient Characteristics
.include CMOS.txt

*Netlist
M11 out1 in1 dd1 dd1 cmosp L=0.4u W=60u AS=48p PS=121.6u AD=48p PD
   =121.6u
M12 out1 in1 0 0 cmosn L=0.4u W=30u AS=24p PS=61.6u AD=24p PD=61.6u
Cl1 out1 0 0.05p
Vdd1 dd1 0 2
Vin1 in1 0 pulse(0 2 0 20p 20p 4n 8n 0)

M21 out2 in2 dd2 dd2 cmosp L=0.4u W=60u AS=48p PS=121.6u AD=48p PD
   =121.6u
M22 out2 in2 0 0 cmosn L=0.4u W=30u AS=24p PS=61.6u AD=24p PD=61.6u
Cl2 out2 0 0.05p
Vdd2 dd2 0 2.2
Vin2 in2 0 pulse(0 2.2 0 20p 20p 4n 8n 0)

M31 out3 in3 dd3 dd3 cmosp L=0.4u W=60u AS=48p PS=121.6u AD=48p PD
   =121.6u
M32 out3 in3 0 0 cmosn L=0.4u W=30u AS=24p PS=61.6u AD=24p PD=61.6u
Cl3 out3 0 0.05p
Vdd3 dd3 0 2.4
Vin3 in3 0 pulse(0 2.4 0 20p 20p 4n 8n 0)

M41 out4 in4 dd4 dd4 cmosp L=0.4u W=60u AS=48p PS=121.6u AD=48p PD
   =121.6u
M42 out4 in4 0 0 cmosn L=0.4u W=30u AS=24p PS=61.6u AD=24p PD=61.6u
Cl4 out4 0 0.05p
Vdd4 dd4 0 2.6
Vin4 in4 0 pulse(0 2.6 0 20p 20p 4n 8n 0)

M51 out5 in5 dd5 dd5 cmosp L=0.4u W=60u AS=48p PS=121.6u AD=48p PD
   =121.6u
M52 out5 in5 0 0 cmosn L=0.4u W=30u AS=24p PS=61.6u AD=24p PD=61.6u
Cl5 out5 0 0.05p
Vdd5 dd5 0 2.8
```

```
Vin5 in5 0 pulse(0 2.8 0 20p 20p 4n 8n 0)

M61 out6 in6 dd6 dd6 cmosp L=0.4u W=60u AS=48p PS=121.6u AD=48p PD
   =121.6u
M62 out6 in6 0 0 cmosn L=0.4u W=30u AS=24p PS=61.6u AD=24p PD=61.6u
Cl6 out6 0 0.05p
Vdd6 dd6 0 3
Vin6 in6 0 pulse(0 3 0 20p 20p 4n 8n 0)

M71 out7 in7 dd7 dd7 cmosp L=0.4u W=60u AS=48p PS=121.6u AD=48p PD
   =121.6u
M72 out7 in7 0 0 cmosn L=0.4u W=30u AS=24p PS=61.6u AD=24p PD=61.6u
Cl7 out7 0 0.05p
Vdd7 dd7 0 3.3
Vin7 in7 0 pulse(0 3.3 0 20p 20p 4n 8n 0)

*Analysis
.tran 0.1n 20n

.control
run
meas tran tin1 when V(in1)=1
meas tran tin2 when V(in2)=1.1
meas tran tin3 when V(in3)=1.2
meas tran tin4 when V(in4)=1.3
meas tran tin5 when V(in5)=1.4
meas tran tin6 when V(in6)=1.5
meas tran tin7 when V(in7)=1.65
meas tran tout1 when V(out1)=1
meas tran tout2 when V(out2)=1.1
meas tran tout3 when V(out3)=1.2
meas tran tout4 when V(out4)=1.3
meas tran tout5 when V(out5)=1.4
meas tran tout6 when V(out6)=1.5
meas tran tout7 when V(out7)=1.65
let tp1 = tout1-tin1
let tp2 = tout2-tin2
let tp3 = tout3-tin3
let tp4 = tout4-tin4
let tp5 = tout5-tin5
let tp6 = tout6-tin6
let tp7 = tout7-tin7
print tp1 tp2 tp3 tp4 tp5 tp6 tp7
.endc
.end
```

3.2 Simulation results

3.2.1 Part 1

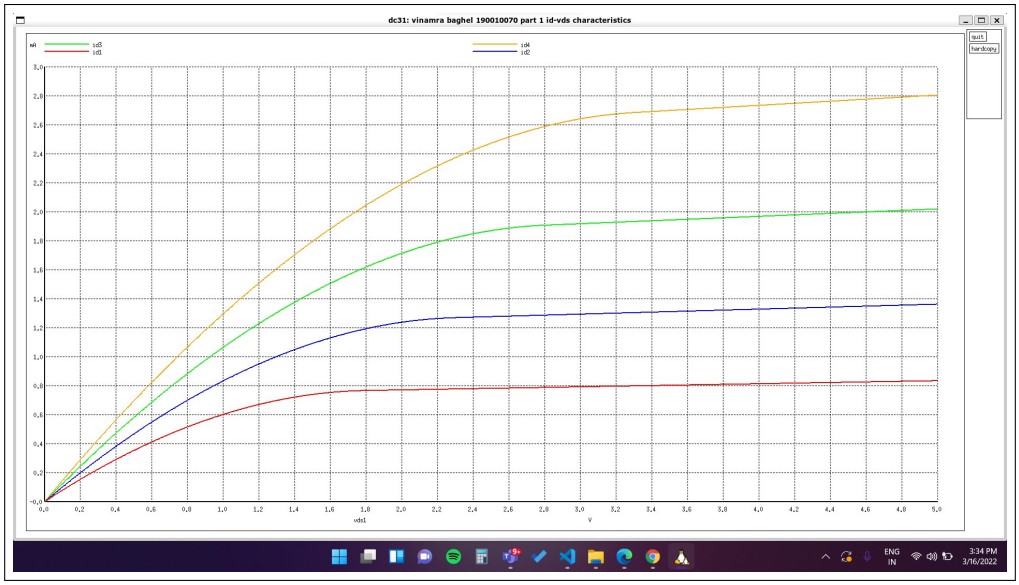
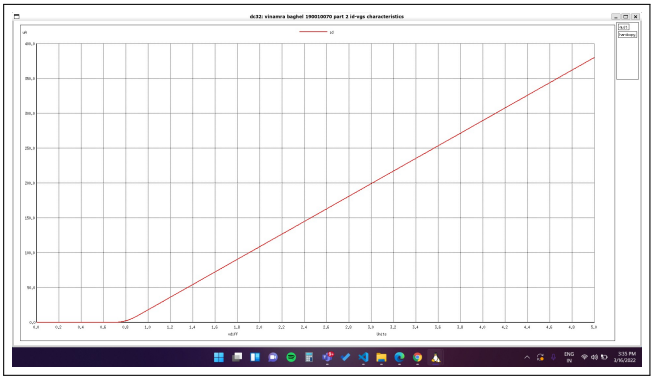
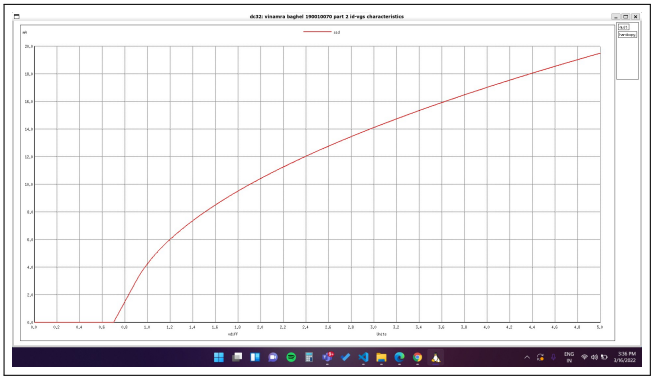


Figure 3: $I_D - V_{DS}$ Characteristics

3.2.2 Part 2

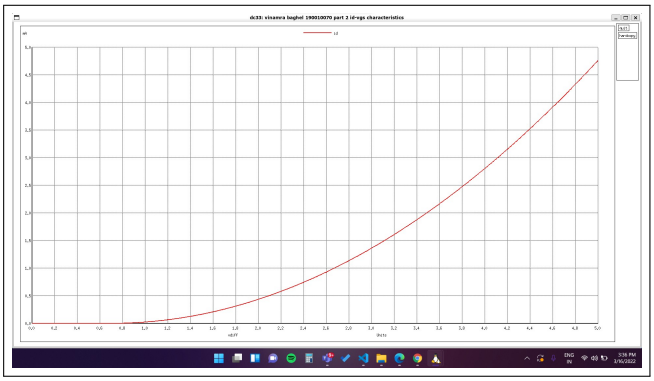


(a) $I_D - V_{GS}$

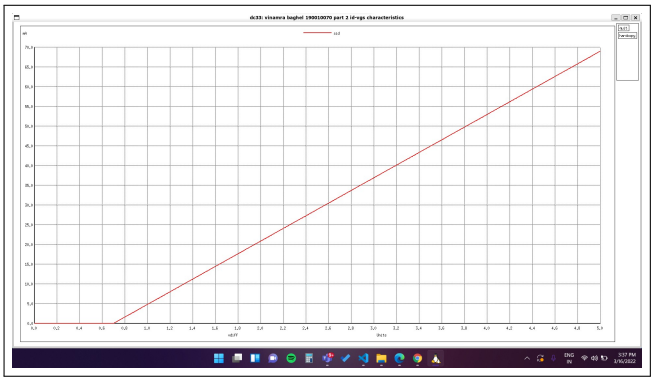


(b) $\sqrt{I_D} - V_{GS}$

Figure 4: $I_D - V_{GS}$ and $\sqrt{I_D} - V_{GS}$ Characteristics for $V_{DS} = 200mV$



(a) $I_D - V_{GS}$



(b) $\sqrt{I_D} - V_{GS}$

Figure 5: $I_D - V_{GS}$ and $\sqrt{I_D} - V_{GS}$ Characteristics for $V_{DS} = 5V$

3.2.3 Part 3

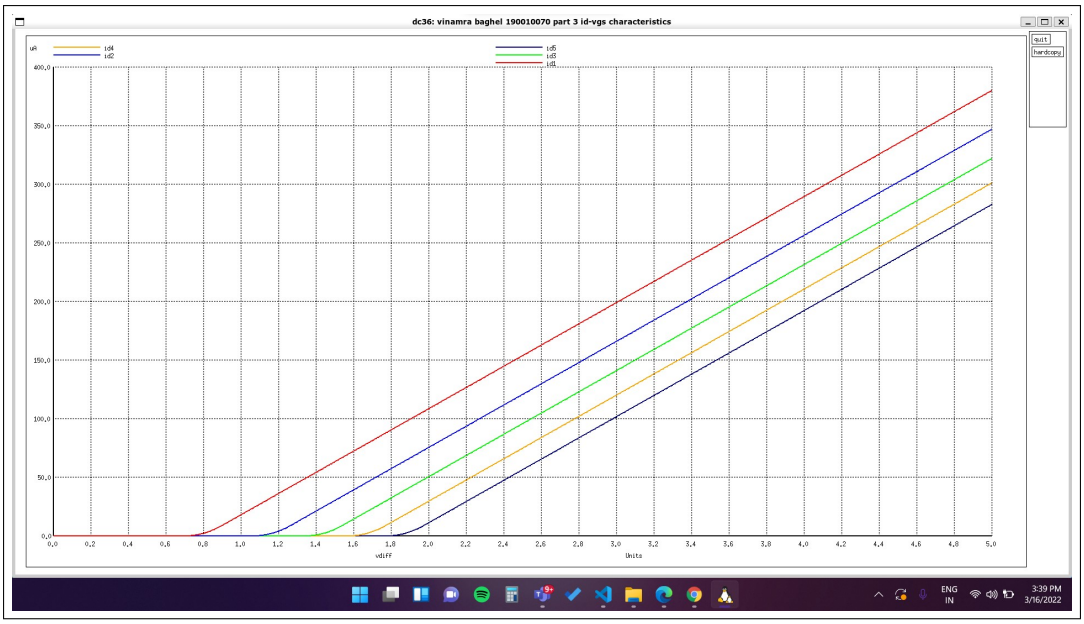


Figure 6: $I_D - V_{GS}$ Characteristics for different V_{SB}

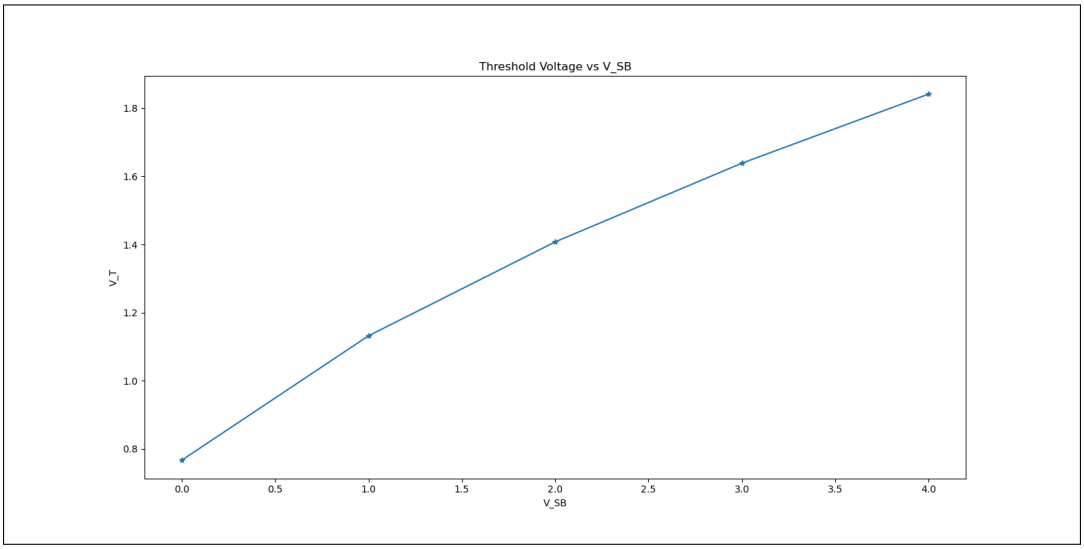


Figure 7: Threshold Voltage vs V_{SB}

3.2.4 CMOS Inverter DC Characteristics

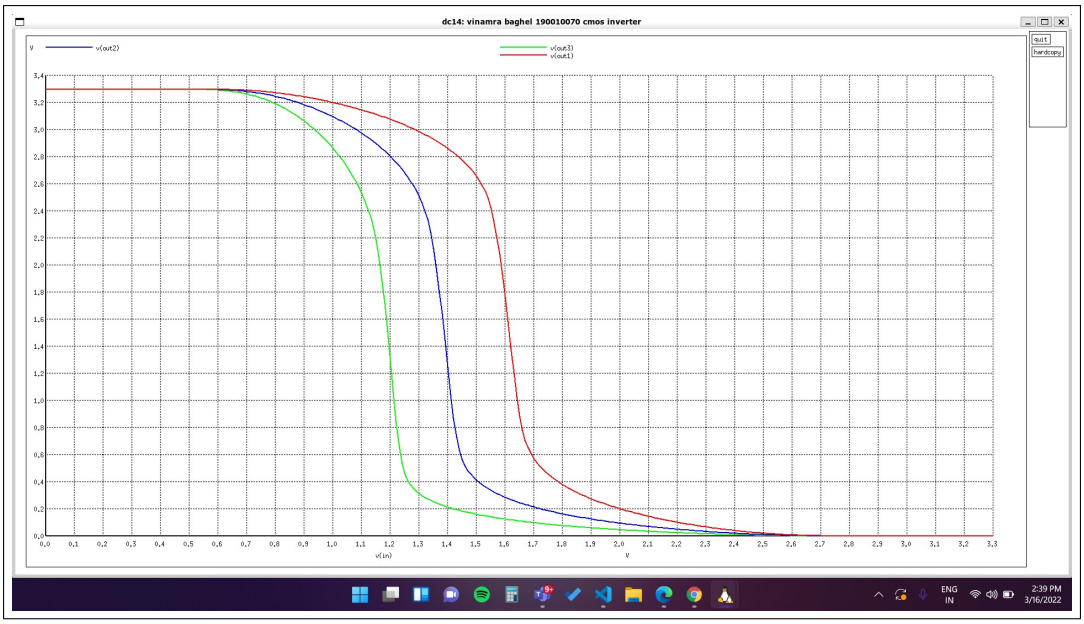


Figure 8: DC Characteristics of CMOS Inverter for different W_p/W_n values

The Switching Threshold Voltage decreases with decreasing W_p/W_n. **Index:**

- **Red:** $W_p/W_n = 60\mu m/30\mu m$
- **Blue:** $W_p/W_n = 60\mu m/60\mu m$
- **Green:** $W_p/W_n = 30\mu m/60\mu m$

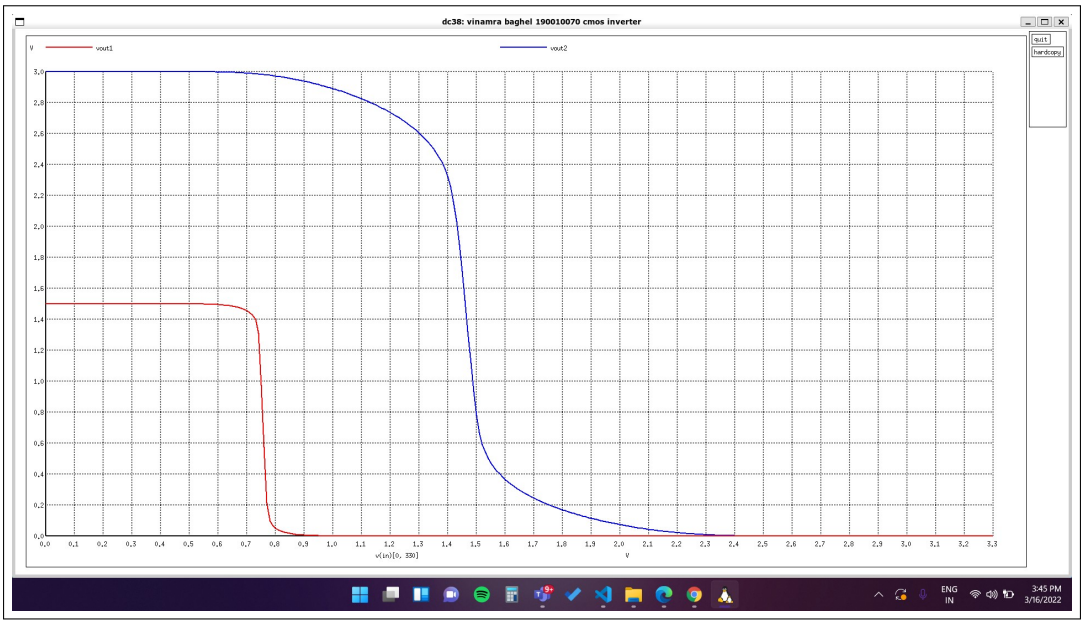


Figure 9: DC Characteristics of CMOS Inverter for different supply voltages

The output starts at the supply voltage for LOW input and ends at 0 for HIGH. **Index:**

- **Red:** Supply voltage, $V_{DD} = 1.5V$
- **Blue:** Supply voltage, $V_{DD} = 3V$

3.2.5 CMOS Inverter Transient Characteristics

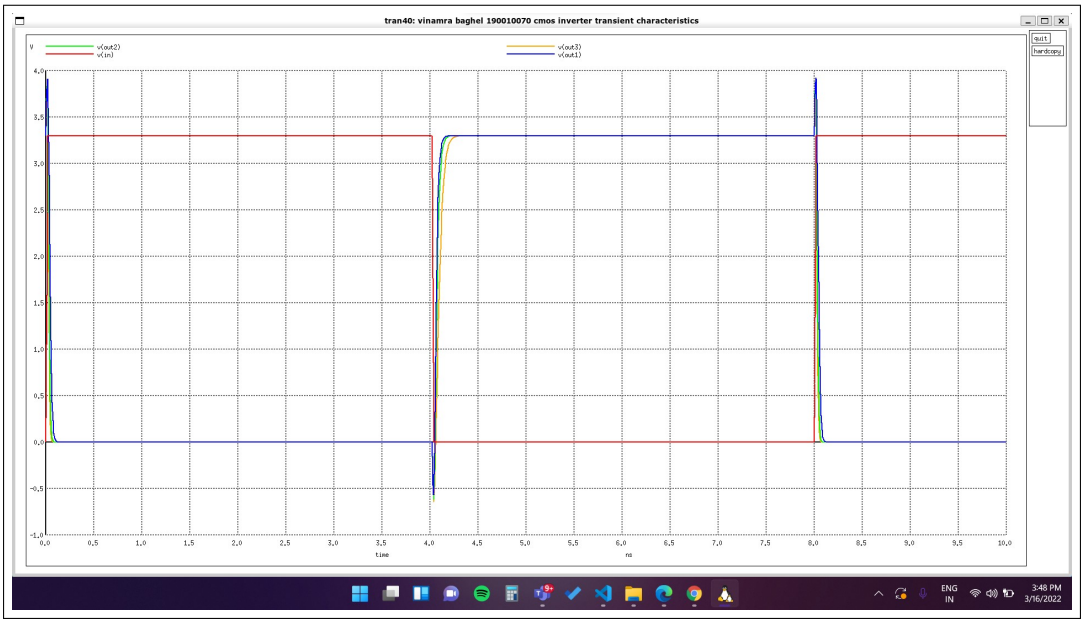


Figure 10: CMOS Inverter Switching Transient Characteristics

Index:

- **Red:** V_{in}
- **Blue:** V_{out} for $W_p/W_n = 60\mu m/60\mu m$
- **Green:** V_{out} for $W_p/W_n = 30\mu m/60\mu m$
- **Orange:** V_{out} for $W_p/W_n = 30\mu m/60\mu m$

Talking about the Rise Time, Fall Time, and Propagation Delay for decreasing W_p/W_n: Rise time **increases**, Fall time **decreases**, and Propagation delay **decreases**.

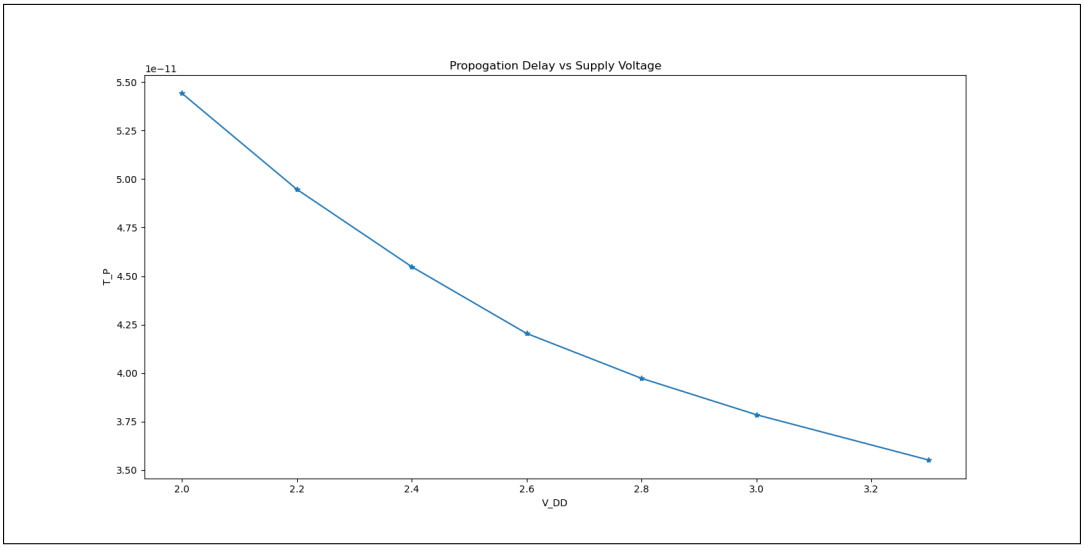


Figure 11: Propagation Delay vs Supply Voltage

The propagation delay **decreases** with an increase in supply voltage.

4 Experimental results

Part 1: R_{DS}, V_0 and r_0.

V_{GS} (in V)	R_{DS} (in kΩ)	V_0 (in V)	r_0 (in kΩ)
2.5	1.237	-34.483	47.301
3	0.967	-34.491	28.977
3.5	0.794	-34.480	19.547
4	0.674	-34.487	14.075

Part 2: V_T, g_m and k.
For $V_{DS} = 200mV$,
$V_T = 0.766V$, $g_m = 9.052 \times 10^{-5}\Omega^{-1}$ and $k = 1.412 \times 10^{-5}AV^{-2}$.
For $V_{DS} = 5V$,
$V_T = 0.762V$, $g_m = 1.703 \times 10^{-3}\Omega^{-1}$ and $k = 5.153 \times 10^{-4}AV^{-2}$.

Part 3: The V_Ts for $V_{SB} = \{0, 1, 2, 3, 4\}$ respectively are:
0.766, 1.132, 1.408, 1.639, and 1.842.
The value of γ came out to be **0.785**.

CMOS DC Characteristics:
Switching Threshold Voltages for $W_p/W_n = 60\mu m/30\mu m$, $W_p/W_n = 60\mu m/60\mu m$, and $W_p/W_n = 30\mu m/60\mu m$ respectively: **1.609V, 1.393V, 1.204V**.

CMOS Transient Characteristics:

W_p/W_n	**Rise Time** (in ps)	**Fall Time** (in ps)	**Propagation Delay** (in ps)
$60\mu m/30\mu m$	8.499	27.776	35.287
$60\mu m/60\mu m$	10.940	18.394	23.954
$30\mu m/60\mu m$	18.514	15.540	19.382

Supply Voltage (in V)	**Propagation Delay** (in ps)
2	54.423
2.2	49.475
2.4	45.486
2.6	42.047
2.8	39.734
3	37.859
3.3	35.523

5 Experiment completion status

I could complete all the parts of the lab. There was no hardware involvement as it was all simulation based. The results were shown to the TA and then submitted.