Date : 25/03/2025

VERIFICATION PLAN

AHB TO APB BRIDGE

Test Case ID	Test Case Name	Description	Expected Outcome
TC_01	**Single Read Test**	Perform a write transaction from AHB to an APB slave register.	APB register should store the correct data.
TC_02	**Single Write Test**	Perform a read transaction from AHB to an APB slave register.	Read data should match the expected value.
TC_03	**Burst Read Test**	Perform a burst read transaction from AHB to APB.	Allows multiple data read in a sequence without needing a separate address phase for each transfer
TC_04	**Burst Write Test**	Perform a burst write transaction from AHB to APB.	Allows multiple data write in a sequence without needing a separate address phase for each transfer
TC_05	**APB Wait State Handling Test**	Introduce wait states in APB transactions and observe bridge response.	AHB should be stalled correctly until the APB transaction completes.
TC_06	**Address Alignment Check Test**	Perform transactions with misaligned addresses on AHB.	Transactions should be properly aligned or generate an error.
TC_07	**Reset and Clock Signal Handling**	Checks reset and clock signals	Ensures that the bridge operates correctly in the overall system context.
TC_08	**Error Handling Test**	Verify bridge behavior when PSLVERR is asserted.	Bridge should propagate HRESP to AHB correctly.
TC_09	**Idle Transaction Handling Test**	Observe the bridge behavior during idle states with no transactions.	Bridge should remain in idle state when there are no operations.

TC_10	**Slave access fail test**	Verify that when an out-of-range address is sent (not mapped to any valid slave), the design correctly flags an error using HRESP = 1 and APB PSELx remains de-asserted.	The DUT should raise HRESP=1 (error response) and prevent access to non-existent slaves. No APB transaction should occur.

COVERAGE PLAN :

Test Case ID	Test Case Name	Description	Expected Outcome
COV_001	Functional Coverage Check	Ensure all functionality paths and sequences are exercised.	Functional Coverage = 100%
COV_002	Statement Coverage Check	Ensure all code statements are executed at least once.	Statement Coverage = 100%
COV_003	Branch Coverage Check	Ensure all conditional branches in the code are evaluated both ways.	Branch Coverage = 100%
COV_004	Expression Coverage Check	Verify complex expressions are evaluated for all possible values.	Expression Coverage > 90%
COV_005	Toggle Coverage Check	Ensure all DUT interface signals toggle at least once during sim.	Toggle Coverage at DUT = 100%

ASSERTION PLAN

Assertion ID	Assertion Name	Location	Description	Expected Behavior
A1	AHB Transfer Valid Check	ahb_monitor.sv	Ensures that HSELAHB and HTRANS are valid before any transfer.	Valid transfer only occurs when HSELAHB=1 & HTRANS ≠ IDLE.

A2	APB PENABLE Requires PSELx	apb_monitor.sv	Verifies that PENABLE is not asserted unless at least one PSELx is set.	PENABLE=1 implies at least one PSELx=1.
A3	Single Slave Selection Check	apb_monitor.sv	Verifies only one slave is selected at a time on PSELx.	countones(PSELx) ≤ 1 at all times.
A4	HRESP Error Response on Invalid Addr	tb_top / scoreboard	Checks if HRESP is asserted when HADDR is out of valid slave address range.	If HADDR ∉ defined range, HRESP=1.
A5	Write with Valid Data Check	apb_monitor.sv	Ensures APB write transactions do not carry zero data unexpectedly.	If PWRITE=1 ⟶ PWDATA must not be zero unless intentional.