

IC DESIGN LAB PROJECT

Design & Implementation of 6T - SRAM Cell (Read, Write Operations)

TOOL USED: CADENCE-VIRTUOSO

REPORTED BY:

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EC24M2013

FULL CUSTOM DESIGN PROJECT
Design & Implementation of 6T - SRAM Cell (Read, Write Operations)

AIM:

- Design and Implementation of 6T SRAM cell.
- Schematic capture using Virtuoso schematic editor.
- Transient and DC analysis of the design using Spectre simulator. (Pre-layout simulation)
- Creating Layout using virtuoso layout editor.
- Physical verification & parasitic extraction.
- Post layout simulation.

TOOLS USED:

- Virtuoso Schematic Editor
- Spectre Simulator
- Virtuoso Layout Editor

PROCEDURE:

- Launch the Virtuoso Schematic Editor using the Cadence tool.
- Design the schematic in the editor's schematic window.
- Generate a symbol for the created schematic.
- Build a test bench using the generated symbol, connecting VDD, GND, and input voltages to facilitate various analyses.
- Conduct AC and transient analysis for the schematic and observe the output waveforms.
- Calculate power consumption and propagation delay from the graph, and tabulate the values.
- Begin designing the layout corresponding to the schematic.
- Perform physical verifications, including Design Rule Check (DRC), Layout vs. Schematic (LVS), and Parasitic Extraction (RCX), for the created layout.
- Use the extracted layout to conduct post-layout simulation in Config mode.
- Compare the results of pre-layout and post-layout simulations, and document the observations and inferences.

CIRCUIT DIAGRAM:

The SRAM memory architecture is structured around the fundamental unit known as the SRAM cell. This cell, typically a 6T configuration, holds a bit of data, representing either a 1 or 0. The architecture is designed for efficient data storage and retrieval, with specific components contributing to its functionality.

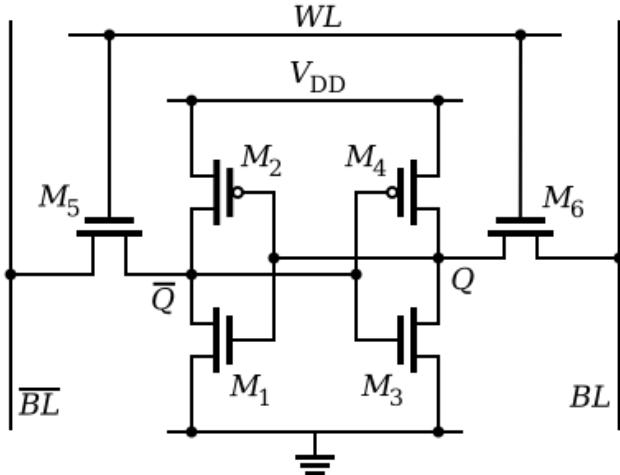


Figure 1: schematic diagram SRAM 6T

OPERATION:

Write operation :

The following is the explanation for writing "0" logic into the SRAM which in turn emphasises the need for stronger access transistors

- Let us consider writing a logic "0" to a cell that has stored a logic "1".
- The write driver makes $BL=0V$ and $BL'=VDD$ as logic '0' is written into the cell. The write driver circuit provides the required voltage to BL and BL' (For write 0, $BL = 0$, $BL' = 1$ and for write 1, $BL=1$, $BL' = 0$).
- Now the corresponding address line is enabled by the decoder circuit which makes $WL=1$.
- The word line (WL) is made high and hence bit lines BL and BL' are connected to the SRAM cell through the access transistors.
- The corresponding data is written into the cell ($Q = 0$ for write logic 0 and $Q = 1$ for write logic 1).
- The Q' side of the cell cannot be pulled high enough to ensure the writing of '1' due to the sizing constraint imposed by the read stability. It ensures that this voltage is kept below 0.4V.
- Hence the new value of the cell has to be written through the transistor M_6 . Data '0' will be written into the cell if node Q is pulled down, below the threshold voltage of M_1 to turn it OFF

For a successful write operation, access transistors should be stronger than the pull-up transistors which are taken care of by the pull-up ratio.

Read operation:

For understanding read operation, we consider the SRAM cell is holding logic "1".

- Considering that logic "1" is stored in the SRAM cell ($Q = 1$ and $Q' = 0$).
- Initially the bit lines BL and BL' are pre-charged to VDD . Then the word line (WL) is made high. So the transistors M_1 , M_4 , M_5 and M_6 (Refer to above figure) will turn ON.

- Therefore BL' gets discharged through the series transistors M5-M1 and BL will remain in its pre-charged state.
- As the voltage difference (ΔV) between the two-bit lines builds up, the sense amplifier is activated which pulls the output level to logic "1". Therefore reading logic "1" from the cell is completed.

The key design issue for the data-read operation is to guarantee that the voltage ΔV does not exceed the threshold of M3, so that the transistor M3 remains turned OFF during the read phase.

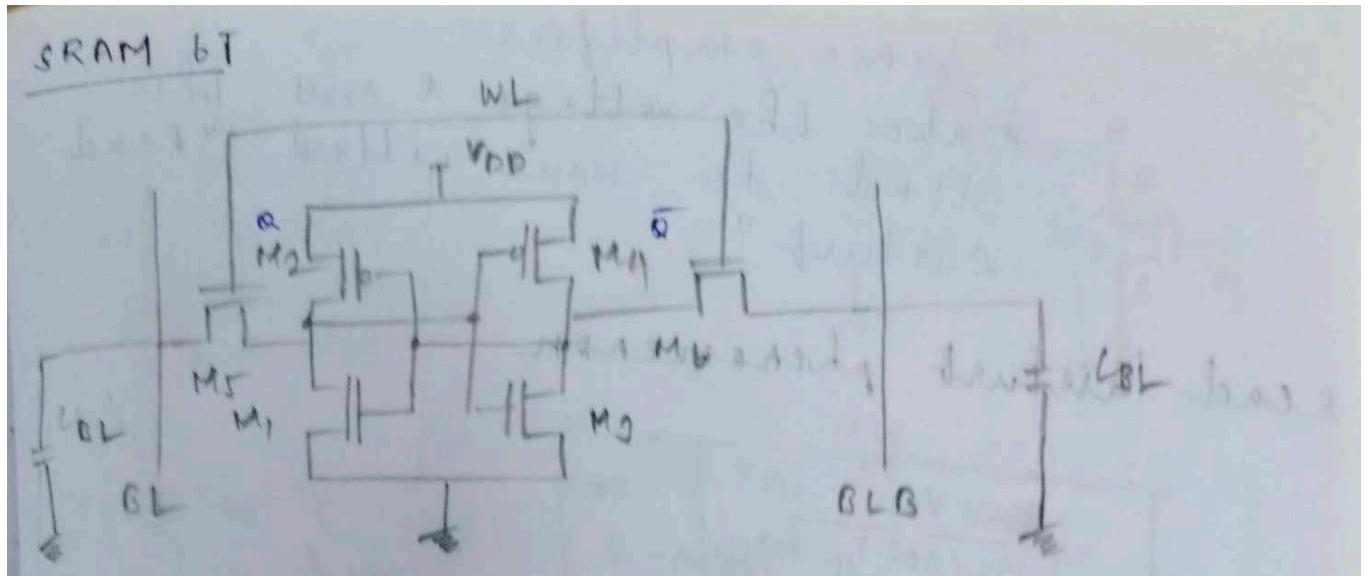
To prevent this, the resistance of M5 should be made larger than that of M1 to prevent ΔV from turning on M3 (Not destroying the stored data). This is defined as the cell ratio.

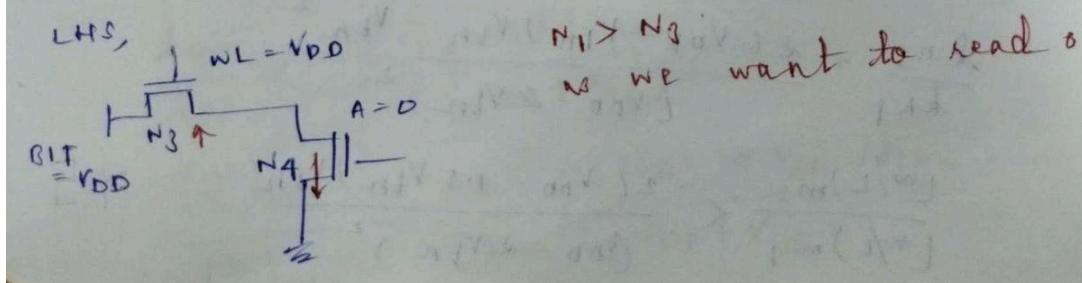
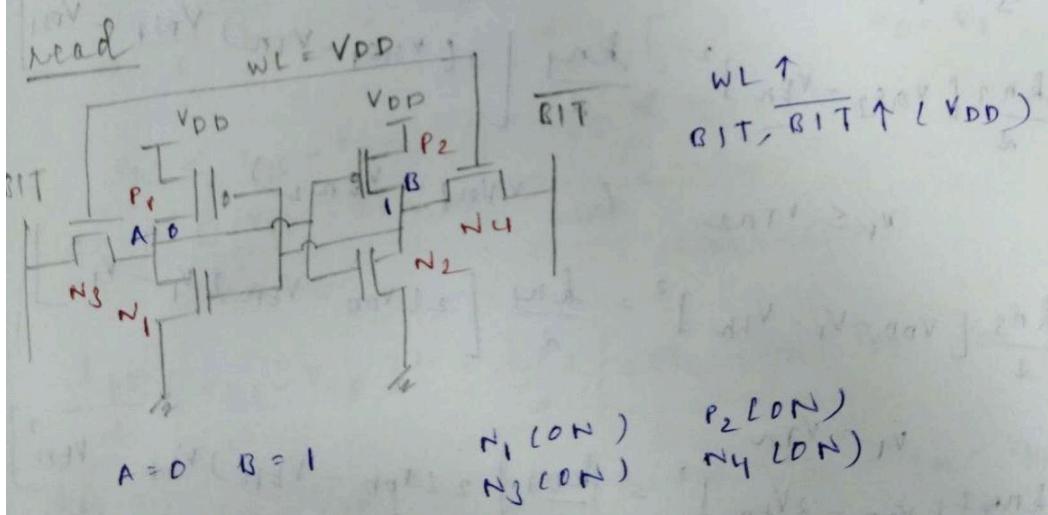
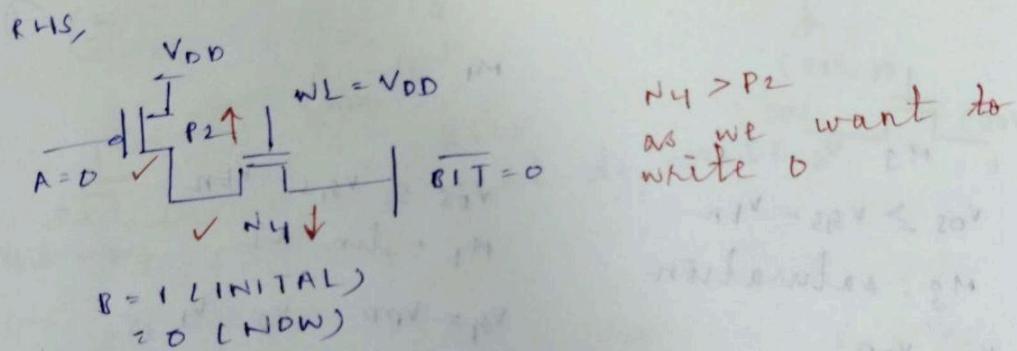
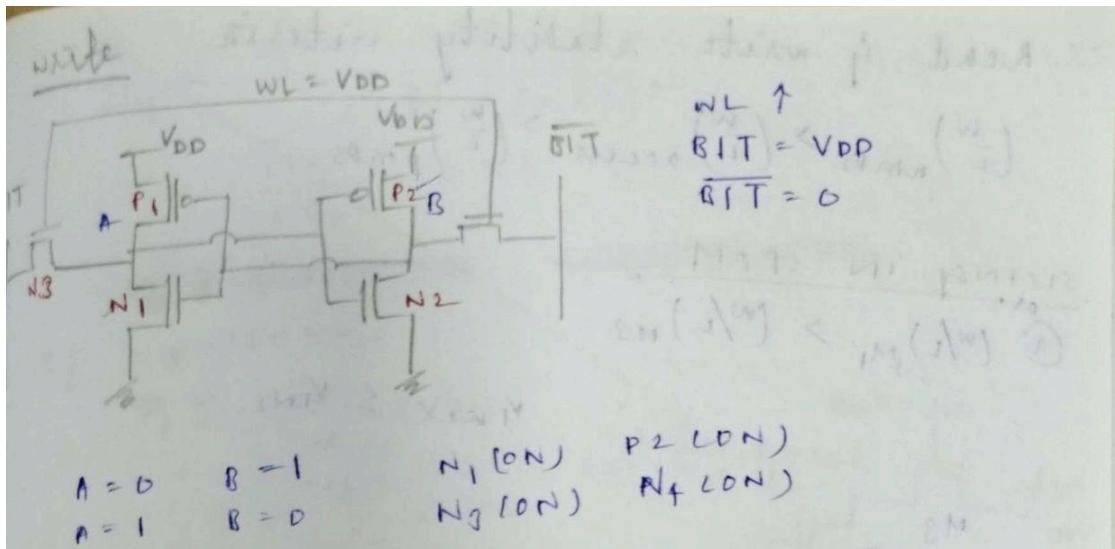
Hold State Stability

Initial condition $WL=0$ and Access Transistors M5 and M6 are OFF

- As access Transistors are in the OFF state the Cell is isolated from BL and BL' , Therefore there is no possibility of the state getting changed, as there will be fewer chances of Noise interference.
- If we plot the VTC of INV1 and INV2 and super-imposing the VTC's we get a butterfly curve.
- As there is no Noise getting added, the Inverters are working with a perfect VTC as shown in above figure. The Hold state Static Noise Margin (SNM) is expected to be Maximum

MANUAL CALCULATIONS:



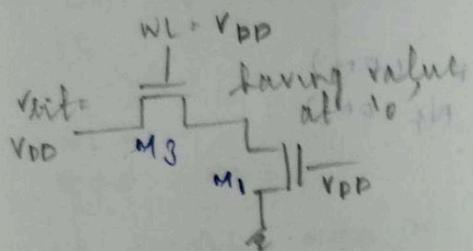


∴ Read & write stability criteria

$$(\frac{W}{L})_{nmos} > (\frac{W}{L})_{access} > (\frac{W}{L})_{pmos}$$

SIZING IN SRAM

① $(\frac{W}{L})_{M_1} > (\frac{W}{L})_{M_3}$



$$(VDD) \frac{1}{M_3} \frac{1}{M_1} (VDD)$$

$$V_{DS} \geq V_{GS} - V_{TN}$$

M_3 : saturation

$$V_G = VDD$$

$$V_S = V_I$$

$$V_{I\max} \leq V_{TN2}$$

D (0)

$$M_1 \frac{1}{M_3} \frac{1}{G} (VDD)$$

$$N_{DS} \leq V_{GS} - V_{TN}$$

M_1 : linear

$$V_G = VDD$$

$$V_D = V_I$$

$$V_S = 0$$

$$\frac{k_{n3}}{2} [V_{GS2} - V_{TN}]^2 = \frac{k_{n1}}{2} \left[2(V_{GS1} - V_{TN}) V_{DS1} - V_{DS1}^2 \right]$$

$$V_I \leq V_{TN2} \quad (\because V_{TN1} = V_{TN2})$$

$$\frac{k_{n3}}{2} [VDD - V_I - V_{TN}]^2 = \frac{k_{n1}}{2} \left[2(VDD - V_{TN}) V_I - V_I^2 \right]$$

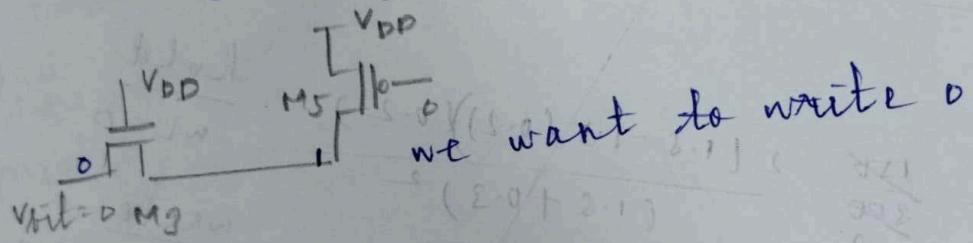
$$V_I = V_{TN}$$

$$\frac{k_{n3}}{2} [VDD - 2V_{TN}]^2 = \frac{k_{n1}}{2} \left[2(VDD - V_{TN}) V_{TN} - V_{TN}^2 \right]$$

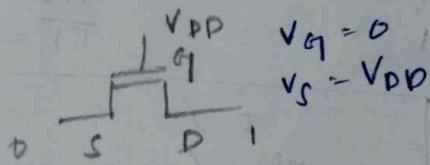
$$\frac{k_{n3}}{k_{n1}} = \frac{2(VDD - V_{TN}) V_{TN} - V_{TN}^2}{(VDD - 2V_{TN})^2}$$

$$\frac{(\frac{W}{L})_{M_3}}{(\frac{W}{L})_{M_1}} < \frac{2(VDD - 1.5V_{TN}) V_{TN}}{(VDD - 2V_{TN})^2}$$

$$\textcircled{b} \quad \left(\frac{w}{l}\right)_{M_3} > \left(\frac{w}{l}\right)_{M_5}$$



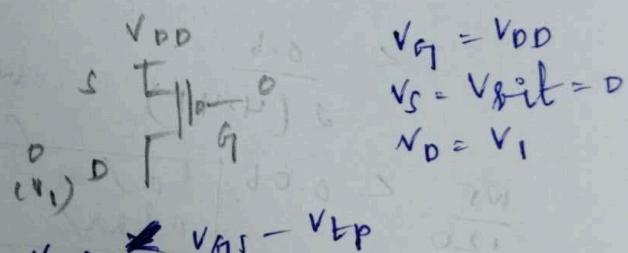
$$V_I \leq V_{TN,2}$$



$$V_{DS} \leq V_{GS} - V_{TN}$$

$$0 \leq V_{DD} - V_{TN}$$

linear



$$V_{DS} \leq V_{GS} - V_{TP}$$

$$0 - V_1 \leq -V_{DD} - V_{TP}$$

saturation

$$\frac{k_{PS}}{2} [V_{GS} - V_{TP}]^2 = \frac{k_{PS}}{2} [2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2]$$

$$\frac{k_{PS}}{2} [0 - V_{DD} - V_{TP}]^2 = \frac{k_{PS}}{2} [2(V_{DD} - V_{TN}) V_{TN} - V_{TN}^2]$$

$$\frac{k_{PS}}{k_{PS}} < \frac{2(V_{DD} - 1.5)V_{TN}}{(V_{DD} + V_{TP})^2}$$

$$\frac{\left(\frac{w}{l}\right)_{M_5}}{\left(\frac{w}{l}\right)_{M_3}} < \frac{\mu_n}{\mu_p} \frac{2(V_{DD} - 1.5)V_{TN}}{(V_{DD} + V_{TP})^2}$$

Taking all the above sizing into consideration, we can conclude that:

substituting the values of V_{DD} and V_{TN}

$$\frac{W}{L}_{m2} < \frac{(2(1.8) - 1.5(0.5))^{0.5}}{(1.8 - 2(0.5))^2}$$

$$\frac{W}{L}_{m4} < \frac{1.05}{0.64} = 1.64$$

$$w_n < 1.64 \times w_p \quad (\text{approximately})$$

$$w_n = 1.5 \times w_p$$

$$\frac{W}{L}_{m5} < \frac{\mu_n \cdot 2(V_{DD} - V_{TN})^{1/2}}{\mu_P \cdot (V_{DD} + V_{TP})^2}$$

$$< \frac{300}{100} \frac{2(1.8 - 1.5(0.5))^{0.5}}{(1.8 + 0.5)^2}$$

$$< \frac{3 \times 1.05}{5.29} = 0.59$$

$$w_a < 0.59 \times w_n$$

$$< 0.59 (1.5 \times w_p)$$

$$< 0.96 \times w_p$$

$$w_a = 1.2 \times w_p \quad (\text{approximately})$$

Substituting in the above equations, we get the following values.

Length of all MOS	CALCULATION	VALUES
Width of PMOS devices (wp)	Minimum width	220 nm
Access transistors width (wa)	$1.2 \times wp$	$1.2 \times 220 = 260 \text{ nm}$
Width of Pull down NMOS transistors (wn)	$1.5 \times wa$	$1.5 \times 260 = 400 \text{ nm}$

2. Read & write stability criteria

$$\left(\frac{W}{L}\right)_{nmos} > \left(\frac{W}{L}\right)_{access} > \left(\frac{W}{L}\right)_{pmos}$$

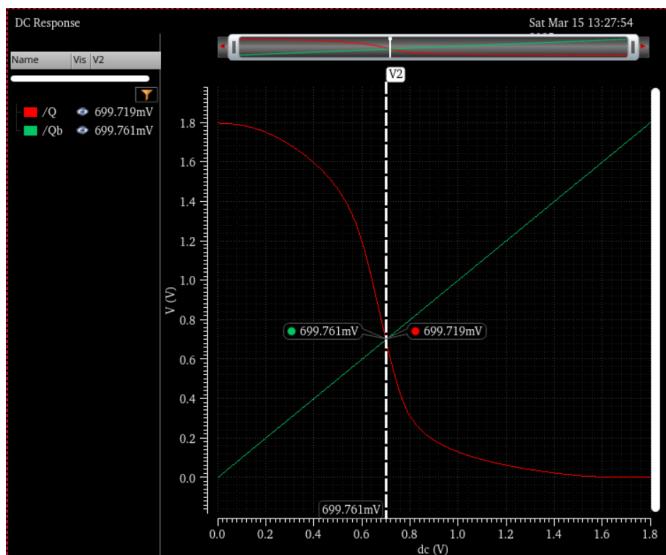
DIFFERENT ATTEMPTS WITH DIFFERENT SIZING OF SRAM TRANSISTOR

1. Taking equal sizing for all transistors. NMOS(W/L) = PMOS(W/L) = 1.2

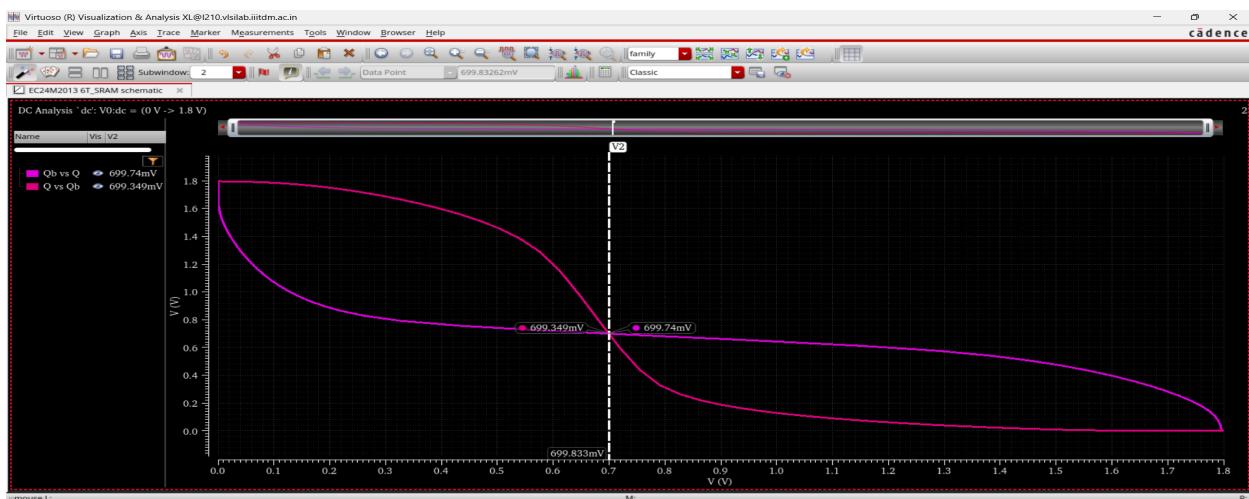
Taking L=100 nm and W=120 nm.

DC ANALYSIS

(W/L = 1.2)



During DC analysis, the following curve was obtained.



We get a threshold voltage of 699.3 mV.

LIMITATION:

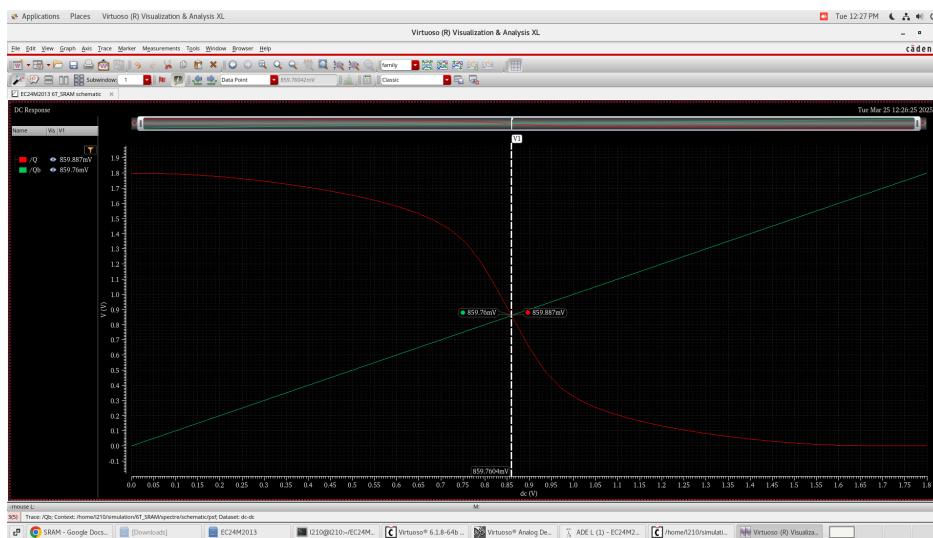
- During a read, the access transistors (M5, M6) try to pull internal nodes (Q or Q') toward bitlines.
- If the access transistor = pull-down = same size, the internal node might flip during read.
- In a write, access transistors must overpower pull-up PMOS to flip the stored value.
- If access = pull-up PMOS = same size, the PMOS may fight back too hard, resisting the write.

2. Taking equal sizing for nmos and equal sizing for pmos. NMOS(W/L) = 1.2 PMOS(W/L) = 2.4

DC ANALYSIS

(taking all nmos to be W/L = 1.2 and pmos to be W/L = 2.4)

During DC analysis, the following curve was obtained.

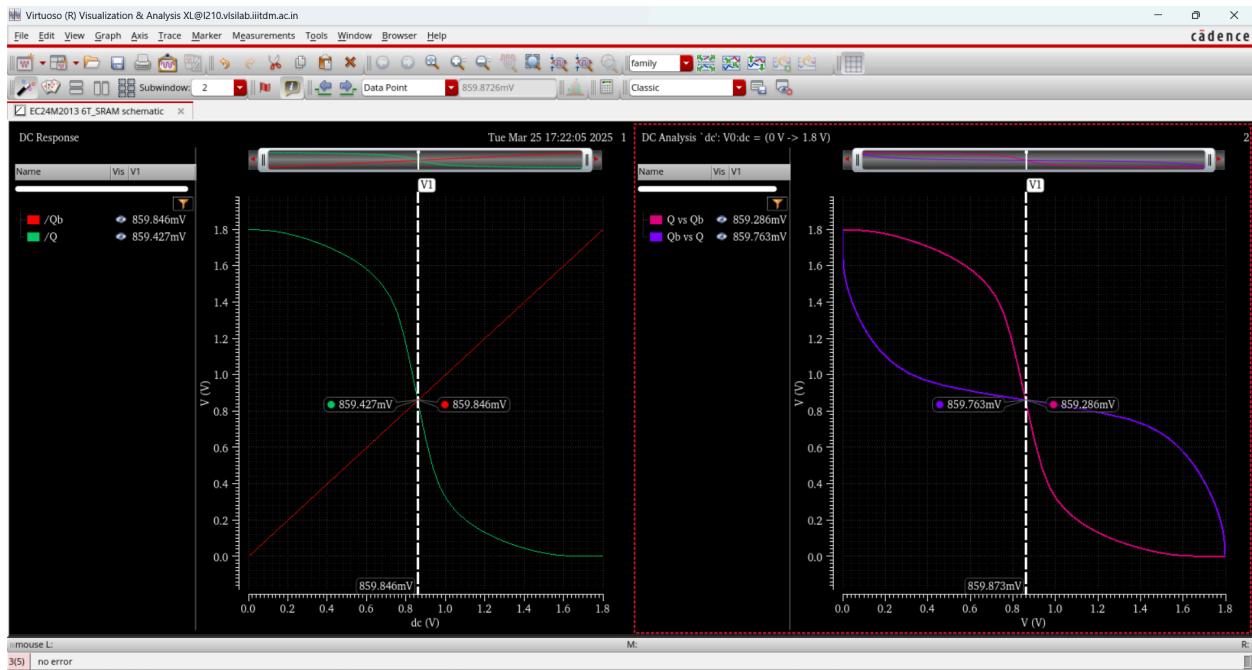


We get a threshold voltage of 859.065 mV.



Adding capacitors,

The following was obtained in DC analysis



LIMITATIONS:

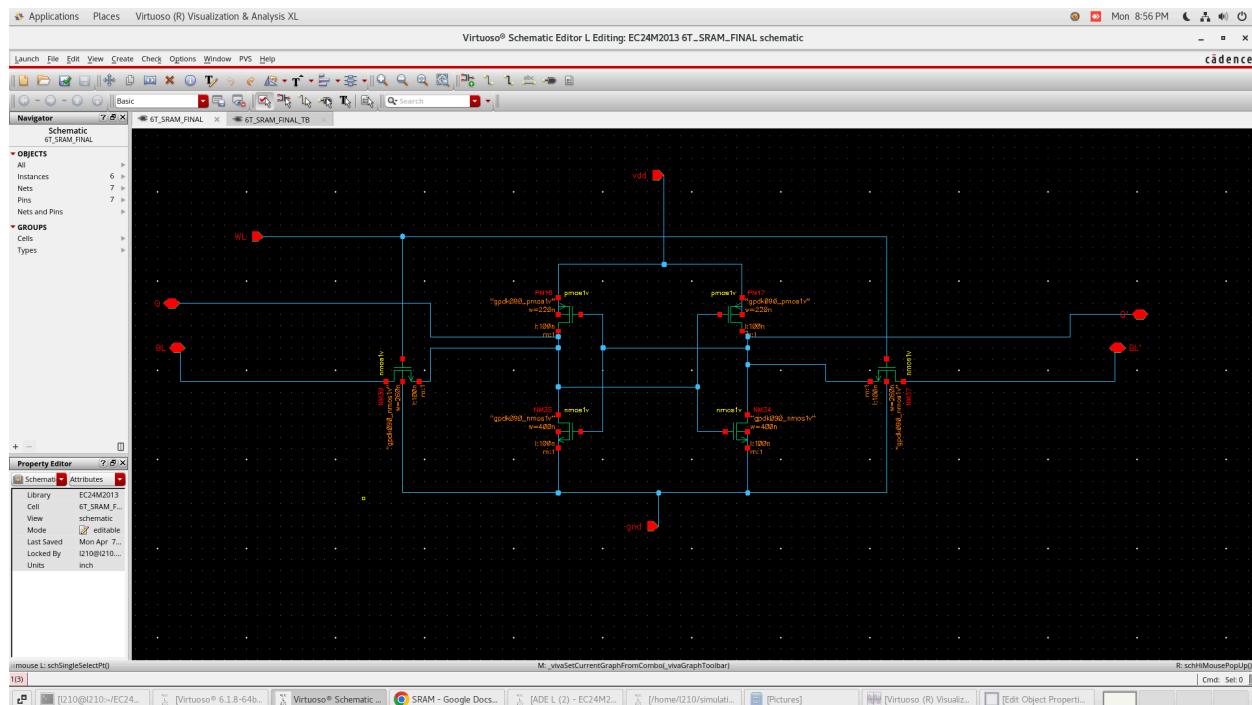
- During a **write '0'**, the bitline is driven low, and the access transistor tries to pull internal node (Q) low.
- But now the **strong PMOS (pull-up)** resists this, trying to keep the node high.
- During read, the cell has to pull the bitline slightly via pull-down NMOS (M_1, M_2).
- If NMOS is small, and PMOS is large:
PMOS weakens the '0' node (pulls up), fighting against the NMOS pulling down.

Hence, to rectify all the above problems, the read write stability criteria is used.

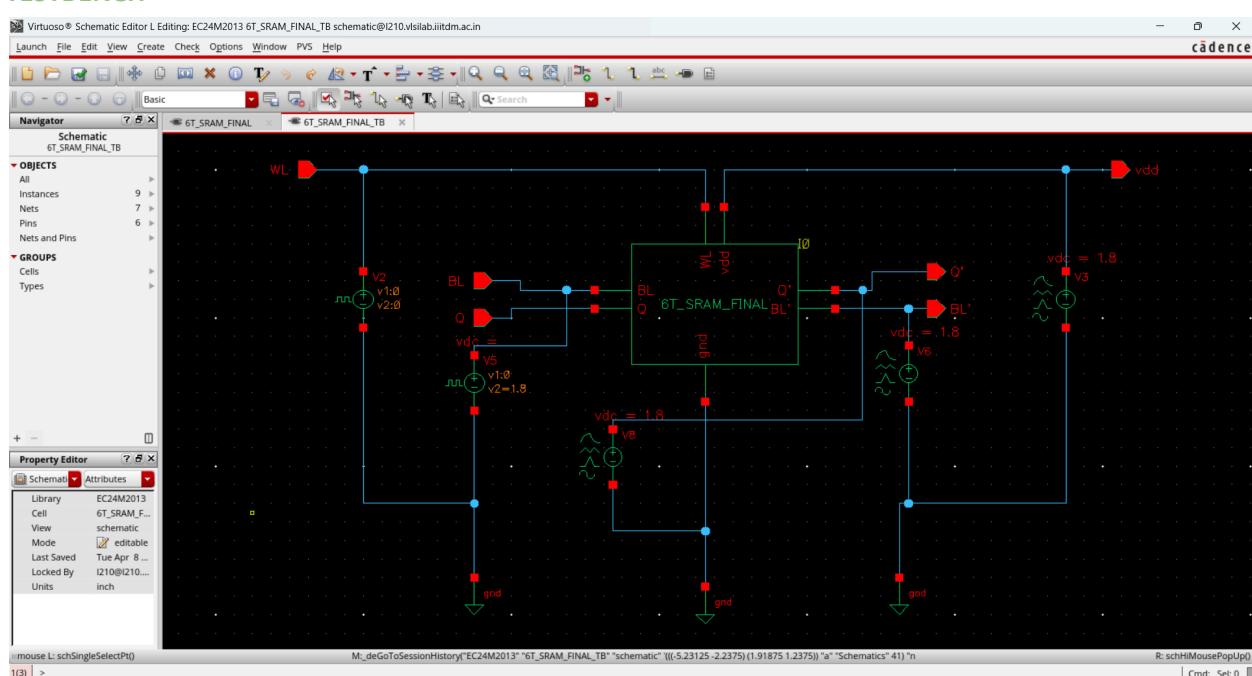
A handwritten note on a piece of paper. The top part reads "Read & write stability criteria". Below it, the inequality $(\frac{W}{L})_{nmos} > (\frac{W}{L})_{access} > (\frac{W}{L})_{pmos}$ is written.

$$(\frac{W}{L})_{nmos} > (\frac{W}{L})_{access} > (\frac{W}{L})_{pmos}$$

SCHEMATIC



TESTBENCH



PRE LAYOUT SIMULATION

CIRCUIT INVENTORY

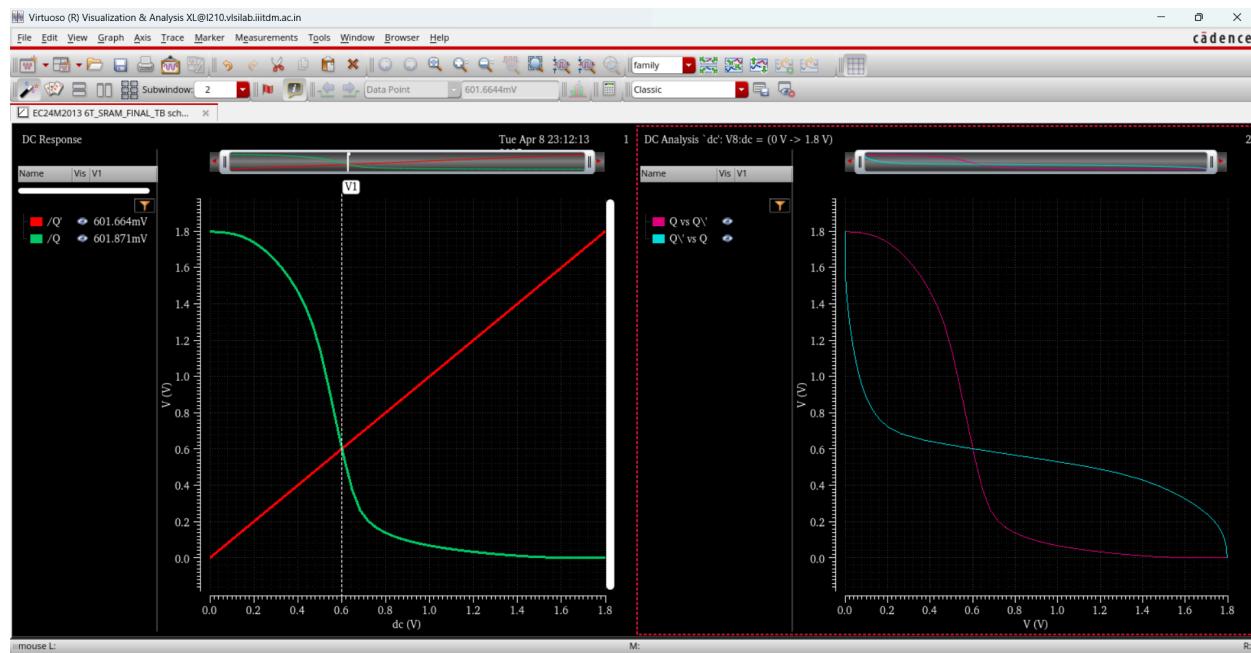
```
Circuit inventory:  
    nodes 6  
bsim3v3 6  
vsourc 5
```

```
Analysis and control statement inventory:  
    dc 2  
    info 7
```

```
Output statements:
```

```
.probe 0  
.measure 0  
save 0
```

DC ANALYSIS



We get a threshold voltage at 601.664 mV.

TRANSIENT ANALYSIS

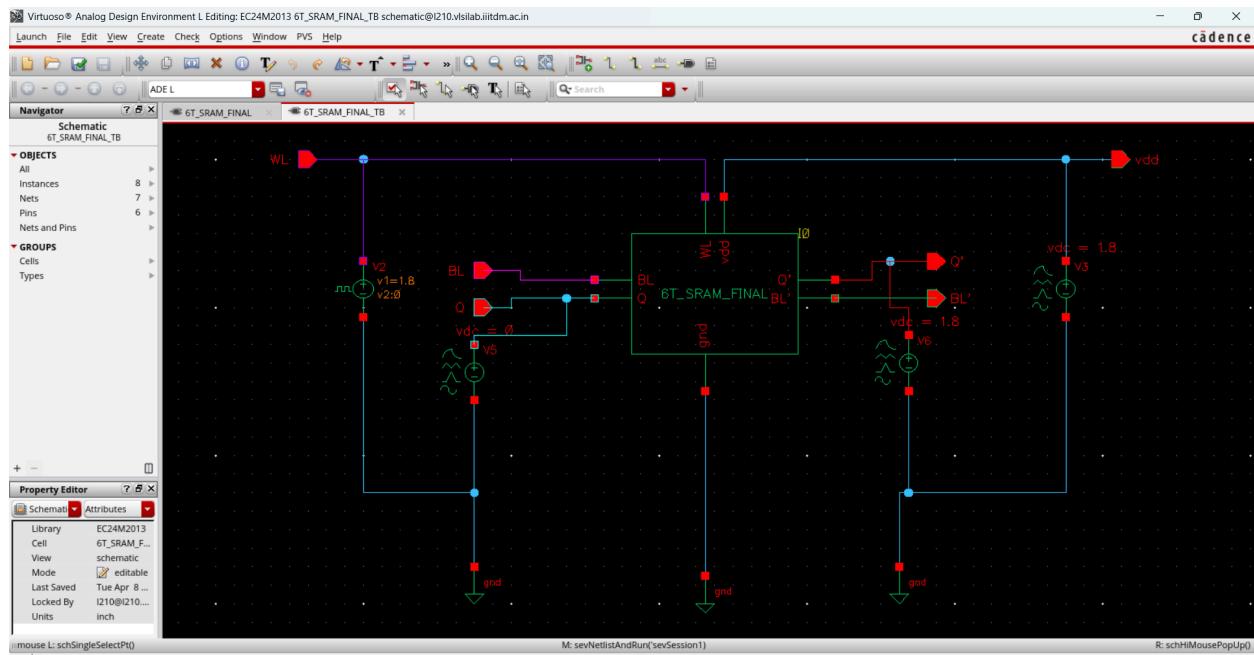
The read and write operation are shown using the transient analysis

Write operation analysis

Write logic "0" operation

BL=0, BL'=1, WL=1 and Q is pulled low, Q' goes high.

Testbench Schematic for Write "0" Operation :



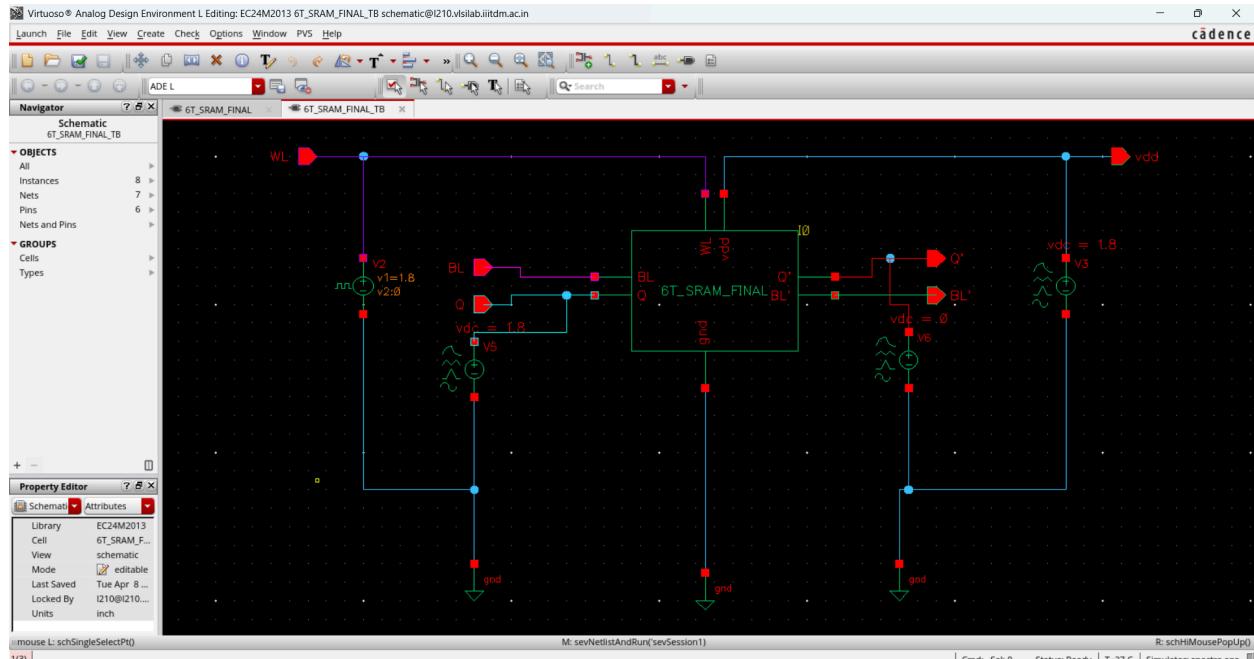
Timing diagram for Write '0' Operation:



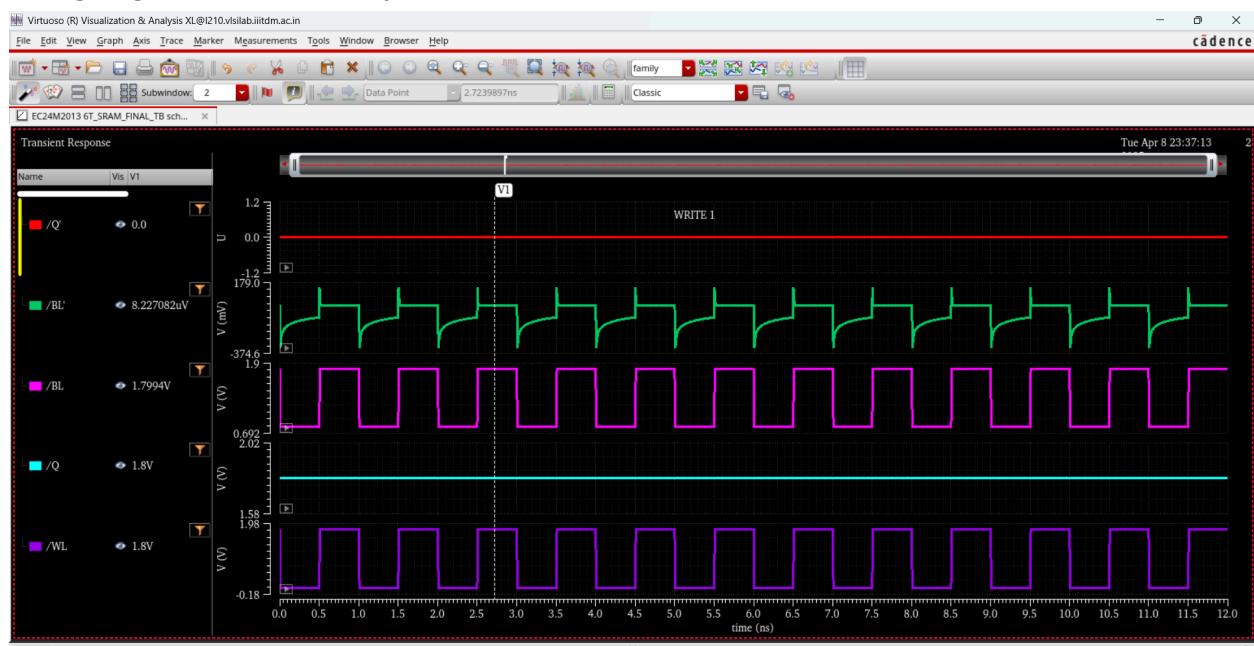
Write logic "1" operation

BL=1, BL'=0, WL=1 and Q is pulled high, Q' goes low.

Testbench Schematic schematic for Write "1" Operation:



Timing diagram for Write "1" Operation:

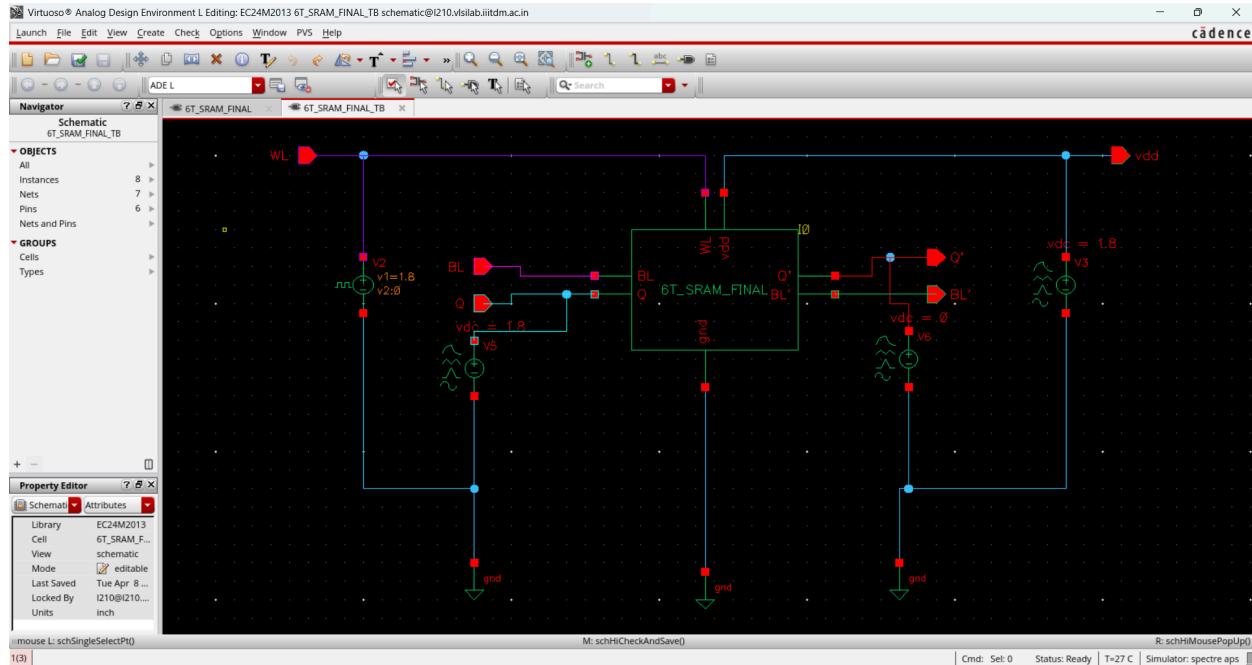


Read operation analysis

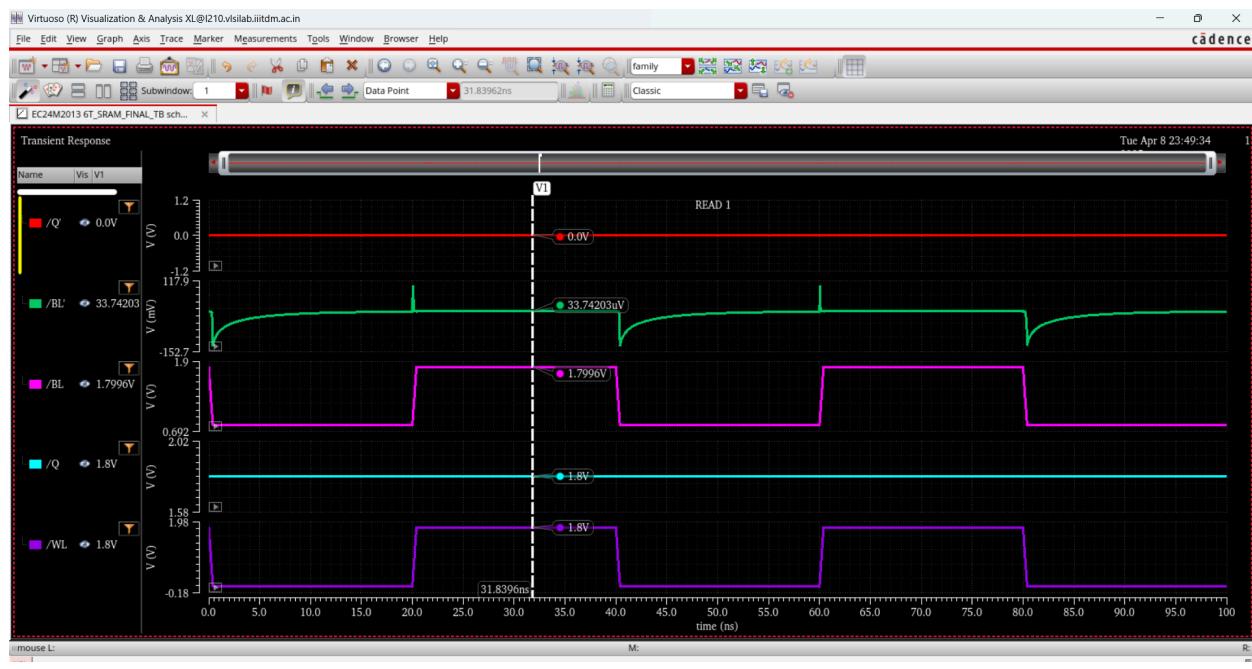
Read logic "1" operation

BL and BL' pre charged, WL=1 → Q=1, so BL stays high, BL' slightly discharges.

Testbench Schematic for Read "1" operation:



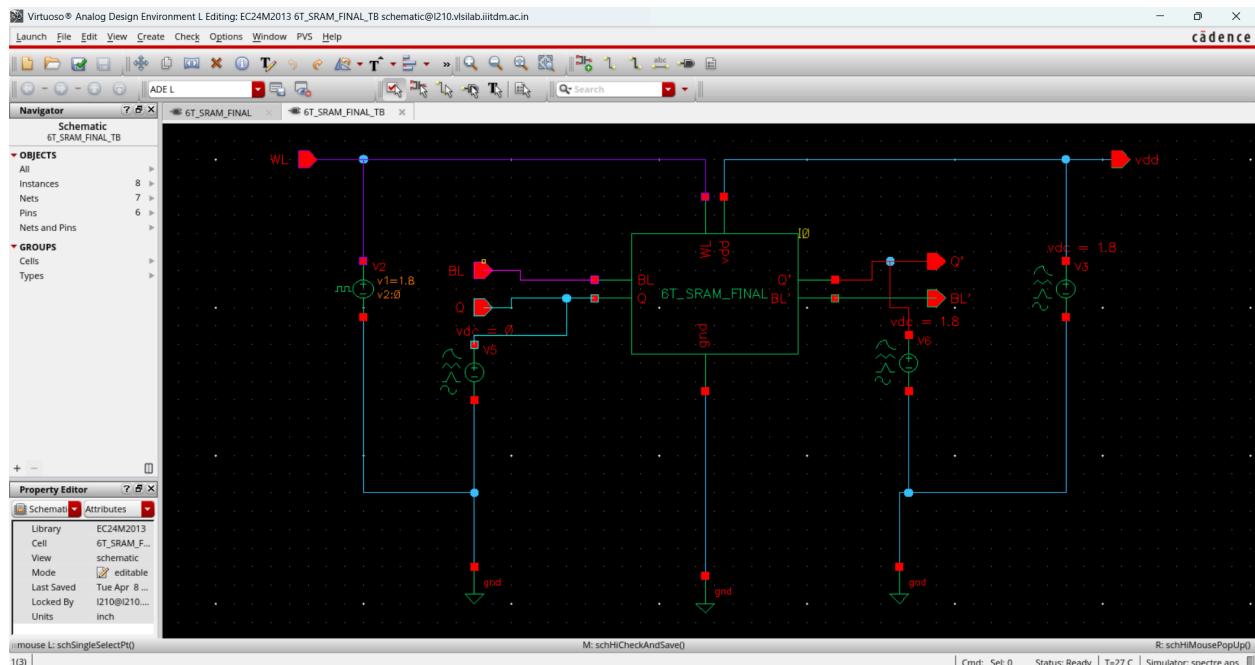
Timing diagram for Read "1" operation:



Read logic "0" operation

BL and BL' precharged, WL=1 → Q=0, so BL slightly discharges, BL' stays high.

Testbench Schematic for Read "0" operation:



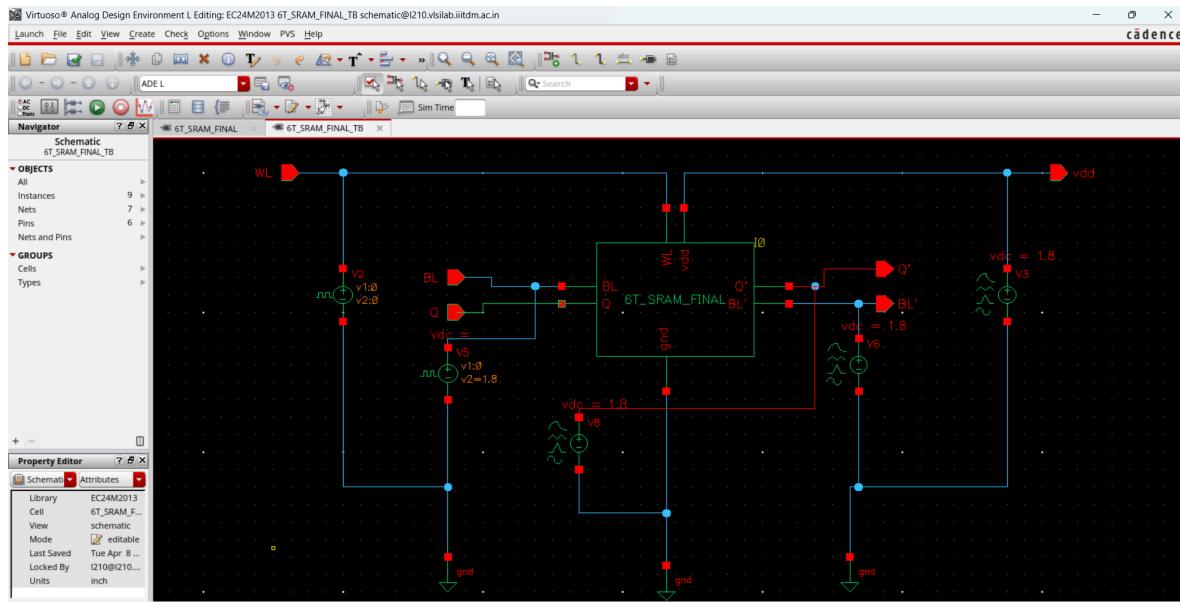
Timing diagram for Read "0" operation:



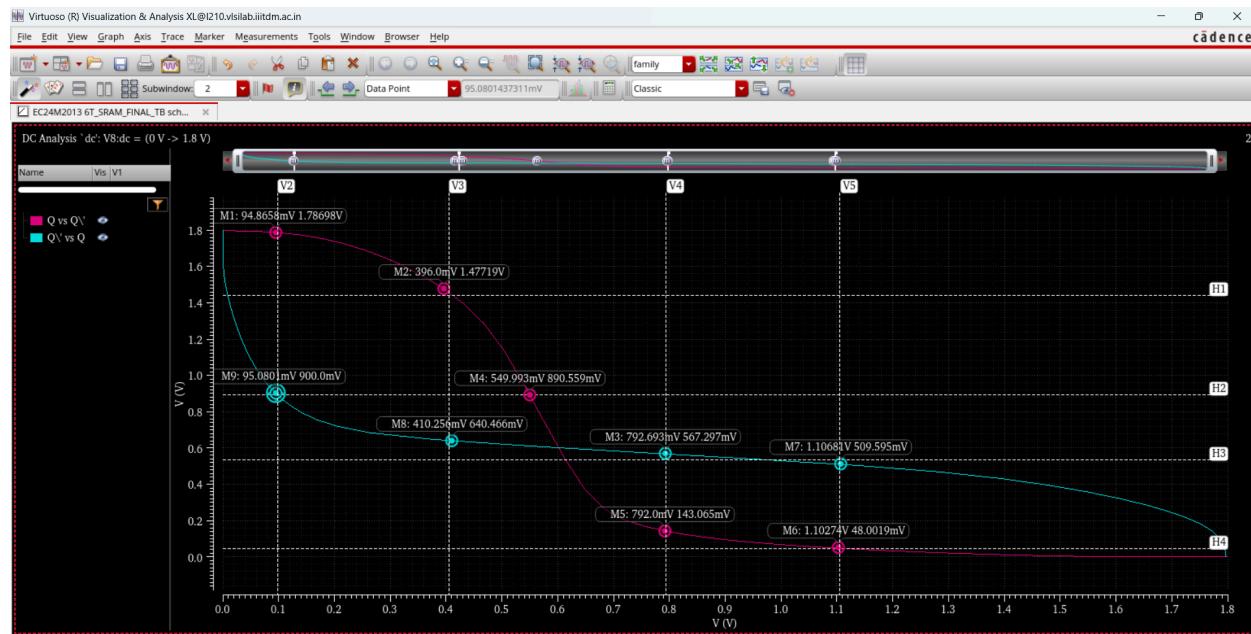
Stability Analysis

Hold state Stability Analysis

WL=0 → Access transistors off, Q and Q' retain their values; BL, BL' don't affect the cell.



Butterfly curve for Hold state:

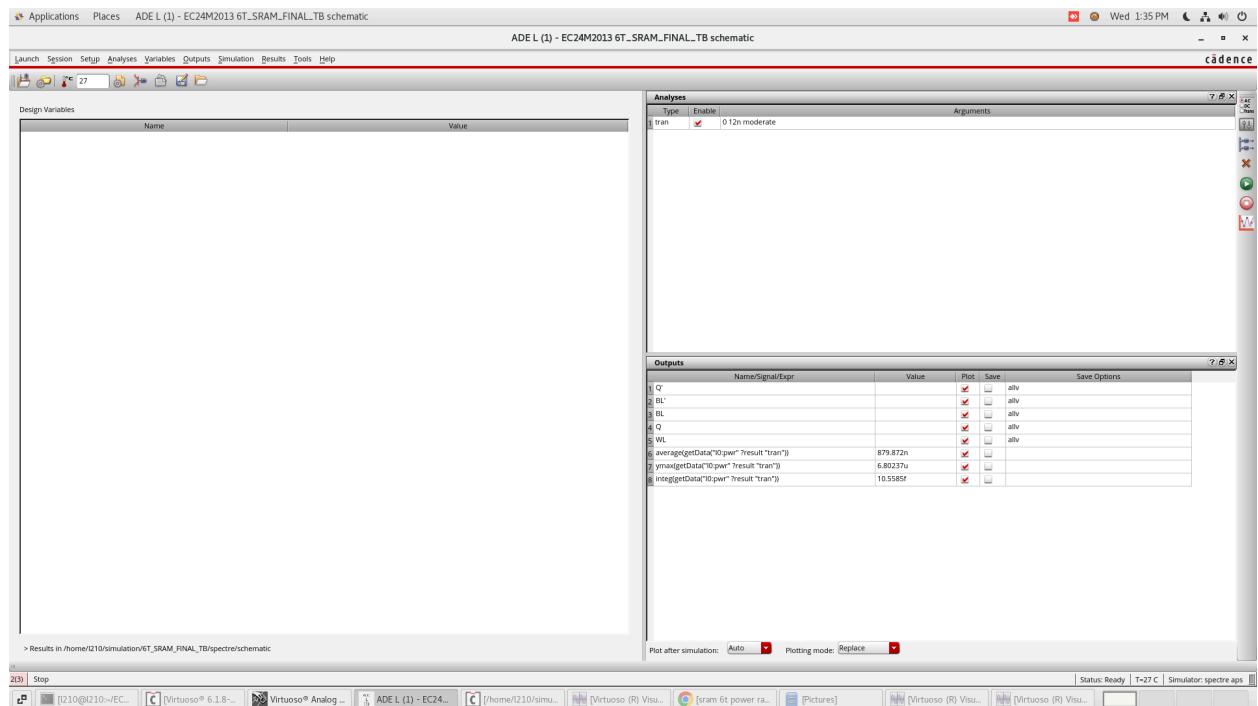
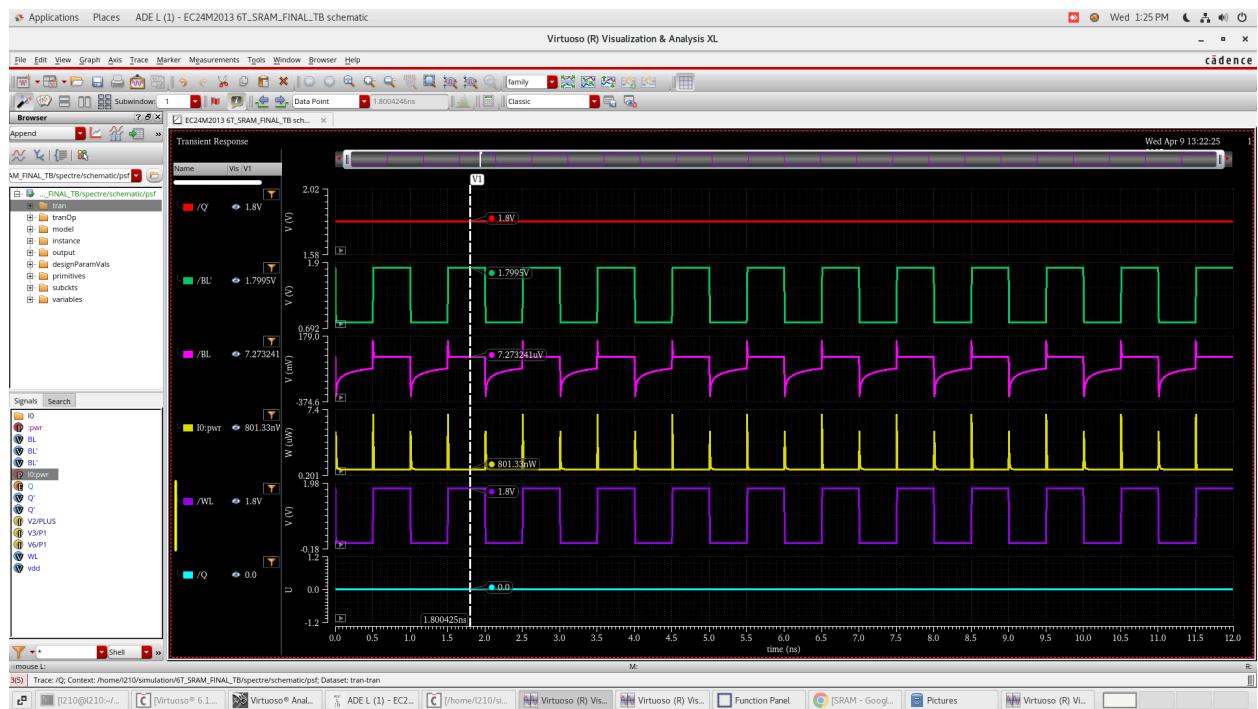


$$SNM = \min (\max(SNM1), \max(SNM2))$$

$$= \min (392.869mV, 314.075mV)$$

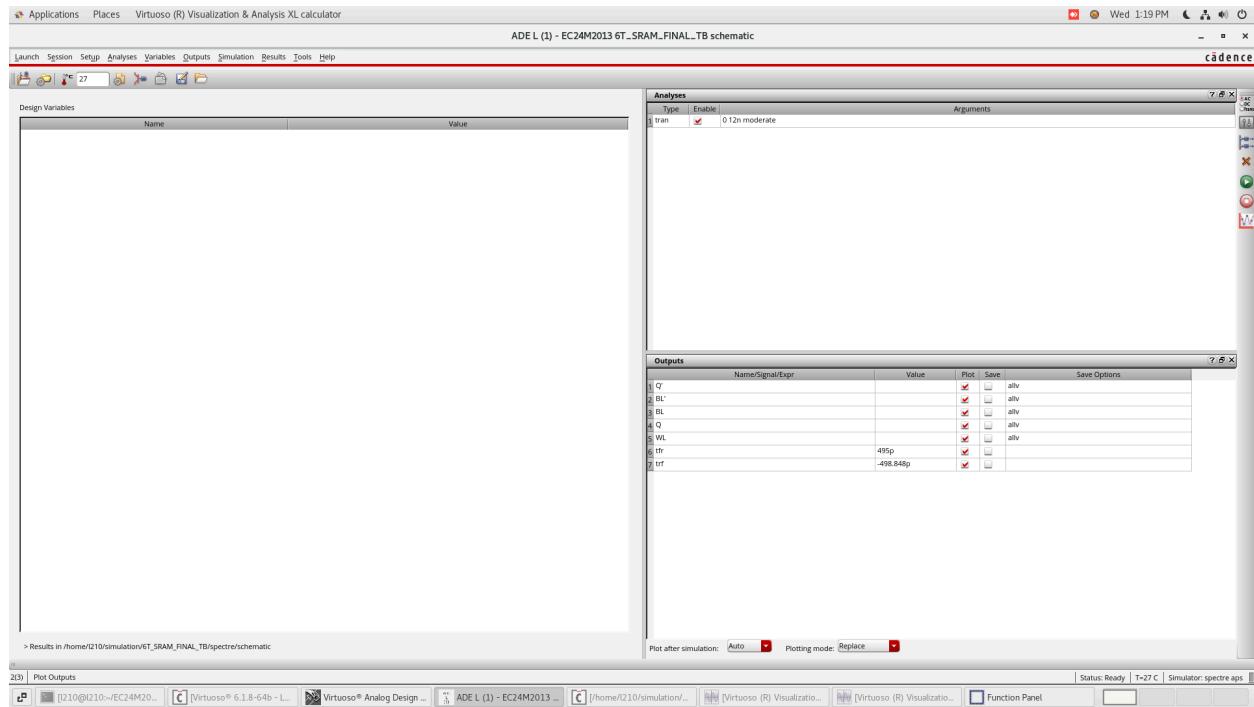
$$= 392.869mV$$

POWER ANALYSIS



The above graph shows the power obtained during pre layout simulation, we get an average power of 879.872 nW.

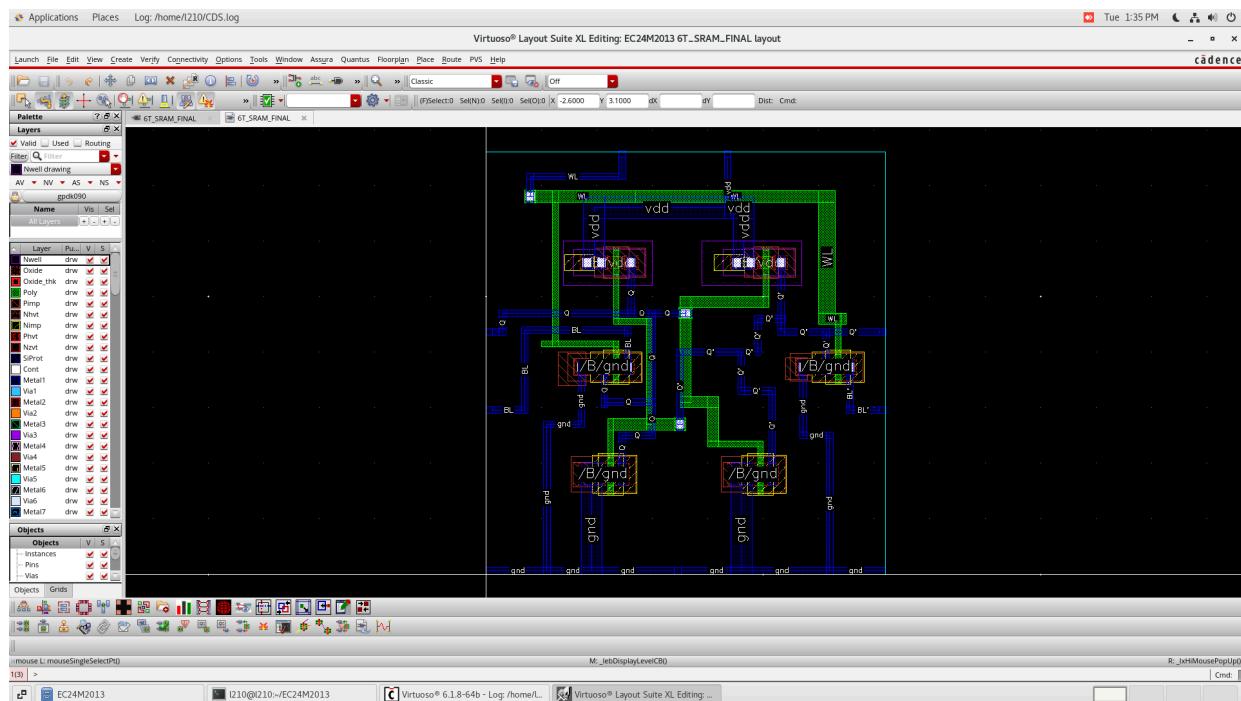
DELAY



We get $tfr = 495$ ps and $trf = 498.848$ ps. The average delay $tpd = (tfr+trf)/2 = 496.924$ ps.

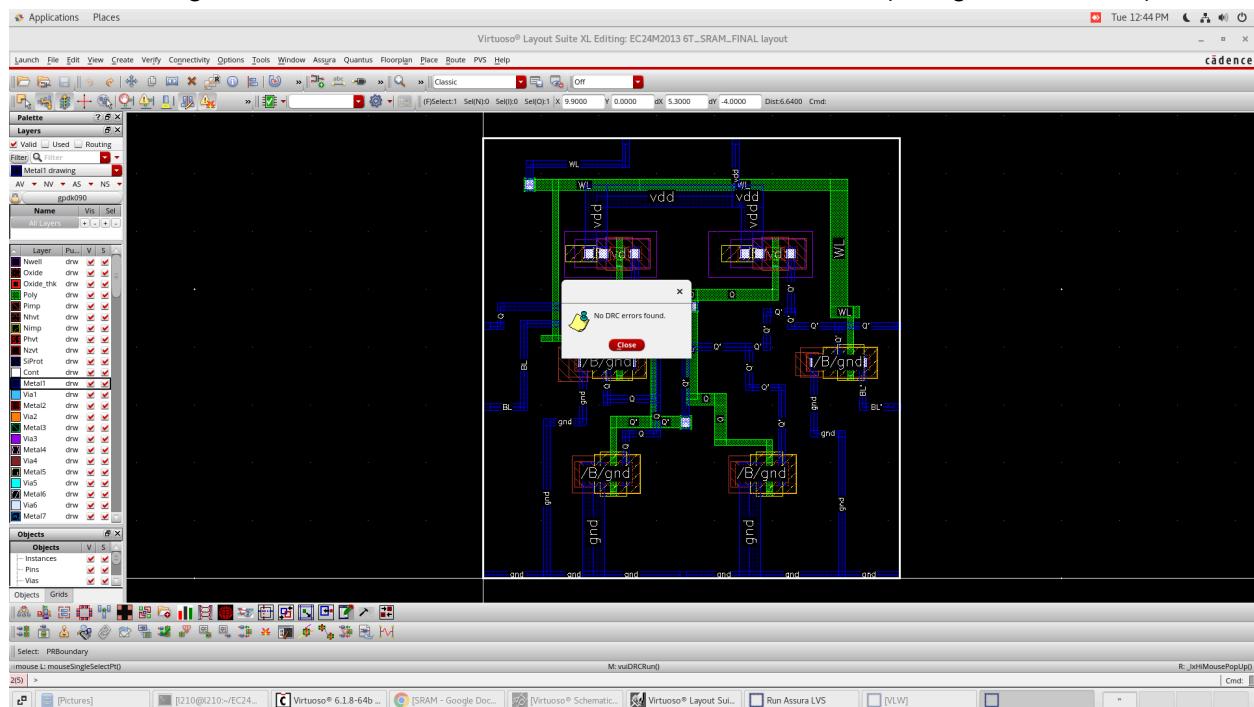
LAYOUT

The layout of 6T SRAM is shown below :



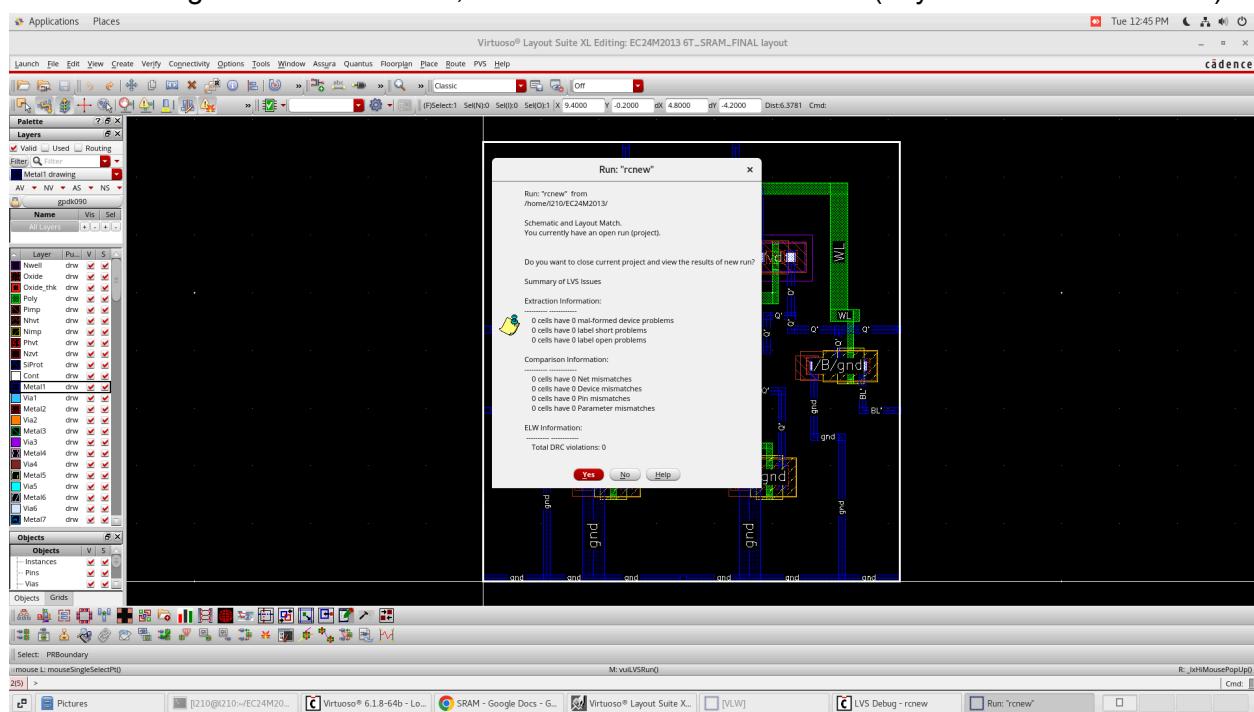
DRC

The below diagram shows the DRC, in which no errors were found. (Design Rule Check)



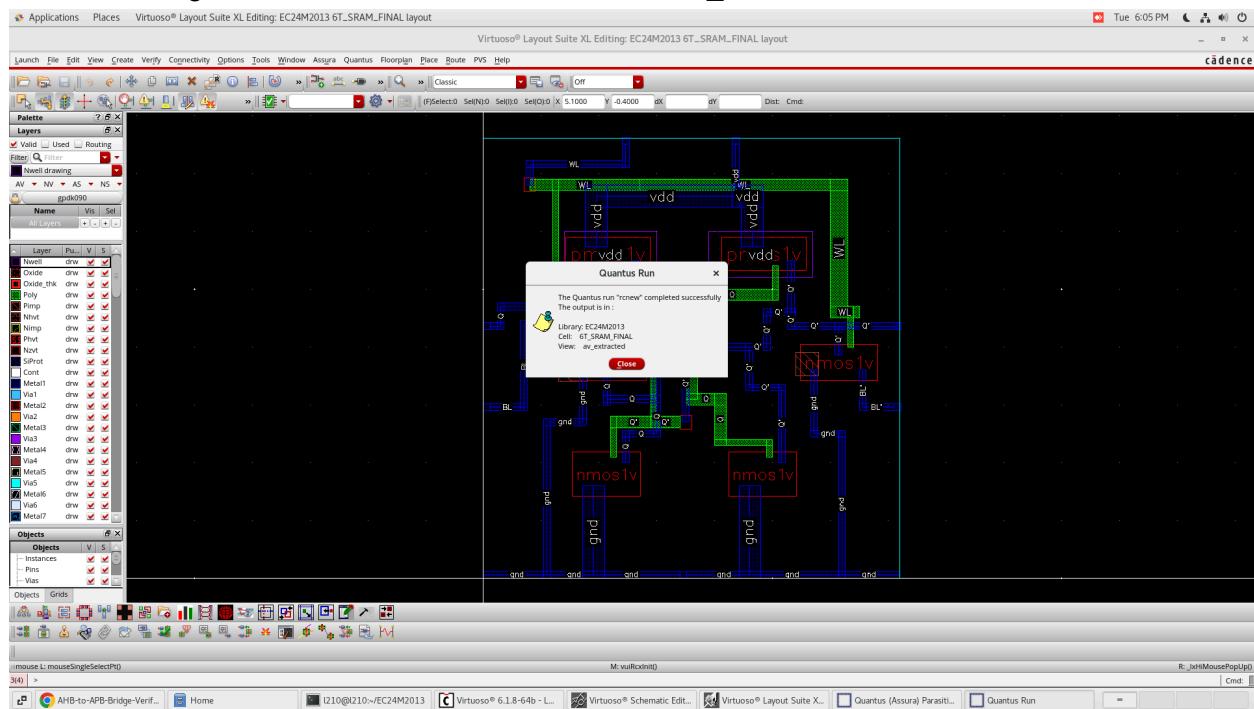
LVS

The below diagram shows the LVS, in which no errors were found. (Layout Versus Schematic)



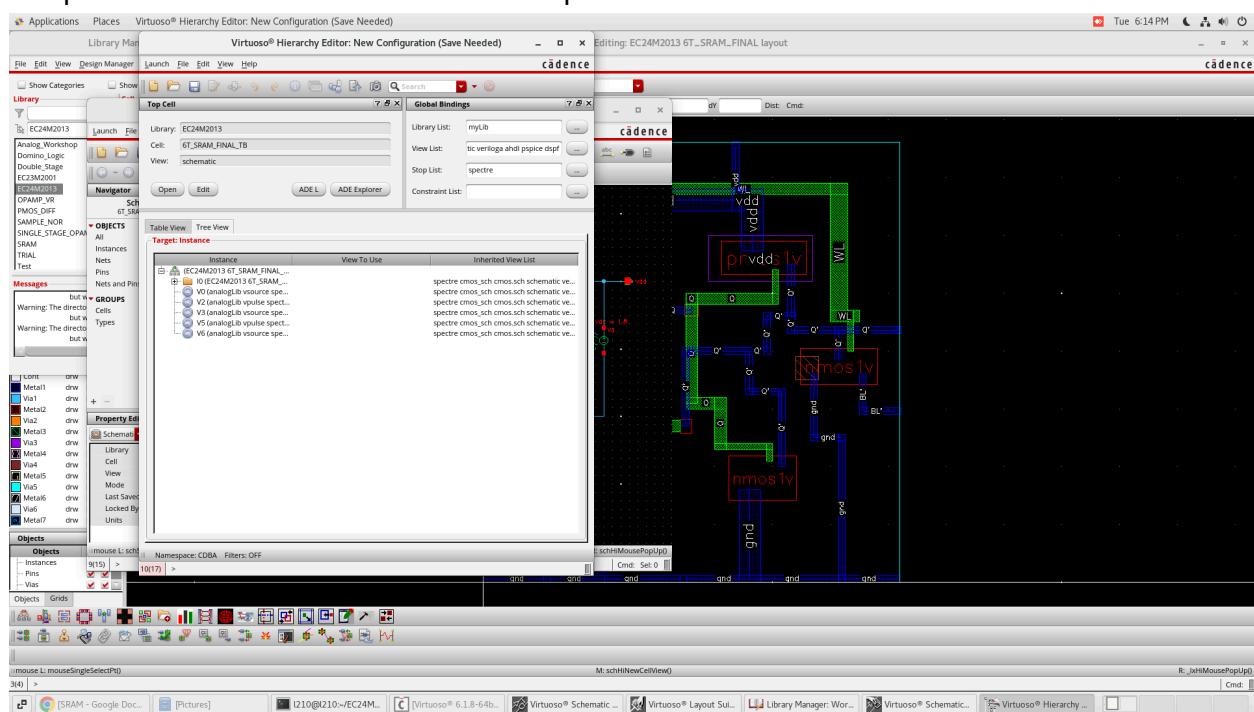
QUANTUS

The below diagram shows the QUANTUS, in which av_extracted was done.



PARASITIC EXTRACTION

The parasitic extraction involves various capacitance and resistance values added.



POST LAYOUT STIMULATION

WRITE 0



WRITE 1



READ 1

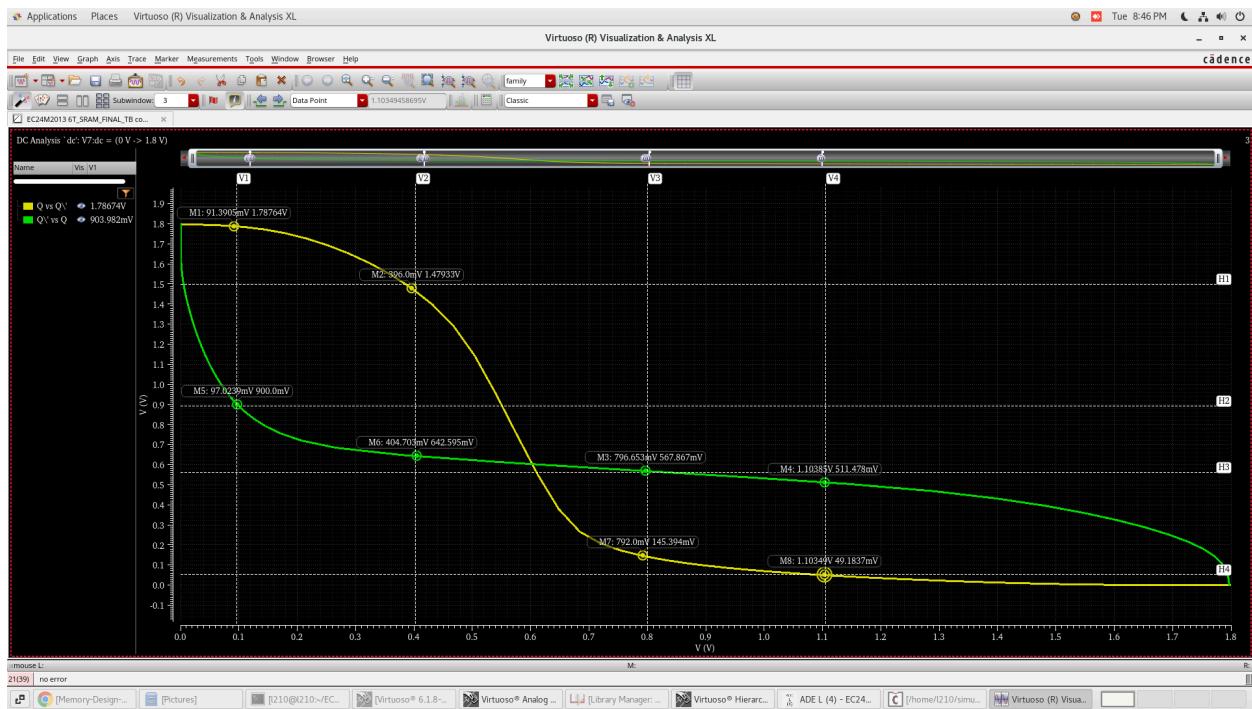


READ 0



HOLD STABILITY

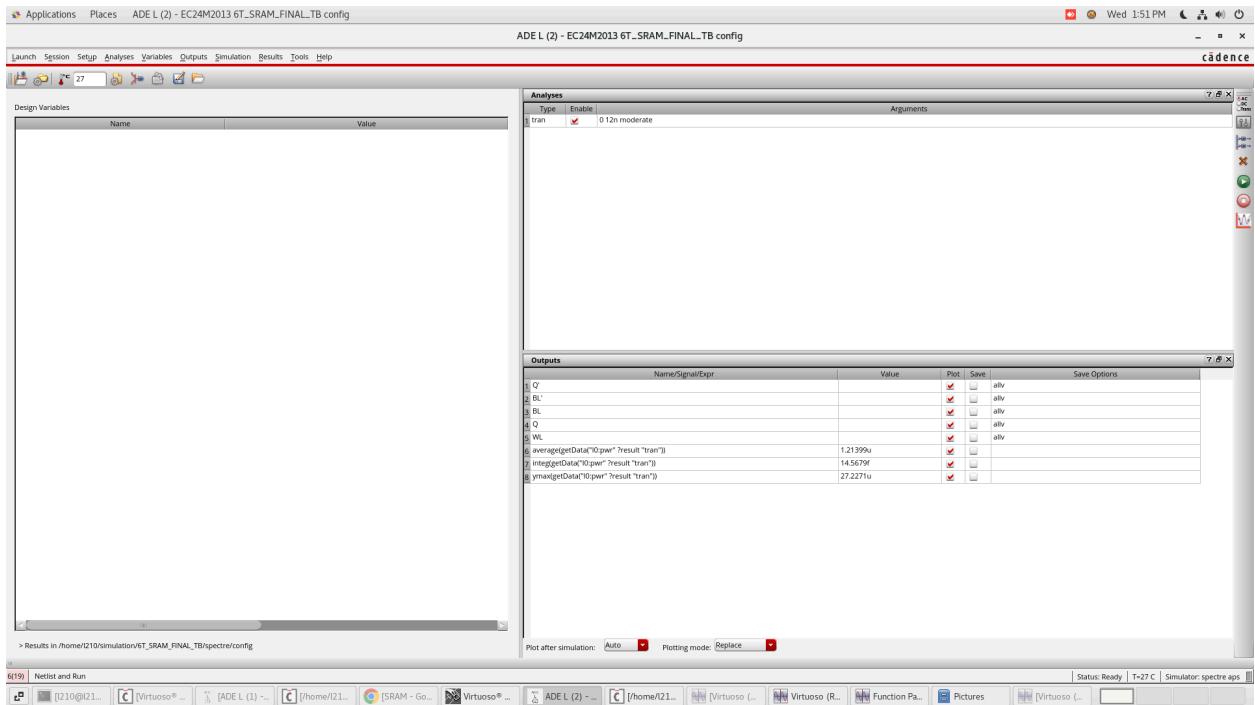
Butterfly curve for Hold state:



$$\begin{aligned} \text{SNM} &= \min(\max(\text{SNM1}), \max(\text{SNM2})) \\ &= \min(305.869\text{mV}, 307.075\text{mV}) \\ &= 307.075\text{mV} \end{aligned}$$

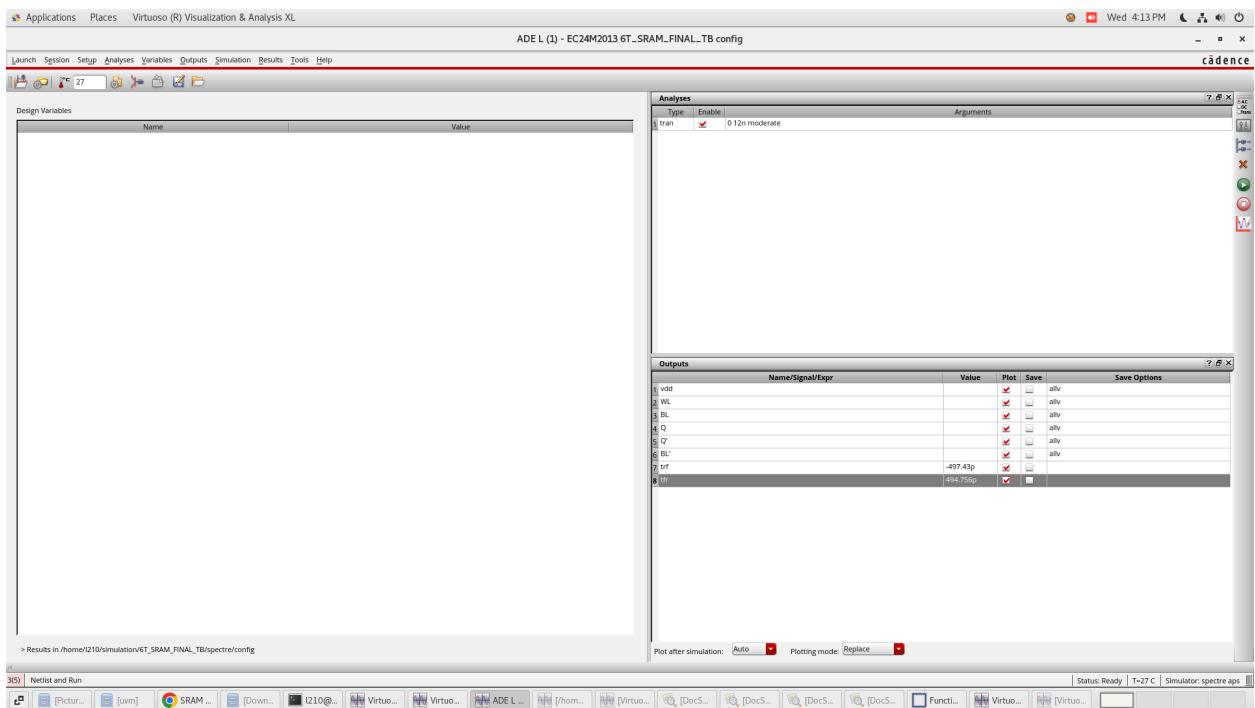
POWER ANALYSIS





The above graph shows the power obtained during post layout simulation, we get an average power of **1213.872 nW**.

DELAY



We get $tfr = 494.755 \text{ ps}$ and $trf = 497.43 \text{ ps}$. The average delay $tpd = (tfr+trf)/2 = 496.0925 \text{ ps}$.

CIRCUIT INVENTORY

```
Scope - 
Scoped user options:
Circuit inventory:
    nodes 58
    bsim3v3 6
    capacitor 137
    resistor 55
    vsource 4
```

INFERENCE

- The various sizing for SRAM 6T was analysed.
- The sizing with respect to read-write stability analysis was taken typically: **Pull-down > Access > Pull-up.**
- The transient analysis for the schematic was conducted for read and write operations.
- The power consumption and propagation delay were observed.
- The design of the layout corresponding to the schematic was made.
- The physical verifications, including Design Rule Check (DRC), Layout vs Schematic (LVS), and Parasitic Extraction (RCX), for the created layout were performed.
- The extracted layout to conduct post-layout simulation in Config mode.
- The results of pre-layout and post-layout simulations, and document the observations and inferences was completed.
- The table summarizing all the obtained values is shown below:

S NO	VARIABLE NAMES	OBTAINED VALUES	
		PRE LAYOUT SIMULATION	POST LAYOUT SIMULATION
1	POWER	879.872nW	1213.872 nW
2	DELAY	496.0925 ps	496.924 p s
3	Circuit inventory	nodes 6 bsim3v3 6 vsource 5	nodes 58 bsim3v3 6 Capacitor 137 Resistor 55 vsource 5

RESULT:

Hence, the pre and post layout simulation along with power and delay analysis of a 6T SRAM is performed successfully. The read and write operations were also observed through transient analysis.

REFERENCE

1. <https://github.com/VardhanSuroshi/Memory-Design-And-Testing>
2. Performance Evaluation of 6T SRAM cell using 90 nm Technology (International Journal of Engineering Research & Technology (IJERT))
3. IEEE CONFERENCE - Design of Ultra Low Power 6T SRAM Cell using 180 nm CMOS Technology for Access Enhancement (2022 International Interdisciplinary Conference on Mathematics, Engineering and Science (MESIICON))