

Network Functions Table

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Table 1: Network Functions

Function Type	CLB	BRAM	Throughput (Gbps)	Latency (μ s)	Reference
Firewall	1150	5	2.9 - 6.6	1.84 - 4.2	[1]
Firewall	8537	1	2	23 - 212	[2]
Firewall	8123	241	92.16	73	[3]
DPI	8377	37	0.8	278	[2]
DPI	8612	438	0.8	2778	[2]
DPI	15206	36	14.4	-	[4]
DPI	713	96	90	-	[5]
DPI	5154	407	80	-	[6]
DPI	6048	399	102.6	-	[7]
AES	2532	0	49.38	-	[8]
AES	4095	0	59.3	2	[9]
AES	2304	0	45	-	[10]
AES	9561	450	119.3	-	[11]
AES	486	0	3.44	-	[12]

References

- [1] R. Ajami and A. Dinh, “Embedded network firewall on fpga,” in *2011 Eighth International Conference on Information Technology: New Generations*, 2011, pp. 1041–1043.
- [2] F. B. Lopes, G. L. Nazar, and A. E. Schaeffer-Filho, “Vnfaccel: An fpga-based platform for modular vnf components acceleration,” in *2021 IFIP/IEEE International Symposium on Integrated Network Management (IM)*, 2021, pp. 250–258.
- [3] A. Fiessler, C. Lorenz, S. Hager, B. Scheuermann, and A. W. Moore, “Hypafilter+: Enhanced hybrid packet filtering using hardware assisted classification and header space analysis,” *IEEE/ACM Transactions on Networking*, vol. 25, no. 6, pp. 3655–3669, 2017.

- [4] Y.-H. E. Yang, W. Jiang, and V. K. Prasanna, "Compact architecture for high-throughput regular expression matching on fpga," ser. ANCS '08. New York, NY, USA: Association for Computing Machinery, 2008, pp. 30–39.
- [5] W. Jiang and V. K. Prasanna, "A fpga-based parallel architecture for scalable high-speed packet classification," in *2009 20th IEEE International Conference on Application-specific Systems, Architectures and Processors*, 2009, pp. 24–31.
- [6] W. Jiang and V. Prasanna, "Large-scale wire-speed packet classification on fpgas," in *Proceedings of the 7th ACM SIGDA International Symposium on Field-Programmable Gate Arrays, FPGA'09*, 02 2009, pp. 219–228.
- [7] J. Fong, X. Wang, Y. Qi, J. Li, and W. Jiang, "Parasplit: A scalable architecture on fpga for terabit packet classification," in *2012 IEEE 20th Annual Symposium on High-Performance Interconnects*, 2012, pp. 1–8.
- [8] D. Smekal, J. Hajny, and Z. Martinasek, "Comparative analysis of different implementations of encryption algorithms on fpga network cards," *IFAC-PapersOnLine*, vol. 51, no. 6, pp. 312–317, 2018, 15th IFAC Conference on Programmable Devices and Embedded Systems PDeS 2018.
- [9] H. Zodpe and A. Sapkal, "An efficient aes implementation using fpga with enhanced security features," *Journal of King Saud University - Engineering Sciences*, vol. 32, no. 2, pp. 115–122, 2020.
- [10] M. I. Soliman and G. Y. Abozaid, "Fpga implementation and performance evaluation of a high throughput crypto coprocessor," *Journal of Parallel and Distributed Computing*, vol. 71, no. 8, pp. 1075–1084, 2011.
- [11] L. Henzen and W. Fichtner, "Fpga parallel-pipelined aes-gcm core for 100g ethernet applications," in *2010 Proceedings of ESSCIRC*, 2010, pp. 202–205.
- [12] Q. Liu, Z. Xu, and Y. Yuan, "High throughput and secure advanced encryption standard on field programmable gate array with fine pipelining and enhanced key expansion," *IET Computers & Digital Techniques*, vol. 9, no. 3, pp. 175–184, 2015.