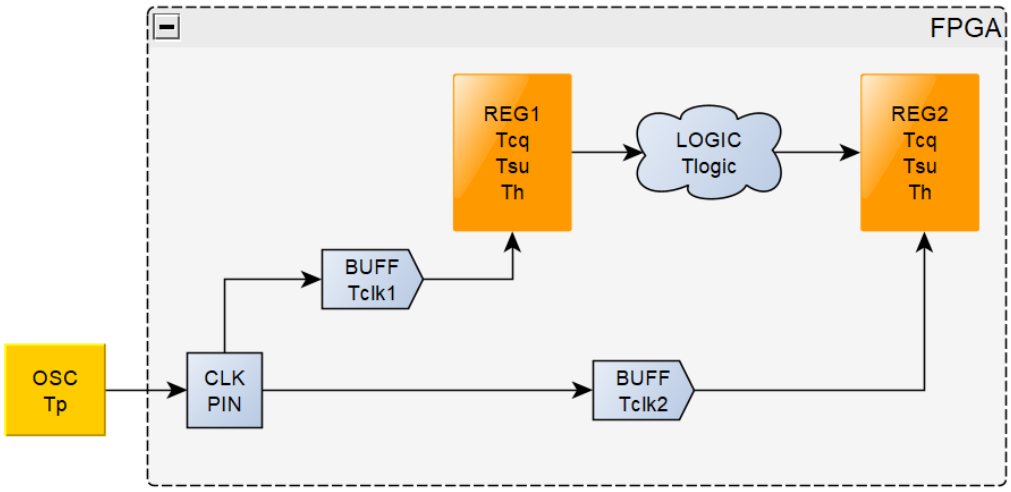
1. Период тактового сигнала



T_{clk1} – задержка от входа FPGA до запускающего триггера;
T_{clk2} – задержка от входа FPGA до защелкивающего триггера;
T_p – период тактового сигнала;
T_{cq} – задержка Clk-to-Q для триггеров;
T_{su} – setup time для триггеров;
T_h – hold time для триггеров;
T_{logic} – задержка через логику;
T_{jit} – джиттер;
T_{un} – дополнительная непредвиденная задержка;
$T_{clk\ skew}$ – расфазировка тактового сигнала.

Setup Time.
Запускающий фронт:

$$\text{Launch Clk Time} = T_{clk1\ max}.$$

Защелкивающий фронт:

$$\text{Latch Clk Time} = T_{clk2\ min} + T_p.$$

Задержка данных:

$$\text{Data Delay} = T_{cq\ max} + T_{logic\ max}.$$

Прибытие данных:

$$\text{Arrival Time} = \text{Launch Clk Time} + \text{Data Delay}.$$

Требуемое время прибытие:

$$\text{Requier Time} = \text{Latch Clk Time} - T_{su}.$$

$$\text{Slack} = \text{Requier Time} - \text{Arrival Time} - T_{jit} - T_{un}.$$

$$\text{Slack} = T_p + T_{clk\ skew} - T_{su} - T_{cq\ max} - T_{logic\ max} - T_{jit} - T_{un}.$$

$$T_{clk\ skew} = T_{clk2\ min} - T_{clk1\ max}.$$

Hold Time.

Запускающий фронт:

$$\text{Launch Clk Time} = T_{clk1\ min}.$$

Защелкивающий фронт:

$$\text{Latch Clk Time} = T_{clk2\ max}.$$

Задержка данных:

$$\text{Data Delay} = T_{cq\ min} + T_{logic\ min}.$$

Прибытие данных:

$$\text{Arrival Time} = \text{Launch Clk Time} + \text{Data Delay}.$$

Требуемое время прибытие:

$$\text{Requier Time} = \text{Latch Clk Time} + T_h.$$

$$\text{Slack} = \text{Arrival Time} - \text{Requier Time} - T_{jit} - T_{un}.$$

$$\text{Slack} = T_{cq\ min} + T_{logic\ min} - T_{clk\ skew} - T_h - T_{jit} - T_{un}.$$

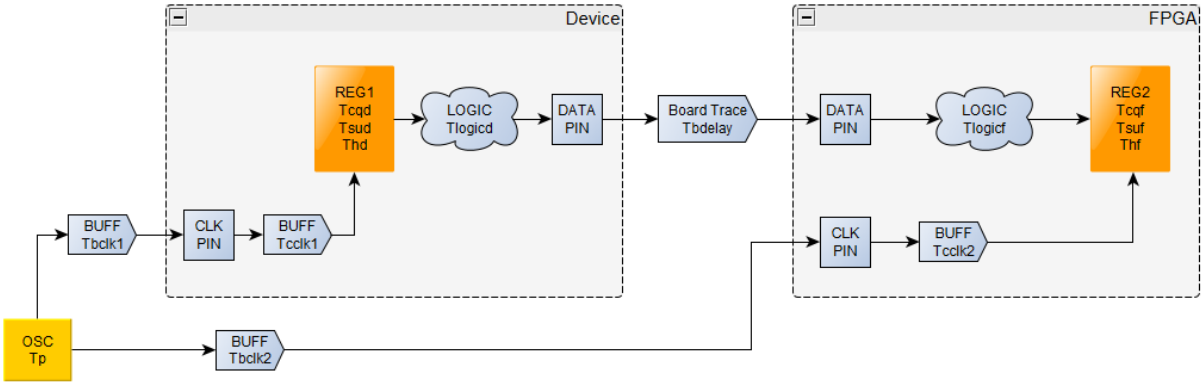
$$T_{clk\ skew} = T_{clk2\ max} - T_{clk1\ min}.$$

Constraints.

- `create_clock -name CLK -period Tp [get_ports CLK_PIN]`
- `set_system_jitter Tjit` или
  `set_input_jitter [get_clocks CLK] Tjit`
- `set_clock_uncertainty -from [get_clocks CLK] -to \`
  `[get_clocks CLK] Tun`

2. Входные ограничения

2.1. System Synchronous



T_{cclk1} – задержка от входа Device до запускающего триггера;
T_{bclk1} – задержка от генератора до входа Device;
T_{cclk2} – задержка от входа FPGA до защелкивающего триггера;
T_{bclk2} – задержка от генератора до входа FPGA;
T_{p} – период тактового сигнала;
T_{cqd} – задержка Clk-to-Q для триггеров Device;
T_{sud} – setup time для триггеров Device;
T_{hd} – hold time для триггеров Device;
T_{logicd} – задержка через логику Device;
T_{cqf} – задержка Clk-to-Q для триггеров FPGA;
T_{suf} – setup time для триггеров FPGA;
T_{hf} – hold time для триггеров FPGA;
T_{logicf} – задержка через логику FPGA;
T_{bdelay} – задержка данных на дорожке платы;
T_{jit} – джиттер;
T_{un} – дополнительная непредвиденная задержка,

Setup Time.

Запускающий фронт:

$$\text{Launch Clk Time} = T_{bclk1\ max} + T_{cclk1\ max}.$$

Защелкивающий фронт:

$$\text{Latch Clk Time} = T_{bclk2\ min} + T_{cclk2\ min} + T_{p}.$$

Задержка данных:

$$\text{Data Delay} = T_{cqd\ max} + T_{logicd\ max} + T_{bdelay\ max} + T_{logicf\ max}.$$

Прибытие данных:

$$\text{Arrival Time} = \text{Launch Clk Time} + \text{Data Delay}.$$

Требуемое время прибытие:

$$\text{Requier Time} = \text{Latch Clk Time} - T_{suf}.$$

$$\text{Slack} = \text{Requier Time} - \text{Arrival Time} - T_{jit} - T_{un}.$$

$$\text{Slack} = \text{Latch Clk Time} - T_{suf} - \text{Launch Clk Time} - \text{Data Delay} - T_{jit} - T_{un}.$$

$$\text{Slack} = T_{bclk2\ min} + T_{cclk2\ min} + T_{p} - T_{suf} - T_{bclk1\ max} - T_{cclk1\ max} - T_{cqd\ max} - T_{logicd\ max} - T_{bdelay\ max} - T_{logicf\ max} - T_{jit} - T_{un}.$$

$$\text{Slack} = T_{p} - \text{Input Delay} - \text{FPGA Delay} - T_{suf} - T_{jit} - T_{un}.$$

В FPGA известны следующие параметры: T_{cclk2}, T_{suf}, T_{logicf}. Остальные необходимо указать.

Constraints 1.

$$\text{Input Delay} = T_{bclk1\ max} - T_{bclk2\ min} + T_{cclk1\ max} + T_{cqd\ max} + T_{logicd\ max} + T_{bdelay\ max}$$

- ```
  create_clock -name CLK -period Tp [get_ports CLK_PIN]
  ```

- ```
  set_input_delay -clock CLK -max Input Delay [get_ports DATA_PIN]
  ```

Constraints 2.

$\text{Latency 1} = T_{bclk1\ max}$

$\text{Latency 2} = T_{bclk2\ min}$

$$\text{Input Delay} = T_{cclk1\ max} + T_{cqd\ max} + T_{logicd\ max} + T_{bdelay\ max}$$

- ```
  create_clock -name CLK_DEV -period Tp
  set_clock_latency -source -late Latency_1 [get_clocks CLK_DEV]

  create_clock -name CLK_FPGA -period Tp [get_ports CLK_PIN]
  set_clock_latency -source -early Latency_2 [get_clocks CLK_FPGA]
  ```

- ```
  set_input_delay -clock CLK_DEV -max \
  Input Delay [get_ports DATA_PIN]
  ```

Hold Time.

Запускающий фронт:

$$\text{Launch Clk Time} = T_{bclk1\ min} + T_{cclk1\ min}.$$

Защелкивающий фронт:

$$\text{Latch Clk Time} = T_{bclk2\ max} + T_{cclk2\ max}.$$

Задержка данных:

$$\text{Data Delay} = T_{cqd\ min} + T_{logicd\ min} + T_{bdelay\ min} + T_{logicf\ min}.$$

Прибытие данных:

$$\text{Arrival Time} = \text{Launch Clk Time} + \text{Data Delay}.$$

Требуемое время прибытие:

$$\text{Requier Time} = \text{Latch Clk Time} + T_{hf}.$$

$$\text{Slack} = \text{Arrival Time} - \text{Requier Time} - T_{jit} - T_{un}.$$

$$\text{Slack} = \text{Launch Clk Time} + \text{Data Delay} - \text{Latch Clk Time} - T_{hf} - T_{jit} - T_{un}.$$

$$\text{Slack} = T_{bclk1\ min} + T_{cclk1\ min} + T_{cqd\ min} + T_{logicd\ min} + T_{bdelay\ min} + T_{logicf\ min} - T_{bclk2\ max} - T_{cclk2\ max} - T_{hf} - T_{jit} - T_{un}.$$

$$\text{Slack} = \text{Input Delay} + \text{FPGA Delay} - T_{hf} - T_{jit} - T_{un}.$$

В FPGA известны следующие параметры: T_{cclk2}, T_{hf}, T_{logicf}. Остальные необходимо указать.

Constraints 1.

$$\text{Input Delay} = T_{bclk1\ min} - T_{bclk2\ max} + T_{cclk1\ min} + T_{cqd\ min} + T_{logicd\ min} + T_{bdelay\ min}$$

- `create_clock -name CLK -period Tp [get_ports CLK_PIN]`

- `set_input_delay -clock CLK -min Input Delay [get_ports DATA_PIN]`

Constraints 2.

Latency 1 = $T_{bclk1\ min}$

Latency 2 = $T_{bclk2\ max}$

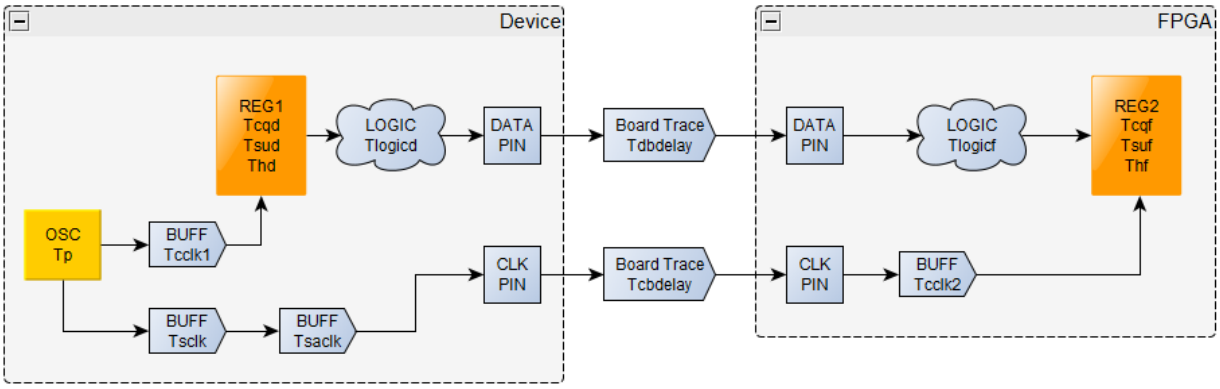
Input Delay = $T_{cclk1\ min} + T_{cqd\ min} + T_{logicd\ min} + T_{bdelay\ min}$

- ```
  create_clock -name CLK_DEV -period Tp
  set_clock_latency -source -early Latency_1 [get_clocks CLK_DEV]

  create_clock -name CLK_FPGA -period Tp [get_ports CLK_PIN]
  set_clock_latency -source -late Latency_2 [get_clocks CLK_FPGA]
  ```

- ```
  set_input_delay -clock CLK_DEV -min \
  Input Delay [get_ports DATA_PIN]
  ```

2.2. Source Synchronous



T_{cclk1} – задержка от OSC до запускающего триггера;
T_{sclk} – задержка от OSC до выхода Device;
T_{saclk} – дополнительная задержка от OSC до выхода Device;
T_{cclk2} – задержка от входа FPGA до защелкивающего триггера;
T_{p} – период тактового сигнала;
T_{cqd} – задержка Clk-to-Q для триггеров Device;
T_{sud} – setup time для триггеров Device;
T_{hd} – hold time для триггеров Device;
T_{logicd} – задержка через логику Device;
T_{cqf} – задержка Clk-to-Q для триггеров FPGA;
T_{suf} – setup time для триггеров FPGA;
T_{hf} – hold time для триггеров FPGA;
T_{logicf} – задержка через логику FPGA;
$T_{dbdelay}$ – задержка данных на дорожке платы;
$T_{cbdelay}$ – задержка тактового сигнала на дорожке платы;
T_{jit} – джиттер;
T_{un} – дополнительная непредвиденная задержка,

Setup Time.

Запускающий фронт:

$$\text{Launch Clk Time} = T_{\text{cclk1 max}}.$$

Защелкивающий фронт:

$$\text{Latch Clk Time} = T_{\text{sclk min}} + T_{\text{saclk}} + T_{\text{cclk2 min}} + T_{\text{cbdelay min}}.$$

Задержка данных:

$$\text{Data Delay} = T_{\text{cqd max}} + T_{\text{logicd max}} + T_{\text{dbdelay max}} + T_{\text{logicf max}}.$$

Прибытие данных:

$$\text{Arrival Time} = \text{Launch Clk Time} + \text{Data Delay}.$$

Требуемое время прибытие:

$$\text{Requier Time} = \text{Latch Clk Time} - T_{\text{suf}}.$$

$$\text{Slack} = \text{Requier Time} - \text{Arrival Time} - T_{\text{jit}} - T_{\text{un}}.$$

$$\text{Slack} = \text{Latch Clk Time} - T_{\text{suf}} - \text{Launch Clk Time} - \text{Data Delay} - T_{\text{jit}} - T_{\text{un}}.$$

$$\text{Slack} = T_{\text{sclk min}} + T_{\text{saclk}} + T_{\text{cclk2 min}} + T_{\text{cbdelay min}} - T_{\text{cclk1 max}} -$$
$$- T_{\text{cqd max}} - T_{\text{logicd max}} - T_{\text{dbdelay max}} - T_{\text{logicf max}} - T_{\text{suf}} - T_{\text{jit}} - T_{\text{un}}$$

$$\text{Slack} = T_{\text{p}} - \text{Input Delay} - \text{FPGA Delay} - T_{\text{suf}} - T_{\text{jit}} - T_{\text{un}}.$$

В FPGA известны следующие параметры: T_{cclk2}, T_{suf}, T_{logicf}. Остальные необходимо указать.

$$\text{Input Delay max} = T_{\text{cclk1 max}} - T_{\text{sclk min}} - T_{\text{saclk}} - T_{\text{cbdelay min}} +$$
$$+ T_{\text{cqd max}} + T_{\text{logicd max}} + T_{\text{dbdelay max}} + T_{\text{p}}$$

$$\text{Input Delay max} = T_{\text{p}} + \text{Data to Pin Delay max} - \text{Clock to Pin Delay min}$$

$$\text{Data to Pin Delay max} = T_{\text{cclk1 max}} + T_{\text{cqd max}} + T_{\text{logicd max}} + T_{\text{dbdelay max}}$$

$$\text{Clock to Pin Delay min} = T_{\text{sclk min}} + T_{\text{saclk}} + T_{\text{cbdelay min}}$$

Hold Time.

Запускающий фронт:

$$\text{Launch Clk Time} = T_{\text{cclk1 min}}.$$

Защелкивающий фронт:

$$\text{Latch Clk Time} = T_{\text{sclk max}} + T_{\text{saclk}} + T_{\text{cclk2 max}} + T_{\text{cbdelay max}} - T_{\text{p}}.$$

Задержка данных:

$$\text{Data Delay} = T_{\text{cqd min}} + T_{\text{logicd min}} + T_{\text{dbdelay min}} + T_{\text{logicf min}}.$$

Прибытие данных:

$$\text{Arrival Time} = \text{Launch Clk Time} + \text{Data Delay}.$$

Требуемое время прибытие:

$$\text{Requier Time} = \text{Latch Clk Time} + T_{\text{hf}}.$$

$$\text{Slack} = \text{Arrival Time} - \text{Requier Time} - T_{\text{jit}} - T_{\text{un}}.$$

$$\text{Slack} = \text{Launch Clk Time} + \text{Data Delay} - \text{Latch Clk Time} - T_{\text{hf}} - T_{\text{jit}} - T_{\text{un}}.$$

$$\text{Slack} = T_{\text{p}} + T_{\text{cclk1 min}} - T_{\text{sclk max}} - T_{\text{saclk}} - T_{\text{cclk2 max}} - T_{\text{cbdelay max}} + \\ + T_{\text{cqd min}} + T_{\text{logicd min}} + T_{\text{dbdelay min}} + T_{\text{logicf min}} - T_{\text{hf}} - T_{\text{jit}} - T_{\text{un}}$$

$$\text{Slack} = \text{Input Delay} + \text{FPGA Delay} - T_{\text{hf}} - T_{\text{jit}} - T_{\text{un}}.$$

В FPGA известны следующие параметры: T_{cclk2}, T_{suf}, T_{logicf}. Остальные необходимо указать.

$$\text{Input Delay min} = T_{\text{p}} + T_{\text{cclk1 min}} - T_{\text{sclk max}} - T_{\text{saclk}} - T_{\text{cbdelay max}} + \\ + T_{\text{cqd min}} + T_{\text{logicd min}} + T_{\text{dbdelay min}}$$

$$\text{Input Delay min} = T_{\text{p}} + \text{Data to Pin Delay min} - \text{Clock to Pin Delay max}$$

$$\text{Data to Pin Delay min} = T_{\text{cclk1 min}} + T_{\text{cqd min}} + T_{\text{logicd min}} + T_{\text{dbdelay min}}$$

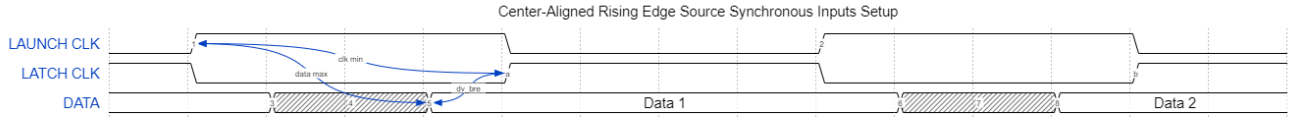
$$\text{Clock to Pin Delay max} = T_{\text{sclk max}} + T_{\text{saclk}} + T_{\text{cbdelay max}}$$

Constraints 1.

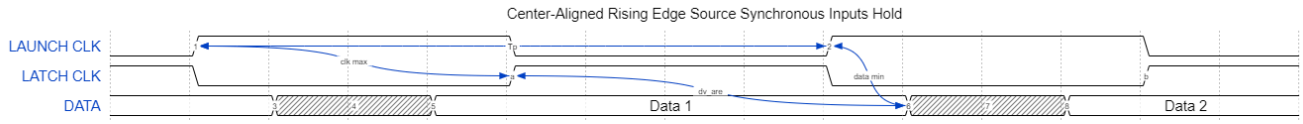
```
# Center-Aligned Rising Edge Source Synchronous Inputs
#
# For a center-aligned Source Synchronous interface, the clock
# transition is aligned with the center of the data valid window.
# The same clock edge is used for launching and capturing the
# data. The constraints below rely on the default timing
# analysis (setup = 1 cycle, hold = 0 cycle).
#
# input     ____              __________
# clock         |__________|           |_____
#                          |
#                   dv_bre | dv_are
#                  <------>|<------>
#             __     _______|________     __
# data        __XXXX____Rise_Data____XXXX__
```

$$T_{saclk} = T_p/2$$

$$dv_{bre} + \text{Data to Pin Delay max} = \text{Clock to Pin Delay min}$$
$$dv_{bre} = T_p - \text{Input Delay max}$$
$$\text{Input Delay max} = T_p - dv_{bre}$$



$$dv_{are} + \text{Clock to Pin Delay max} = T_p + \text{Data to Pin Delay min}$$
$$dv_{are} = \text{Input Delay min}$$
$$\text{Input Delay min} = dv_{are}$$



- `create_clock -name CLK -period Tp [get_ports CLK_PIN]`
- `set_input_delay -clock CLK -max (Tp- dv_bre) [get_ports DATA_PIN]`
- `set_input_delay -clock CLK -min dv_are [get_ports DATA_PIN]`

Constraints 2.

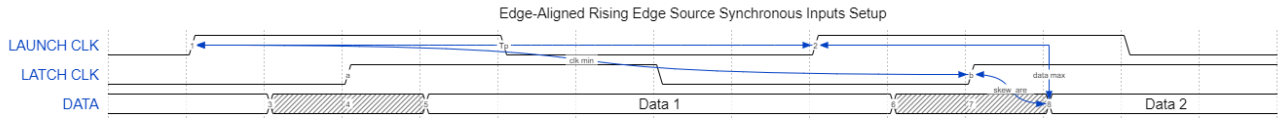
```
# Edge-Aligned Rising Edge Source Synchronous Inputs
# (Using an MMCM/PLL)
#
# For an edge-aligned Source Synchronous interface, the clock
# transition occurs at the same time as the data transitions.
# In this template, the clock is aligned with the end of the
# data. The constraints below rely on the default timing
# analysis (setup = 1 cycle, hold = 0 cycle).
#
# input    __________                    ___________________
# clock              |__________________|                   |__________
#                                       |
#                                skew_bre|skew_are
#                                <------>|<------>
#              ____________________      |      ____________________
# data     XX____Rise_Data____XXXXXXXXXXXXXXXXX____________________XX
```

$$T_{saclk} = T_p$$

$$\text{skew}_{are} + \text{Clock to Pin Delay min} = T_p + \text{Data to Pin Delay max}$$

$$\text{skew}_{are} = \text{Input Delay max}$$

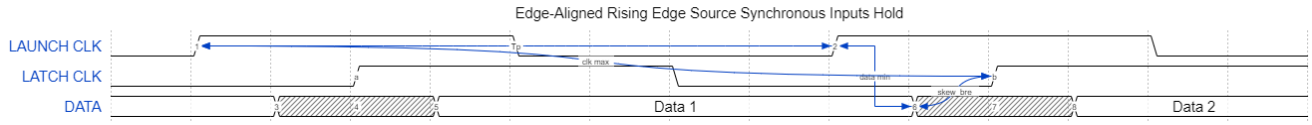
$$\text{Input Delay max} = \text{skew}_{are}$$



$$\text{skew}_{bre} + T_p + \text{Data to Pin Delay min} = \text{Clock to Pin Delay max}$$

$$\text{skew}_{bre} = -\text{Input Delay min}$$

$$\text{Input Delay min} = -\text{skew}_{bre}$$



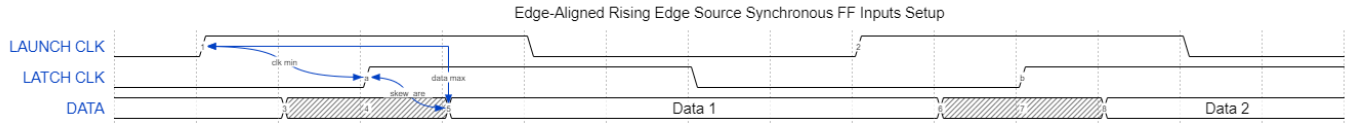
- `create_clock -name CLK -period Tp [get_ports CLK_PIN]`
- `set_input_delay -clock CLK -max skew_are [get_ports DATA_PIN]`
- `set_input_delay -clock CLK -min -skew_bre [get_ports DATA_PIN]`

Constraints 3.

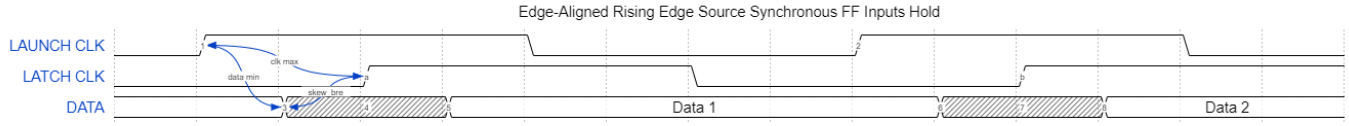
```
# Edge-Aligned Rising Edge Source Synchronous Inputs
# (Using a direct FF connection)
#
# For an edge-aligned Source Synchronous interface, the clock
# transition occurs at the same time as the data transitions.
# In this template, the clock is aligned with the beginning of the
# data. The constraints below rely on the default timing
# analysis (setup = 1 cycle, hold = 0 cycle).
#
# input    __________                    ________________
# clock              |__________________|                |__________
#                                      |
#                                skew_bre|skew_are
#                                <------>|<------>
#              ___________________       |       ___________________
# data     XXX_____________________XXXXXXXXXXXXXXXXX____Rise_Data___XXX
```

$$T_{saclk} = 0$$

$$skew_{are} + \text{Clock to Pin Delay min} = \text{Data to Pin Delay max}$$
$$skew_{are} = \text{Input Delay max} - T_p$$
$$\text{Input Delay max} = skew_{are} + T_p$$



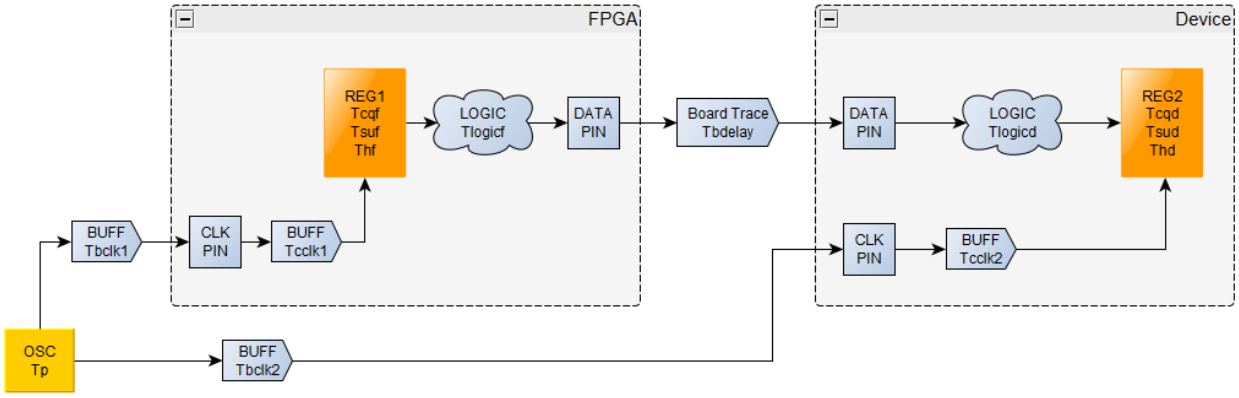
$$skew_{bre} + \text{Data to Pin Delay min} = \text{Clock to Pin Delay max}$$
$$skew_{bre} = T_p - \text{Input Delay min}$$
$$\text{Input Delay min} = T_p - skew_{bre}$$



- `create_clock -name CLK -period Tp [get_ports CLK_PIN]`
- `set_input_delay -clock CLK -max (Tp+skew_are)[get_ports DATA_PIN]`
- `set_input_delay -clock CLK -min (Tp-skew_bre)[get_ports DATA_PIN]`

3. Выходные ограничения

3.1. System Synchronous



T_{cclk1} – задержка от входа FPGA до запускающего триггера;
T_{bclk1} – задержка от генератора до входа FPGA;
T_{cclk2} – задержка от входа Device до защелкивающего триггера;
T_{bclk2} – задержка от генератора до входа Device;
T_{p} – период тактового сигнала;
T_{cqd} – задержка Clk-to-Q для триггеров Device;
T_{sud} – setup time для триггеров Device;
T_{hd} – hold time для триггеров Device;
T_{logicd} – задержка через логику Device;
T_{cqf} – задержка Clk-to-Q для триггеров FPGA;
T_{suf} – setup time для триггеров FPGA;
T_{hf} – hold time для триггеров FPGA;
T_{logicf} – задержка через логику FPGA;
T_{bdelay} – задержка данных на дорожке платы;
T_{jit} – джиттер;
T_{un} – дополнительная непредвиденная задержка,

Setup Time.

Запускающий фронт:

$$\text{Launch Clk Time} = T_{bclk1\ max} + T_{cclk1\ max}.$$

Защелкивающий фронт:

$$\text{Latch Clk Time} = T_{bclk2\ min} + T_{cclk2\ min} + T_p.$$

Задержка данных:

$$\text{Data Delay} = T_{cqf\ max} + T_{logicf\ max} + T_{bdelay\ max} + T_{logicd\ max}.$$

Прибытие данных:

$$\text{Arrival Time} = \text{Launch Clk Time} + \text{Data Delay}.$$

Требуемое время прибытие:

$$\text{Requier Time} = \text{Latch Clk Time} - T_{sud}.$$

$$\text{Slack} = \text{Requier Time} - \text{Arrival Time} - T_{jit} - T_{un}.$$

$$\text{Slack} = \text{Latch Clk Time} - T_{sud} - \text{Launch Clk Time} - \text{Data Delay} - T_{jit} - T_{un}.$$

$$\text{Slack} = T_{bclk2\ min} + T_{cclk2\ min} + T_p - T_{sud} - T_{bclk1\ max} - T_{cclk1\ max} - T_{cqf\ max} - T_{logicf\ max} - T_{bdelay\ max} - T_{logicd\ max} - T_{jit} - T_{un}.$$

$$\text{Slack} = T_p - \text{Output Delay} - \text{FPGA Delay} - T_{jit} - T_{un}.$$

В FPGA известны следующие параметры: T_{cclk1}, T_{cqf}, T_{logicf}. Остальные необходимо указать.

Constraints 1.

$$\text{Output Delay} = T_{bclk1\ max} - T_{bclk2\ min} - T_{cclk2\ min} + T_{sud} + T_{bdelay\ max} + T_{logicd\ max}$$

- `create_clock -name CLK -period Tp [get_ports CLK_PIN]`

- `set_output_delay -clock CLK -max Output Delay [get_ports DATA_PIN]`

Constraints 2.

$\text{Latency 1} = T_{bclk1\ max}$

$\text{Latency 2} = T_{bclk2\ min}$

$\text{Output Delay} = T_{sud} + T_{bdelay\ max} + T_{logicd\ max} - T_{cclk2\ min}$

- ```
  create_clock -name CLK_DEV -period Tp
  set_clock_latency -source -early Latency_2 [get_clocks CLK_DEV]

  create_clock -name CLK_FPGA -period Tp [get_ports CLK_PIN]
  set_clock_latency -source -late Latency_1 [get_clocks CLK_FPGA]
  ```

- ```
  set_output_delay -clock CLK_DEV -max \
  Output Delay [get_ports DATA_PIN]
  ```

Hold Time.

Запускающий фронт:

$$\text{Launch Clk Time} = T_{bclk1\ min} + T_{cclk1\ min}.$$

Защелкивающий фронт:

$$\text{Latch Clk Time} = T_{bclk2\ max} + T_{cclk2\ max}.$$

Задержка данных:

$$\text{Data Delay} = T_{cqf\ min} + T_{logicf\ min} + T_{bdelay\ min} + T_{logicd\ min}.$$

Прибытие данных:

$$\text{Arrival Time} = \text{Launch Clk Time} + \text{Data Delay}.$$

Требуемое время прибытие:

$$\text{Requier Time} = \text{Latch Clk Time} + T_{hd}.$$

$$\text{Slack} = \text{Arrival Time} - \text{Requier Time} - T_{jit} - T_{un}.$$

$$\text{Slack} = \text{Launch Clk Time} + \text{Data Delay} - \text{Latch Clk Time} - T_{hd} - T_{jit} - T_{un}.$$

$$\text{Slack} = T_{bclk1\ min} + T_{cclk1\ min} + T_{cqf\ min} + T_{logicf\ min} + T_{bdelay\ min} + T_{logicd\ min} - T_{bclk2\ max} - T_{cclk2\ max} - T_{hd} - T_{jit} - T_{un}.$$

$$\text{Slack} = \text{Output Delay} + \text{FPGA Delay} - T_{jit} - T_{un}.$$

В FPGA известны следующие параметры: T_{cclk1}, T_{cqf}, T_{logicf}. Остальные необходимо указать.

Constraints 1.

$$\text{Output Delay} = T_{bclk1\ min} - T_{bclk2\ max} - T_{cclk2\ max} + T_{bdelay\ min} + T_{logicd\ min} - T_{hd}$$

- `create_clock -name CLK -period Tp [get_ports CLK_PIN]`
- `set_output_delay -clock CLK -min Output Delay [get_ports DATA_PIN]`

Constraints 2.

$\text{Latency 1} = T_{bclk1\ min}$

$\text{Latency 2} = T_{bclk2\ max}$

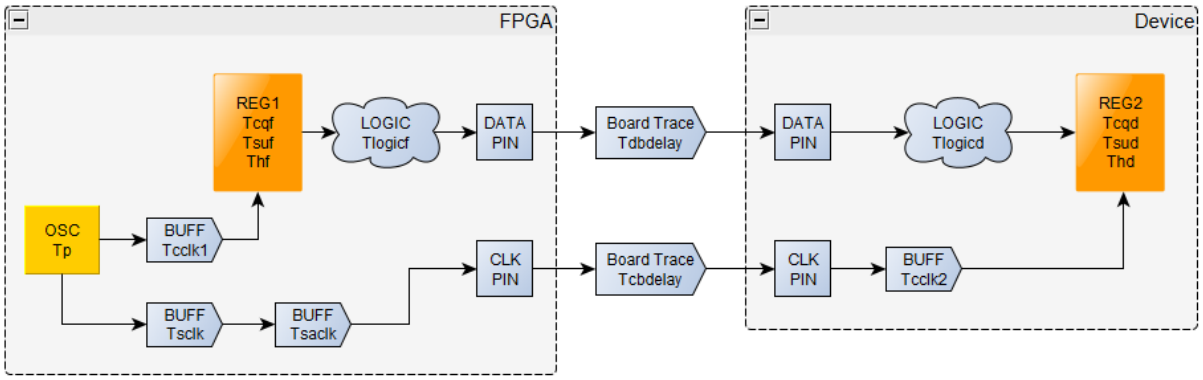
$\text{Output Delay} = T_{bdelay\ min} + T_{logicd\ min} - T_{hd} - T_{cclk2\ max}$

- ```
  create_clock -name CLK_DEV -period Tp
  set_clock_latency -source -late Latency_2 [get_clocks CLK_DEV]

  create_clock -name CLK_FPGA -period Tp [get_ports CLK_PIN]
  set_clock_latency -source -early Latency_1 [get_clocks CLK_FPGA]
  ```

- ```
  set_output_delay -clock CLK_DEV -min \
  Output Delay [get_ports DATA_PIN]
  ```

3.2. Source Synchronous



T_{cclk1} – задержка от OSC до запускающего триггера;
T_{sclk} – задержка от OSC до выхода Device;
T_{saclk} – дополнительная задержка от OSC до выхода FPGA;
T_{cclk2} – задержка от входа Device до защелкивающего триггера;
T_{p} – период тактового сигнала;
T_{cqd} – задержка Clk-to-Q для триггеров Device;
T_{sud} – setup time для триггеров Device;
T_{hd} – hold time для триггеров Device;
T_{logicd} – задержка через логику Device;
T_{cqf} – задержка Clk-to-Q для триггеров FPGA;
T_{suf} – setup time для триггеров FPGA;
T_{hf} – hold time для триггеров FPGA;
T_{logicf} – задержка через логику FPGA;
$T_{dbdelay}$ – задержка данных на дорожке платы;
$T_{cbdelay}$ – задержка тактового сигнала на дорожке платы;
T_{jit} – джиттер;
T_{un} – дополнительная непредвиденная задержка,

Setup Time.

Запускающий фронт:

$$\text{Launch Clk Time} = T_{\text{cclk1 max}}.$$

Защелкивающий фронт:

$$\text{Latch Clk Time} = T_{\text{sclk min}} + T_{\text{saclk}} + T_{\text{cclk2 min}} + T_{\text{cbdelay min}}.$$

Задержка данных:

$$\text{Data Delay} = T_{\text{cqf max}} + T_{\text{logicf max}} + T_{\text{dbdelay max}} + T_{\text{logicd max}}.$$

Прибытие данных:

$$\text{Arrival Time} = \text{Launch Clk Time} + \text{Data Delay}.$$

Требуемое время прибытие:

$$\text{Requier Time} = \text{Latch Clk Time} - T_{\text{sud}}.$$

$$\text{Slack} = \text{Requier Time} - \text{Arrival Time} - T_{\text{jit}} - T_{\text{un}}.$$

$$\text{Slack} = \text{Latch Clk Time} - T_{\text{sud}} - \text{Launch Clk Time} - \text{Data Delay} - T_{\text{jit}} - T_{\text{un}}.$$

$$\text{Slack} = T_{\text{sclk min}} + T_{\text{saclk}} + T_{\text{cclk2 min}} + T_{\text{cbdelay min}} - T_{\text{cclk1 max}} -$$
$$- T_{\text{cqf max}} - T_{\text{logicf max}} - T_{\text{dbdelay max}} - T_{\text{logicd max}} - T_{\text{sud}} - T_{\text{jit}} - T_{\text{un}}$$

$$\text{Slack} = T_{\text{p}} - \text{Output Delay} - \text{FPGA Delay} - T_{\text{jit}} - T_{\text{un}}.$$

В FPGA известны следующие параметры: $T_{\text{sclk min}}$, T_{saclk}, T_{cclk1} T_{cqf}, T_{logicf}. Остальные необходимо указать.

$$\text{Output Delay max} = T_{\text{dbdelay max}} + T_{\text{logicd max}} + T_{\text{sud}} - T_{\text{cclk2 min}} - T_{\text{cbdelay min}} + T_{\text{p}}$$

$$\text{Output Delay max} = T_{\text{p}} + \text{Pin to Data Delay max} - \text{Pin to Clock Delay min}$$

$$\text{Pin to Data Delay max} = T_{\text{dbdelay max}} + T_{\text{logicd max}} + T_{\text{sud}}$$
$$\text{Pin to Clock Delay min} = T_{\text{cclk2 min}} + T_{\text{cbdelay min}}$$

Hold Time.

Запускающий фронт:

$$\text{Launch Clk Time} = T_{\text{cclk1 min}}.$$

Защелкивающий фронт:

$$\text{Latch Clk Time} = T_{\text{sclk max}} + T_{\text{saclk}} + T_{\text{cclk2 max}} + T_{\text{cbdelay max}} - T_{\text{p}}.$$

Задержка данных:

$$\text{Data Delay} = T_{\text{cqf min}} + T_{\text{logicf min}} + T_{\text{dbdelay min}} + T_{\text{logicd min}}.$$

Прибытие данных:

$$\text{Arrival Time} = \text{Launch Clk Time} + \text{ Data Delay}.$$

Требуемое время прибытие:

$$\text{Requier Time} = \text{Latch Clk Time} + T_{\text{hd}}.$$

$$\text{Slack} = \text{Arrival Time} - \text{Requier Time} - T_{\text{jit}} - T_{\text{un}}.$$

$$\text{Slack} = \text{Launch Clk Time} + \text{ Data Delay} - \text{Latch Clk Time} - T_{\text{hd}} - T_{\text{jit}} - T_{\text{un}}.$$

$$\text{Slack} = T_{\text{p}} + T_{\text{cclk1 min}} - T_{\text{sclk max}} - T_{\text{saclk}} - T_{\text{cclk2 max}} - T_{\text{cbdelay max}} +$$
$$+T_{\text{cqf min}} + T_{\text{logicf min}} + T_{\text{dbdelay min}} + T_{\text{logicd min}} - T_{\text{hd}} - T_{\text{jit}} - T_{\text{un}}$$

$$\text{Slack} = \text{Output Delay} + \text{FPGA Delay} - T_{\text{jit}} - T_{\text{un}}.$$

В FPGA известны следующие параметры:$T_{\text{sclk min}}$, T_{saclk}, T_{cclk1} T_{cqf}, T_{logicf}. Остальные необходимо указать.

$$\text{Output Delay min} = T_{\text{p}} + T_{\text{dbdelay min}} + T_{\text{logicd min}} - T_{\text{hd}} - T_{\text{cclk2 max}} - T_{\text{cbdelay max}}$$

$$\text{Output Delay min} = T_{\text{p}} + \text{Pin to Data Delay min} - \text{Pin to Clock Delay max}$$
$$\text{Pin to Data Delay min} = T_{\text{dbdelay min}} + T_{\text{logicd min}} - T_{\text{hd}}$$
$$\text{Pin to Clock Delay max} = T_{\text{cclk2 max}} + T_{\text{cbdelay max}}$$

Constraints 1.

```
#  Rising Edge Source Synchronous Outputs
#
#  Source synchronous output interfaces can be constrained either by the max data skew
#  relative to the generated clock or by the destination device setup/hold requirements.
#
#  Max Skew Case:
#  The skew requirements for FPGA are known from system level analysis.
#
# forwarded                  _____________
# clock        ____________|             |_________
#                          |
#                  bre_skew|are_skew
#                  <------>|<------>
#             _____        |        _____________
# data        _____XXXXXXXXXXXXXXXXX_____________XXXXX
#
# Example of creating generated clock at clock output port
# create_generated_clock -name <gen_clock_name> -multiply_by 1 -source \
# [get_pins <source_pin>] [get_ports <output_clock_port>]
# gen_clock_name is the name of forwarded clock here. It should be used below for defining
"fwclk".
```

$$T_{saclk} = 0$$

Необходимое условие: Slack ≥ 0. Пусть $T_{jit} = T_{un} = 0$

Для Setup:

$$\text{Slack} = 0$$

$$T_{sclk\,min} + T_{saclk} + T_{cclk2\,min} + T_{cbdelay\,min} - T_{cclk1\,max} -$$
$$- T_{cqf\,max} - T_{logicf\,max} - T_{dbdelay\,max} - T_{logicd\,max} - T_{sud} = 0$$

$$\text{Forwareded Clk Delay min} = T_{sclk\,min} + T_{saclk}$$
$$\text{Pin to Clock Delay min} = T_{cclk2\,min} + T_{cbdelay\,min}$$
$$\text{Pin to Data Delay max} = T_{cclk1\,max} + T_{cqf\,max} + T_{logicf\,max}$$
$$\text{Data to Pin Delay max} = T_{dbdelay\,max} + T_{logicd\,max} + T_{sud}$$

$$0 = \text{Forwareded Clk Delay min} + \text{Pin to Clock Delay min} -$$
$$-\text{Pin to Data Delay max} - \text{Data to Pin Delay max}$$

$$\text{Data to Pin Delay max} - \text{Forwareded Clk Delay min} =$$
$$= \text{Pin to Clock Delay min} - \text{Pin to Data Delay max} + T_p - T_p$$

$$are_{skew} = \text{Data to Pin Delay max} - \text{Forwareded Clk Delay min}$$

$$\text{Output Delay max} = T_p + \text{Pin to Data Delay max} - \text{Pin to Clock Delay min}$$

$$are_{skew} = T_p - \text{Output Delay max}$$

$$\text{Output Delay max} = T_p - are_{skew}$$

Для Hold:

$$\text{Slack} = 0$$

$$T_p + T_{\text{cclk1 min}} - T_{\text{sclk max}} - T_{\text{saclk}} - T_{\text{cclk2 max}} - T_{\text{cbdelay max}} +$$
$$+T_{\text{cqf min}} + T_{\text{logicf min}} + T_{\text{dbdelay min}} + T_{\text{logicd min}} - T_{\text{hd}} = 0$$

$$\text{Forwareded Clk Delay min} = T_{\text{sclk max}} + T_{\text{saclk}}$$
$$\text{Pin to Clock Delay min} = T_{\text{cclk2 max}} + T_{\text{cbdelay max}}$$
$$\text{Pin to Data Delay max} = T_{\text{cclk1 min}} + T_{\text{cqf min}} + T_{\text{logicf min}}$$
$$\text{Data to Pin Delay max} = T_{\text{dbdelay min}} + T_{\text{logicd min}} - T_{\text{hd}}$$

$$0 = T_p + \text{Pin to Data Delay min} + \text{Data to Pin Delay min} -$$
$$- \text{Forwareded Clk Delay max} - \text{Pin to Clock Delay max}$$

$$\text{Forwareded Clk Delay max} - \text{Data to Pin Delay min} =$$
$$= T_p + \text{Pin to Data Delay min} - \text{Pin to Clock Delay max}$$

$$\text{bre}_{\text{skew}} = \text{Forwareded Clk Delay max} - \text{Data to Pin Delay min}$$

$$\text{Output Delay min} = T_p + \text{Pin to Data Delay min} - \text{Pin to Clock Delay max}$$

$$\text{Output Delay min} = \text{bre}_{\text{skew}}$$

- `create_clock -name CLK -period Tp [get_ports CLK_PIN]`
- `create_generated_clock -name FWCLK -multiply_by 1 -source \ [get_pins CLK_PIN] [get_ports CLK_OUT_PIN]`
- `set_input_delay -clock FWCLK -max (Tp - are_skew) [get_ports DATA_PIN]`
- `set_input_delay -clock FWCLK -min bre_skew [get_ports DATA_PIN]`

Constraints 2.

```
#  Rising Edge Source Synchronous Outputs
#
#  Source synchronous output interfaces can be constrained either by the max data skew
#  relative to the generated clock or by the destination device setup/hold requirements.
#
#  Setup/Hold Case:
#  Setup and hold requirements for the destination device and board trace delays are known.
#
# forwarded         ____                        ____________________
# clock                 |_____________________|                    |_____________
#                                               |
#                                      tsu      |    thd
#                                   <---------->|<---------->
#                                    ___________|____________
# data @ destination    XXXXXXXXX___________________________XXXXX
#
# Example of creating generated clock at clock output port
# Example of creating generated clock at clock output port
# create_generated_clock -name <gen_clock_name> -multiply_by 1 -source \
# [get_pins <source_pin>] [get_ports <output_clock_port>]
# gen_clock_name is the name of forwarded clock here. It should be used below for defining "fwclk".
```

$$T_{saclk} = 0$$

Необходимое условие: Slack ≥ 0. Пусть $T_{jit} = T_{un} = T_{cbdelay\ min} = 0$

Для Setup:

$$Slack = 0$$

$$T_{sclk\ min} + T_{saclk} + T_{cclk2\ min} + T_{cbdelay\ min} - T_{cclk1\ max} -$$
$$- T_{cqf\ max} - T_{logicf\ max} - T_{dbdelay\ max} - T_{logicd\ max} - T_{sud} = 0$$

$$\text{Forwareded Clk Dev Delay min} = T_{sclk\ min} + T_{saclk} + T_{cbdelay\ min}$$
$$\text{Data to Dev Pin Delay max} = T_{cclk1\ max} + T_{cqf\ max} + T_{logicf\ max} + T_{dbdelay\ max}$$

$$\text{Forwareded Clk Dev Delay min} - \text{Data to Dev Pin Delay max} +$$
$$+ T_{cclk2\ min} - T_{logicd\ max} - T_{sud} = 0$$

$$T_{sud} = T_p + \text{Forwareded Clk Dev Delay min} - \text{Data to Dev Pin Delay max}$$

$$T_{sud} - T_p + T_{cclk2\ min} - T_{logicd\ max} - T_{sud} = 0$$
$$T_{sud} + T_{dbdelay\ max} - T_{dbdelay\ max} - T_p + T_{cclk2\ min} - T_{logicd\ max} - T_{sud} = 0$$

$$\text{Output Delay max} = T_{dbdelay\ max} + T_{logicd\ max} + T_{sud} - T_{cclk2\ min} + T_p$$
$$T_{sud} + T_{dbdelay\ max} - \text{Output Delay max} = 0$$

$$\text{Output Delay max} = T_{sud} + T_{dbdelay\ max}$$

Для Hold:

$$\text{Slack} = 0$$

$$T_p + T_{cclk1\ min} - T_{sclk\ max} - T_{saclk} - T_{cclk2\ max} - T_{cbdelay\ max} +$$
$$+T_{cqf\ min} + T_{logicf\ min} + T_{dbdelay\ min} + T_{logicd\ min} - T_{hd} = 0$$

$$\text{Forwareded Clk Dev Delay max} = T_{sclk\ max} + T_{saclk} + T_{cbdelay\ max}$$
$$\text{Data to Dev Pin Delay min} = T_{cclk1\ min} + T_{cqf\ min} + T_{logicf\ min} + T_{dbdelay\ min}$$

$$T_p - \text{Forwareded Clk Dev Delay max} + \text{Data to Dev Pin Delay min} -$$
$$- T_{cclk2\ max} + T_{logicd\ min} - T_{hd} = 0$$

$$T_{hd} = \text{Data to Dev Pin Delay max} - \text{Forwareded Clk Dev Delay min}$$

$$T_p + T_{hd} - T_{cclk2\ max} + T_{logicd\ min} - T_{hd} = 0$$

$$T_p + T_{dbdelay\ min} - T_{cclk2\ max} + T_{logicd\ min} - T_{hd} - T_{dbdelay\ min} + T_{hd} = 0$$

$$\text{Output Delay min} = T_p + T_{dbdelay\ min} + T_{logicd\ min} - T_{hd} - T_{cclk2\ max}$$
$$\text{Output Delay min} - T_{dbdelay\ min} + T_{hd} = 0$$

$$\text{Output Delay min} = T_{dbdelay\ min} - T_{hd}$$

- `create_clock -name CLK -period Tp [get_ports CLK_PIN]`
- `create_generated_clock -name FWCLK -multiply_by 1 -source \ [get_pins CLK_PIN] [get_ports CLK_OUT_PIN]`
- `set_input_delay -clock FWCLK -max (Tdbmax + Tsu) [get_ports DATA_PIN]`
- `set_input_delay -clock FWCLK -min (Tdbmin + Thd) [get_ports DATA_PIN]`