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Fall Semester 2022-2023

MVLD504– Analog IC Design

M. Tech VLSI Design

School of Electronics Engineering

Vellore Institute of Technology

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Slot: L27 + L28

Differential Amplifier

1. **Aim:**

To design a differential amplifier with active load with the following specification (Input common mode range)

ICMR+ = 1.6 V (Input common mode range)

ICMR- = 0.7V

Gain>=20dB

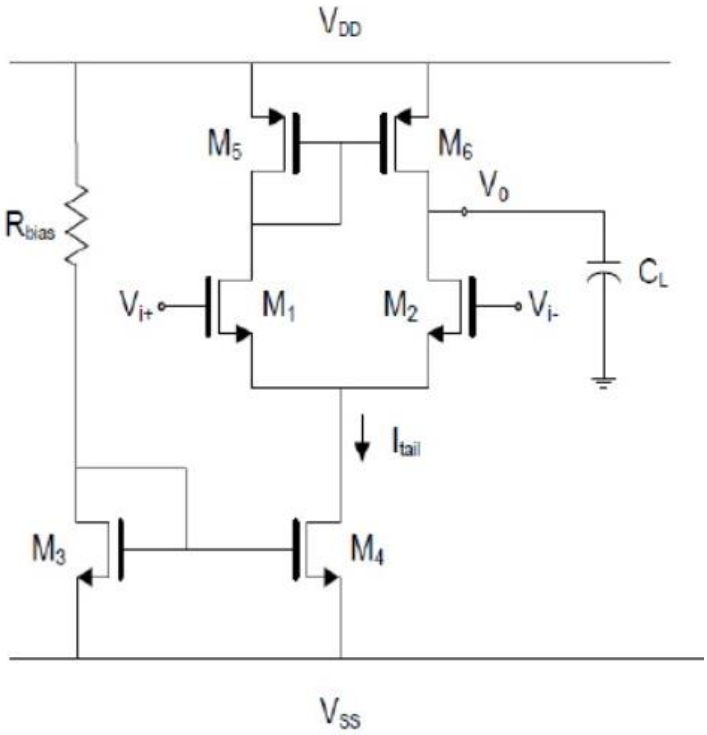
Slew rate –5V/µS

GBW>=5MHZ

Power<3mw

Cl=10pf

2. Design:



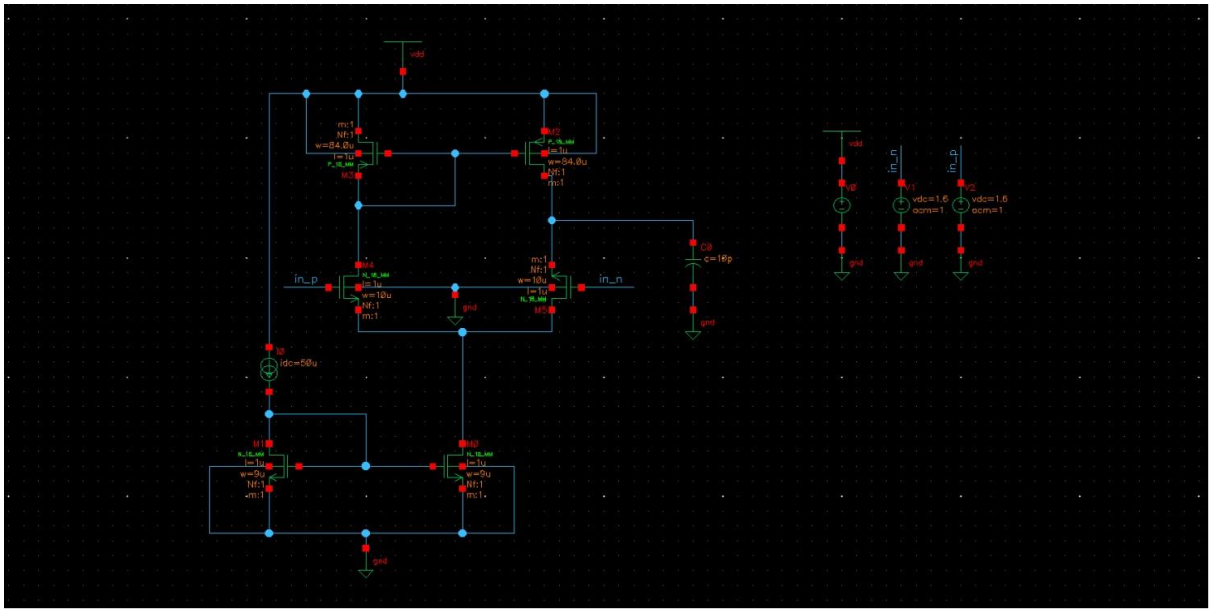


Fig. Differential Amplifier Schematic

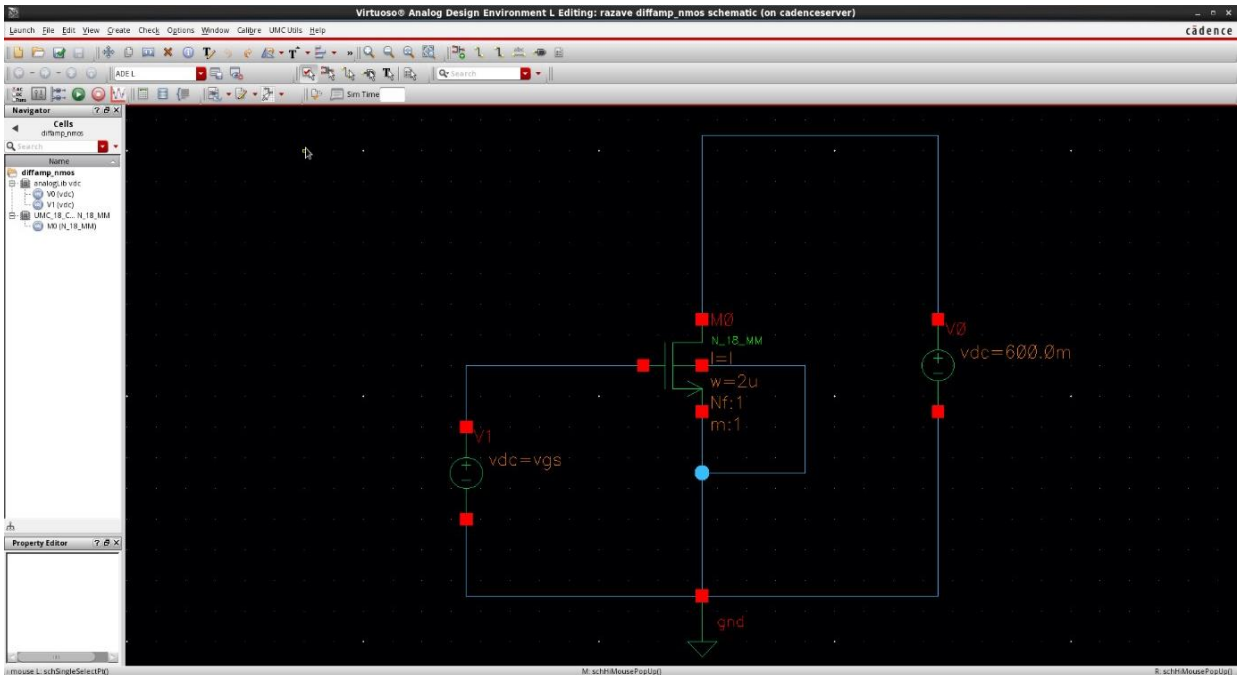


Fig. NMOS Characterization

3. <u>Procedure & Calculation:</u>

1) Determine current requirements:

Slewrate = I_{tail}/C_L

$I_{tail} = I_4 = \text{Slewrate} \cdot C_L = 5 \times 10 \times 10^{-12} / 10^{-6}$

$I_4 = 50\,\mu A$

$I_{1,2} = \frac{I_{tail}}{2} = \frac{I_4}{2} = 25\,\mu A$

(∵ M5-6 mirrors current in differential pair since I_1 should be equal I_2 As M5 is in series with M_1, ~~$I_1 = I_5$~~

$I_1 = I_5 = 25\,\mu A$

2) Design of input pair:

i) $GBW = \frac{g_m}{2\pi f C_L}$

From GBW & C_L, g_m of input pair is obtained

$GBW = \frac{g_{m1,2}}{2\pi f C_L}$

$\therefore 5 \times 10^{-6} = \frac{g_{m1,2}}{2\pi \times 10 \times 10^{-12}}$

$\therefore g_{m1,2} = 3.1415 \times 10^{-4} = 314.15 \times 10^{-6}$

ii) g_m/i_d calculations:-

$I_1 = I_2 = 25\,\mu A$

$\frac{g_m}{i_d} = 314.15\,\mu / 25\,\mu = 12.566$ ~~$\frac{g_m}{i_d} = 12.56$~~.

$\boxed{\frac{g_m}{i_d} = 12.56}$

iii) Channel length:

Channel length obtained from DC gain $A_V = \frac{g_{m1,2}}{g_{ds2} + g_{ds6}}$

Gain requirement = 20dB ⟶ 10

Gain (Av) = 10.

$A_V = \frac{g_{m1,2}}{g_{ds2} + g_{ds6}}$ ∴ $10 = \frac{314.15\mu}{g_{ds2} + g_{ds6}}$

$g_{ds2} + g_{ds6} = 31.4\mu$ assuming conductance is equally distributed among M2 & M6

$\therefore g_{ds2} = g_{ds6} = 314\mu/2 = 15.7\mu$

3) Intrinsic gain of input transistors:

Intrinsic gain $= \frac{g_m}{g_{ds}}$.

$314.15\mu / 15.7\mu = 20.009$

4) Channel length & Intrinsic gain requirement:

Choose L from gm/id vs gm/gds for various L values
Ex: L = 0.18μ from graph procedure.

5) Find Id/W vs gm/id graph:

Id/W = 14.5338 obtained.

6) Find width:

$W = \frac{Id}{Id/W} \longrightarrow 25\mu / 14.533$ ∴ W = 1.7202 μm

∴ For input pair, fix W = 1.72 μm.

7) Find Vgs.

From gm/Id vs Vgs graph
Find Vgs value for which gm/Id = 12.56
Vgs obtained is 539.703 mV

(8) Current through MOSFETs:

Considering lengths of MOSFET to be 180nm.

$V_{gs} = V_{g1} - V_{s1}$
$V_{s1min} = V_{dsat4}$
$V_{g1} = V_{gs1} + V_{s1}$
$V_{g1} >= V_{gs1} + V_{dsat4}$
We know that $V_{inmin} = 0.7V$ (given)
ICMR = −0.7V

V_{gs1} is obtained from gm over id vs vgs graph of i/p pair.
V_{gs} is obtained as 589.703mV

$V_{dsat} <= 0.7 - V_{gs1}$
$= 0.7 - 0.5897 = 0.1103V = 110.3mV$

9) Vdsat vs gm/id graph:

i) W calculation:

$W = id / (id/W) = 50u / 8.3138$
$W = 6.014\mu m$

ii) Calculat^n of Vgs from gm/id vs Vgs graph:

Vgs is obtained as 541.82mV

10) Design of current mirror load:

$V_{dd} / V_{gs\,5,6} = V_{d1,2}$
$V_{d1,2} > V_{g1} - V_{th1}$

$V_{d2} + V_{tu1} >= V_{inmax}$

$V_{du12} >= V_{inmax} - V_{tu1}$

$V_{du12} >= V_{in\,max} - (v_{gs1} - V_{dsat1})$

$V_{du12} = V_{gs16}$

$V_{gs16} >= V_{dd} - V_{du12}$

$V_{du12} >= 1.6 - (589.70m - 131.37m)$

$V_{du12} >= V_{dd} - V_{du12}$

$V_{gs16} >= 1.8 - 1.1416$

$V_{sgs16} >= 0.6584V$

$\boxed{V_{sg} = 0.6584V}$

ii) PMOS width:

Assuming $V_{sg} >= 0.6$

$Gm/id = 14.13$

$Id/W = -3.502167$

$W = 7.138 \times 10^{-6}$

Assuming $V_{sg} >= 0.58$

$Gm/id = 15.363$

$Id/W = -2.60652$

$W = 9.59133 * 10^{-6}$

Assuming $V_{sg} >= 0.56$

$Gm/id = 16.5645$

$Id/W = -1.8963$

$W = 1.316 * 10^{-6}$

∴ Pmos width is fixed as 9.59133μm

4. Results:

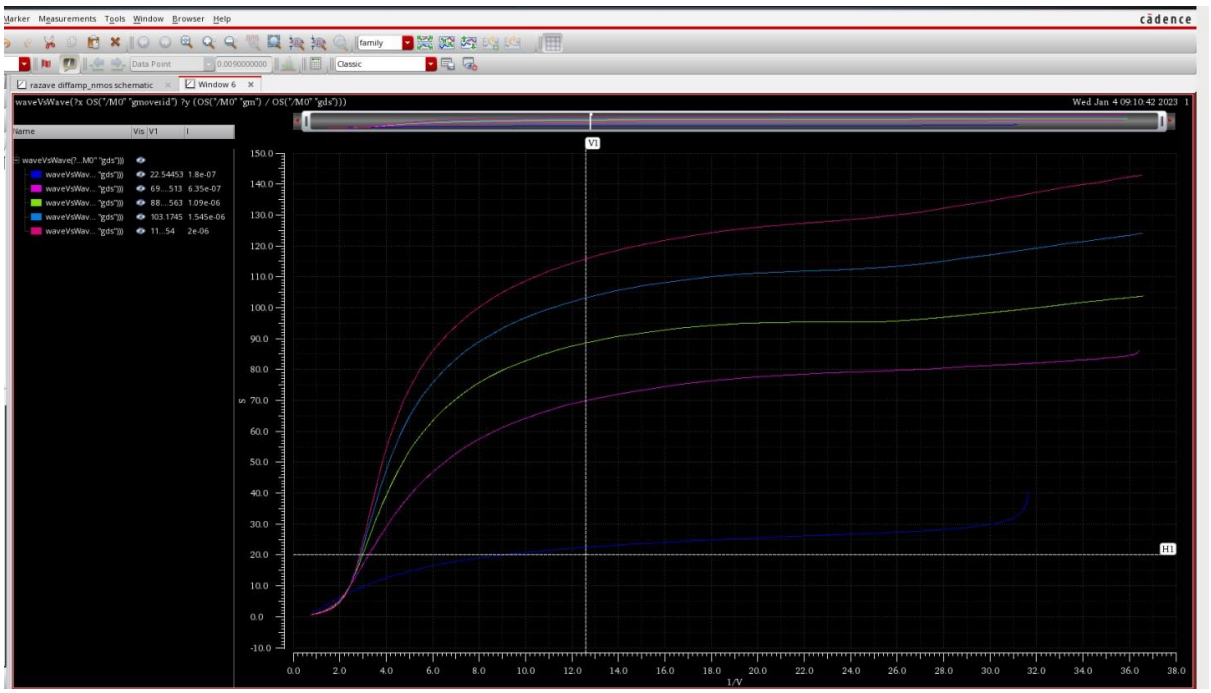


Fig. Gm/id vs id/w graph

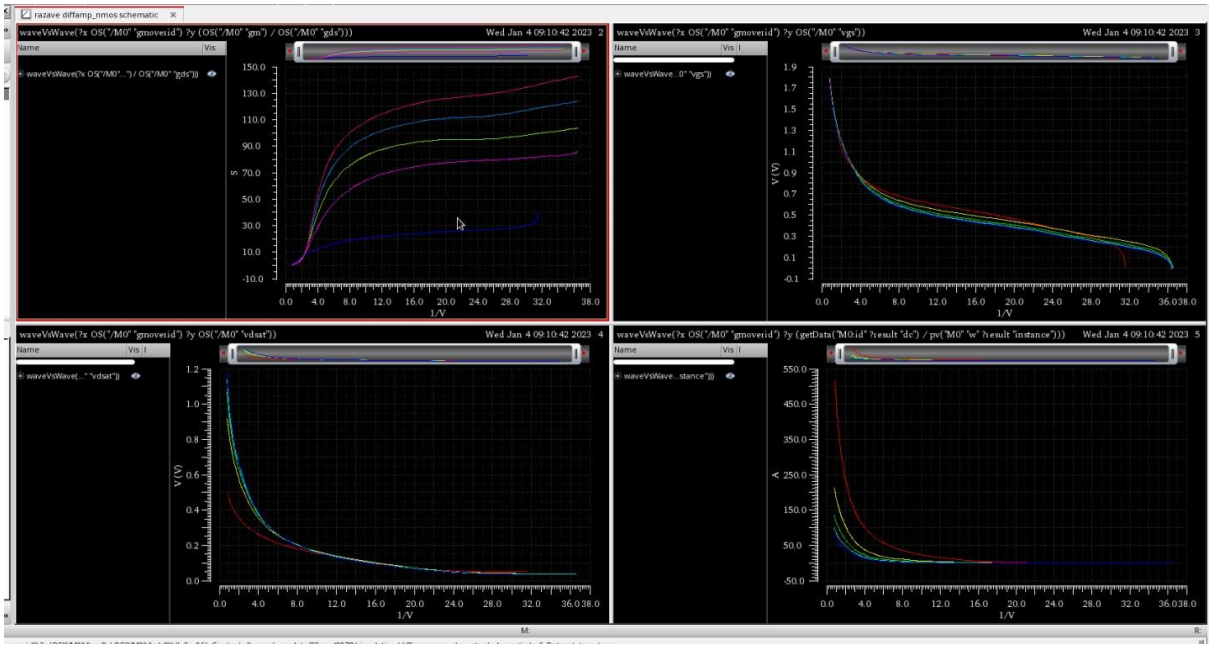


Fig.OS graphs for various L values .

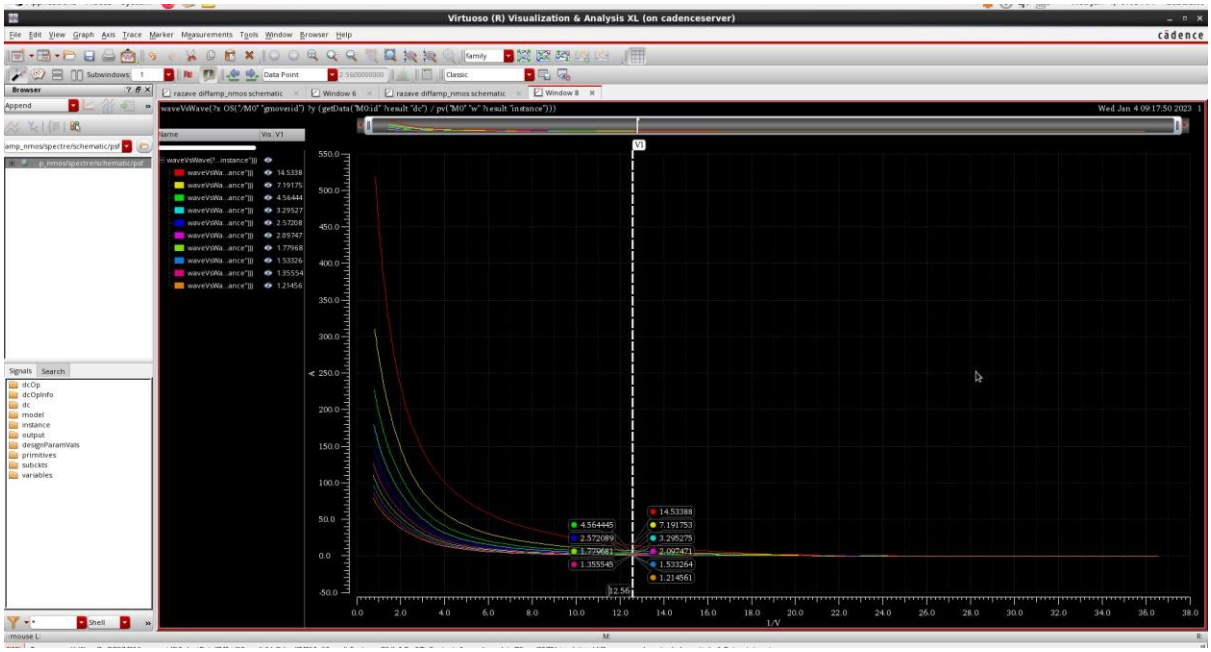


Fig. Id/w graph

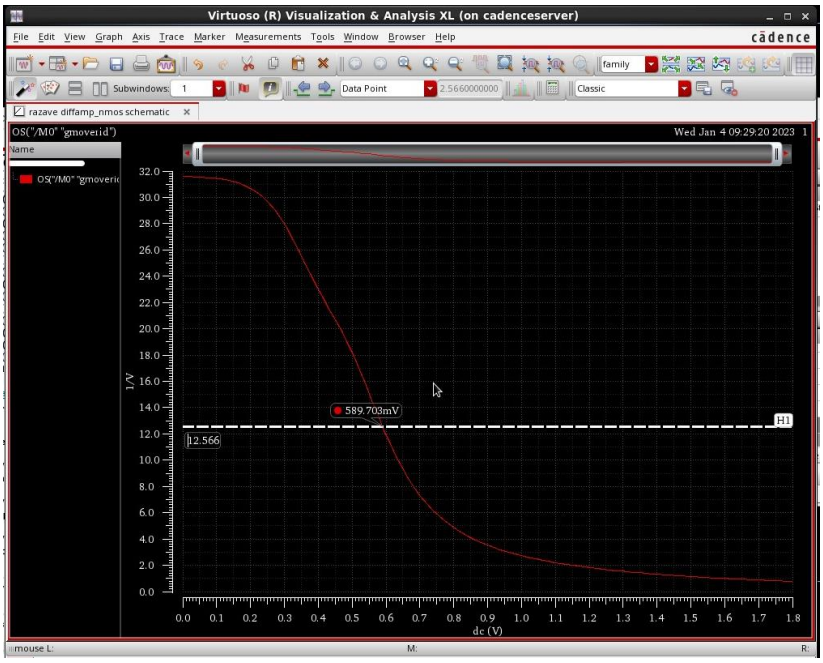


Fig. Vgs graph

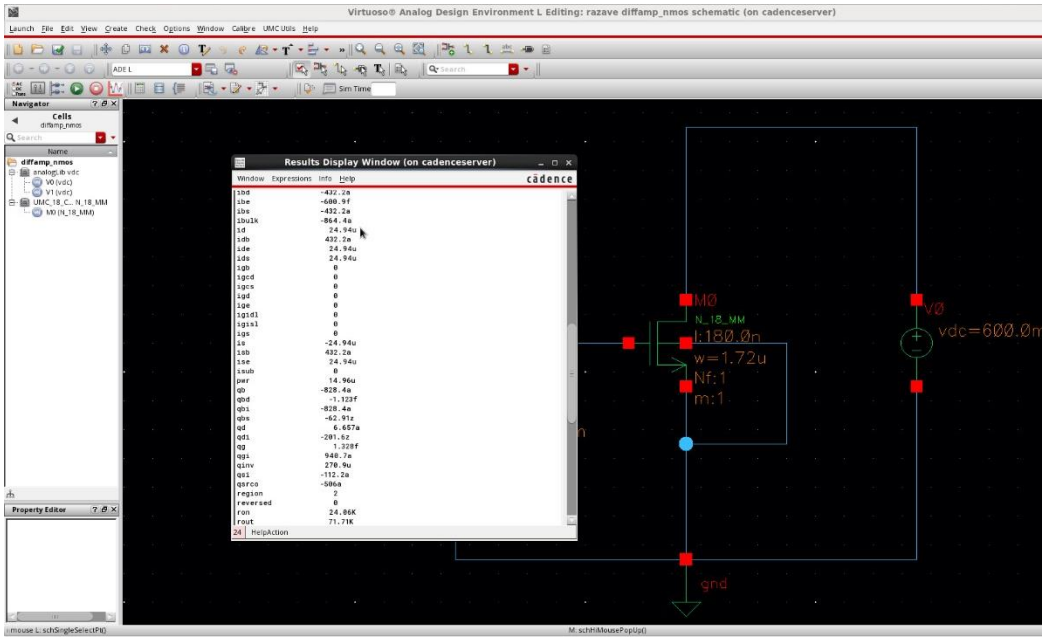
5. 

Fig. Id graph

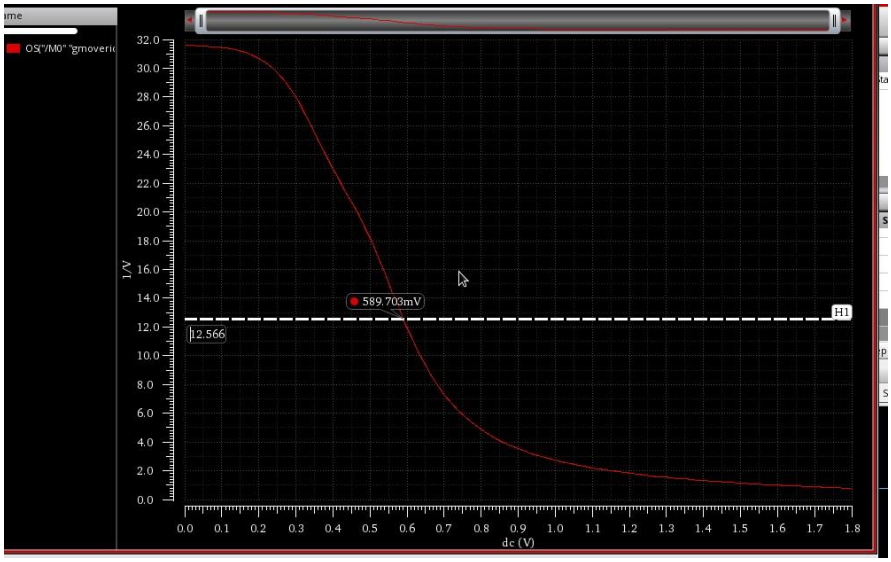


Fig. gmoverid vs vgs graph

Now plot Vdsat vs gm/id graph

1. Open result browser after adding the simulation file of the nmos.
2. Now from the parameters plot both Vdsat and gm/id graphs in the same window
3. Now change one of the axis and plot gm/id vs Vdsat
4. Draw a horizontal trace at vdsat value to obtain required gm/id value

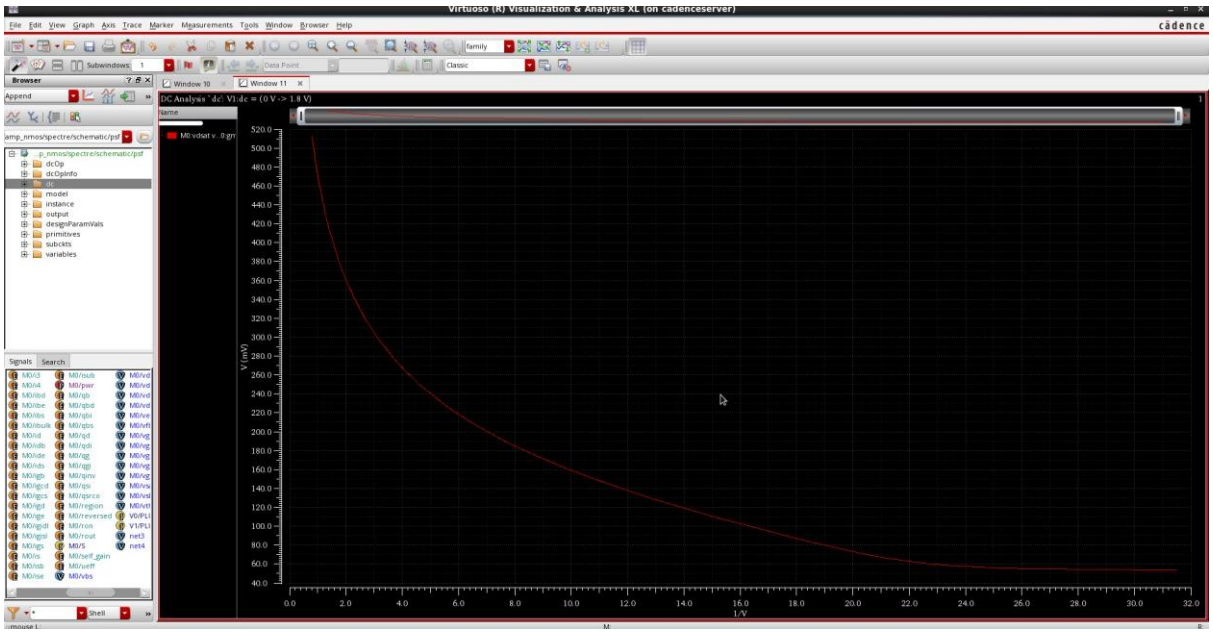


Fig. Vdsat graph

Plot gm/id vs Id/W graph

1. Open result browser after adding the simulation file of the nmos.
2. Now from the parameters plot both Id/w and gm/id graphs in the same window
3. Now change one of the axis and plot gm/id vs Vdsat
4. Draw a trace at gm/id value to obtain required id/w value
5. Here the value of Id/w is obtained by sending both id and w traces to calculator

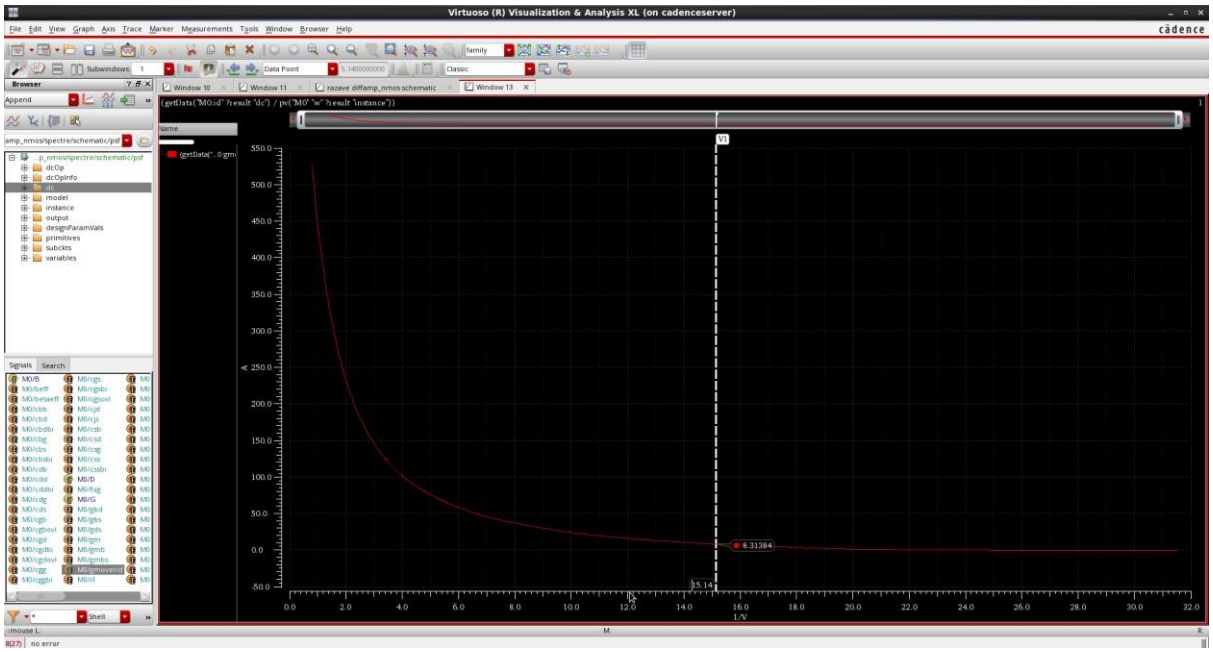


Fig. id/w graph

From the graph Id/w is obtained as 8.3138A

We know that current through tail source is 50u

Calculate the value of W

W=id/(idoverw) =50u/8.3138

W=6.014um

Calculate Vgs from gm/id vs Vgs graph

Vgs is obtained as 541.182mv

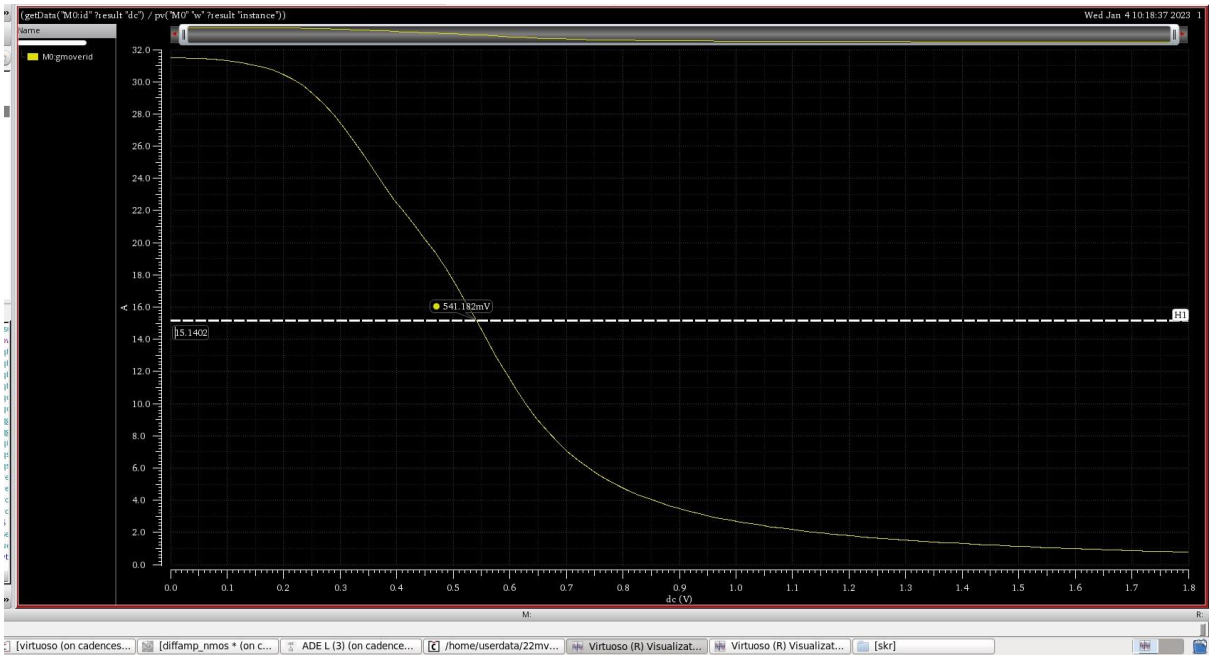


Fig. gmoverid vs Vgs

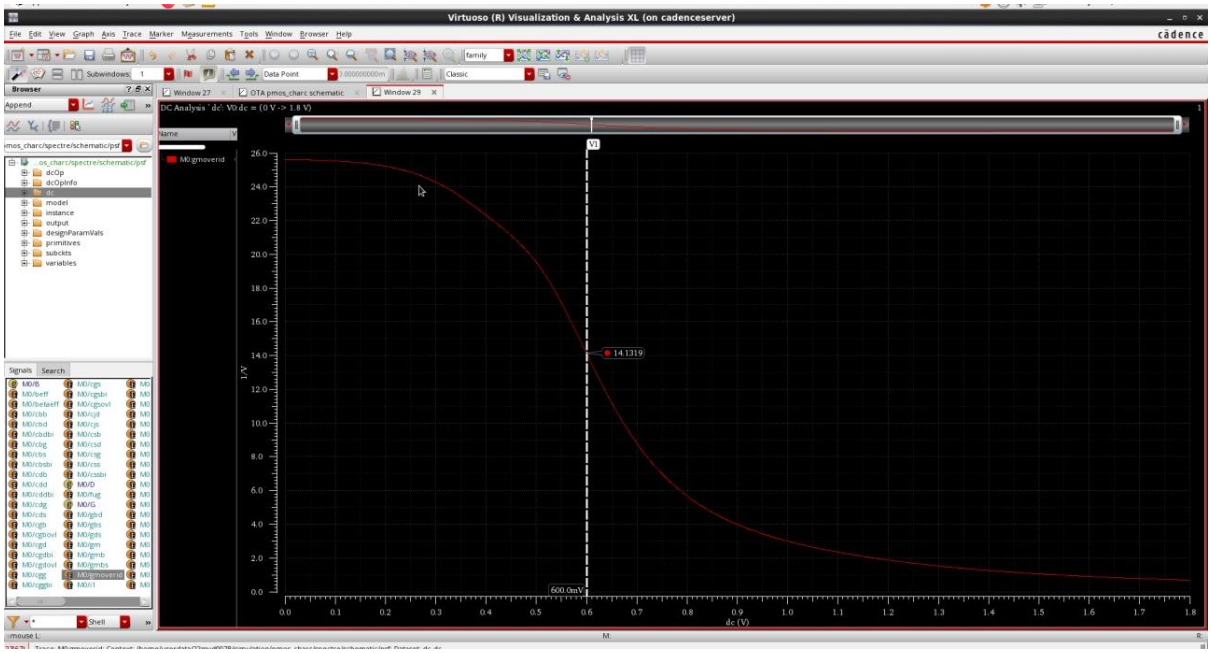


Fig. gmoverid for current mirror load

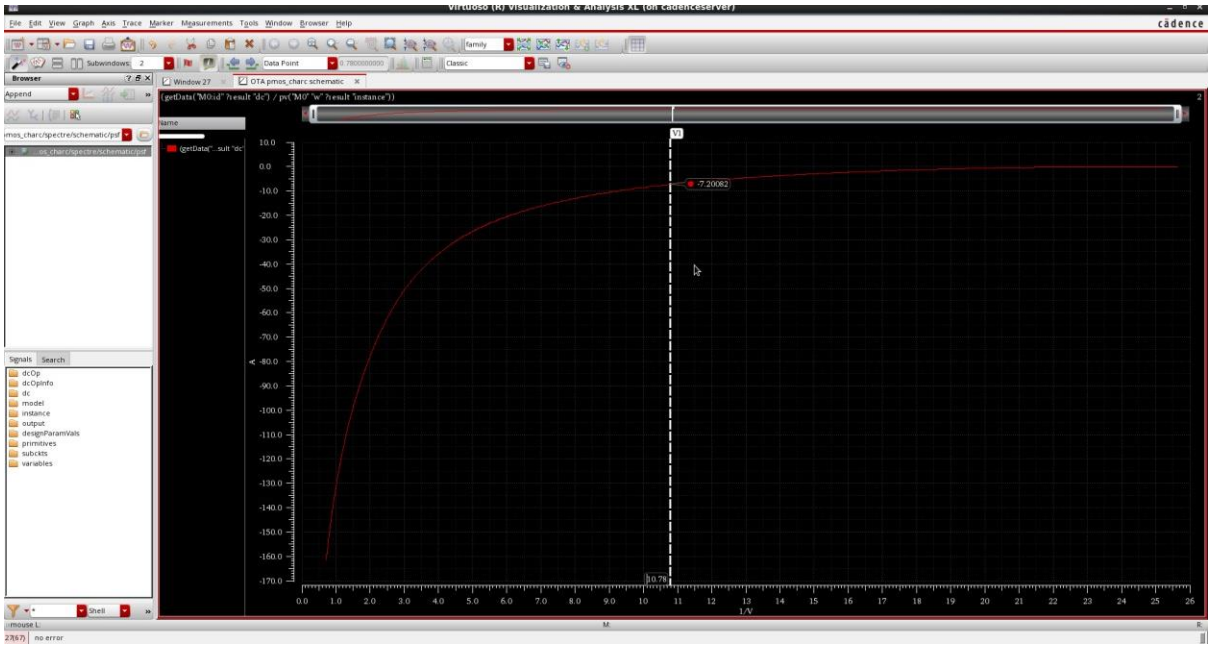


Fig. gmoverid vs id/w graph for current mirror load

From the graph for gm/id=10.7871 we obtained Id/W= -7.2008

Find the value of W

From the values of id and Id/w find the values of W

W is obtained as 3.4718 x 10^-6

Now Construct the total circuit with the widths obtained and apply ICMR+ and ICMR- to the circuit and check if all the mosfets are in saturation. If they are not in saturation reduce the Vgs value and find all the above parameters again and find the Width again.

Inference:

In this assignment the Differential Amplifier is implemented with Active Load with necessary calculations such that It offers the Gain of 40dB along with given specifications and performed its AC analysis.