

1. Which interrupt has the highest priority?
a) INTR b) TRAP c) RST6.5
2. In 8085 name the 16 bit registers?
a) Stack pointer b) Program counter c) a & b
3. Which of the following is hardware interrupts?
a) RST5.5, RST6.5, RST7.5 b) INTR, TRAP c) a & b
4. What is the RST for the TRAP?
a) RST5.5 b) RST4.5 c) RST4
5. What are level Triggering interrupts?
a) INTR&TRAP b) RST6.5&RST5.5 c) RST7.5&RST6.5
6. Which interrupt is not level sensitive in 8085?
a) RST6.5 is a raising edge-triggering interrupt.
b) RST7.5 is a raising edge-triggering interrupt.
c) a & b.
7. What are software interrupts?
a) RST 0 - 7 b) RST 5.5 - 7.5 c) INTR, TRAP
8. Which stack is used in 8085?
a) FIFO b) LIFO c) FILO
9. Why 8085 processor is called an 8 bit processor?
a) Because 8085 processor has 8 bit ALU.
b) Because 8085 processor has 8 bit data bus.
c) a & b.
10. What is SIM?
a) Select Interrupt Mask b) Sorting Interrupt Mask c) Set Interrupt Mask.
11. RIM is used to check whether, _____
a) The write operation is done or not
b) The interrupt is Masked or not
c) a & b
12. What is meant by Maskable interrupts?
a) An interrupt which can never be turned off.
b) An interrupt that can be turned off by the programmer.
c) none
13. In 8086, Example for Non maskable interrupts are
a) Trap b) RST6.5 c) INTR
14. What does microprocessor speed depends on?
a) Clock b) Data bus width c) Address bus width
15. Can ROM be used as stack?
a) Yes b) No c) sometimes yes, sometimes no
16. Which processor structure is pipelined?
a) all x80 processors b) all x85 processors c) all x86 processors
17. Address line for RST3 is?
a) 0020H b) 0028H c) 0018H
18. In 8086 the overflow flag is set when
a) The sum is more than 16 bits
b) Signed numbers go out of their range after an arithmetic operation
c) Carry and sign flags are set

- d) During subtraction
19. The advantage of memory mapped I/O over I/O mapped I/O is,
- a) Faster
 - b) Many instructions supporting memory mapped I/O
 - c) Require a bigger address decoder
 - d) All the above
20. $\overline{\text{BHE}}$ of 8086 microprocessor signal is used to interface the
- a) Even bank memory
 - b) Odd bank memory
 - c) I/O
 - d) DMA
21. In 8086 microprocessor the following has the highest priority among all type interrupts.
- a) NMI
 - b) DIV 0
 - c) TYPE 255
 - d) OVER FLOW
22. In 8086 microprocessor one of the following statements is not true.
- a) Coprocessor is interfaced in MAX mode
 - b) Coprocessor is interfaced in MIN mode
 - c) I/O can be interfaced in MAX / MIN mode
 - d) Supports pipelining
23. 8088 microprocessor differs with 8086 microprocessor in
- a) Data width on the output
 - b) Address capability
 - c) Support of coprocessor
 - d) Support of MAX / MIN mode
24. Address line for TRAP is?
- a) 0023H b) 0024H c) 0033H

Key:

1.1 C 1.2 C 1.3 C 1.4 B 1.5 B 1.6 B
1.7 A 1.8 B 1.9 A 1.10 C 1.11 B 1.12 B
1.13 A 1.14 C 1.15 B 1.16 C 1.17 C 1.18 B
1.19 D 1.20 B 1.21 A 1.22 B 1.23 A 1.24 B

1. The contents of different registers are given below. Form **Effective addresses** for different addressing modes are as follow :
Offset = 5000H
[AX]- 1000H, [BX]- 2000H, [SI]- 3000H, [DI]- 4000H, [BP]- 5000H,
[SP]- 6000H, [CS]- 0000H, [DS]- 1000H, [SS]- 2000H, [IP]- 7000H.
 - I. MOV AX, [5000H]
a) 5000H b) 15000H c) 10500H
 - II. MOV AX, [BX] [SI]
a) 13000H b) 15000H c) 12000H
 - III. MOV AX, 5000H [BX] [SI]
a) 20000H b) 1A000H c) 1A00H
2. The conditional branch instruction JNS performs the operations when if ____
a) ZF=0 b) SF=0 c) PF=0 d) CF=0
3. Vector address of TRAP
a) 24H b) 36H c) 24 d) 18H
4. SOD pin can drive a D flip-flop?
a) SOD cannot drive any flip-flops.
b) SOD cannot drive D flip-flop, but can drive any other flop-flops.
c) Yes, SOD can drive D flop-flop.
d) No, SOD cannot drive any other flop-flops except D flop-flop.
5. IDIV and DIV instructions perform the same operations for?
a) Unsigned number b) Signed number c) Signed number & Unsigned number d) none of above.
6. What is the output of the following code
AL=88 BCD, CL=49 BCD
ADD AL, CL
DAA
a) D7, CF=1 b) 37, CF=1 c) 73, CF=1 d) 7D, CF=1
7. What is the output of the following code
AL= 49 BCD, BH= 72 BCD
SUB AL, BH
DAS
a) AL=D7, CF=1. b) AL=7D, CF=1. c) AL=77, CF=1 d) none of them.
8. What is the output of the following code
AL= -28 decimal, BL=59 decimal
IMUL BL
AX=?, MSB=?
a) AX= F98CH, MSB=1. b) AX= 1652, MSB=1. c) BX F9C8H, MSB=1. d) BX= 1652, MSB=1.
9. What is the output of the following code
AL= 00110100 BL= 00111000
ADD AL, BL
AAA
a) AL = 6CH b) 12H c) 12 d) C6H
10. What is the output of the following code
AL=00110101 BL= 39H

SUB AL, BL

AAS

a) AL= 00000100, CF=1 b) BL=00000100, CF=0 c) AL=11111100 CF=1 d) BL=00000100, CF=1

11. What is the output of the following code

CF =0, BH = 179

RCL BH, 1

a) CF=0, OF= 1, BH= 01100101 b) CF=1, OF=1, BH=01100110

c) CF=1, OF =0, BH= 01001101 d) CF=0, OF=0, BH=00101100

12. What is the output of the following code

SI=10010011 10101101, CF=0

SHR SI, 1

a) 37805, CF=1, OF=1 b) 18902, CF=1, OF=1

c) 19820, CF=1, OF=1 c) 53708, CF=1, OF=1

13. What is the output of the following code

BX=23763CL=8

ROL BX, CL

a) 0101110011010011, CF=0

b) 1101001101011100, CF=0

c) 0110100010011101, CF=1

c) 1011100110001100, CF=1

14. What is the output of the following code

PUSH AL

a) Decrement SP by 2 & push a word to stack

b) Increment SP by 2 & push a word to stack

c) Decrement SP by 2 & push a AL to stack

d) Illegal

15. What is the output of the following code

AX = 37D7H, BH = 151 decimal

DIV BH

a) AL = 65H, AH= 94 decimal

b) AL= 5EH, AH= 101 decimal

c) AH= E5H, AL= 5EH

d) AL= 56H, AH= 5EH

16. In 8086 microprocessor one of the following instructions is executed before an arithmetic operation

a) AAM b) AAD c) DAS d) DAA

Key:

2.1 (I) B	(II) C	(III) B	2.2 B	2.3 A	2.4 C	2.5 B
2.6 B	2.7 C		2.8 A	2.9 C	2.10 A	2.11 B
2.12 B	2.13 B		2.14 D	2.15 B	2.16 B	

1. Access time is faster for
 - a) ROM b) SRAM c) DRAM
2. In 8279 Strobed input mode, the control line goes low. The data on return lines is strobed in the _____.
 - a) FIFO byte by byte b) FILO byte by byte c) LIFO byte by byte
 - d) LILO byte by byte.
3. ____ bit in ICW₁ indicates whether the 8259A is cascade mode or not?
 - a) LTIM=0 b) LTIM=1 c) SNGL=0 d) SNGL=1
4. In 8255, under the I/O mode of operation we have ____ modes. Under which mode will have the following features
 - i) A 5 bit control port is available.
 - ii) Three I/O lines are available at Port C.
 - a) 3, Mode2 b) 2, Mode 2 c) 4, Mode 3 d) 3, Mode 2
5. In ADC 0808 if _____ pin high enables output.
 - a) EOC b) I/P0-I/P7 c) SOC d) OE
6. In 8279, a scanned sensor matrix mode, if a sensor changes its state, the ____ line goes _____ to interrupt the CPU.
 - a) CS, high b) A₀, high c) IRQ, high d) STB, high
7. In 8279 Status Word, data is read when _____ pins are low, and write to the display RAM with _____ are low.
 - a) A₀, CS, RD & A₀, WR, CS. b) CS, WR, A₀ & A₀, CS, RD
 - c) A₀, RD & WR, CS d) CS, RD & A₀, CS.
8. In 8279, the keyboard entries are debounced and stored in an _____, that is further accessed by the CPU to read the key codes.
 - a) 8-bit FIFO b) 8-byte FIFO c) 16 byte FIFO d) 16 bit FIFO
9. The 8279 normally provides a maximum of _____ seven segment display interface with CPU.
 - a) 8 b) 16 c) 32 d) 18
10. For the most Static RAM the write pulse width should be at least
 - a) 10ns b) 60ns c) 300ns d) 1μs
11. BURST refresh in DRAM is also called as
 - a) Concentrated refresh b) distributed refresh c) Hidden refresh d) none
12. For the most Static RAM the maximum access time is about
 - a) 1ns b) 10ns c) 100ns d) 1μs
13. Which of the following statements on DRAM are correct?
 - i) Page mode read operation is faster than RAS read.
 - ii) RAS input remains active during column address strobe.
 - iii) The row and column addresses are strobed into the internal buffers using RAS and CAS inputs respectively.
 - a) i & iii b) i & ii c) all d) iii
14. 8086 microprocessor is interfaced to 8253 a programmable interval timer. The maximum number by which the clock frequency on one of the timers is divided by
 - a) 2¹⁶ b) 2⁸ c) 2¹⁰ d) 2²⁰

15. 8086 is interfaced to two 8259s (Programmable interrupt controllers). If 8259s are in master slave configuration the number of interrupts available to the 8086 microprocessor is
a) 8 b) 16 c) 15 d) 64

Key:

3.1 B	3.2 A	3.3 C	3.4 B	3.5 D	3.6 C
3.7 A	3.8 B	3.9 B	3.10 B	3.11 A	
3.12 C	3.13 C	3.14 A	3.15 D		

1. The coprocessors operate in _____ with a processor on the same buses and with the same instruction _____.
a) Parallel, byte stream. b) Series, byte stream.
c) Series, bite stream d) Parallel, bite stream.
2. Why 8087 is referred to as Coprocessor?
i) Because 8087 is used in parallel with main processor in a system, rather than serving as a main processor itself.
ii) Because 8087 is used in serial with main processor in a system, rather than serving as a main processor itself.
iii) Because main Microprocessor handles the general program execution and the 8087 handles specialized math computations.
a) i & iii b) ii & iii c) iii only. d) i only.
3. 8087 connection to 8086, to enable the _____ bank of memory _____ pins are to be connected.
a) Lower, BHE b) Upper, BHE c) Lower, INT
d) Upper, INT.
4. _____ Connection and the _____ instruction will solve the problem of synchronization between processor and coprocessor.
a) INT & NMI, WAIT b) RQ/GT₀ & RQ/GT₁, FWAIT
c) BUSY & TEST, FWAIT d) S₀ & QS₀, WAIT
5. _____ input is available, so that another coprocessor can be connected and function in _____ with the 8087. .
a) RQ/GT₀, parallel b) RQ/GT₁, parallel c) QS₁ & QS₀, parallel
d) S₀ & S₁, parallel.
6. In 8087, _____ many register stack are there? And of _____ registers. These registers are used as _____ stack.
a) 7, 40 bit, FIFO. b) 8, 60 bit, LILO. c) 8, 80 bit, LIFO d) 7, 80 bit, FILO.
7. If _____ and _____ connections are made so that an error condition in 8087 can interrupt to the processor.
a) BHE, RQ/GT₁ b) BUSY, TEST c) INT, NMI d) RQ/GT₀, RQ/GT₁
8. In 8087, which instruction is used for division real reversed _____.
a) FDIV b) FIDIVR c) FDIVR d) FDIVRP
9. Which of the following is of compare instruction in 8087?
a) FTST b) FPREM c) FPATAN d) FLDI
10. In 8087 coprocessor one of the following instructions is not valid
a. FSIN
b. FPTAN
c. FIDIV
d. FSQRT
11. One of the following signals belongs to the 8087 coprocessor is
a. HOLD
b. BUSY
c. TEST
d. NMI

Key:

4.1 A 4.2 A 4.3 B 4.4 A 4.5 B 4.6 C
4.7 C 4.8 C 4.9 A 4.10 A 4.11 C

1. The 8051 microcontroller is of ____ pin package as a _____ processor.
a) 30, 1 byte b) 20, 1 byte c) 40, 8 bit d) 40, 8 byte
2. The SP is of ____ wide register. And this may be defined anywhere in the _____.
a) 8 byte, on-chip 128 byte RAM. b) 8 bit, on chip 256 byte RAM.
c) 16 bit, on-chip 128 byte ROM d) 8 bit, on chip 128 byte RAM.
3. After reset, SP register is initialized to address _____.
a) 8H b) 9H c) 7H d) 6H
4. What is the address range of SFR Register bank?
a) 00H-77H b) 40H-80H c) 80H-7FH d) 80H-FFH
5. Which pin of port 3 is has an alternative function as write control signal for external data memory?
a) P3.8 b) P3.3 c) P3.6 d) P3.1
6. What is the Address (SFR) for TCON, SCON, SBUF, PCON and PSW respectively?
a) 88H, 98H, 99H, 87H, 0D0H. b) 98H, 99H, 87H, 88H, 0D0H
c) 0D0H, 87H, 88H, 99H, 98H d) 87H, 88H, 0D0H, 98H, 99H
7. Match the following:
1) TCON i) contains status information
2) SBUF ii) timer / counter control register.
3) TMOD iii) idle bit, power down bit
4) PSW iv) serial data buffer for Tx and Rx.
5) PCON v) timer/ counter modes of operation.
a) 1->ii, 2->iv, 3->v, 4->i, 5->iii. b) 1->i, 2->v, 3->iv, 4->iii, 5->ii.
c) 1->v, 2->iii, 3->ii, 4->iv, 5->i. d) 1->iii, 2->ii, 3->i, 4->v, 5->iv.
8. Which of the following is of bit operations?
i) SP
ii) P2
iii) TMOD
iv) SBUF
v) IP
a) ii, v only b) ii, iv, v only c) i, v only d) iii, ii only
9. Serial port interrupt is generated, if ____ bits are set
a) IE b) RI, IE c) IP, TI d) RI, TI
10. In 8051 which interrupt has highest priority?
a) IE1 b) TF0 c) IE0 d) TF1
11. Intel 8096 is of ____ bit microcontroller family called as _____.
a) 8, MCS51 b) 16, MCS51 c) 8, MCS96 d) 16, MCS96
12. 8096 has following features fill up the following,
i) ____ Register file,
ii) ____ I/O Ports
iii) ____ architecture.
a) 256 byte, five 8bit, register to register
b) 256 byte, four 8bit, register to register
c) 232 byte, five 8bit, register to register
d) 232 byte, six 8 bit, register to register
13. How many synchronous and asynchronous modes are there in serial port of 8096?

- a) 2, 2 respectively b) 3,1 respectively c) 1, 3 respectively d) 1, 2 respectively
14. In 8096 we have _____ interrupt sources and _____ interrupt vectors.
a) 18, 8 b) 21, 6 c) 21, 8 d) 16, 8
15. 8096 has ____ general purpose I/O ports, Port 2 includes _____ of the following
i) two quasi-bidirectional I/O lines
ii) two output lines
iii) four input lines
iv) open drain outputs
a) 4, i, iv b) 6, ii, iii c) 4, i,ii,iii d) 6, i, ii, iv
16. 8096 write-protected mode, no code can write to memory address between ____.
a) 2020 to 3FFFH b) 8000 to FFFFH c) 2000 to 3FFFH d) 2020 to 202FH
17. If the __ pin is __ , then we have the option of using the ____ ROM or EPROM together with ____ memory and devices.
a) EA, high, internal, external
b) EA, low, internal, external
c) EA, high, external, internal
d) EA, low, external, internal
18. In 8096, CCB bit 3 is ____.
a) write strobe mode select b) address valid strobe select
c) bus width select d) Internal read control mode
19. In 8096, mode ____ of serial port are ____ modes commonly used for ____ communications.
a) 1, 8bit, single processor b) 0, 7bit, multiple microcontroller
c) 2, 9 bit, multiple processors d) 3, 8 bit, multiple microcontroller
20. What is the function of watchdog timer?
a) The watchdog Timer is an external timer that resets the system if the software fails to operate properly.
b) The watchdog Timer is an internal timer that sets the system if the software fails to operate properly.
c) The watchdog Timer is an internal timer that resets the system if the software fails to operate properly.
d) None of them

Key:

5.1 C 5.2 D 5.3 C 5.4 D 5.5 C 5.6 A
5.7 A 5.8 A 5.9 D 5.10 C 5.11 D 5.12 C
5.13 C 5.14 C 5.15 C 5.16 C 5.17 A 5.18 B
5.19 C 5.20 C

1. Which of the following instruction perform as of indirect RAM to accumulator?
a) MOV A, R_n b) MOV @R_i, A c) MOV A, @R_i d) MOV R_n, A
2. ACALL instruction allows specifying _____ address in the instruction and calling subroutine within _____ program memory block.
a) 2byte, 3K b) 11bit, 2K c) 9bit, 2K d) 1byte, 3K
3. Which of the following instruction perform the move accumulator to external RAM of 16bit address?
a) MOV @ DPTR, A b) MOVX @ Ri, A
c) MOV A, @ Ri d) MOVX @ DPTR, A
4. Which of the following instruction perform jump indirect relative to DPTR
a) JMP A+DPTR b) JMP DPTR
c) JMP @A+DPTR d) SJMP A+DPTR
5. Which of the following instruction is wrong
a) INC DPTR b) MOV @DPTR, A
c) MOV A, @A+DPTR d) DEC DPTR
6. Which of the following instruction is of logical instructions?
i) CPL A
ii) JC rel
iii) DA A
iv) ANL A, R_n
v) RR A
vi) CPL bit
a) i, v b) v, iii, I c) iv, ii d) v, iii, ii
7. What instruction performs Compare immediate to indirect and jump if not equal.
a) CJNE A, #data, rel b) CJNE R_n, #data, rel
c) CJNE @ Ri, #data, rel d) CJNE A, data, rel
8. What is the Result of **RR A** instruction if accumulator contains 1000 0000.
a) 0000 0001 b) 0000 0000 c) 0100 0000 d) 0000 0010
9. MOV 45, #4FH
MOV R0, 45H
INC R0
MOV @R0, #30H
What is the location value of R0 and the content at that place?
a) 45H, 4F b) 50H, 30H c) 30H, 50H d) 50H, 45H
10. Which of the following is of type memory initialized Directive?
i) DS ii) SET iii) DW iv) DBIT
a) i, iii b) ii c) iii d) iv, ii
11. Which of the following is not a program linking directive
i) EXTRN ii) SEGMENT iii) NAME iv) PUBLIC v) USING
a) iv, v b) ii, iiic) i, iii d) ii, v
12. SP of 8051 is of ____ wide and it is loaded with the default value of ____ after reset.
a) 2 byte, 08H b) 8 bit, 07H c) 1 byte, 09H d) 8 bit, 06H
13. Which of the following instruction is used to set bit port directly?
a) SET P1.0 b) MOV P1.0, bit c) SETB P1.0 d) JB P1.0, bit
14. MOV A, #56H
MOV R1, #50H

MOV 50H, # 45H

XCHD A, @R1

What is the result at A, R1?

- a) 56H, 45H b) 45H, 50H c) 50H, 56H d) 45H, 56H

Key:

6.1 C 6.2 B 6.3 D 6.4 C 6.5 B 6.6 A
6.7 C 6.8 C 6.9 B 6.10 C 6.11 D 6.12 B
6.13 C 6.14 D

1. In 8051 an external interrupt 1 vector address is of _____ and causes of interrupt if _____.
 - a) 000BH, a high to low transition on pin INT1
 - b) 001BH, a low to high transition on pin INT1
 - c) 0013H, a high to low transition on pin INT1
 - d) 0023H, a low to high transition on pin INT1
2. Serial port vector address is of _____. And causes an interrupt when _____.
 - a) 0013H, either TI or RI flag is set
 - b) 0023H, either TI or RI flag is reset
 - c) 0013H, either TI or RI flag is reset
 - d) 0023H, either TI or RI flag is set
3. In serial communication modes, mode 1 the Baud rate =
 - a) $BR = 2^{SMOD} / 32 * (\text{Timer 0 over flow rate})$
 - b) $BR = 2^{SMOD} / 16 * (\text{Timer 1 over flow rate})$
 - c) $BR = 2^{SMOD} / 16 * (\text{Timer 0 over flow rate})$
 - d) $BR = 2^{SMOD} / 32 * (\text{Timer 1 over flow rate})$
4. In modes 2 and 3, if _____ bit of SCON bit is set will causes enable multiprocessor communication and is of _____ bit address.
 - a) SM1, 9EH b) TB8, 9CH c) SM2, 9DH d) SM0, 9FH
5. Interfacing LCD with 89C51 _____ data lines are used along with the _____ signals.
 - a) 6, RS, RW b) 5, RW, EN c) 8, RS, EN, RW d) 9, RS, EN, RW
6. Resolution of ADC is defined as
 - a) $1 / (2^N - 1)$ b) $2^N - 1$ c) $1 / (2^N - 1)$ d) $2^N - 1$
7. In microcontroller and LCD interface which line will instruct the LCD that microcontroller is sending data?
 - a) DB0 b) RW c) EN d) RS
8. Which bit of TMOD will exactly configure timer / counter as a timer or counter.
 - i) TMOD.6 of C/T for timer 1 ii) TMOD.6 of C/T for timer 0
 - iii) TMOD.2 of C/T for timer 0 iv) TMOD.2 of C/T for timer 1
 - a) i, ii b) ii, iv c) i, iii d) iii, iv

Key:

7.1 C 7.2 D 7.3 D 7.4 C 7.5 C 7.6 C 7.7 C 7.8 C

1. Segmentation unit allows segments of _____ size at maximum.
a) 4Gbytes b) 6Mbytes c) 4Mbytes d) 6Gbytes
2. If _____ input pin of 80386 if activated, allows address pipelining during 80386 bus cycles.
a) BS_{16} b) NA c) PEREQ d) ADS
3. Virtual Mode Flag bit can be set using _____ instruction or any task switch operation only in the _____ mode
a) IRET, Virtual b) POPF, Real c) IRET, protected d) POPF, protected
4. The interrupt vector table of 80386 has been allocated _____ space starting from _____ to _____.
a) 1Kbyte, 00000H, 003FFH b) 2Kbyte, 10000H, 004FFH
c) 3Kbyte, 01000H, 007FFH d) 4Kbyte, 01000H, 009FFH
5. The _____ bit decides whether it is a system descriptor or code/data segment descriptor
a) P b) S c) D d) G
6. A new signal group on the 80486 is the _____.
a) PARITY b) DP_0 - DP_3 c) PCHK d) all
7. _____ is used to control the cache with two new control bits not present in the 80386 microprocessor. What are the bits used to control the 8K byte cache?
a) CR_0 , CD, NW b) CR_0 , NW, PWT
c) Control Register Zero, PWT, PCD d) none
8. To prevent another master from taking over the bus during a critical operation, the 486 can assert its _____ signal.
a) LOCK# or PLOCK# b) HOLD or BOFF c) HLDA d) HOLD
9. 80386 support which type of descriptor table from the following?
a) TDS b) ADS c) GDS d) MDS
10. 80386 support overall _____ addressing modes to facilitate efficient execution of higher level language programs.
a) 9 b) 10 c) 11 d) 12

Key:

8.1 A 8.2 B 8.3 C 8.4 A 8.5 B 8.6 D
8.7 A 8.8 A 8.9 C 8.10 C