A Linear-Logarithmic CMOS Image Sensor With Adjustable Dynamic Range

Myunghan Bae, Byoung-Soo Choi, Sung-Hyun Jo, Hee-Ho Lee, Pyung Choi, and Jang-Kyoo Shin

***Abstract*— A new pixel structure is proposed for wide dynamic range CMOS image sensors. A pixel based on a three-transistor active pixel sensor has two linear responses and a logarithmic response using additional circuits. The photogate surrounding the n$^+$/p-sub photodiode exists for the second linear response. The logarithmic response is due to the biased MOS cascode. The proposed pixel was designed and fabricated using a 0.35-μm 2-poly 4-metal standard CMOS process. The dynamic range of the pixel is higher than 106 dB. A test chip with a pixel pitch of 10 × 10 μm^2 and a 160 × 120 pixel array is evaluated.**

***Index Terms*— CMOS image sensor, dynamic range, linear-logarithmic response, photogate.**

I. Introduction

RECENTLY, some of the CMOS image sensors (CISs) emphasize a wide dynamic range performance and a high sensitivity performance in low light conditions [1], [2]. If the slope of response of pixel is steep, the pixel may have high sensitivity and a narrow dynamic range. A pixel with wide dynamic range has a gentle slope of response. Accordingly, the dynamic range and the sensitivity have a tradeoff relationship. The auto gain control (AGC) circuit is used to compensate for the slope. There has been much research on the dynamic range expansion of an image sensor because the AGC can adjust the slope of the output.

Typical dynamic range extension methods include the methods of using the mid-pulse to remove a portion of the signal, multi-sampling for representing a single image by combining the data of different exposure times, and logarithmic pixels with nonlinear responses [3]–[13]. There is a midlevel pulse method that exhibits a linear–linear characteristic [3]. During the integration time, some of the signal is abandoned by the supplied pulse to the transfer gate. This can slightly extend the dynamic range by maintaining the sensitivity in low light conditions. One characteristic of the midlevel pulse method is that it can be implemented without structural changes to the pixel. The multiple sampling method synthesizes different accumulation time images into a single image with wide dynamic range [10]. It has improved upon the double sampling method, which combines images with long and short integration times. The multiple sampling method can have a wider dynamic range than that of double sampling because it synthesizes more images. This method, which contains no structural change of the pixel, requires additional circuits such as memory and a signal synthesis circuit. It is difficult to express the images of a movable object. Logarithmic pixels have a nonlinear characteristic [4]. Because the signal has a logarithmic response, the dynamic range of a logarithmic pixel can be significantly expanded. However, the output swing is several hundred millivolts with low sensitivity. Logarithmic pixels have poor image quality owing to a small output swing. In terms of dynamic range, this method is the most interesting technique.

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The authors are with the School of Electronics Engineering, College of IT Engineering, Kyungpook National University, Daegu 702-701, South Korea (e-mail: mhbae@ee.knu.ac.kr; bschoi@ee.knu.ac.kr; shjo@ee.knu.ac.kr; heeholee@ee.knu.ac.kr; p0choi@ee.knu.ac.kr; jkshin@ee.knu.ac.kr).

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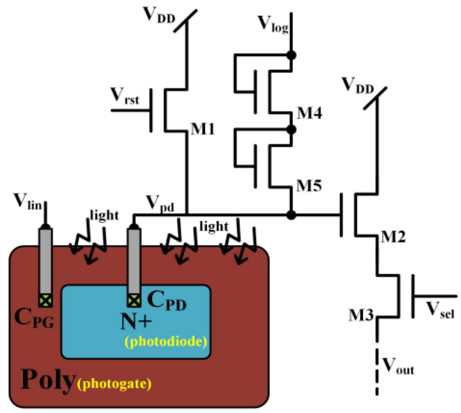


Fig. 1. Schematic of the proposed lin–log pixel with a cross-sectional view of the photodiode.

In this paper, we present a new wide dynamic range technique for a pixel while maintaining a high sensitivity at low light conditions. At extreme light conditions, the pixel can better enlarge the dynamic range by a logarithmic response. The pixel, based on the three–transistor (3–Tr) active pixel sensor (APS), consists of a photogate for a change of linear sensitivity and a MOS cascode for a logarithmic response. The dynamic range can be flexibly adjusted by using the two applied voltages. The proposed pixel was designed using a 0.35–μm standard CMOS process, and its characteristics were evaluated.

II. Proposed Pixel

A. Pixel Structure

Figure 1 shows the schematic of the proposed linear–logarithmic (lin–log) pixel with a cross-sectional view of photodetector. The lin–log pixel based on 3–Tr APS has additional circuits, a photogate and a MOS cascode. The photogate surrounds the N^+/P-sub photodiode. The MOS cascode, linked to its gate and drain, is connected to the sensing node of the pixel. Positive bias voltages can extend the dynamic range of the pixel, and are applied to the photogate and the MOS cascode. The bias voltage applied to the photogate (V_{lin}) controls the second linear response in the moderate illumination level, and the bias voltage applied to the MOS cascade (V_{log}) manages the logarithmic response in the high illumination level.

B. Operational Principle

The proposed lin–log pixel has three levels of sensitivity. There are two linear responses, the first linear response and the second response, and the logarithmic response by the MOS cascode. The first linear response achieves high sensitivity by using only the photodiode. The second response is less sensitive, because the capacitance of the photodiode and the photogate is united to increase the capacitance. The logarithmic response not only significantly extends the dynamic range but also is insensitive to light intensity.

The first linear mode is a response of a conventional 3–Tr APS with an N^+/P-sub photodiode. The operational principle of other responses of the proposed pixel is as follow, where $V_{t,photo}$ is the threshold voltage of the photogate MOSFET and $V_{t,m}$ is the threshold voltage of the cascade MOSFET (M_4 and M_5). When the level of photodiode (V_{PD}) is less than $V_{lin} - V_{t,photo}$ also true when $V_{PD} > V_{log} - 2V_{t,m}$, the channel of the photogate is constituted and the capacitance of photogate (C_{PG}) is linked to the capacitance of photodiode (C_{PD}) through this channel. Thus, the total capacitance of the sensing node approaches a value equal to $C_{PD} + C_{PG}$. For this reason, the lin–log pixel goes into second linear mode and the sensitivity decreases significantly. When the level of V_{PD} falls below $V_{log} - 2V_{t,m}$, the proposed lin–log pixel emerges from the logarithmic response according to whether the MOS cascode is switched on. The logarithmic response is analogous to that of a conventional logarithmic pixel. In addition, the level of V_{lin} must be greater than the level of V_{log} to perform the desired lin–log operation. Otherwise, the second linear response should dissipate when the level of V_{log} becomes equal to the level of V_{lin}. The concrete operational principle of the proposed lin–log pixel is indicated in Equations (1–3). Thus, the dynamic range of the pixel can simply be flexible by a tuning between the linear region and the logarithmic region through the appropriate setting of the bias voltages (V_{lin} and V_{log}).

$$\mathbf{V_{rst} \geq V_{PD} > V_{lin} - V_{t,photo} : V_{PD} = \frac{\Delta Q}{C_{PD}}} \tag{1}$$

$$\mathbf{V_{lin} - V_{t,photo} \geq V_{PD} > V_{log} - 2V_{t,m} : V_{PD} = \frac{\Delta Q}{C_{PD} + C_{PG}}} \tag{2}$$

$$\mathbf{V_{log} - 2V_{t,m} \geq V_{PD} : V_{PD} = V_{log} - 2\frac{kT}{q}\ln\left(\frac{i_{PD}}{i_o}\right)} \tag{3}$$

Figure 2 shows the conceptual diagram of the proposed lin–log pixel operation. Per the theoretical description, the operations are visually expressed for each region.

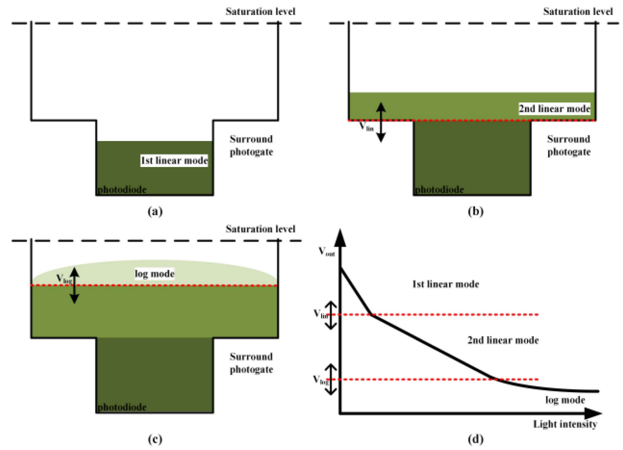


Fig. 2. Conceptual diagram of proposed lin–log pixel operation: (a) first linear mode, (b) second linear mode, (c) logarithmic mode, and (d) output characteristics.

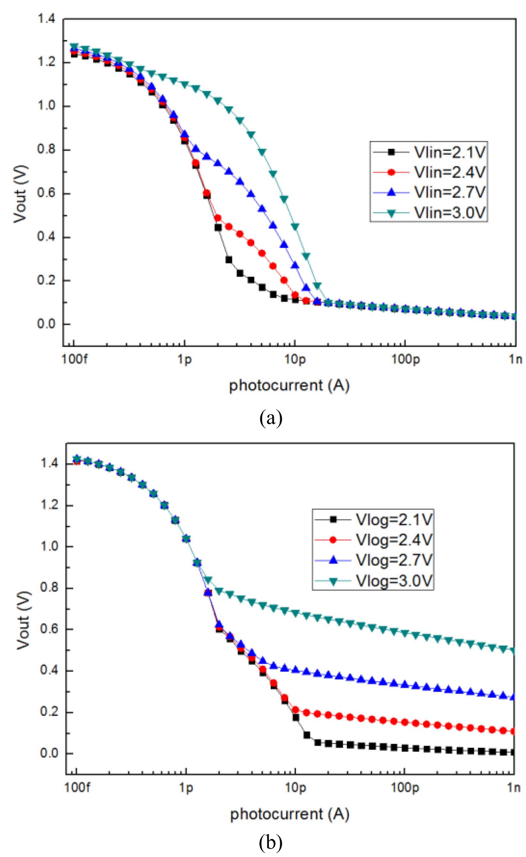
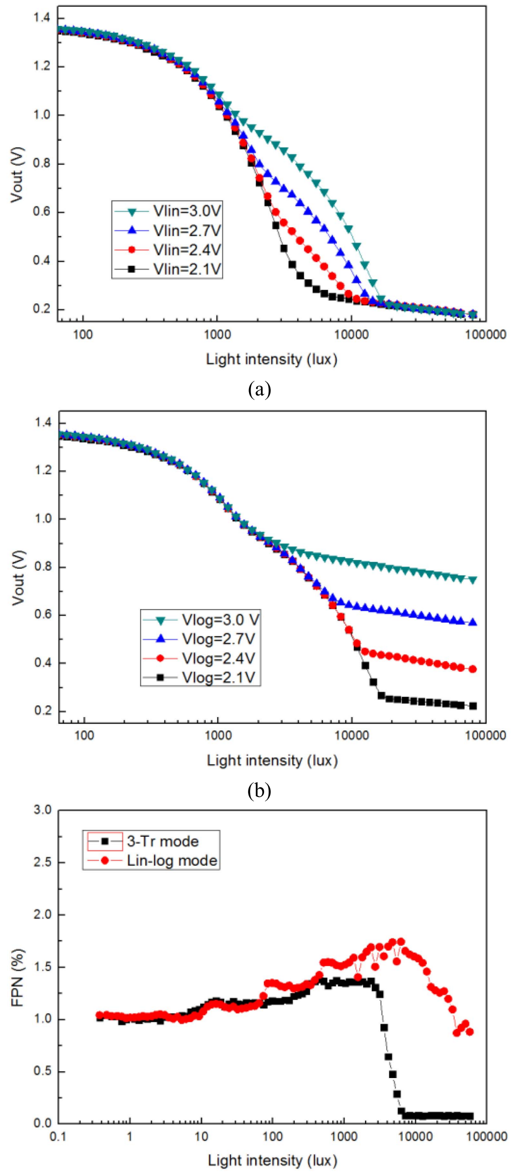


Fig. 3. Simulated photo response curves of the proposed lin–log pixel: (a) change of V_{lin} and (b) change of V_{log}.

Consequently, the proposed lin–log pixel has the conceptual output characteristics shown in Fig. 2(d).

III. Simulation and Experiments

The proposed pixel is simulated using Cadence Spectre with the parameters of the 0.35–μm standard CMOS process. Figure 3 shows the photo response curves simulated from the lin–log pixel according to the change in the bias voltages. The bias voltage applied to photogate is able to shift a starting



(c)

Fig. 4. Measured photo response curves of the proposed lin-log pixel (a) variation of V_{lin}, (b) variation of V_{log}, and (c) variation of FPN. (30 fps).

point of the second linear response, as shown in Fig. 3(a). The second linear response is less sensitive than the first linear response and occurs more quickly as the applied voltage increases. The logarithmic response is not influenced by the bias voltage applied to the photogate. The bias voltage applied to the MOS cascode is able to shift the starting point of the logarithmic response, as shown in Fig. 3(b). The level of V_{lin} must be greater than the level of V_{log}, or the second linear response may fade away. Consequently, the proposed lin–log pixel is intended to extend the dynamic range as adjusting the sensitivity and response. The simulation results are similar to the conceptual output characteristic shown in Fig. 2(d).

The proposed lin–log pixel is designed and fabricated using a 0.35–μm standard CMOS process. A test chip with a pixel pitch of 10 × 10 μm^2 consists of a 160 × 120 pixel array, a horizontal scanner, a vertical scanner, and a column multiplexer.

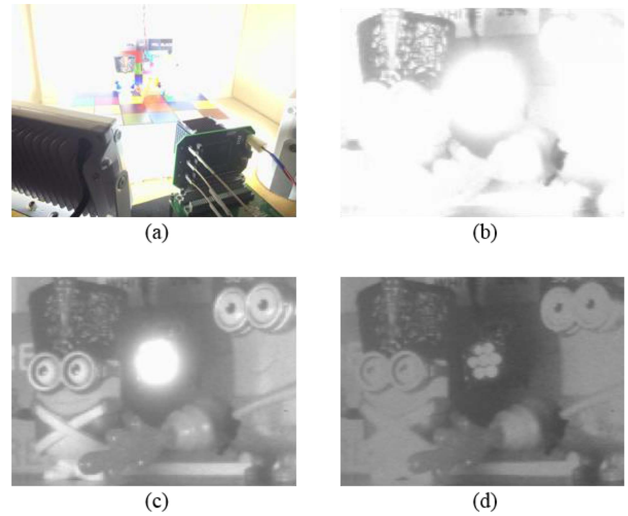


Fig. 5. Captured sample images (a) experimental environments, (b) at first linear mode (without V_{lin} and V_{log}), (c) at second linear mode (with only V_{lin}) and (d) at logarithmic mode (with V_{lin} and V_{log}).

TABLE I
PERFORMANCE OF THE PROPOSED LIN-LOG IMAGE SENSOR

Parameters	Performance
Technology	0,35-µm standard CMOS
Power supply	3.3 V
Pixel pitch	10 x 10 μm^2
Fill factor	28.4 %
Array size	160 x 120
Detector type	photodiode and photogate
Dynamic range	79 dB (without V_{lin} & V_{log})
	> 106 dB (with V_{lin} & V_{log})
Sensitivity	257 mV/lux·sec (first linear mode)
	51 mV/lux·sec (second linear mode)
	70 mV/dec (logarithmic mode)
FPN	0.953 % (dark)
Dark signal	146.3 mV/s @ 25ºC
SNR	42.7 dB (max)

Figure 4 shows the measured photo response curves of the proposed lin–log pixel. The results confirm that the lin–log pixel operates in light conditions according to the expectations and the simulations. The response curve expresses distinctive characteristics. At a low illumination level, the lin–log pixel in the first linear region has high sensitivity. The sensitivity is reduced by the photogate at a moderate illumination level. The second linear region is adjustable by the bias voltage. At a high illumination level, the MOS cascode is responsible for logarithmic operations. Thus, the proposed lin–log pixel exhibits two linear responses and one logarithmic response. Moreover, these results demonstrate that the dynamic range can be modified as expected. Although the light source can have a range of 0.37 lux to 79,568 lux, the pixel is able to react in higher illumination level. Thus, the dynamic range of the pixel is much greater than 106 dB. Fixed pattern noise (FPN) of the lin-log mode has similar trends with the 3-Tr mode at a low illumination level. However, at the high illumination level, the FPN of the lin-log mode was greater than that of the 3-Tr mode as shown in the Fig. 4(c).

The CIS system is composed of a test chip, a 10-bit analog to digital converter (ADC), and a field programmable

TABLE II
COMPARISON OF THE PROPOSED Lin-Log IMAGE SENSOR WITH PREVIOUSLY Lin-Log IMAGE SENSOR

	[6]	[9]	[12]	This work
Technology	0.5-µm (standard)	0.5-µm (CIS)	0. 35-µm (standard)	0.35-µm (standard)
Operating voltage	5 V	3.3 V (Analog) 1.8V (Digital)	3.3 V	3.3 V
Pixel pitch	20.7 x 20.7 µm^2	2.25 x 2.25 µm^2	13 x 13 µm^2	10 x 10 um^2
Fill factor	34 %	N/A	15.3 %	28.4 %
Array size	N/A	320 x 240	N/A	160 x 120
Pixel level transistors	6	2.5 (2-shared)	4	5
Dynamic range	94.8 dB	105 dB	97 dB	> 106 dB
Logarithmic sensitivity	48 mV/dec	90 LSB/dec	N/A	70 mV/dec

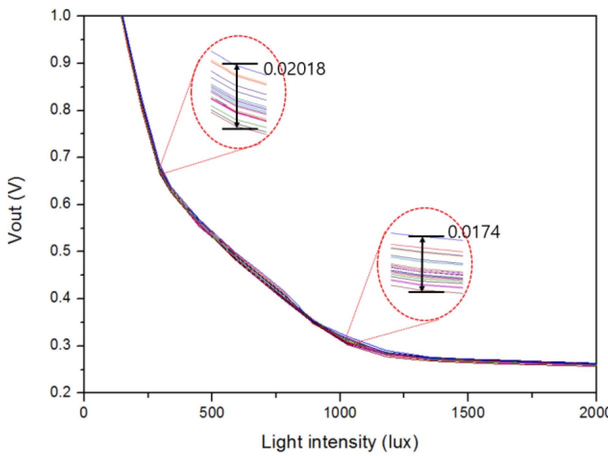


Fig. 6. Measured knee point variation of the proposed lin-log pixels. (1 fps).

gate array (FPGA). The FPGA plays a role as a microcontroller unit. It control the horizontal scanner, the vertical scanner, and the column multiplexer in the test chip. Figure 5 shows the captured sample images with the CIS system. The system adopts a lamp to provide brighter light as shown in Fig. 5(a). Figure 5(b) was captured during the first linear mode, which operated without V_{lin} and V_{log}. It is so saturated that it is difficult to distinguish the shapes of the subjects. The image in Fig. 5(c) reveals perceptible shapes of the subjects because the CIS is operated in the second linear response by the applied V_{lin}. When V_{lin} and V_{log} are applied, the CIS system can adapt to brighter light, unlike the linear modes. The image in the logarithmic mode reveals even the elements of LED as shown in Fig. 5(d). Accordingly, the dynamic range is significantly extended from the effect of the photogate and the MOS cascode. Furthermore, the dynamic range can be adjusted simply by tuning the level of the bias voltages, V_{lin} and V_{log}.

Figure 6 shows the measured knee point variation of proposed lin–log pixels. It was measured using the response of random 20 pixels in the array. The variation is mainly caused by the threshold voltage variation of MOSFET and the random reset noise in each pixel. The knee point variation in the linear response and knee point variation in the logarithmic response are 0.02 V and 0.017 V, respectively, when $V_{lin} = 3$ V and $V_{log} = 2.4$ V. It is greatly affected by the variation because the signal swing is small in the logarithmic response. Thus, we are studying to reduce the variation of the non-linear response.

The performance of the proposed lin–log image sensor is summarized in Table I and the comparison of the proposed lin-log image sensor with previously lin-log image sensors is presented in Table II.

IV. CONCLUSION

We proposed a new pixel structure based on a 3–Tr APS with a lin–log response. Along with the MOS cascode, the photogate has been incorporated in the pixel. The new linear–logarithmic pixel was demonstrated to have a high linear sensitivity at very low illumination levels. At moderate illumination levels, the proposed pixel becomes a less sensitive linear response, owing to a coupling of the photogate and photodiode capacitances. The bias voltage of the photogate can control the sensitivity transition point of the proposed APS under the linear response region. At high illumination levels, the bias voltage of the MOS cascode is responsible for logarithmic operations. The proposed lin–log pixel exhibits two linear responses and a logarithmic response. Thus, the dynamic range of the pixel was improved considerably by the additional circuits. The dynamic range can be adjusted flexibly by applying the bias voltages to the photogate and the MOS cascode.

REFERENCES

[1] E. R. Fossum, "CMOS image sensors: Electronic camera-on-a-chip," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1689–1698, Oct. 1997.
[2] M. Bigas, E. Cabruja, J. Forest, and J. Salvi, "Review of CMOS image sensors," *Microelectron. J.*, vol. 37, pp. 433–451, May 2006.
[3] N. Akahane, S. Sugawa, S. Adachi, K. Mori, T. Ishiuchi, and K. Mizobuchi, "A sensitivity and linearity improvement of a 100-dB dynamic range CMOS image sensor using a lateral overflow integration capacitor," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 851–858, Apr. 2006.
[4] B. Choubey, S. Aoyoma, S. Otim, D. Joseph, and S. Collins, "An electronic-calibration scheme for logarithmic CMOS pixels," *IEEE Sensors J.*, vol. 6, no. 4, pp. 950–956, Aug. 2006.
[5] S. Lee and K. Yang, "High dynamic-range CMOS image sensor cell based on self-adaptive photosensing operation," *IEEE Trans. Electron Devices*, vol. 53, no. 7, pp. 1733–1735, Jul. 2006.
[6] J. Rhee and Y. Joo, "Dual-mode wide dynamic range CMOS active pixel sensor," *Electron. Lett.*, vol. 41, no. 24, pp. 1322–1323, Nov. 2005.

[7] M. Vatteroni, P. Valdastri, A. Sartori, A. Menciassi, and P. Dario, "Linear–logarithmic CMOS pixel with tunable dynamic range," *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 1108–1115, Apr. 2011.

[8] G. Storm, R. Henderson, J. E. D. Hurwitz, D. Renshaw, K. Findlater, and M. Purcell, "Extended dynamic range from a combined linear-logarithmic CMOS image sensor," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2095–2106, Sep. 2006.

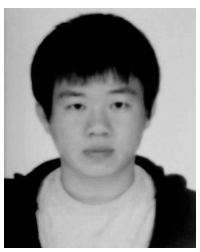
[9] J. Lee, I. Baek, D. Yang, and K. Yang, "On-chip FPN calibration for a linear-logarithmic APS using two-step charge transfer," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1989–1994, Jun. 2013.

[10] M. Sasaki, M. Mase, S. Kawahito, and Y. Tadokoro, "A wide-dynamic-range CMOS image sensor based on multiple short exposure-time read-out with multiple-resolution column-parallel ADC," *IEEE Sensors J.*, vol. 7, no. 1, pp. 151–158, Jan. 2007.

[11] M.-W. Seo *et al.*, "A low noise wide dynamic range CMOS image sensor with low-noise transistors and 17b column-parallel ADCs," *IEEE Sensors J.*, vol. 13, no. 8, pp. 2922–2929, Aug. 2013.

[12] M. Bae, S.-H. Jo, B.-S. Choi, H. H. Lee, P. Choi, and J.-K. Shin, "Variable-dynamic-range complementary metal-oxide-semiconductor image sensor with gate/body-tied metal oxide silicon field effect transistor-type photodetector using feedback structure," *Sensors Mater.*, vol. 28, pp. 13–19, Jan. 2016.

[13] M. Bae, S. H. Jo, B. S. Choi, H. H. Lee, P. Choi, and J. K. Shin, "Wide dynamic range linear-logarithmic CMOS image sensor using photogate and cascode MOSFET," *Electron. Lett.*, vol. 52, no. 3, pp. 198–200, 2016.



Myunghan Bae received the B.S. and M.S. degrees from the School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, South Korea, in 2010 and 2012, respectively, where he is currently pursuing the Ph.D. degree. His current research is focused on the study of the CMOS image sensor and its applications.

Byoung-Soo Choi received the B.S. degree in electronics engineering from Yeungnam University, Gyeongsan, South Korea, in 2013, and the M.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea, in 2015. He is currently pursuing the Ph.D. degree with Kyungpook National University. His current fields of interest are the CMOS image sensor and its applications.

Sung-Hyun Jo received the B.S. and M.S. degrees from the School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, South Korea, in 2008 and 2011, respectively, where he is currently pursuing the Ph.D. degree. His current fields of interest are in the CMOS image sensor and its applications.

Hee-Ho Lee received the M.S. and Ph.D. degrees from the School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, South Korea, in 2012 and 2016, respectively. His current fields of interest are in biosensors and their applications.

Pyung Choi received the B.S. degree from Yonsei University, Seoul, South Korea, in 1980, the M.S. degree from Ohio State University, OH, USA, in 1985, and the Ph.D. degree from the Georgia Institute of Technology, GA, USA, in 1990. He is currently a Full Professor with the Department of Electrical Engineering, Kyungpook National University, Daegu, South Korea. His major interests are analog VLSIs, IC modeling, and CAD.

Jang-Kyoo Shin received the B.S. degree in electronics engineering from Seoul National University, Seoul, South Korea, in 1978, the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 1980, and the Ph.D. degree in electrical engineering from Colorado State University, Colorado, USA, in 1991. He is a Professor with the School of Electronics Engineering, Kyungpook National University, Daegu, South Korea. His current fields of interest are semiconductor sensors and intelligent sensor systems.