A High Dynamic Range CMOS Image Sensor for Scientific Imaging Applications

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***Abstract*—This paper presents a high dynamic range CMOS image sensor that utilizes a combined linear-logarithmic readout scheme with built-in linear-logarithmic switching point detection for scientific imaging applications. The proposed readout architecture adjusts each individual pixel to operate in either linear or logarithmic readout mode according to the input illumination level. This realizes direct high-throughput image reconstruction enabling a hybrid combination of linear and logarithmic pixel outputs in the same image frame without introducing complicated post-signal processing. A novel feature of fine-tuning the overall dynamic range and contrast of the output image is also achieved using this readout method. An image sensor chip consisting of a 16×16 7-T pixel array with n-well/p-sub photodiodes and the proposed readout architecture has been implemented in $0.5\ \mu\mathrm{m}$ CMOS technology. The sensor chip has been evaluated through both electrical and optical characterizations, demonstrating an overall dynamic range of 121 dB. As a proof of concept, scientific imaging results on clusters of nano particles ($\mathrm{CoFe_2O_4}$) and optical fiber sensor are presented and discussed.**

***Index Terms*—CMOS image sensor, high dynamic range, linear-logarithmic switching point, scientific imaging.**

I. Introduction

In scientific imaging applications such as biophysics and radiography, high dynamic range (DR) sensors are favored for their ability to distinguish low contrast signal from high background illumination and to reconstruct an image that covers a wide illumination range from various light emitting objects. Traditional 3-T active pixel sensors (APS) [1] have good signal-to-noise ratio (SNR) but suffer from low DR due to linear optical-electrical conversion and limited charge well-capacity of the silicon photodetector used. Logarithmic (log) mode APS on the other hand [2], increase the DR by logarithmically encoding the optical signal, but have serious drawbacks such as high fixed pattern noise (FPN) due to threshold voltage variation of the readout transistor and poor SNR for low light detection [3]. Many techniques have been proposed to improve the DR performance beyond log mode APS, these include: 1) well-capacity adjustment [4] that splits the integration process into a subset of short integration intervals to allow for increased maximum detectable photocurrent; 2) a digital pixel structure [5] that converts the photocurrent into a sequence of pulse-width modulated digital outputs by using a self-reset feedback loop; 3) a digital pixel architecture that combines time-to-digital converter with a fine 6-bit ADC to enhance the DR performance while keeping the SNR high [6]; and 4) a multicapture scheme that performs multiple readout from pixel array at different integration times [7]–[9] with final image reconstructed using a combination of wide dynamic range pixel outputs. All the techniques mentioned above require either complicated pixel level operation or time-consuming post-signal processing or even both, resulting in low throughput image readout and high-power consumption due to intensive use of digital and mixed-signal circuitry. It is desirable to perform the DR enhancement algorithm directly at the pixel level and possibly within analog domain for further reducing power consumption and low-level hardware complexity.

Reported work [10] has introduced a combined linear-log operation at pixel level. This technique realizes high DR readout operation by acquiring both linear and log mode outputs from each pixel in the array, and uses post-signal processing to determine the linear-log switching point for image reconstruction. The final high DR image is obtained by replacing the saturated linear pixel outputs, as determined by the switching point, with log mode outputs, giving extended DR while not degrading the SNR performance for low light detection. This process is computationally expensive and data intensive. In this paper, we are proposing a new readout method that provides relief from the complexity of post-signal processing and also improves the throughput of image readout by directly integrating the linear-log switching operation at chip level. This is accomplished by inserting a switching point detection feedback loop into the pixel readout path. The built-in detection circuit consists of a comparator that periodically compares the linear mode pixel output with an externally controllable reference voltage, which defines the linear-log switching point. Therefore, the dynamic operating ranges for both linear and log mode readout is determined with significantly reduced complexity of post-signal processing. We have also demonstrated a novel feature of fine-tuning the DR and contrast of an output image by controlling the switching point, thus adjusting the density of linear and log pixel outputs in a given image frame. The proposed readout architecture has been implemented using minimum number of transistors at pixel level and sharing the readout circuits among the entire pixel array, leading to further reduced hardware complexity. The fabricated sensor chip has been successfully applied to a few test cases of scientific imaging applications, during which both sensor functionality and performance were evaluated.

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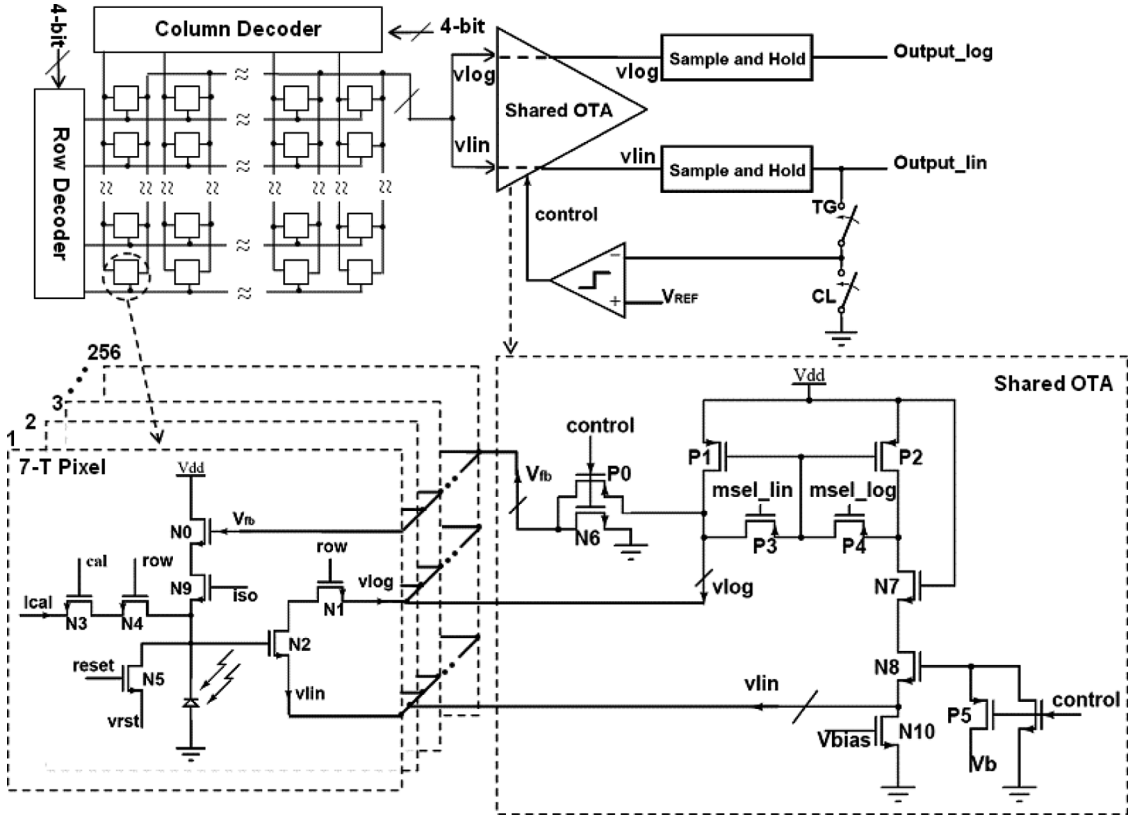


Fig. 1. Architecture of image sensor with proposed built-in linear-log switching point detection circuit.

This paper is organized as follows. Section II explains the system level operation of the high DR image readout with built-in linear-log switching point detection, showing the essential circuit blocks. Section III provides circuitry implementation in detail at both pixel and chip level. Section IV shows chip characterization results and the image reconstruction method, followed by two scientific imaging experiments. Section V concludes the accomplished work.

II. Image Sensor Architecture

The image sensor architecture is shown in Fig. 1. The sensor chip consists of a 16×16 array of pixels with n-well/p-sub photodiodes and a seven-transistor (7-T) structure. The chip level readout amplifier was implemented using a shared structure to reduce the number of transistor at each pixel [10]. The shared operational amplifier (*Shared OTA*) is partly switched on and off for adjusting the pixel operation between linear and log mode readout, and this will be explained in the following section. Other units of the CMOS image sensor include two switched-capacitor (SC) sample-and-hold circuits for sampling linear and log mode outputs, and a global comparator connected in a feedback loop between the pixel's linear output and *Shared OTA* as a built-in linear-log switching point detection block. Since the aim of our prototype was to provide a proof of concept, we kept a small pixel count (16×16) to keep the area of the chip small for cost and complexity reasons. Next, we explain the readout operation of an individual pixel.

The pixel starts by working in linear mode as a conventional APS. The *Shared OTA* reconfigures itself as a source follower whose output *vlin* is connected to a sample-and-hold SC circuit for final readout. The global comparator takes the linear mode output (*Output_lin*) from each pixel and compares it with an external reference voltage $V_{\rm ref}$ that decides the switching point for the image sensor to go automatically from linear to log readout mode. If the detected illumination intensity exceeds the threshold level pre-defined by $V_{\rm ref}$, a low voltage *control* signal is generated and fed back into *Shared OTA*, reconfiguring the pixel readout mode into log operation. The output is then sampled via a second SC circuit; and, if the detected illumination falls below the switching point, the pixel readout is complete and linear output will be used for final image reconstruction. Within a given frame, only pixels sensing high input optical power will operate in dual linear-log mode and this foregoes the need for pixels sensing low light to enter into log mode operation, as is required in [10] due to their image reconstruction process. Therefore our readout method leads to reduced power consumption with minimum post-signal processing ahead and improved readout throughput especially at low light detection. Also note that the externally controllable reference voltage $V_{\rm ref}$ adjusts the number of linear mode pixel outputs and the number of log mode pixel outputs across the pixel array under any given background illumination by controlling the switching point, resulting in a final reconstructed image whose contrast and overall DR can be finely tuned to achieve good image quality. This sets our design apart from other similar readout methods whose linear-log switching is also carried out at chip level but all have a fixed switching point [11], [12] . The image reconstruction process of our design including setting the switching point will be explained in detail in Section IV.

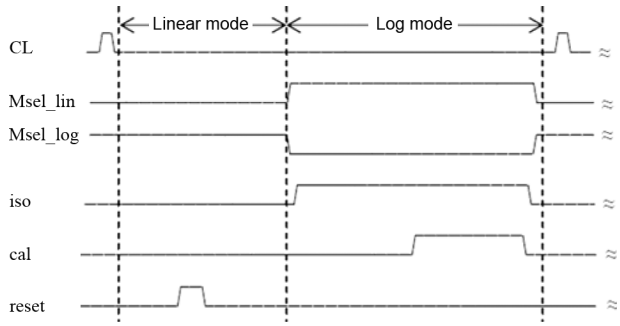


Fig. 2. Simplified timing diagram of linear-log readout operation.

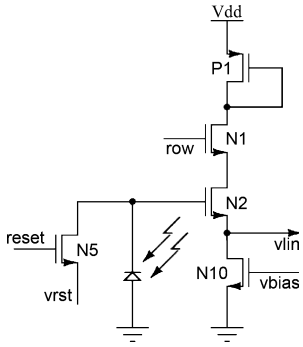


Fig. 3. Simplified schematic of linear mode operation.

III. Circuit Implementation

A. Pixel Implementation

As mentioned earlier, a complete pixel readout structure consists of two parts: one that resides inside pixel array as 7-T pixel and one that is a *Shared OTA* utilized by all the pixels during serial pixel readout. This allows for reduced transistor count at each pixel given the level of complexity of readout operation, thus facilitating a high fill factor implementation. It can be seen from Fig. 1 that transistors N1 and N2 from *Shared OTA* are borrowed from each individual pixel, which is time multiplexed to connect with *Shared OTA* during readout. To understand the linear-log readout operation, please see Fig. 2 for the simplified timing diagram. Initially, two nonoverlapping mode selection signals *msel_lin* (low) and *msel_log* (high) are applied to the *Shared OTA*, forcing the pixel into conventional linear mode operation. *CL* resets the global comparator by connecting its negative input to ground, generating a mode switching signal *control* (high) back into the *Shared OTA*. Transistors N9 and N0 are then turned off to minimize their leakage current contribution to the photocurrent during photodiode integration operation. The gate of N8 is connected to ground by *control*, which disables the right branch (P2, N7, and N8) of the *Shared OTA*. The left branch of the *Shared OTA* now works as a source follower (N2, N10) with diode connected load (P1). Linear integration of the photocurrent at this source follower input produces a linear mode output *vlin* that is sampled and held by the following SC circuit. The simplified schematic of linear mode pixel readout is shown in Fig. 3.

The linear mode output *Output_lin* after the SC circuit is compared with $V_{\rm ref}$. If the background illumination reaches the threshold value defined by switching point, *Output_lin* will exceed $V_{\rm ref}$ and the comparator will then generate a low voltage

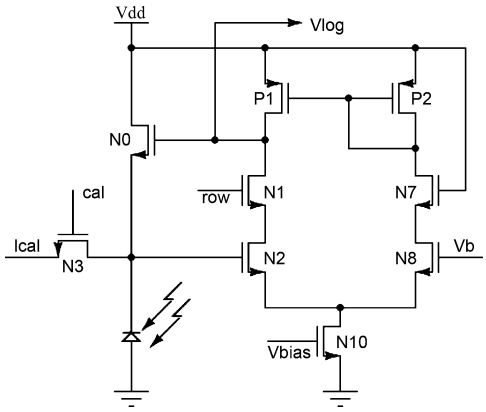


Fig. 4. Simplified schematic of log mode operation.

control signal, forcing the pixel to operate in log mode. During log mode operation, *msel_lin* is high and *msel_log* is low, reconfiguring the *Shared OTA* into a cascoded amplifier with differential input and single-ended output. The amplifier's positive input transistor N8 is biased at $V_b = 2$ V and its negative input N2 is connected to the photodiode. Fig. 4 shows the simplified schematic of log mode operation. The amplifier's output is connected to the gate of N0 in a negative feedback loop, which constantly fixes the photodiode node voltage to V_b. The photocurrent, being typically in the order of few hundreds of femto or pico amperes, will drive transistor N0 into subthreshold region

$$I_{ph} = I_{s0}\exp\left(\frac{V_{gs0}-V_{th0}}{nv_t}\right)\left(1-\exp\left(\frac{-V_{ds0}}{v_t}\right)\right). \quad (1)$$

For AMI06 0.5 μm CMOS technology, we have

$$I_{s0} = \mu_0\frac{W}{L}\sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\phi_s}}v_t^2 \approx 58.28\frac{W}{L}nA. \quad (2)$$

In the above two equations, v_t is the thermal voltage and I_{ph} represents the photocurrent. Since the source of N0 is biased at V_b, then $1-\exp(-V_{ds0}/v_t) \approx 1$ and only the gate voltage of N0 varies logarithmically with the photocurrent, giving the following equation:

$$V_{g0} = nv_t\ln\frac{I_{ph}}{I_{s0}} + V_{th0} + V_b. \quad (3)$$

Note in log mode we have a provision for a calibration switch *Ical* (N3) that is used to connect a current source *Ical* to the photodiode for FPN suppression by reducing the effect from the threshold voltage variation of N0. Soon after V_{g0} is readout, an on-chip current source I_{cal} of 5 μA, which is much larger than the estimated maximum I_{ph}, is connected in parallel with the photodiode via N3, pulling N0 into saturation region

$$V_{g0\_cal} \approx \sqrt{\frac{2I_{cal}}{\mu_n c_{ox}\left(\frac{W}{L}\right)_{N0}}} + V_{th0} + V_b. \quad (4)$$

The calibration output V_{g0_cal} is then read out again via the same SC circuit, which outputs the difference between V_{g0_cal} and V_{g0}

$$V_{g0} - V_{g0\_cal} = nv_t\ln\frac{I_{ph}}{I_{s0}} - \sqrt{\frac{2I_{cal}}{\mu_n c_{ox}\left(\frac{W}{L}\right)_{N0}}}. \quad (5)$$

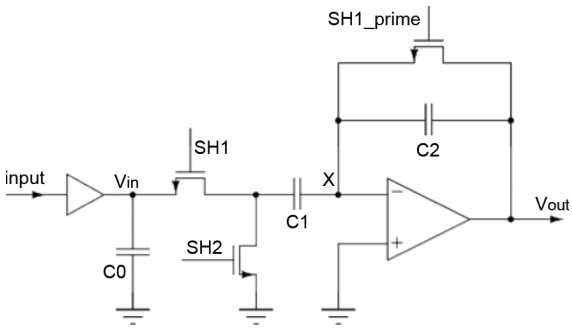


Fig. 5. Schematic of sample-and-hold SC circuit.

The log mode computation with calibration is a quick process since: 1) there is no photocurrent integration required and 2) the calibration utilizes N0 working in saturation region, which provides high-speed settling of the output transient response.

Also note that the log mode operation is only performed on pixels that are highly illuminated defined through the reference voltage $V_{\rm ref}$, while the rest of the pixel array operates in linear readout mode. A given image readout is essentially a hybrid combination of some outputs from linear mode pixels and others from log mode pixels. This forgoes the need to use complicated post-signal processing for image reconstruction since linear-log switching is directly carried out at chip level.

B. Sample-and-Hold Circuit

In this design, two sample-and-hold SC circuits are used for separate linear output *vlin* and log output *vlog* sampling. The final output from each individual pixel for image reconstruction is determined by the feedback *control* signal, which triggers the off-chip data acquisition device to pick the right output. In future research, we could implement a shared sample-and-hold circuit and utilize simple digital block to automate this readout process. Fig. 5 shows schematic of the SC circuit. In this design, an input buffer with -1 dB DC gain and a compensation capacitor $C0$ of 1 pF were used to stabilize the input signal and to adjust the input common-mode voltage for proper operation of the SC circuit. A cascoded differential input and single-ended output amplifier similar to the *Shared OTA* serves as the op-amp block. Both sampling capacitor $C1$ and holding capacitor $C2$ are 1 pF. Fig. 6 shows the operation timing diagram for difference double sampling. During time $t_0 \sim t_3$, the input voltage (say V_{in1}) at the *input* terminal shown in Fig. 5 is sampled and held at the output; during time $t_4 \sim t_5$ the second input (say V_{in2}) is utilized to perform difference double sampling, resulting in a small signal output voltage at time t_5

$$V_{\rm out} = V_{in1} - V_{in2}. \tag{6}$$

In order to minimize the charge injection effect, *SH1_prime* is turned off 0.5 μs earlier than *SH1* at t_2.

For linear mode readout, $V_{in1} = V_{\rm reset}$ and $V_{in2} = V_{pd}$, where $V_{\rm reset} = 2$ V is the reset voltage and V_{pd} is the photodiode node voltage after integration. The small signal output is linearly proportional to the light intensity

$$V_{out\_linear} = \frac{(I_{ph} t_{int})}{C_{pd}} \tag{7}$$

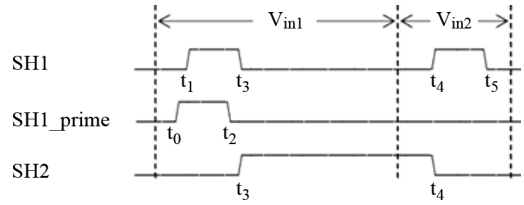


Fig. 6. Operation timing diagram of sample-and-hold SC circuit.

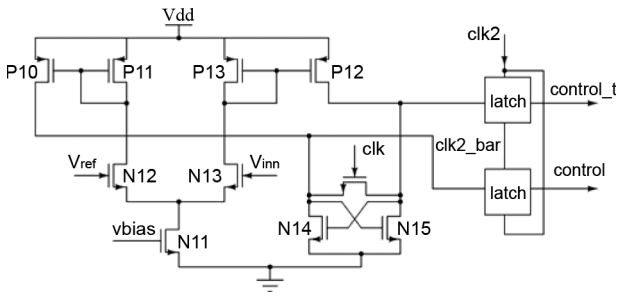


Fig. 7. Schematic of the global comparator.

where $t_{\rm int}$ is the integration time and C_{pd} is the integration capacitance at photodiode node, which is 124.95 fF in our implementation.

For log mode readout, $V_{in1} = V_{g0}$ and $V_{in2} = V_{g0\_cal}$, the output is logarithmically proportional to the light intensity as shown in (5).

C. Comparator

Fig. 7 shows the schematic of the global comparator [13] that generates the feedback *control* signal. Input transistor N12 is connected to $V_{\rm ref}$, while the other input V_{inn} is connected to the linear mode output from the SC circuit. During preamplification stage, current mirror transistor pairs P10/P11 and P12/P13 are used to pre-amplify the difference between the two input signals while clock signal *clk* resets the outputs of analog latch N14/N15 to 0.8 V. Immediately after *clk* goes low, the analog latch starts to regenerate the pre-amplified input signals to full scale defined by V_{dd} and ground. A digital latch is cascaded after the analog latch to further regenerate a clean and stable digital output. The comparator output will not change until the D-latch is triggered by the clock signals *clk2* and *clk2_bar*.

IV. Measurement Results

Fig. 8 shows the microphotograph of the fabricated sensor chip in AMI 0.5 μm two-poly and three-metal CMOS technology. The chip measures 1.5 mm $\times$ 1.5 mm and is packaged in DIP40. Both chip characterization and scientific imaging experiments have been carried out on the fabricated image sensor. An ALTERA DE2 kit with Cyclone II FPGA was used for digital control of the image sensor and an NI DAQ USB-6251 card was used for data acquisition. A custom made LABVIEW program and a MATLAB program were both used to reconstruct the image. A fiber-lit high intensity optical power source [Dolan–Jenner Industries, Inc.] was used as background illumination and an optical power meter with calibrated photodiode

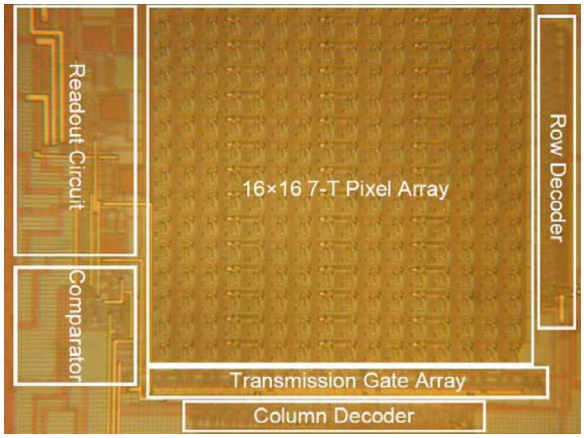


Fig. 8. Microphotograph of fabricated sensor chip.

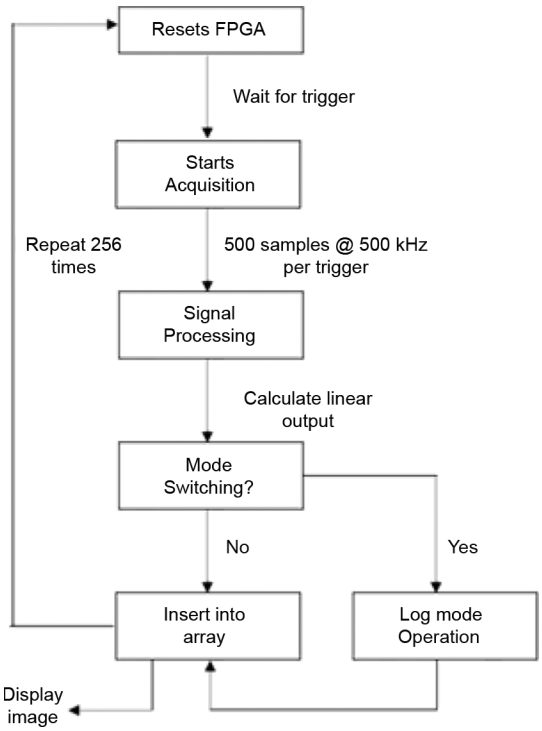


Fig. 9. Simplified flow diagram of data acquisition.

[Thorlabs, Inc.] from 400 to 1100 nm wavelength was used during optical testing.

A. Chip Characterization and Image Reconstruction

The chip characterization was carried out using the setup in [14]. Main parameters of the optical performance of our image sensor were obtained, including dark current, optical-electrical response curves, FPN for both linear and log readout operation modes, and DR performance. Fig. 9 shows the implemented software flow diagram for data acquisition. It uses an off-chip FPGA to provide control signals to the image sensor, and this can be easily ported into the CMOS chip in future implementations. The FPGA first resets the sensor chip to standby mode, during which the pixel array is disconnected from the readout circuit and all the active control switches are turned off. The

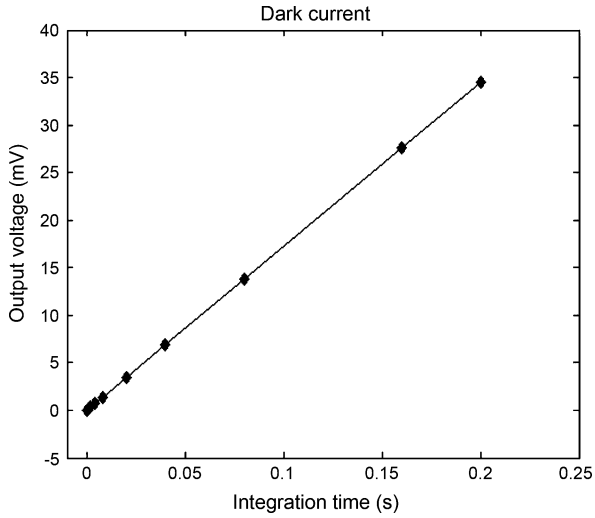


Fig. 10. Dark current measurement result.

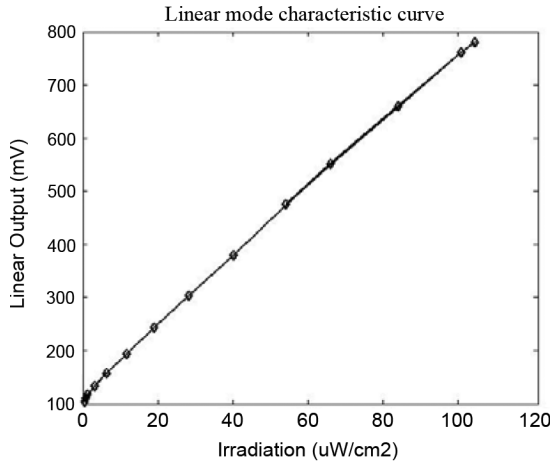
FPGA then enables the *Shared OTA* to serially scan throughout the entire pixel array. For each pixel readout, the FPGA will generate a digital pulse to the DAQ card to trigger the data acquisition, followed by a simple signal processing in LABVIEW to calculate an output that represents either linear or log mode readout result, depending on the illumination level and switching point. The calculated output value is then converted into an 8-bit gray code and is inserted into a 16×16 bit-map file, which will be used as final reconstructed image. Both MATLAB and LABVIEW are used to display the final image. The detailed image reconstruction algorithm will be explained shortly in this section.

Fig. 10 shows the dark current measurement result, which was obtained by sweeping the integration time from 200 μs to 200 ms, while keeping the image sensor shielded from external optical signal. The integrated dark signal was measured to be 172.8 mV/s, which corresponds to a dark current of $13.8\ \mathrm{nA/cm^2}$.

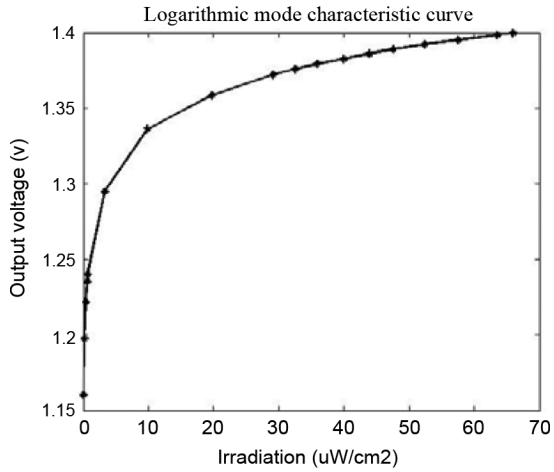
Figs. 11 and 12 present the optical-electrical characteristic curves, measured under an illumination wavelength of 550 nm. Fig. 11(a) shows the linear mode characteristic curve, during which the optical power was swept from $60.5\ \mathrm{nW/cm^2}$ to $114\ \mu\mathrm{W/cm^2}$ and the resulting curve shows over 98% of linearity. Fig. 11(b) presents the characteristic curve for log mode operation, during which the optical power was swept from $66\ \mu\mathrm{W/cm^2}$ to $70\ \mathrm{mW/cm^2}$. In both cases, DR performance is defined by

$$\mathrm{DR} = 20 \log \left(\frac{V_{\mathrm{sat}}}{\sigma_{\mathrm{read}}} \right). \tag{8}$$

The minimum detectable optical power used in both characterizations was limited by the readout noise (σ_{read}, as summarized in Table I) of the linear and log operation modes. Please note that for linear mode readout the readout noise also includes the integrated dark current. The maximum optical power is limited by the voltage swing (V_{sat}) of readout SC circuit for log readout and charge well-capacity of the photodiode for linear



(a) Linear mode characteristic curve



(b) Log mode characteristic curve

Fig. 11. Electrical-optical characteristic curves.

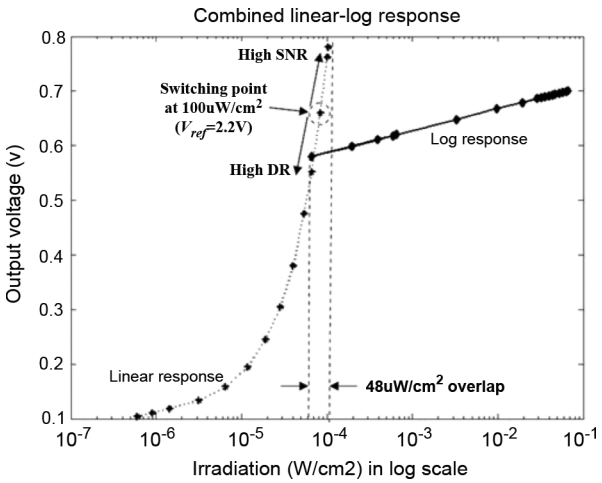


Fig. 12. Combined linear-log response curve.

readout. The combined linear-log response curve that represents the overall DR performance is shown in Fig. 12 (the input optical power is drawn in log scale and log outputs are scaled to match the linear output range). Note that there is $48\ \mu\mathrm{W/cm^2}$

TABLE I
SPECIFICATIONS OF HIGH DYNAMIC RANGE (DR) IMAGE SENSOR

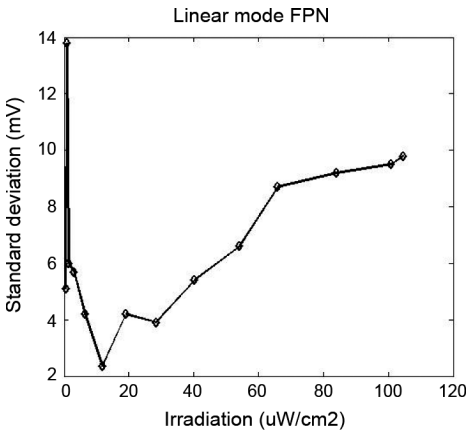
Technology	AMI 0.5μm CMOS
Power supply	3.3V
Pixel array	16×16
Pixel size	23.4μm×27.15μm
Photodiode area	156.06μm^2
Fill factor	24.56%
Linear sensitivity	503mV/lux.s
Linear readout noise	σ_{read} = 0.998mV
Logarithmic sensitivity	79.98mV/dec of illumination
Logarithmic readout noise	σ_{read} = 0.7mV
FPN (Linear / Log)	≤2.48% / ≤8.34%
Dark current	13.8nA/cm^2
Dynamic range (Linear / Log)	65.5dB / 60.51dB
Combined dynamic range	121.26dB

overlap among the dynamic operation ranges of linear and log readout mode. This overlap in the pixel's linear-log operation serves dual purposes.

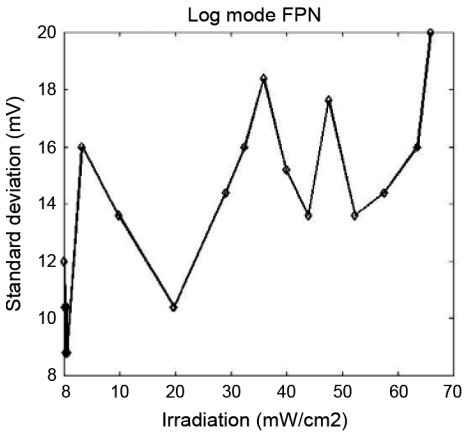
1) The switching point can be adjusted within this region. Moving it upwards along the linear response curve will result in higher density of linear outputs in the output image, leading to higher SNR; similarly moving the switching point downwards will improve the DR performance and lower the image contrast due to increased density of log outputs. Therefore, the DR and contrast of output image can be finely tuned (as will be shown in ***scientific imaging experiments***). In our design, the overlap region corresponds to a V_{ref} from 2.10 to 2.30 V and Fig. 12 shows an example switching point at an illumination of $100\ \mu\mathrm{W/cm^2}$ when the reference voltage is set to 2.2 V.
2) Within this overlap region, the log mode output is calibrated so that it matches the linear response curve. Therefore, the discontinuity of the output image due to linear-log switching within this region can be minimized.

Our image reconstruction algorithm is carried out as follows: we first obtain combined linear-log response curve, as shown in Fig. 12, and determine the overlap region between the linear and log responses. Within this region, log response is calibrated to match the linear response to minimize the discontinuity between linear and log outputs. Then, within this overlap region, we store the mapping information between the switching points (can be any point along the linear response curve within the region) and their corresponding illumination levels. Since this mapping information is known, the process of image acquisition and linear-log reconstruction is straightforward with simple steps.

1) Set V_{ref} to specify the linear-log switching point and acquire the final output from each pixel according to the decision made by the built-in switching point detection circuit.
2) Map either linear or log output from each pixel to the switching point to determine the relative illumination intensity sensed by each pixel.



(a) FPN of linear mode readout



(b) FPN of log mode readout

Fig. 13. FPN measurement results.

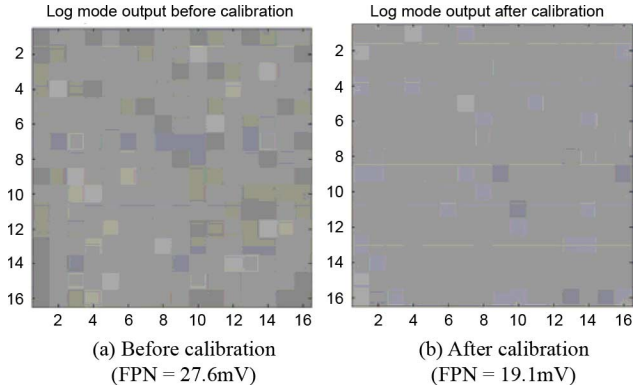
3) All pixel outputs are then converted to 8-bit gray codes and final high DR image is reconstructed.

Please note that the calibration process to acquire the mapping information within the overlap region is carried out before the actual image acquisition but is not required for every image frame. In our testing, it was performed only once before every scientific imaging experiment.

Fig. 13 shows the FPN performance, which is defined as the standard deviation of pixel array outputs under uniform illumination. For linear mode operation, the FPN is less than 13.8 mV, corresponding to 2.48% of total linear mode response. For log mode operation, the FPN is less than 20 mV after calibration, corresponding to 8.34% of total log mode response. The high FPN for log mode response is expected due to small output voltage swing and spatial variation of the calibration current *Ical* that is distributed among the entire pixel array. Fig. 14 shows two log mode output sample images under uniform illumination before and after FPN calibration.

B. Scientific Imaging Experiments

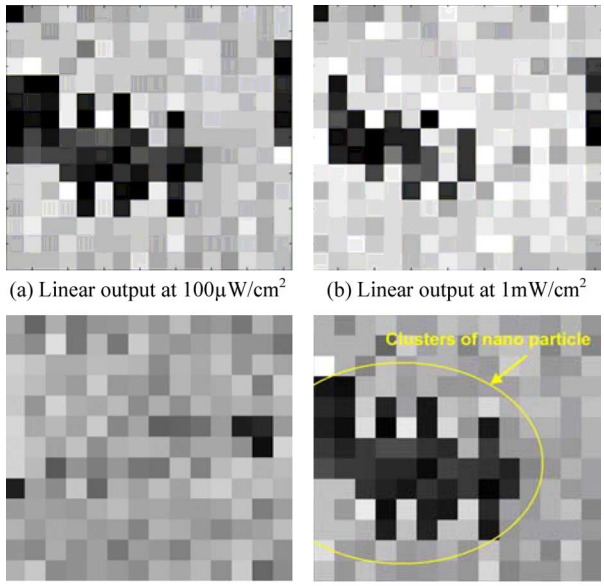
The high DR readout operation was performed in two scientific imaging experiments, including imaging clusters of magnetic nano particles ($CoFe_2O_4$) and an optical fiber sensor. The magnetic nano particles are often used as biological tags



(a) Before calibration (FPN = 27.6mV)

(b) After calibration (FPN = 19.1mV)

Fig. 14. Log mode output images before and after FPN calibration.



(a) Linear output at 100μW/cm^2

(b) Linear output at 1mW/cm^2

(c) Linear output at 10mW/cm^2

(d) Combined linear-log output at 10mW/cm^2

Fig. 15. Images of nano particle cluster under various illumination levels ($V_{\text{ref}} = 2.20$ V).

for separation and purification of biological samples and magnetic detection. In current setups, an expensive CCD camera is typically used to image the presence or absence of magnetic particles in the field of view. However, expensive filters and optical lenses are required making the systems bulky and increasing overall cost. We aim to use our image sensor for direct imaging without the need for expensive filters to block the background illumination. During this experiment, samples of nano particles contained in a glass slide were directly mounted on the image sensor and illuminated under various optical power levels and final images were reconstructed in MATLAB. Fig. 15 presents the results under a reference voltage of 2.20 V, corresponding to a switching point of 100 $\mu\text{W/cm}^2$, as shown in Fig. 12. Fig. 15(a) shows the linear mode output when the background illumination was set to 100 $\mu\text{W/cm}^2$, the picture shows the presence of cluster. It can be observed that the image was well constructed using only linear mode readout due to the low background illumination. However, in real scientific

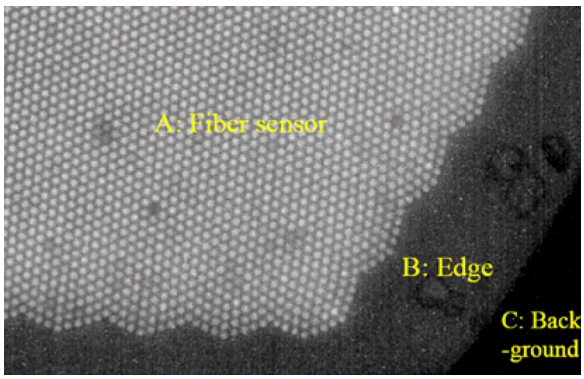
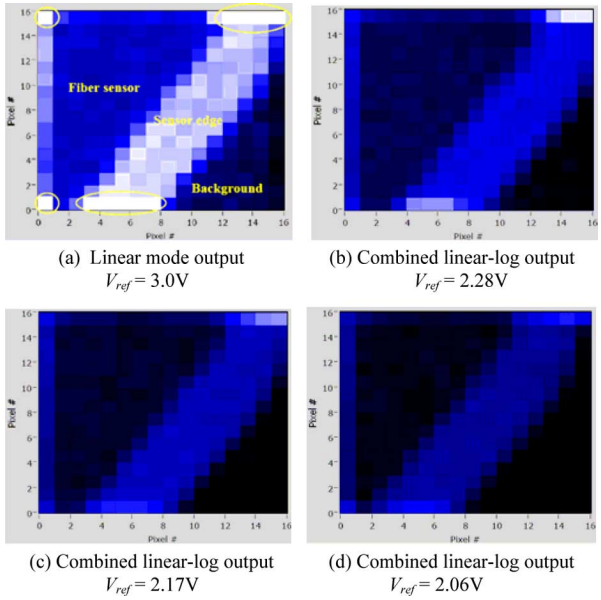


Fig. 16. Image of optical fiber sensor captured using cooled CCD.



(a) Linear mode output $V_{ref} = 3.0$V

(b) Combined linear-log output $V_{ref} = 2.28$V

(c) Combined linear-log output $V_{ref} = 2.17$V

(d) Combined linear-log output $V_{ref} = 2.06$V

Fig. 17. Images of optical fiber sensor at various reference voltages.

imaging apparatus, the background illumination would be much higher. As we gradually increased the background illumination [Fig. 15(b) and (c)] to 10 $\mathrm{mW/cm^2}$, which was far beyond the switching point, some pixels started to get saturated, and finally, the image of cluster sample could not be reconstructed using only linear mode readout due to limited DR performance. After we performed combined linear-log readout operation under the same background illumination at 10 $\mathrm{mW/cm^2}$, high DR image [Fig. 15(d)] was captured and the nano particle clusters (highlighted area) could be clearly seen again. This sensor chip therefore proves to be an ideal candidate for many magnetic separation, purification and detection applications typically encountered in lab-on-a-chip applications.

During the second experiment, the sensor chip was used to image an optical fiber sensor that has been widely used for chemical vapor sensing applications [15]. Fig. 16 shows an image of the corner of fiber sensor obtained by a cooled CCD camera. Since the CCD camera has a limited DR, a bandpass excitation filter was used to block the background illumination light. From the picture, we can observe three different parts: *fiber sensor area* that consists of an array of fluorescent microsensors, *sensor edge*, and *background*. The *sensor edge* is typically the most illuminated area in this sensor in the absence of the excitation filter.

The same part of the fiber sensor has been imaged using the fabricated sensor chip without the help of excitation filter to test the high DR readout operation. Therefore the *sensor edge* should look brighter than the *fiber sensor area* and *background*. In this experiment, we will demonstrate the fine-tuning function that realizes fully controllable switching between linear and log mode readout (through V_{ref}) and consequently adjusts the contrast and DR of the output image. The optical output power from the background excitation light was kept at a high level of 10 $\mathrm{mW/cm^2}$ during the entire experiment. Fig. 17(a)–(d) present a sequence of real-time output images reconstructed using LABVIEW *Intensity Graph* module, which presents highly illuminated area using bright colors and weakly illuminated area using dark colors. During this experiment, V_{ref} was gradually decreased from 3.0 to 2.06 V. Such a decrease in reference voltage lowers the switching point and this should increase the density of log mode pixel outputs in a give image frame and thereby increase the total DR of image at the cost of reduced contrast. Fig. 17(a) shows the output image at $V_{\mathrm{ref}} = 3.0$ V, which exceeds the upper limit of the overlap region defined in Fig. 12, thus putting the entire pixel array into linear mode operation. From the image, we can clearly observe the *fiber sensor area*, the *sensor edge*, and the *background*. The highlighted areas represent saturated pixel outputs (termed here as "bad pixel"). Despite the poorly reconstructed "bad pixel" areas due to high background illumination, the image does show a very good contrast between the boundaries of different mediums, which indicates a good SNR performance from linear mode operation. As the reference voltage gradually decreases the switching point for the pixel to enter into log mode operation is lowered, resulting in increased number of log mode pixel outputs. Thus, the previously saturated pixel outputs are replaced by log mode outputs [see Fig. 17(b) and (c)]. The image has poorer contrast but provides wider illumination coverage. As the reference voltage is further lowered to 2.06 V, the switching point becomes so low that even pixels sensing very low illumination will switch to log mode operation, resulting in very high density of log mode outputs and consequently poor overall SNR performance in the output image. As can be observed from Fig. 17(d), the *background* and *fiber sensor area* can hardly be distinguished. Note that Fig. 17(a) and (d) are output images captured using two reference voltages outside the overlap region shown in Fig. 12, and the results suggest that in order to achieve good image quality the reference voltage should be chosen from within the overlap region.

What we have just demonstrated is a tuning ability to tradeoff image contrast for DR performance in the output image using the fabricated sensor chip.

TABLE II
PERFORMANCE SUMMARY OF VARIOUS HIGH DYNAMIC RANGE CMOS IMAGE SENSORS

	[4]	[5]	[9]	[10]	[12]	[16]	This work
Technology	0.8μm	0.5μm	0.35μm	0.18μm	0.35μm	0.25μm	0.5μm
Pixel size (μm^2)	N/A	30×30	18×18	5.6×5.6	7.5×7.5	10×10	23.4×27.15*
Pixel level transistors	4	19	18	7	4	5	7
Fill factor	49%	N/A	15%	33%	37%	60%	24.56%*
Dynamic range	96dB	104dB	97dB	143dB	124dB	140dB	121dB
High dynamic range technique	Well-capacity adjustment	Self-reset	Multiple reset	Combined linear-log	Combined linear-log	Logarithmic	Combined linear-log
Linear-log switching	N/A	N/A	N/A	Off chip	On chip, fixed	N/A	On chip, adjustable
FPN_{max} (%/mV)	0.24%/18	0.1%/**	0.14%/**	10.59%/34.65***	≤5.3%/13***	≤8.54%/111***	≤11.4%/27.6***

*: Both pixel size and fill factor can be improved with more advanced technology. **: Not mentioned in the paper.
***: Raw FPN in log readout, represented in two forms: standard deviation (mV) of pixel array outputs and its percentage (%) in total log response.

V. CONCLUSION

We have presented a high DR CMOS image sensor, whose specifications are summarized in Table I. The implemented image sensor utilizes a combined linear-log readout technique with chip level linear-log switching point detection functionality that performs adjustment on the pixel readout operation, leading to reduced complexity in post-signal processing and improved throughput for image reconstruction especially at low light detection. The sensor chip was fabricated in $0.5\ \mu m$ CMOS technology and silicon experiment results have confirmed a total DR of 121.26 dB. The externally controllable reference voltage offers a flexible solution for adjusting the DR and contrast of reconstructed image without complicated post-signal processing. This imager is ideally suited for quick scientific imaging that requires detection of low light scattering or fluorescence in the presence of strong background illumination. We have successfully demonstrated image acquisition on clusters of nano particles and an optical fiber sensor under high background illumination and results have been presented.

Table II compares the performance of our CMOS image sensor with some previously published work. The measured dynamic range falls into the mid-to-high range, and a novel feature of adjustable on-chip linear-log switching that significantly relives the complexity of post-signal processing is achieved. It is also evident from the table that the log mode or combined linear-log imagers can generally achieve better DR performance with less complicated pixel level circuit design than traditional linear mode imagers utilizing sophisticated high dynamic range readout techniques, but the FPN introduced from log mode operation is significantly higher due to small output voltage swing and threshold voltage variation of the readout transistor. However, for certain yes-or-no scientific imaging applications as presented in this paper, the FPN requirement can be less stringent than that of traditional consumer applications.

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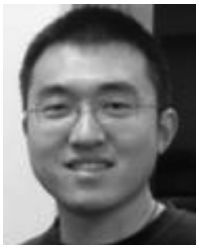

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